Technical White Paper

Floating Ground Hot-Swap Architecture to Enable Robust Protection on 800V or ±400V DC Power Distribution

Avishek Pal, Applications Engineer, Input Power Protection and Distribution
Rakesh Panguloori, Applications Manager, Input Power Protection and Distribution

ABSTRACT

Artificial intelligence (AI) data centers are driving an unprecedented surge in power demand, exceeding 100kW per rack, requiring a shift from traditional 50V DC power distribution to high-voltage direct current (HVDC) architectures at 800V or ±400V. To overcome protection challenges in these HVDC systems, this paper discusses a floating ground hot-swap architecture using a low-voltage controller configured with a reference connected to the load terminal rather than to the system ground. Experimental validation demonstrates a successful 800V operation with a controlled inrush current and microsecond fault detection, while reducing copper usage by 45% and improving efficiency by 5%.

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Trademarks

1 Introduction

The exponential growth of AI, high-performance computing (HPC), and cloud services is driving an unprecedented surge in data center power demands. Traditional 50V DC power distribution architectures, once sufficient for kilowatt-scale IT racks, are rapidly approaching physical and economic limits as AI workloads push rack densities from 10kW–30kW to over 100kW, and eventually toward 1MW. As documented in reference 1, data center power architectures are transitioning from traditional power shelves to power sidecars, where power is delivered to IT racks on an 800V or ±400V HVDC bus. By significantly increasing the distribution voltage, 800VDC systems reduce copper usage by up to 45%, minimize I^2R losses, and improve end-to-end efficiency by as much as 5%.

In an HVDC power architecture, as shown in Figure 1-1, the three-phase 480V AC power from the utility grid is converted into an 800V or ±400V DC bus using high-efficiency rectifiers. Through a hot-swap circuit, the power from the HVDC bus is fed into an intermediate bus converter (IBC) module, which converts the 800V or ±400V DC to intermediate voltages (for example, 48V, 12V, or 6V) for server racks. Finally, the power is stepped down to the GPU supply voltages of less than 1V using multiphase DC-DC power converters. The HVDC domain introduces new challenges for system protection and monitoring, particularly during hot-swap events. To address these challenges, a floating ground hot-swap architecture is proposed in this article. This document covers the principle of operation, system design, component selection, and experimental results of the proposed solution.

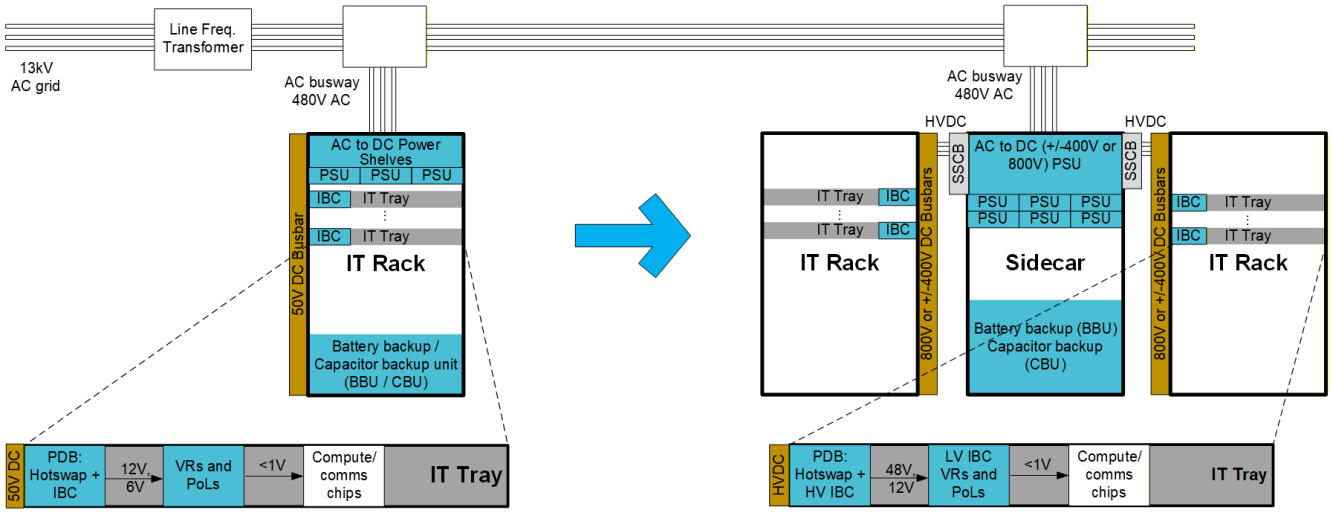

Figure 1-1. Data Center Power Distribution Architecture Evolution

2 Floating Ground Hot-Swap Architecture

A high-voltage hot-swap architecture is designed based on the floating ground concept by using the existing low-voltage, low-side, hot-swap controller by TI, the TPS23521 device. The TPS23521 device provides standard hot-swap functions such as hot-plug, inrush current management, undervoltage, overvoltage, overcurrent, and short-circuit protections.

As shown in Figure 2-1, the TPS23521 device uses VEE as a reference and drives the GATE of the hot-swap FET with respect to VEE. Unlike in a standard hot-swap configuration, the controller reference, VEE, is left floating and connected to the load terminal, VOUT, instead of to the system ground, GND. By powering between the VCC and VEE pins through an isolated bias power supply, the system emulates a scalable, floating ground hot-swap architecture making the TPS23521 appropriate for ±400V or 800V rails. The capacitor (CSS), connected between the SS pin and the FET drain through a 1kΩ resistor, determines the slew rate of the GATE voltage during start-up. The CSS is internally connected to the GATE pin, functioning as a gate-to-drain capacitor for Q1. When VCC is applied, the TPS23521 device begins GATE charging and turns on Q1. Once the gate-to-source voltage crosses the VTH, the entire GATE current discharges the CSS capacitor, thereby linearly discharging the drain-to-source (VDS) voltage of Q1. The FET Q1 operates in the Miller plateau region and acts as a source follower, where VOUT follows the GATE with a slew rate determined by the CSS capacitor. When the VDS of Q1 reaches zero, the GATE to VEE voltage increases further to VCC to VEE, enabling Q1 to operate

in full conduction mode. The low-side current sensing keeps the overcurrent and short-circuit protections intact during start-up and steady-state conditions.

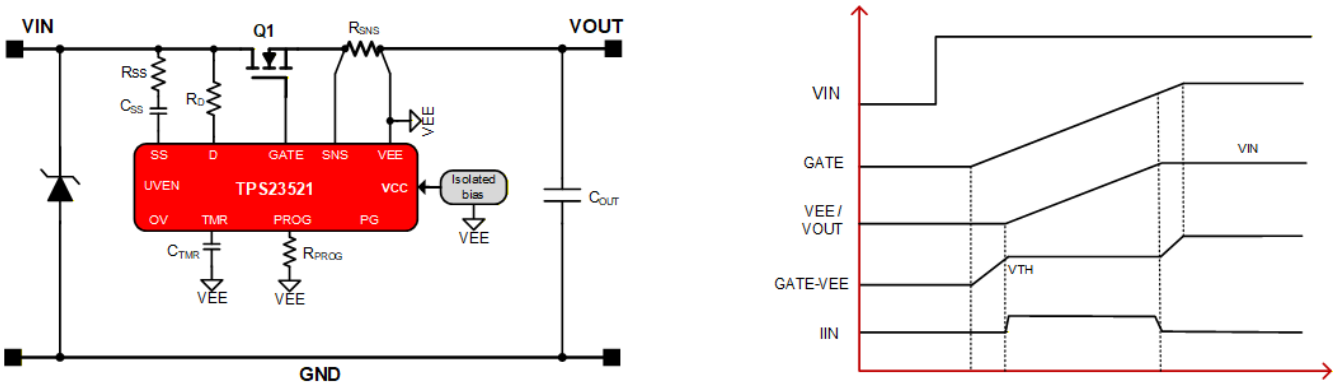

Figure 2-1. Illustration of the Floating Ground Hot-Swap Architecture and Start-Up Timing Diagram

3 System Design Considerations

Leveraging the floating ground hot-swap architecture discussed in the previous section, a complete hot-swap solution is built by using several TI components listed below.

- **TPS23521:** A low-side, high-performance, hot-swap controller as the core element to enable hot-plug, inrush current management, undervoltage, overvoltage, overcurrent, and short-circuit protections.
- **UCC28704:** Flyback controller to generate the bias power supply for all the building blocks.
- **OPA210:** An operational amplifier used in a differential configuration to scale down from the 800V input power supply voltage and interface with the UVEN and OV pins of the TPS23521 device.
- **INA238:** For precise current, voltage, and power monitoring through an I2C to enable digital telemetry over the **ISO1644** (I2C isolator) device for intelligent rack management.
- **ISOM8110:** Opto-emulator that provides an isolation barrier between the control circuit and the output discharge circuit.

As shown in the block diagram (see Figure 3-1), the floating ground hot-swap architecture allows a truly scalable solution, whether of the power level or supply rail voltage ±400V / 800V. Thus, making the architecture compatible for installations with either two wires or three wires (including chassis ground).

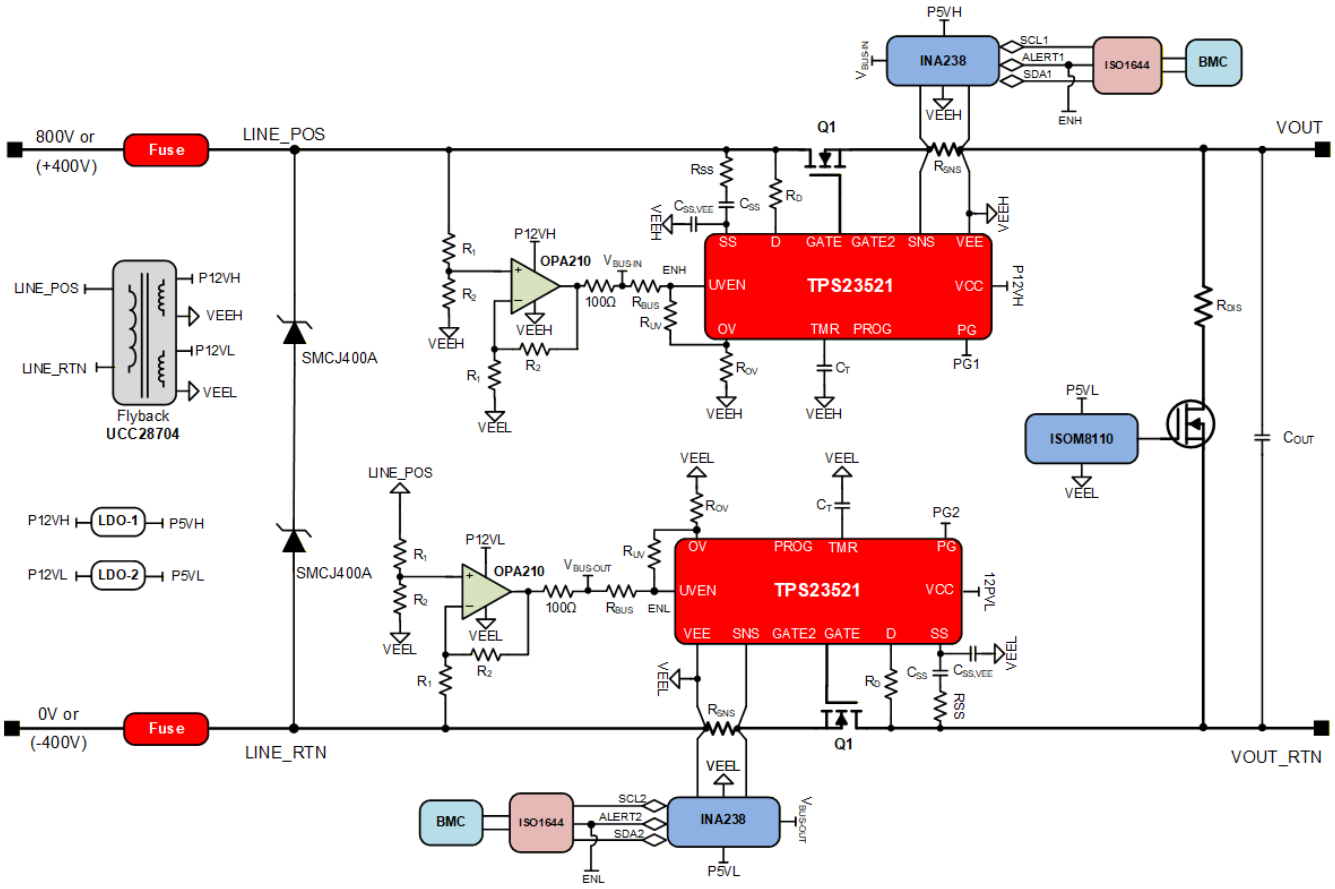

Figure 3-1. Block Diagram of the Floating Ground Hot-Swap Solution on High-Side and Low-Side Power Paths

4 Design Guidelines and Component Selection

In this section, the component selection is presented for the system specifications outlined in Table 4-1.

Table 4-1. Typical System Specifications

Design Parameter	Value
Input voltage range	2-wire ± 400V or 800V
Output capacitance	100µF
Steady-state thermal design power (TDP) rating	17kW
Overcurrent protection	25A
Fault timer duration (typical)	200µs
Maximum ambient temperature	60ºC
Undervoltage lockout threshold	720V
Overvoltage lockout threshold	880V

- **Selection of a current sense resistor, R_{SNS}** : The maximum load current is 17000W/720V = 23.6A. To provide some margin, set the target current limit to 25A. The PROG pin allows for selecting a sense voltage of either 25mV or 40mV. Select 25mV for lower power dissipation and then compute R_{SNS} using Equation 1.

$$R_{SNS} = \frac{V_{SNS,CL1}}{I_{CL1}} = \frac{25mV}{25A} = 1m\Omega \quad (1)$$

A current sense resistance of 1mΩ, 3W (WSL39211L000FEA) is used in this design.

- **Selection of soft-start capacitors, C_{SS} and $C_{SS,VEE}$** : Compute the minimum inrush current where the timer runs during start-up using the Equation 2.

$$I_{INR,\,TMR\,.\,min} = \frac{V_{SNS,\,TMR2\,.\,min}}{R_{SNS}} = \frac{1.5mV}{1m\Omega} = 1.5A \quad (2)$$

To avoid running the timer during inrush, the inrush current must be sufficiently lower than 1.5A. Target 200mA of inrush current for a better FET SOA margin during start-up. Compute the target C_{SS} using the Equation 3.

$$C_{SS} = \frac{C_{OUT} \times I_{GATE,\,SRS,\,START}}{I_{INR,\,TGT}} = \frac{100\mu F \times 20\mu A}{200mA} = 10nF \quad (3)$$

Two multilayer ceramic capacitors (GRM32E5C2J223FWA3L), 0.022µF, 630VDC, and C0G are used in series for C_{SS}. Also, TI recommends adding a capacitor $C_{SS,VEE}$ that is three times larger than C_{SS} between the SS pin and VEE to improve transient immunity during soft start.

Finally, the start-up time can be computed using Equation 4.

$$T_{START} = \frac{C_{SS} \times V_{IN}}{I_{GATE,\,SRS,\,START}} = \frac{11nF \times 800V}{20\mu A} = 440ms \quad (4)$$

- **Selection of VDS switch-over threshold**: The threshold voltage at which the TPS23521 device switches from the lower current threshold ($3mV/R_{SNS}$) to the higher current threshold ($25mV/R_{SNS}$) can be selected through a resistor R_D. A higher VDS threshold provides better transient immunity but exposes the FET to increased SOA stress. Start with a VDS switch-over voltage of 100V and calculate R_D using Equation 5.

$$R_D = 30k\Omega \times \left(\frac{V_{DS,\,SW}}{1.5V} - 1\right) = 30k\Omega \times \left(\frac{100V}{1.5V} - 1\right) = 1970k\Omega \quad (5)$$

Three resistors (TNPV1206680KBEEN) 680KΩ and 700V are used in series. The effective switch-over voltage is obtained as 103.5V.

- **Fault timer selection:** The timer determines how long the hot-swap can allow overload before timing out and can be programmed using C_T. To set 200µs, use Equation 6.

$$C_T = \frac{T_{FLT} \times I_{TMR,\,SRS}}{V_{TMR}} = \frac{200\mu s \times 10\mu A}{1.5V} = 1.3nF \quad (6)$$

A ceramic capacitor (CC0603JRX7R8BB152), 1.5nF is used.

- **Input voltage monitoring:** The OPA210 device is used as a differential amplifier to scale down (gain of R_2/R_1) and monitor the input bus voltage. Select resistors R_1 and R_2 to set gain of 1/10 as in Equation 7.

$$V_{BUS-IN} = \{INPUT(+) - INPUT(-)\} \times \frac{R_2}{R_1} = 800V \times \frac{20.5k\Omega}{3 \times 680k\Omega} = 8V \quad (7)$$

The scaled bus voltage V_{BUS-IN} is used to set the undervoltage and overvoltage threshold on the input bus by following the standard process in the TPS23521 datasheet.

- **FET selection and SOA analysis:** The silicon carbide (SiC) combo JFET (UG3SC120009K4S), 1200V, and 8.8mΩ is used in this design. As documented in reference 2, the FET SOA must be analyzed for three stressful events, such as start-up, start-up into short, and overcurrent events.
  1. During start-up, with an inrush current of 100mA, the system takes approximately 440ms to charge a 100µF output capacitor from 0V to 800V. The UG3SC120009K4S FET can support > 300mA at 70°C with a drain-to-source voltage of 800V, thus providing an SOA margin of > 50%
  2. During a start into short, the gate ramps up very slowly due to a large capacitance at the gate through the SS pin. To evaluate the FET stress, the current pulse must be approximated as a rectangular pulse. In this design, the FET stress is approximated with a 500µs (the equivalent rectangular pulse of the current waveform), 1.5A, and 880V pulse. The UG3SC120009K4S FET can handle a current pulse of 2.2A for 500µs at 880V and a junction temperature of 100°C, thus giving an SOA margin of 50%.

3. During an overload event, the TPS23521 device operates in current limiting mode, which is a risk for the hot-swap FET. To overcome that risk, the INA238 device is configured with an overcurrent alert at 22A, and the alert output of the INA238 device is used to disable the TPS23521 device at the UVEN pin. This function emulates a circuit breaker event without causing any stress on the FET.

- **Power good interface with the downstream load:** The TPS23521 device generates power good (PG) signals with reference to the grounds VEEH and VEEL of the TPS23521 device. These signals are passed through digital isolators and then combined to control the downstream load, which avoids load during start-up, thereby placing very low SOA stress on the hot-swap FETs.
- **Output discharge circuit:** To meet the safety requirements of the IEC 62368-1 standard, the hot-swap solution has incorporated a circuit to discharge the output capacitance in <2 seconds. When the hot-swap FET is turned OFF, or the input is disconnected, the discharge resistor (R_{DIS}) is engaged to discharge COUT. A 2kΩ, 10W resistor (AC10AT0002001JAB00) is selected to discharge 100µF in 1.5 seconds.
- **TVS diode selection:** The transient protection component, TVS diode, can be selected by following the guidelines outlined in reference 3. Two SMCJ400A diodes connected in series are placed at the input side.

5 Test Results

The proposed solution is verified and test results for all the stressful events are presented in this section. Figure 5-1 shows the inrush behavior during start-up while charging a 100µF capacitance to 800V. Figure 5-2 illustrates the start-up behavior of the circuit with a short-circuit at the output terminals. As demonstrated, the current peaks to 3A (lower current limit level), where the TPS23521 device detects and terminates the fault path. In case of a gradual overcurrent fault, the INA238 device alerts at 22A and pulls down the EN pin of the TPS23521 device, thereby disabling the hot-swap FET in 10µs, as shown in Figure 5-3.

Figure 5-4 shows the circuit behavior during an output short-circuit fault in the steady state. The INA238 and TPS23521 devices both detect the fast-rising short-circuit current and disable the FETs in a few µs.

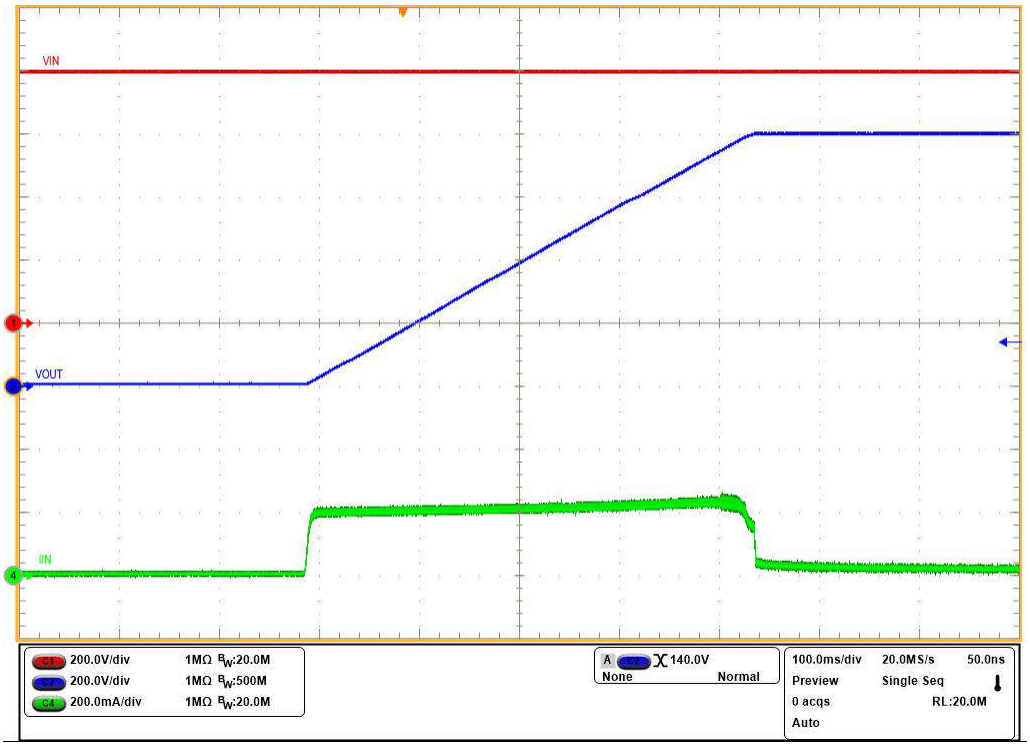

Figure 5-1. Start Up at 800V With 100µF Capacitance

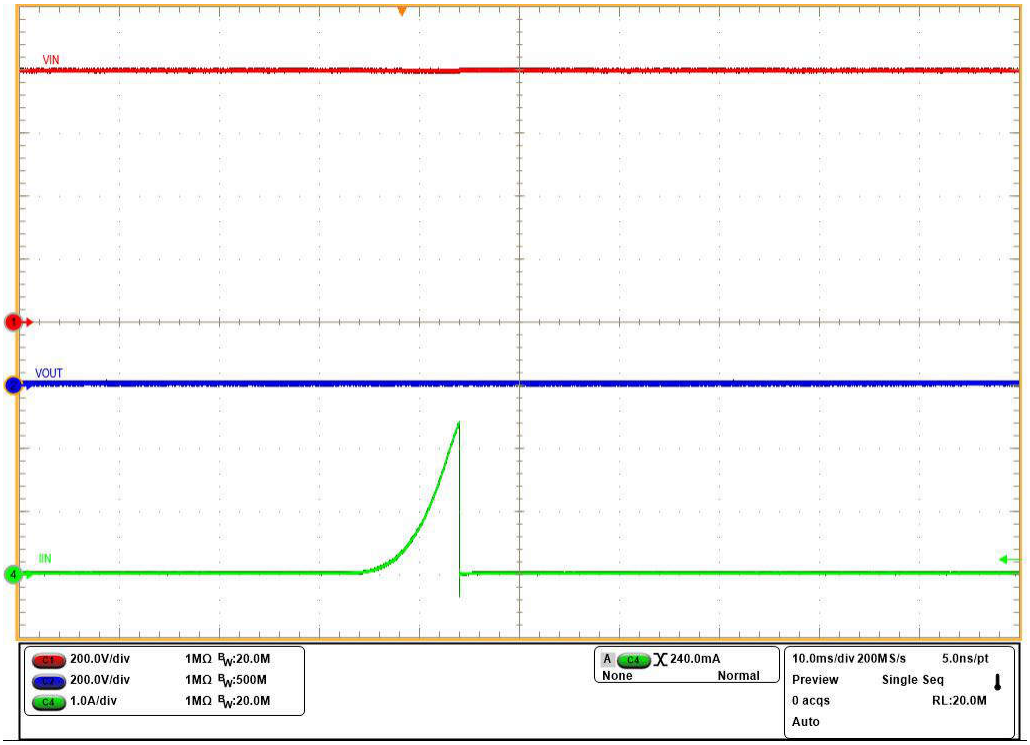

Figure 5-2. Start Up Into Short at 800V VIN

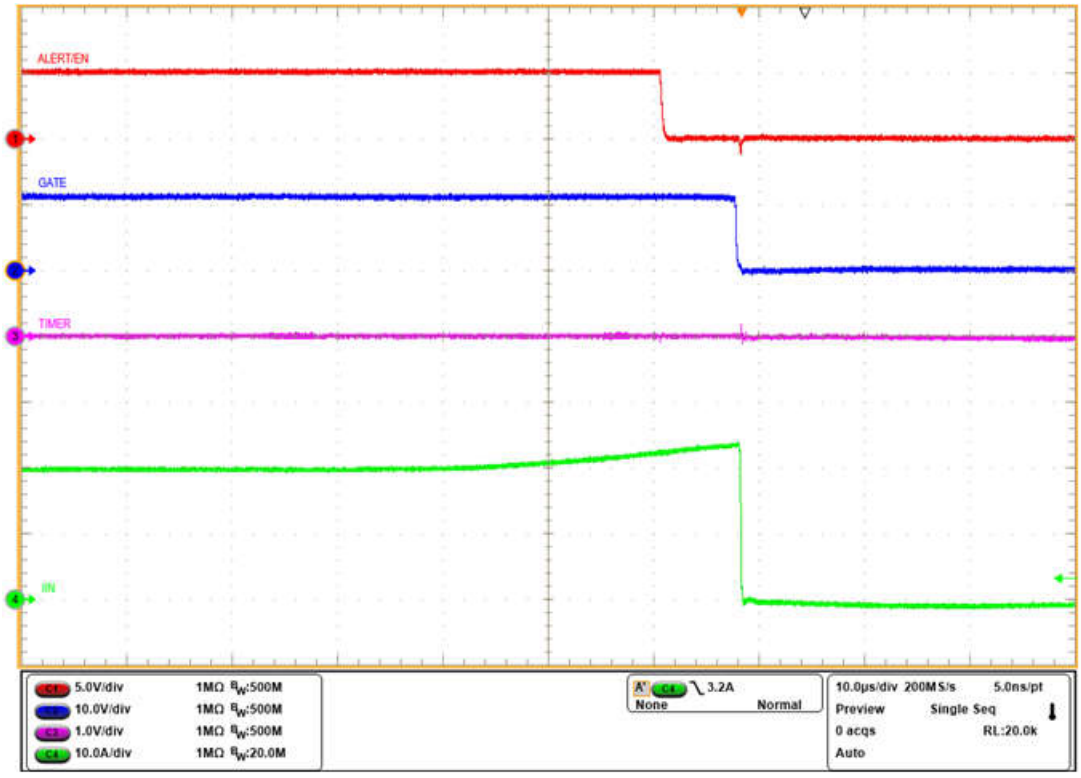

Figure 5-3. Circuit Response During Gradual Overcurrent

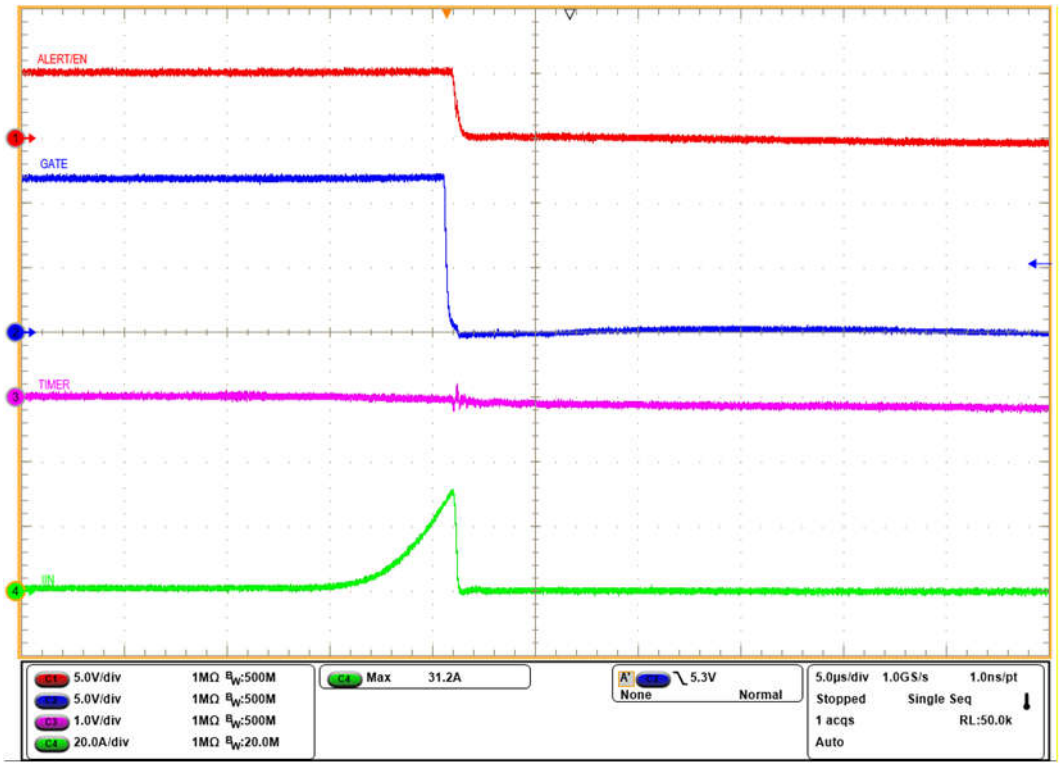

Figure 5-4. Circuit Response During an Output Short Circuit

6 Conclusion

The ever-increasing power levels of server systems have pushed data centers to transition from a traditional AC power distribution to distribute power on an HVDC bus, thus bringing new challenges for system protection and monitoring, particularly during hot-swap events. The proposed floating ground hot-swap architecture enables a scalable and robust protection solution, thereby facilitating faster adoption of an HVDC power distribution in modern data centers.

7 References

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Related Websites

- Texas Instruments, TPS23521 datasheet.
- Texas Instruments, UCC28704 datasheet.
- Texas Instruments, OPA210 datasheet.
- Texas Instruments, INA238 datasheet.
- Texas Instruments, ISO1644 datasheet.
- Texas Instruments, ISOM8110 datasheet.

Keywords: TPS23521, hot-swap, enterprise systems, AI server, Input protection

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