Feature Differences Between TPS65950 and TPS65951

ABSTRACT

This document shows the differences in features, the ball comparison and, the delta registers between the TPS65950 and TPS65951 devices.

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1 Feature Differences Between TPS65950 and TPS65951

Table 1. Feature Differences for TPS65950 and TPS65951

Module	TPS65950	TPS65951	Implication
Power		Remove VSIM LDO	LDO not available
Power		RFID.EN ball not present	Cannot control an external regulator/peripheral
Power		Removed 2nd processor control signals - CLKEN2, INT2 and NSLLEP2	No multiprocessor support for wakeup/sleep, etc.
Power	Battery removal detection not available	Add battery removal detection signal (MANU_BRIX ball)	Additional feature/flexibility
Power	VMBCH comparator threshold is set to 3.2 V.	VMBCH comparator threshold is set to 3.1 V.	
Power	Device can be restarted by pressing PWRON push button for 8 seconds, but this is not default setting at power up, software needs to program the STOPON_PWRON bit after the first power up.	Device can be switched off by pressing PWRON push button for 8 seconds (this is default setting at power up). STOPON_PWRON is set to 1 at power up and is read-only.	PWRON button functionality will be impacted due to the new feature.
Power	The following detections are enabled at power up and can be disabled if required: VBUS and VBAT detection, RTC request, USB and AC charger insertion, PWRON button press.	The following wake-up functions are enabled by default and cannot be disabled: VBUS and VBAT detection, RTC request, USB charger insertion, PWRON button press.	Cannot disable the mentioned wake-up events.
USB	Compliant with OTG version 1.3	OTG 1.3 and 2.0 compliancy selectable by register access (bit 0 of OTHER_FUNC_CTRL).	
USB	VBUS voltage tolerance range is 0 to 7 V	Increased VBUS input voltage tolerance range to –2 V to 20 V in USB device mode	
USB	N/A	Improved USB reset logic as described below: A power down of the USB PHY is performed by setting the PHY_PWR_CTRL[0] PHYPWD bit to 1. It resets the PHY, ULPI state-machine, and USB interrupts. It does not reset the USB registers.	
USB	ULPI bus impedance is 90 Ω.	ULPI bus impedance changed to 50 Ω.	PCB layout will be impacted as compared to TPS65950.
USB	Charge pump output was available on VBUS pin.	Added dedicated output for USB charge pump. New ball VUSBIN.CPOUT	

Table 1. Feature Differences for TPS65950 and TPS65951 (continued)

Module	TPS65950	TPS65951	Implication
BCI	Complete battery charger module available for AC and USB charging.	Replaced battery charger module with state-machine that controls an external charger. Only USB charger is supported.	
BCI	USB charger detection is present.	New USB charger detection module	FSM and software charger detection available for detecting USB100 and USB500 charger type.
BCI	Compliant with battery charging specification ver 1.0	Compliant with battery charging specification ver 1.1	
BCI	N/A	Battery node discharge feature in case of battery removal.	
BCI	No charger LED included	New charger LED indicator available	Charger status can be seen from LED
Audio	N/A	Digital mic decimator performance improved. 0 db PDM inputs involve 0 dBFs data output (with default gain setting: 0dB)	
Audio	Headset UART functionality available	Headset UART functionality removed.	Cannot use UART+audio mode
Audio		One digital mic and PCM BT interface is removed	1. Only one stereo digital uplink path available 2. No Bluetooth® PCM interface available
Audio	Can be master or slave when using audio interface	Must be master on audio interface because CLK256FS ball removed and no FS available for external device	
MADC		Removed external channels ADCIN4, ADCIN5, and ADCIN6. Removed internal channels ADCIN10, ADCIN11 and ADCIN15.	
MADC	Acquisition time is programmable within 5 to 20 µs, default is 12 µs	Increased acquisition time from 5 to 171 6 µs. Default is 12 µs.	
AUX	Keypad available	Removed keypad	No keypad functions
Audio	Vibra driver: Ron (maximum) = 8 Ω	Vibra driver improvement, Ron is reduced. Ron (maximum) = 5 Ω	
USB		Carkit feature removed	No carkit features
USB		VUSB.3P1 output voltage adjustable	

2 Ball Characteristic Comparison

Table 2 shows the ball comparison for TPS65950 and TPS65951.

Table 2. Ball Characteristic Comparison

TPS65950			TPS65951		
NetName	Ball Name	Number of Balls	NetName	Ball Name	Number of Balls
32KCLKOUT	N10	1	32KCLKOUT	J6	1
32KXIN	P16	1	32KXIN	L12	1
32KXOUT	P15	1	32KXOUT	L13	1
ADCIN0	H4	1	ADCIN0	K1	1
ADCIN1	J3	1	ADCIN1	G3	1
ADCIN2	G3	1	ADCIN2	F4	1
AGND	N15	1	AGND	G7	1
AUXL	F1	1	AUXL	E1	1
AUXR	G1	1	AUXR	F3	1

Table 2. Ball Characteristic Comparison (continued)

TPS65950			TPS65951		
NetName	Ball Name	Number of Balls	NetName	Ball Name	Number of Balls
AVSS1	J4 / J6 / J7 / J8 / E5	5	AVSS1	G4	1
AVSS2	R10	1	AVSS2	K7	1
AVSS3	M15	1	AVSS3	K11	1
AVSS4	C7	1	AVSS4	A6	1
BCIAUTO	N1	1			
BKBAT	M14	1	BKBAT	J12	1
BOOT0	K11	1	BOOT0	J13	1
BOOT1	J11	1	BOOT1	G10	1
BT.PCM.VDR/ GPIO16/DIG.MIC.CLK0	C3	1	BT.PCM.VDR/ GPIO16/DIG.MIC.CLK0	C3	1
BT.PCM.VDX/ GPIO17/DIG.MIC.CLK1	C5	1			
			CHRG_DET_N	K6	1
CLK256FS	D13	1			
CLKEN	C6	1	CLKEN	F6	1
CLKEN2	D7	1			
CLKREQ	G10	1	CLKREQ	B13	1
CP.CAPM	T6	1	CP.CAPM	N5	1
CP.CAPP	T7	1	CP.CAPP	N6	1
CP.GND	R6	1	CP.GND	K5	1
CP.IN	R7	1	CP.IN	M5	1
CTSI/ BERDATA.OUT/ ADCIN3	P11	1	ADCIN3	K8	1
DATA0/UART4.TXD	K14	1	DATA0/UART4.TXD	H11	1
DATA1/UART4.RXD	K13	1	DATA1/UART4.RXD	H10	1
DATA2/UART4.RTSI	J14	1	DATA2	G8	1
DATA3/UART4.CTSO/ GPIO.12	J13	1	DATA3/GPIO.12	H9	1
DATA4/GPIO.14	G14	1	DATA4/GPIO.14	F9	1
DATA5/GPIO.3	G13	1	DATA5/GPIO.3	F8	1
DATA6/GPIO.4	F14	1	DATA6/GPIO.4	E10	1
DATA7/GPIO.5	F13	1	DATA7/GPIO.5	E11	1
DGND	H13 / H9 / H10 / H11	4	DGND	G11	1
DIR/GPIO.10	L13	1	DIR/GPIO.10	J10	1
DN/UART3.TXD	T11	1	DN/UART3.TXD	J8	1
DP/UART3.RXD	T10	1	DP/UART3.RXD	J7	1
EAR.M	A7	1	EAR.M	D6	1
EAR.P	A6	1	EAR.P	C6	1
GND.LEFT	C10	1	GND.LEFT	C8	1
GND.LEFT	C9	1			
GND.RIGHT	C11	1	GND.RIGHT	C9	1
GND.RIGHT	C12	1			
GPIO.0/CD1/ JTAG.TD0	P12	1	GPIO.0/CD1/ JTAG.TD0	M8	1
GPIO.1/CD2/ JTAG.TMS	N12	1	GPIO.1/CD2/ JTAG.TMS	L9	1

Table 2. Ball Characteristic Comparison (continued)

TPS65950			TPS65951		
NetName	Ball Name	Number of Balls	NetName	Ball Name	Number of Balls
GPIO.15/TEST2	P13	1	GPIO.15/TEST2	L10	1
GPIO.2/TEST1	L4	1	GPIO.2/TEST1	J3	1
GPIO.6/CLKOK/ PWM0/TEST3	M4	1	GPIO.6/CLKOK/ PWM0/TEST3	K3	1
GPIO.7/ VIBRA.SYNC.PWM1/ TEST4	N14	1	GPIO.7/ VIBRA.SYNC.PWM1/ TEST4	M13	1
HFCLKIN	A14	1	HFCLKIN	B11	1
HFCLKOUT	R12	1	HFCLKOUT	N8	1
HSMIC.M	F3	1	HSMIC.M	E3	1
HSMIC.P	E3	1	HSMIC.P	E4	1
HSOL	B4	1	HSOL	C5	1
HSOR	B5	1	HSOR	A5	1
I2C.CNTL.SCL	D5	1	I2C.CNTL.SCL	D5	1
I2C.CNTL.SDA	D4	1	I2C.CNTL.SDA	E5	1
I2S.CLK	L3	1	I2S.CLK	J4	1
I2S.DIN	K4	1	I2S.DIN	H3	1
I2S.DOUT	K3	1	I2S.DOUT	H4	1
I2S.SYNC	K6	1	I2S.SYNC	K2	1
ICTLAC1	N7	1			
ICTLAC2	P2	1			
ICTLUSB1	P6	1			
ICTLUSB2	P1	1			
ID	R11	1	ID	L8	1
IHF.LEFT.M	B10	1	IHF.LEFT.M	A8	1
IHF.LEFT.P	B9	1	IHF.LEFT.P	B8	1
IHF.RIGHT.M	B12	1	IHF.RIGHT.M	A9	1
IHF.RIGHT.P	B11	1	IHF.RIGHT.P	B9	1
INT1	F10	1	INT1	B10	1
INT2	F9	1			
IO.1P8	C8	1	IO.1P8	E7	1
JTAG.TCK/ BERCLK	B16	1	JTAG.TCK/ BERCLK	D11	1
JTAG.TDI/ BERDATA	A15	1	JTAG.TDI/ BERDATA	B12	1
KPD.C0	G8	1			
KPD.C1	H7	1			
KPD.C2	G6	1			
KPD.C3	F7	1			
KPD.C4	G7	1			
KPD.C5	F4	1			
KPD.C6	H6	1			
KPD.C7	G4	1			
KPD.R0	K9	1			
KPD.R1	K8	1			
KPD.R2	L8	1			
KPD.R3	K7	1			

Table 2. Ball Characteristic Comparison (continued)

TPS65950			TPS65951		
NetName	Ball Name	Number of Balls	NetName	Ball Name	Number of Balls
KPD.R4	L9	1			
KPD.R5	J10	1			
KPD.R6	K10	1			
KPD.R7	L7	1			
LEDA/VIBRA.P	F15	1	LEDA/VIBRA.P	E9	1
LEDB/VIBRA.M	G15	1	LEDB/VIBRA.M	F11	1
LEDGND	F16	1	LEDGND	F10	1
LEDSYNC/GPIO.13	G11	1	LEDSYNC/GPIO.13	A12	1
MANU	L10	1			
			MANU_BRIX	K9	1
MIC.MAIN.M	F2	1	MIC.MAIN.M	E2	1
MIC.MAIN.P	E2	1	MIC.MAIN.P	D2	1
MIC.SUB.M/DIG.MIC.1	H2	1	MIC.SUB.M/DIG.MIC.1	G5	1
MIC.SUB.P/DIG.MIC.0	G2	1	MIC.SUB.P/DIG.MIC.0	F5	1
MICBIAS.GND	D3	1	MICBIAS.GND	D1	1
MICBIAS1.OUT/VMIC1.OUT	D1	1	MICBIAS1.OUT/VMIC1.OUT	B1	1
MICBIAS2.OUT/VMIC2.OUT	D2	1	MICBIAS2.OUT/VMIC2.OUT	C1	1
MSECURE	H8	1	MSECURE	B7	1
NRESPWRON	A13	1	NRESPWRON	C10	1
NRESWARM	B13	1	NRESWARM	A11	1
NSLEEP1	P7	1	NSLEEP1	C11	1
NSLEEP2	G9	1			
NXT/GPIO.11	M13	1	NXT/GPIO.11	J11	1
PCHGAC	N4	1			
PCHGUSB	N6	1			
PCM.VCK	R1	1	PCM.VCK	M1	1
PCM.VDR	T2	1	PCM.VDR	L4	1
PCM.VDX	T15	1	PCM.VDX	H8	1
PCM.VFS	R16	1	PCM.VFS	N12	1
PreDriv.LEFT/VMID	B7	1	PreDriv.LEFT/VMID	E6	1
PreDriv.RIGHT/ADCIN7	B8	1	PreDriv.RIGHT/ADCIN7	D7	1
PWROK1	B14	1			
PWROK2/I2C.SR.SDA	C4	1	PWROK2/I2C.SR.SDA	C4	1
PWRON	A11	1	PWRON	F7	1
REGEN	A10	1	REGEN	D8	1
RFID.EN	A2	1			
RTSO/CLK64K.OUT/ BERCLK.OUT/ADCIN5	N11	1			
RXAF/ADCIN6	N9	1			
START.ADC	J9	1	START.ADC	L11	1
STP/GPIO.9	L14	1	STP/GPIO.9	K10	1
SYSEN	C13	1	SYSEN	E8	1
TEST	A1	1	TEST	A1	1
TEST.RESET	T16	1	TEST.RESET	N13	1
TESTV1	T1	1	TESTV1	N1	1
TESTV2	A16	1	TESTV2	A13	1

Table 2. Ball Characteristic Comparison (continued)

TPS65950			TPS65951		
NetName	Ball Name	Number of Balls	NetName	Ball Name	Number of Balls
TXAF/ADCIN4	N8	1			
UART1.RXD/GPIO.8	D8	1			
UART1.TXD	B1	1			
UCLK	L15	1	UCLK	J9	1
VAC	N5	1			
			USBCHRG_ENZ	J5	1
			USBCHRG_STATZ	H5	1
VAUX1.OUT	M2	1	VAUX1.OUT	J2	1
VAUX12S.IN	L1	1	VAUX12S.IN	H1	1
VAUX2.OUT	M3	1	VAUX2.OUT	J1	1
VAUX3.OUT	G16	1	VAUX3.OUT	F12	1
VAUX4.IN	B2	1	VAUX4.IN	A2	1
VAUX4.OUT	B3	1	VAUX4.OUT	B3	1
VBAT	R5	1	VBAT	L5	1
VBAT.LEFT	D10	1	VBAT.LEFT	A7	1
VBAT.LEFT	D9	1			
VBAT.RIGHT	D11	1	VBAT.RIGHT	A10	1
VBAT.RIGHT	D12	1			
VBAT.USB	R9	1	VBAT.USB	N7	1
			VBATVIBRA	D9	1
VBATS	P4	1			
VBUS	R8	1	VBUS	H7	1
VCCS	P5	1			
VDAC.IN	K1	1	VDAC.IN	G1	1
VDAC.OUT	L2	1	VDAC.OUT	H2	1
VDD1.GND	B15	1	VDD1.GND	C12	1
VDD1.GND	C15	1	VDD1.GND	C13	1
VDD1.GND	C16	1			
VDD1.IN	D14	1	VDD1.IN	E12	1
VDD1.IN	E14	1	VDD1.IN	E13	1
VDD1.IN	E15	1			
VDD1.L	C14	1			
VDD1.L	D15	1	VDD1.SW (1)	D12	1
VDD1.L	D16	1	VDD1.SW (1)	D13	1
VDD1.OUT	E13	1	VDD1.FB (1)	D10	1
VDD2.GND	R15	1	VDD2.GND	M11	1
VDD2.GND	T14	1	VDD2.GND	N11	1
VDD2.IN	P14	1	VDD2.IN	M9	1
VDD2.IN	R13	1	VDD2.IN	N9	1
VDD2.L	R14	1	VDD2.SW(1)	M10	1
VDD2.L	T13	1	VDD2.SW(1)	N10	1
VDD2.OUT	N13	1	VDD2.FB(1)	M12	1
VHSMIC.OUT	E4	1	VHSMIC.OUT	D3	1
VINT.IN	K15	1	VINT.IN	H13	1
VINTANA1.OUT	H3	1	VINTANA1.OUT	F2	1

(1) Different name but same function

Table 2. Ball Characteristic Comparison (continued)

TPS65950			TPS65951		
NetName	**Ball Name**	**Number of Balls**	**NetName**	**Ball Name**	**Number of Balls**
VINTANA2.OUT	B6	1	VINTANA2.OUT	B6	1
VINTANA2.OUT	J2	1	VINTANA2.OUT	F1	1
VINTDIG.OUT	L16	1	VINTDIG.OUT	H12	1
VINTUSB1P5.OUT	P8	1	VINTUSB1P5.OUT	M6	1
VINTUSB1P8.OUT	P10	1	VINTUSB1P8.OUT	M7	1
VIO.GND	R2	1	VIO.GND	L3	1
VIO.GND	T3	1	VIO.GND	M2	1
			VIO.GND	N2	1
VIO.IN	P3	1	VIO.IN	M4	1
VIO.IN	R4	1	VIO.IN	N4	1
VIO.L	R3	1	VIO.SW (2)	M3	1
VIO.L	T4	1	VIO.SW (2)	N3	1
VIO.OUT	N3	1	VIO.FB (2)	L2	1
VMMC1.IN	C1	1	VMMC1.IN	C2	1
VMMC1.OUT	C2	1	VMMC1.OUT	B2	1
VMMC2.IN	A3	1	VMMC2.IN	A4	1
VMMC2.OUT	A4	1	VMMC2.OUT	B4	1
VMODE1	F8	1			
VMODE2/I2C.SR.SCL	D6	1	VMODE2/I2C.SR.SCL	B5	1
VPLLA3R.IN	H15	1	VPLLA3R.IN	F13	1
VPPL1.OUT	H14	1	VPPL1.OUT	G9	1
VPRECH	N2	1	VPRECH	L1	1
			VPROG	K4	1
VREF	N16	1	VREF	K13	1
			VREFGND	K12	1
VRTC.OUT	K16	1	VRTC.OUT	G12	1
VSDI.CSI.OUT	J15	1	VSDI.CSI.OUT	G13	1
VSIM.OUT	K2	1			
			VSL.OUT	G2	1
VUSB.3P1	P9	1	VUSB.3P1	L7	1
			VUSBIN.CPOUT	L6	1
Total number of balls		**209**			**164**

(2) Different name but same function

3 Register Differences

Table 3. Audio Registers

Address	Register Name	TPS65950	TPS65951	Comment
0x82	PIH_ISR_P2	Register is used	Register is spare	INT2 is removed.
0x87	INTBR_IDCODE_23_16	Value 0x09	Value 0x77	Device IDCODE is different.
0x88	INTBR_IDCODE_31_24	Value 0x10	Value 0x2b	Device IDCODE is different.
0x99	GPIODATAIN2	Bit [0] is used	Bit [0] is spare	GPIO8 is removed.
0x9A	GPIODATAIN3	Bit [1] is used	Bit [1] is spare	GPIO17 is removed.
0x9C	GPIODATADIR2	Bit [0] is used	Bit [0] is spare	GPIO8 is removed.
0x9D	GPIODATADIR3	Bit [1] is used	Bit [1] is spare	GPIO17 is removed.
0x9F	GPIODATAOUT2	Bit [0] is used	Bit [0] is spare	GPIO8 is removed.
0xA0	GPIODATAOUT3	Bit [1] is used	Bit [1] is spare	GPIO17 is removed.
0xA2	GPIO_CLEARGPIODATAOUT2	Bit [0] is used	Bit [0] is spare	GPIO8 is removed.
0xA3	GPIO_CLEARGPIODATAOUT3	Bit [1] is used	Bit [1] is spare	GPIO17 is removed.
0xA5	GPIO_SETGPIODATAOUT2	Bit [0] is used	Bit [0] is spare	GPIO8 is removed.
0xA6	GPIO_SETGPIODATAOUT3	Bit [1] is used	Bit [1] is spare	GPIO17 is removed.
0xA8	GPIO_DEBEN2	Bit [0] is used	Bit [0] is spare	GPIO8 is removed.
0xA9	GPIO_DEBEN3	Bit [1] is used	Bit [1] is spare	GPIO17 is removed.
0xAD	GPIOPUPDCTR3	Bits [1:0] used	Bits [1:0] spare	GPIO8 is removed.
0xAF	GPIOPUPDCTR5	Bits [3:2] used	Bits [3:2] spare	GPIO17 is removed.
0xB2	GPIO_ISR2A	Bit [0] is used	Bit 0 is spare	GPIO8 is removed.
0xB3	GPIO_ISR3A	Bit [1] is used	Bit 1 is spare	GPIO17 is removed.
0xB5	GPIO_IMR2A	Bit [0] is used	Bit 0 is spare	GPIO8 is removed.
0xB6	GPIO_IMR3A	Bit [1] is used	Bit 1 is spare	GPIO17 is removed.
0xB7	GPIO_ISR1B	Register is used	Register is spare	Because INT2 is removed, this register is not used.
0xB8	GPIO_ISR2B	Register is used	Register is spare	Because INT2 is removed, this register is not used.
0xB9	GPIO_ISR3B	Register is used	Register is spare	Because INT2 is removed, this register is not used.
0xBA	GPIO_IMR1B	Register is used	Register is spare	Because INT2 is removed, this register is not used.
0xBB	GPIO_IMR2B	Register is used	Register is spare	Because INT2 is removed, this register is not used.
0xBC	GPIO_IMR3B	Register is used	Register is spare	Because INT2 is removed, this register is not used.
0xC2	GPIO_EDR3	Bits [1:0] used	Bits [1:0] spare	GPIO8 is removed.
0xC4	GPIO_EDR5	Bits [3:2] used	Bits [3:2] spare	GPIO17 is removed.

Table 4. USB Registers

Address	Register Name	TPS65950	TPS65951	Comment
0x00	PRODUCT_ID_LOW	0x2	0x5	USB ID changed
0x19	CARKIT_CTRL	Bits [6:4] and [0] used for audio	Bits [6:4] and [0] reserved	Feature removed
0x1A	CARKIT_CTRL_SET	Bits [6:4] and [0] used for audio	Bits [6:4] and [0] reserved	Feature removed
0x1B	CARKIT_CTRL_CLR	Bits [6:4] and [0] used for audio	Bits [6:4] and [0] spare	Feature removed
0x1C	CARKIT_INT_DELAY	Bits [6:0] used	Bits [6:0] spare	Feature removed
0x1D	CARKIT_INT_EN	Bits [4:2] used	Bits [4:2] spare	Feature removed
0x1E	CARKIT_INT_EN_SET	Bits [4:2] used	Bits [4:2] spare	Feature removed
0x1F	CARKIT_INT_EN_CLR	Bits [4:2] used	Bits [4:2] spare	Feature removed
0x20	CARKIT_INT_STS	Bits [2:1] used	Bits [2:1] reserved	Feature removed
0x21	CARKIT_INT_LATSH	Bits [2:1] used	Bits [2:1] reserved	Feature removed
0x22	CARKIT_PLS_CTRL	Bits [3:0] used	Bits [3:0] spare	Feature removed
0x23	CARKIT_PLS_CTRL_SET	Bits [3:0] used	Bits [3:0] spare	Feature removed
0x24	CARKIT_PLS_CTRL_CLR	Bits [3:0] used	Bits [3:0] spare	Feature removed
0x25	TRANS_POS_WIDTH	Bits [7:0] used	Bits [7:0] spare	Feature removed
0x26	TRANS_NEG_WIDTH	Bits [7:0] used	Bits [7:0] spare	Feature removed
0x27	RCV_PLTY_RECOVERY	Bits [7:0] used	Bits [7:0] spare	Feature removed
0x30	MCPC_CTRL	Bits [7:2] used	Bits [7:2] spare	Feature removed
0x31	MCPC_CTRL_SET	Bits [7:2] used	Bits [7:2] spare	Feature removed
0x32	MCPC_CTRL_CLR	Bits [7:2] used	Bits [7:2] spare	Feature removed
0x33	MCPC_IO_CTRL	Bits [5]/[3]/[2] used	Bits [5]/[3]/[2] spare	Feature removed
0x34	MCPC_IO_CTRL_SET	Bits [5]/[3]/[2] used	Bits [5]/[3]/[2] spare	Feature removed
0x35	MCPC_IO_CTRL_CLR	Bits [5]/[3]/[2] used	Bits [5]/[3]/[2] spare	Feature removed
0x80	OTHER_FUNC_CTRL	Bits [7:6] and [2] used	Bits [7:6] and [2] spare, bit 0 used	New feature added in TPS65951. Bit 0: If 0, then OTG 1.3 and if 1 then OTG 2.0.
0x81	OTHER_FUNC_CTRL_SET	Bits [7:6] and [2] used	Bits [7:6] and [2] spare	Feature removed
0x82	OTHER_FUNC_CTRL_CLR	Bits [7:6] and [2] used	Bits [7:6] and [2] spare	Feature removed
0x83	OTHER_IFC_CTRL	Bit [1] used	Bit [1] spare	Feature removed
0x84	OTHER_IFC_CTRL_SET	Bit [1] used	Bit [1] spare	Feature removed
0x85	OTHER_IFC_CTRL_CLR	Bit [1] used	Bit [1] spare	Feature removed
0x86	OTHER_INT_EN_RISE	Bit [1] used	Bit [1] spare	Feature removed
0x87	OTHER_INT_EN_RISE_SET	Bit [1] used	Bit [1] spare	Feature removed
0x88	OTHER_INT_EN_RISE_CLR	Bit [1] used	Bit [1] spare	Feature removed
0x89	OTHER_INT_EN_FALL	Bit [1] used	Bit [1] spare	Feature removed
0x8A	OTHER_INT_EN_FALL_SET	Bit [1] used	Bit [1] spare	Feature removed
0x8B	OTHER_INT_EN_FALL_CLR	Bit [1] used	Bit [1] spare	Feature removed
0x8C	OTHER_INT_STS	Bit [1] used	Bit [1] spare	Feature removed
0x8D	OTHER_INT_LATCH	Bit [1] used	Bit [1] spare	Feature removed
0x97	CARKIT_SM_1_INT_EN		Register removed	Feature removed
0x98	CARKIT_SM_1_INT_EN_SET		Register removed	Feature removed
0x99	CARKIT_SM_1_INT_EN_CLR		Register removed	Feature removed
0x9A	CARKIT_SM_1_INT_STS		Register removed	Feature removed
0x9B	CARKIT_SM_1_INT_LATCH		Register removed	Feature removed
0x9C	CARKIT_SM_2_INT_EN		Register removed	Feature removed
0x9D	CARKIT_SM_2_INT_EN_SET		Register removed	Feature removed
0x9E	CARKIT_SM_2_INT_EN_CLR		Register removed	Feature removed

Table 4. USB Registers (continued)

0x9F	CARKIT_SM_2_INT_STS		Register removed	Feature removed
0xA0	CARKIT_SM_2_INT_LATCH		Register removed	Feature removed
0xA1	CARKIT_SM_CTRL		Register removed	Feature removed
0xA2	CARKIT_SM_CTRL_SET		Register removed	Feature removed
0xA3	CARKIT_SM_CTRL_CLR		Register removed	Feature removed
0xA4	CARKIT_SM_CMD		Register removed	Feature removed
0xA5	CARKIT_SM_CMD_SET		Register removed	Feature removed
0xA6	CARKIT_SM_CMD_CLR		Register removed	Feature removed
0xA7	CARKIT_SM_CMD_STS		Register removed	Feature removed
0xA8	CARKIT_SM_STATUS		Register removed	Feature removed
0xA9	CARKIT_SM_NEXT_STATUS		Register removed	Feature removed
0xAA	CARKIT_SM_ERR_STATUS		Register removed	Feature removed
0xAB	CARKIT_SM_CTRL_STATE		Register removed	Feature removed
0xC2	TPH_DP_CON_MIN		Register removed	Feature removed
0xB8	OTHER_FUNC_CTRL2	Bits [7:1] reserved	Bits [7:1] used	New feature added in TPS65951. Added control for modifying output impedance and drive strength in HS mode for improving eye-diagram.
0xB9	OTHER_FUNC_CTRL2	Bits [7:1] reserved	Bits [7:1] used	New feature added in TPS65951. Added control for modifying output impedance and drive strength in HS mode for improving eye-diagram.
0xBA	OTHER_FUNC_CTRL2	Bits [7:1] reserved	Bits [7:1] used	New feature added in TPS65951. Added control for modifying output impedance and drive strength in HS mode for improving eye-diagram.
0xC3	TPH_DP_CON_MAX		Register removed	Feature removed
0xC4	TCR_DP_CON_MIN		Register removed	Feature removed
0xC5	TCR_DP_CON_MAX		Register removed	Feature removed
0xC6	TPH_DP_PD_SHORT		Register removed	Feature removed
0xC7	TPH_CMD_DLY		Register removed	Feature removed
0xC8	TPH_DET_RST		Register removed	Feature removed
0xC9	TPH_AUD_BIAS		Register removed	Feature removed
0xCA	TCR_UART_DET_MIN		Register removed	Feature removed
0xCB	TCR_UART_DET_MAX		Register removed	Feature removed
0xCD	TPH_ID_INT_PW		Register removed	Feature removed
0xCE	TACC_ID_INT_WAIT		Register removed	Feature removed
0xCF	TACC_ID_INT_PW		Register removed	Feature removed
0xD0	TPH_CMD_WAIT		Register removed	Feature removed
0xD1	TPH_ACK_WAIT		Register removed	Feature removed
0xD2	TPH_DP_DISC_DET		Register removed	Feature removed
0xE0	CARKIT_4W_DEBUG		Register removed	Feature removed
0xE1	CARKIT_5W_DEBUG		Register removed	Feature removed
0xF6	PSM_EN_TEST_SET		Register removed	Feature removed
0xF7	PSM_EN_TEST_CLR		Register removed	Feature removed

Table 5. Power Registers

Address	Register Name	TPS65950	TPS65951	Comment
0x2E	PWR_ISR1	Bit [5] unused Bit [1] used	Bit 5 used Bit 1 spare	Bit [5] used for battery presence, hardware pin is MANU_BRIX. No VAC capability available, so no CHG_PRES interrupt.
0x2F	PWR_IMR1	Bit [5] unused Bit [1] used	Bit 5 used Bit 1 spare	Bit [5] used for battery presence, hardware pin is MANU_BRIX. No VAC capability available, so no CHG_PRES interrupt.
0x30	PWR_ISR2	Used	Spare	INT2 removed
0x31	PWR_IMR2	Used	Spare	INT2 removed
0x33	PWR_EDR1	Bits [3:2] used	Bits [3:2] spare	No VAC capability available, so no CHG_PRES interrupt
0x34	PWR_EDR2	Bits [5:4] spare	Bits [5:4] used	Used for battery presence, hardware pin is MANU_BRIX.
0x36	CFG_P1_TRANSITION	R/W, reset 0xFF	RO, reset 3F Bit 1 spare	Not possible to mask power-up events anymore (STARTON_xxx). Bit [7] (SWBUG) power up event is removed. Bit [1] not used as VAC capability is removed.
0x37	CFG_P2_TRANSITION	R/W, reset 0xFF	RO, reset 3F Bit 1 spare	Not possible to mask power-up events anymore (STARTON_xxx). Bit [7] (SWBUG) power-up event is removed. Bit [1] not used as VAC capability is removed.
0x38	CFG_P3_TRANSITION	R/W, reset 0xFF	RO, reset 0x7F Bit 1 spare	Not possible to mask power-up events anymore (STARTON_xxx). Bit [7] (SWBUG) power-up event is removed. Bit [1] not used as VAC capability is removed.
0x39	CFG_P123_TRANSITION	Bits [6:0] R/W, reset 0x2B	Bits [6:0] RO, reset 0x2B	Because bits [6:0] are RO in TPS65951 it is not possible to change these features. Refer to detailed description in the register file. *Bit [7] is EEPROM dependant; must take care to set it properly for software compatiblity.
0x3D	BOOT_BCI	Used	Spare	BCI module is removed so this register is not used.
0x44	PROTECTED_KEY	Bits [7:0]	Bits [7:0]	config_key unlock sequence modified Refer to register manual.
0x45	STS_HW_CONDITION	Bit [5] Bit [1] used	Bit [5] Bit [1] spare	Internally the two control signals SLEEP1 and SLEEP2 are tied together. Both of these internal signals can be controlled by SLEEP1 (available externally). Bit [1] (STS_CHG) always 0 as no VAC.
0x46	P1_SW_EVENTS	Bit [6] R/W, reset 0	Bit [6] RO, reset 1	STOPON_PWRON always on (PWRON_8s feature cannot be disabled)
0x47	P2_SW_EVENTS	Bit [6] R/W, reset 0	Bit [6] RO, reset 1	STOPON_PWRON always on (PWRON_8s feature cannot be disabled)

Table 5. Power Registers (continued)

Address	Register Name	TPS65950	TPS65951	Comment
0x48	P3_SW_EVENTS	Bit [6] R/W, reset 0	Bit [6] RO, reset 1	STOPON_PWRON always on (PWRON_8s feature cannot be disabled)
0x51	RESERVED_E	Bits [2:0] reserved	Bits [2:0] RW, reset 0x7	VBUS/ID power-up event debounce time increased to 233 ms to disable USB 500 charger detection compliancy.
0x68	MISC_CFG	Bit [4] reset = 1	Bit [4] reset = 0	32k drive capability default is 5 pF now (instead of 40 pF)
0x92	VSIM_DEV_GRP	Used	Spare	VSIM removed in TPS65951
0x93	VSIM_TYPE	Used	Spare	VSIM removed in TPS65951
0x94	VSIM_REMAP	Used	Spare	VSIM removed in TPS65951
0x95	VSIM_DEDICATED	Used	Spare	VSIM removed in TPS65951
0xD8	VUSB_DEDICATED1	Bits [7:5]: Reserved Bit [3]: SW2VBAT Bit [2]: SW2VBUS	Bits [7:5]: VSEL, RW Bits [3:2]: USBIN_SW, RW, Reset: 0x1	Refer to new register description and the specifications for new architecture on TPS65951.
0xE9	32KCLKOUT_DEV_GRP	Bits [7:5] RW	Bits [7:5] RO	32k clock resource cannot be unassigned to the processors: always on in ACTIVE state.
0xEB	32KCLKOUT_REMAP	Bits [3:0] RW	Bits [3:0] RO	32k clock resource active state cannot be remap: always on in ACTIVE state.
0xEF	MAINREF_DEV_GRP	Bits [7:5] RW	Bits [7:5] RO	Main ref resource cannot be unassigned to the processors: always on in ACTIVE state
0xF1	MAINREF_REMAP	Bits [3:0] RW	Bits [3:0] RO	Main ref resource active state cannot be remap: always on in ACTIVE state.

Table 6. Auxillary Registers

Address	Register Name	TPS65950	TPS65951	Comment
0x02	RTSELECT_LSB	Bits [6:4] used	Bits [6:4] spare	External channels ADCIN4, ADCIN5, and ADCIN6 removed
0x3	RTSELECT_M+B43SB	Bits [3:2] used	Bits [3:2] spare	Channel 10 (ICHG), 11 (VCHG), 15 (USBMEAS) removed
0x04	RTAVERAGE_LSB	Bits [6:4] used	Bits [6:4] spare	External channels ADCIN4-5-6 removed
0x05	RTAVERAGE_MSB	Bits [3:2] used	Bits [3:2] spare	Channel 10 (ICHG), 11 (VCHG), 15 (USBMEAS) removed
0x06	SW1SELECT_LSB	Bits [6:4] used	Bits [6:4] spare	External channels ADCIN4, ADCIN5, and ADCIN6 removed
0x07	SW1SELECT_MSB	Bits [3:2] used	Bits [3:2] spare	Channel 10 (ICHG), 11 (VCHG), 15 (USBMEAS) removed
0x08	SW1AVERAGE_LSB	Bits [6:4] used	Bits [6:4] spare	External channels ADCIN4, ADCIN5, and ADCIN6 removed
0x09	SW1AVERAGE_MSB	Bits [3:2] used	Bits [3:2] spare	Channel 10 (ICHG), 11 (VCHG), 15 (USBMEAS) removed
0x0A	SW2SELECT_LSB	Bits [6:4] used	Bits [6:4] spare	External channels ADCIN4, ADCIN5, and ADCIN6 removed
0x0B	SW2SELECT_MSB	Bits [3:2] used	Bits [3:2] spare	Channel 10 (ICHG), 11 (VCHG), 15 (USBMEAS) removed
0x0C	SW2AVERAGE_LSB	Bits [6:4] used	Bits [6:4] spare	External channels ADCIN4, ADCIN5, and ADCIN6 removed
0x0D	SW2AVERAGE_MSB	Bits [3:2] used	Bits [3:2] spare	Channel 10 (ICHG), 11 (VCHG), 15 (USBMEAS) removed
0x0F	ACQUISITION	Bits [7:4] reserved	Bits [7:4] used	Test register became functional register: acquistion time can be configured in a wider range and applies to all conversions.
0x12	CTRL_SW1	Bit [3] used	Bit [3] spare	No EOC_BCI as no more BCI conversion
0x13	CTRL_SW2	Bit [3] used	Bit [3] spare	No EOC_BCI as no more BCI conversion
0x1F	RTCH4_LSB		Spare	External channel ADCIN4 removed
0x20	RTCH4_MSB		Spare	External channel ADCIN4 removed
0x21	RTCH5_LSB		Spare	External channel ADCIN5 removed
0x22	RTCH5_MSB		Spare	External channel ADCIN5 removed
0x23	RTCH6_LSB		Spare	External channel ADCIN6 removed
0x24	RTCH6_MSB		Spare	External channel ADCIN6 removed
0x2B	RTCH10_LSB		Spare	ICHG channel removed
0x2C	RTCH10_MSB		Spare	ICHG channel removed
0x2D	RTCH11_LSB		Spare	VCHG channel removed
0x2E	RTCH11_MSB		Spare	VCHG channel removed
0x3F	GPCH4_LSB		Spare	External channel ADCIN4 removed
0x40	GPCH4_MSB		Spare	External channel ADCIN4 removed
0x41	GPCH5_LSB		Spare	External channel ADCIN5 removed
0x42	GPCH5_MSB		Spare	External channel ADCIN5 removed

Table 6. Auxillary Registers (continued)

Address	Register Name	TPS65950	TPS65951	Comment
0x43	GPCH6_LSB		Spare	External channel ADCIN6 removed
0x44	GPCH6_MSB		Spare	External channel ADCIN6 removed
0x4B	GPCH10_LSB		Spare	ICHG channel removed
0x4C	GPCH10_MSB		Spare	ICHG channel removed
0x4D	GPCH11_LSB		Spare	VCHG channel removed
0x4E	GPCH11_MSB		Spare	VCHG channel removed
0x57	BCICH0_LSB		Spare	BCI conversions removed
0x58	BCICH0_MSB		Spare	BCI conversions removed
0x59	BCICH1_LSB		Spare	BCI conversions removed
0x5A	BCICH1_MSB		Spare	BCI conversions removed
0x5B	BCICH2_LSB		Spare	BCI conversions removed
0x5C	BCICH2_MSB		Spare	BCI conversions removed
0x5D	BCICH3_LSB		Spare	BCI conversions removed
0x5E	BCICH3_MSB		Spare	BCI conversions removed
0x5F	BCICH4_LSB		Spare	BCI conversions removed
0x60	BCICH4_MSB		Spare	BCI conversions removed
0x63	MADC_ISR2		Spare	INT2 line removed
0x64	MADC_IMR2		Spare	INT2 line removed
0x74 → 0xC6	BCI registers			GAIA BCI removed and replaced: refer to TPS65951 BCI register description
0xE5	KEYP_ISR2		Spare	INT2 line removed
0xE6	KEYP_IMR2		Spare	INT2 line removed

4 TPS65951 Registers – Accessory and BCI

This section presents a summary of the hardware interface for the TPS65951 product. Each module instance within the design is shown below, together with the module register map and bit definitions for each bit field.

4.1 Instance Summary

The table below shows the base address and address space for the TPS65951 module instances.

Table 7. Instance Summary

Module Name	Base Address	Size
ACCESSORY VINTDIG	0x0000 0074	43 bytes
BCC VPRECH	0x0000 00AA	21 bytes

4.2 ACCESSORY VINTDIG

This section provides information on the accessories module instances within this product. Each of the registers within the module instance is described separately below.

4.2.1 ACCESSORY VINTDIG Register Summary

Table 8. ACCESSORY VINTDIG Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset
AUDIO_CTRL	RW	8	0x00	0x81
BCIA_CTRL	RW	8	0x00	0x82
SPARE1	RO	8	0x00	0x8D
SPARE2	RW	8	0x00	0x8E
FACTDATA0	RO	8	0x00	0x8F
FACTDATA1	RO	8	0x00	0x90
FACTDATA2	RO	8	0x00	0x91
FACTDATA3	RO	8	0x00	0x92
FACTDATA4	RO	8	0x00	0x93
FACTDATA5	RO	8	0x00	0x94
FACTDATA6	RO	8	0x00	0x95
FACTDATA7	RO	8	0x00	0x96
FACTDATA8	RO	8	0x00	0x97
FACTDATA9	RO	8	0x00	0x98
FACTDATA10	RO	8	0x00	0x99

4.2.2 ACCESSORY VINTDIG Register Description

Table 9. AUDIO_CTRL

Address Offset	0x81
Description	
Type	RW

7	6	5	4	3	2	1	0
RESERVED				RX2TX_PATH_EN			RX2TX_LOOP_EN

Bits	Field Name	Description	Type	Reset
7:4	RESERVED		RO R returns 0s	0x0
3:1	RX2TX_PATH_EN	Audio loop path selection. Only available if RX2TX_LOOP_EN bit is set to 1. 0x0: Audio Left path 1 is root. 0x1: Audio Right path 1 is root. 0x2: Audio Left path 2 is root. 0x3: Audio Right path 2 is root. 0x4: Voice path is root.	RW	0x0
0	RX2TX_LOOP_EN	Audio loop path defined in RX2TX_PATH_SEL register is set when this bit is set to 1.	RW	0

Table 10. BCIA_CTRL

Address Offset	0x82
Description	
Type	RW

7	6	5	4	3	2	1	0
RESERVED					BTEMP_EN	RESERVED	MESBAT_EN

Bits	Field Name	Description	Type	Reset
7:3	RESERVED		RO R returns 0s	0x00
2	BTEMP_EN	Must be set to 1 before TEMP measure through MADC	RW	0
1	RESERVED		RO R returns 0s	0
0	MESBAT_EN	Must be set to 1 before battery measure through MADC	RW	0

Table 11. SPARE1

Address Offset	0x8D
Description	
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO	0X00

Table 12. SPARE2

Address Offset	0x8E
Description	
Type	RW

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RW	0X00

Table 13. FACTDATA0

Address Offset	0x8F
Description	EEPROM register bits
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO	0X00

Table 14. FACTDATA1

Address Offset	0x90
Description	EEPROM register bits
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO	0X00

Table 15. FACTDATA2

Address Offset	0x91
Description	EEPROM register bits
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO	0X00

Table 16. FACTDATA3

Address Offset	0x92
Description	EEPROM register bits
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO	0X00

Table 17. FACTDATA4

Address Offset	0x93
Description	EEPROM register bits
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO	0X00

Table 18. FACTDATA5

Address Offset	0x94
Description	EEPROM register bits
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO	0X00

Table 19. FACTDATA6

Address Offset	0x95
Description	EEPROM register bits
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO	0X00

Table 20. FACTDATA7

Address Offset	0x96
Description	EEPROM register bits
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO R returns 0s	0X00

Table 21. FACTDATA8

Address Offset	0x97
Description	EEPROM register bits
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO R returns 0s	0X00

Table 22. FACTDATA9

Address Offset	0x98
Description	
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO R returns 0s	0X00

Table 23. FACTDATA10

Address Offset	0x99
Description	
Type	RO

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RO R returns 0s	0X00

4.3 Battery Charger Control VPRECH – Battery Charger Controller (VPRECH Domain)

This section provides information on the BCC Module Instance within this product. Each of the registers within the Module Instance is described separately below.

4.3.1 BCC VPRECH Register Summary

Table 24. ACC_VPRECH Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Physical Address
BCC_CTRL	RW	8	0x04	0xAA
BCC_CTRL2	RW	8	0x00	0xAB
BCC_STS	RO	8	0x20	0xAC
USB_CHRG_CTRL1	RW	8	0x00	0xAD
USB_CHRG_CTRL2	RW	8	0x00	0xAE
LED_DRIVER_CTRL	RW	8	0x02	0xAF
FACTCFG0_VPRCH	RW	8	0x40	0xB3
FACTCFG1_VPRCH	RW	8	0x00	0xB4
SPARE1_VPRECH	RW	8	0x00	0xB5
SPARE2_VPRECH	RO	8	0x00	0xB6
BCIISR1	RW	8	0x00	0xB9
BCIIMR1	RW	8	0x7F	0xBA
BCISIR	RW	8	0x00	0xBD
BCIEDR1	RW	8	0x66	0xBE
BCISIHCTRL	RW	8	0x00	0xC0

4.3.2 ACC_VRPECH Register Descriptions

Table 25. BCC_CTRL

Address Offset	0xAA
Description	Battery charger controller (BCC) enable and status bits.
Type	RW

7	6	5	4	3	2	1	0
RESERVED				WATCHDOG_MAX_CHGEN_TIME		WATCHDOG_RST	SW_CHRGOFF

Bits	Field Name	Description	Type	Reset
7:4	RESERVED		RO R returns0s	0x0
3:2	WATCHDOG_MAX_ CHGEN_TIME	Set the value of watchdog maximum charger enable time when CHGMODE_SW is set to 1. 00: Counter maximum value set to 16 seconds. 01: Counter maximum value set to 32 seconds. 10: Counter maximum value set to 64 seconds. 11: Counter maximum value set to 127 seconds.	RW	0x1
1	WATCHDOG_RST	0: Normal operation mode 1: Watchdog is reset. Maximum counter value is load. Set automatically to 0. Value 1 is not available on OCP read access.	RW W Toggle	0
0	SW_CHRGOFF	0: Normal operation mode 1: Reset all charger logic and enable signals Software reset of all charger logic and control signals. Clear of the reset is done by writing 0 in the register.	RW W Toggle	0

Table 26. BCC_CTRL2

Address Offset	0xAB
Description	Battery charger controller (BCC) software control register.
Type	RW

7	6	5	4	3	2	1	0
RESERVED			SW_USB_DET_EN	RESERVED	SW_VACCHRG_EN	SW_USBCHARG_EN	CHGMODE_SW

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		RO	0x0
4	SW_USB_DET_EN	SW enable of USB detection. Enable charger detection (used to enable CHGD IBIAS block).	RW	0
3	SW_CHRG_DET	SelectUSB charger driven current . Only active when CHMODE_SW is set to 1. Set CHRG_DET signal. Status of CHRG_EN signal when CHMODE_SW is set to 0. 0: 100-mA charger type 1: 500-mA charger type	RW	0
2	RESERVED		RO	0x0
1	SW_USBCHRG_EN	Only active when CHMODE_SW is set to 1. Set USBCHRG_EN signal. 0: USBCHRG_EN signal is 0 (USB charger is disabled). 1: USBCHRG_EN signal is 1 (USB charger is enabled). Status of USBCHRG_EN signal when CHMODE_SW is set to 0. Read 0: USBCHRG_EN signal is 0 (USB charger is disabled). Read 1: USBCHRG_EN signal is 1 (USB charger is enabled). This bit is reset to 0 wheh the BATTERY_PRESENCE signal is 0 (battery pack is removed).	RW	0
0	CHGMODE_SW	When set to 1, software directly controls enable signals. FSM control is bypass and FSM is reset. 0: Software control is disabled. 1: Software control is enabled. Cannot be set to 0 by software access.	RW	0

Table 27. BCC_STS

Address Offset	0xAC
Description	Battery charger controller (BCC) status bits.
Type	RO

7	6	5	4	3	2	1	0
RESERVED		VPRECH_STS	BATTERY_PRESENCE_STS	RESERVED	USB_P_STS	USB_DET_STS	

Bits	Field Name	Description	Type	Reset
7:6	RESERVED		RO	0x0
5	VPRECH_STS	Asserted when VPRECH supply is present. Read 0: VPRECH not present or under reset Read 1: VPRECH present	RO	1
4	BATTERY_PRESENCE_STS	Status of battery presence. 0: Battery not present	RO	0

Bits	Field Name	Description	Type	Reset
		1: Battery present		
3	RESERVED		RO	0
2	USB_P_STS	Status of USBVBUS_PRES signal with 30 ms debounce time. When set to 1, FSM is active(according to CHGMODE_SW)	RO	0
1:0	USB_DET_STS	Status of USB charger presence and USB charger type. Read 0x0: 00 => No USB charger detected Read 0x1: 01 => 100-mA charger detected Read 0x2: 10 => 500-mA charger detected Read 0x3: 11 => Undefined	RO	0x0

Table 28. USB_CHRG_CTRL1

Address Offset	0xAD
Description	
Type	RW

7	6	5	4	3	2	1	0
VBUSOV_PRECH	CHGD_SERX_DM_LOWV	CHGD_SERX_DP_LOWV	CHGD_VDX_LOWV	CHGD_SERX_EN_LOWV	CHGD_VDX_SRC_EN_LOWV	CHGD_IDX_SRC_EN_LOWV	USB_SW_CTRL_EN

Bits	Field Name	Description	Type	Reset
7	VBUSOV_PRECH	Status of VBUSOVPRECH	RO	0
6	CHGD_SERX_DM_ LOWV	Dedicated CHGD SERX DM comparator output used in contact detect if DPDM_SWAP EEPROM bit is 1	RO	0
5	CHGD_SERX_DP_ LOWV	Dedicated CHGD SERX DP comparator output used in contact detect if DPDM_SWAP EEPROM bit is 0	RO	0
4	CHGD_VDX_LOWV	VDAT_REF DM comparator output used in charger detect if DPDM_SWAP EEPROM bit is 0. VDAT_REF DP comparator output used in charger detect if DPDM_SWAP EEPROM bit is 1.	RO	0
3	CHGD_SERX_EN_ LOWV	Enable SERX comparators on DP and DM	RW	0
2	CHGD_VDX_SRC_ EN_LOWV	Enable VDP_SRC buffer, IDM_SINK, and VDAT_REF_DM comp if DPDM_SWAP EEPROM bit is 0. Enable VDM_SRC buffer, IDP_SINK, and VDAT_REF_DP comp if DPDM_SWAP EEPROM bit is 1.	RW	0
1	CHGD_IDX_SRC_ EN_LOWV	Enable IDP_SRC and RDM_DWN if DPDM_SWAP EEPROM bit is 0. Enable IDM_SRC and RDP_DWN if DPDM_SWAP EEPROM bit is 1.	RW	0
0	USB_SW_CTRL_EN	Let the software control USB current sources and comparator outputs directly through register.	RW	0

Bits	Field Name	Description	Type	Reset
		USB dedicated FSM for detection is bypassed if this bit is set to 1.		

Table 29. USB_CHRG_CTRL2

Address Offset	0xAE
Description	
Type	RW

7	6	5	4	3	2	1	0
RESERVED						USB_500	USB_100

Bits	Field Name	Description	Type	Reset
7:2	RESERVED		RO R returns 0s	0x00
1	USB_500	Sets the USB500_P signal. This bit can be written when the USB_SW_CTRL_EN bit is set to 1. 0: USB500_P signal is 0. 1: USB500_P signal is 1. Status of FSM USB500_P signal when USB_SW_CTRL_EN bit is set to 0. In this case, a write to this bit has no effect.	RW	0
0	USB_100	Sets the USB100_P signal. This bit can be written when the USB_SW_CTRL_EN bit is set to 1. 0: USB100_P signal is 0. 1: USB100_P signal is 1. Status of FSM USB100_P signal when USB_SW_CTRL_EN bit is set to 0. In this case, a write to this bit has no effect.	RW	0

Table 30. LED_DRIVER_CTRL

Address Offset	0xAF
Description	
Type	RW

7	6	5	4	3	2	1	0
RESERVED	LEDC_PLS_WIDTH		LEDC_SW_EN	LEDC_SWMODE	LEDCCTRL		

Bits	Field Name	Description	Type	Reset
7	RESERVED		RO R returns 0s	0
6:5	LEDC_PLS_WIDTH	Select pulse width modulation of LED flashing 00: LED always on 01: 1.0 sec 10: 1.5 sec 11: 2.0 sec	RW	0x0
4	LEDC_SW_EN	Enable LED driver feature managed by software 0: LED is disabled. 1: LED is enabled.	RW	0

Bits	Field Name	Description	Type	Reset
3	LEDC_SWMODE	Enable switch between hardware LED driver controller mode and SW LED driver control mode 0: LED enable is controlled by the hardware LED driver controller. 1: LED enable is controlled with LEDC_SW_EN.	RW	0
2:0	LEDCCTRL	Defined current of LED driver 000: 3.5 mA 001: 0.875 mA 010: 1.75 mA 011: 7 mA 100: 14 mA Other codes: 0 mA	RW	0x2

Table 31. FACTCFG0_VPRCH

Address Offset	0xB3
Description	EEPROM bits for VPRECH calibration. Can be written only during test mode.
Type	RW

7	6	5	4	3	2	1	0
DPDM_SWAP	CHRG_DET_CFG	DATACON_EN	WATCHDOG16_32	IPRECH_TRIM			

Bits	Field Name	Description	Type	Reset
7	DPDM_SWAP	EEPROM register. Reset value set by EEPROM. SWAP DP/DM for charger detection.	RW	0
6	CHRG_DET_CFG	Reset value set by EEPROM bit CHG_DET_CFG default value given by EEPROM and is equal to 1. 0: CHRG_DET_N output = CHRG_DET signal 1: CHRG_DET_N output = Not CHRG_DET signal	RW	1
5	DATACON_EN	Reset value set by EEPROM Default value of DATACON_EN given by EEPROM must be 1. Data connection state of USB charger detection state-machine 0: Bypass 1: Normal mode	RW	1
4	WATCHDOG16_32	EEPROM reset value. Default value of DATACON_EN given by EEPROM must be 1. 0: 32 minutes when HW control. 1: 16 minutes when HW control.	RW	0
3:0	IPRECH_TRIM		RW	0x0

Table 32. FACTCFG1_VPRCH

Address Offset	0xB4
Description	EEPROM bits for VPRECH calibration. Can be written only during test mode.
Type	RW

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED		RW	0x00

Table 33. SPARE1_VPRECH

Address Offset	0xB5
Description	Spare register.
Type	RW

7	6	5	4	3	2	1	0
RESERVED				NEWBITFIELD1			

Bits	Field Name	Description	Type	Reset
7:4	RESERVED		RO R returns 0s	0x0
3:0	NEWBITFIELD1	BCI dedicated spare bits.	RW	0x0

Table 34. SPARE2_VPRECH

Address Offset	0xB6
Description	Spare register.
Type	RO

7	6	5	4	3	2	1	0
RESERVED				NEWBITFIELD1			

Bits	Field Name	Description	Type	Reset
7:4	RESERVED		RO R returns 0s	0x0
3:0	NEWBITFIELD1	BCI dedicated spare bits.	RO	0x0

Table 35. BCIISR1

Address Offset	0xB9
Description	The INTERRUPT STATUS ISR1 register is used to determine which monitoring function interrupt triggered the interrupt line PO_BCI_SIH_INT1_N request. When a bit in this register is set to 1, it indicates that the corresponding monitoring function is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the INTERRUPT STATUS ISR1 register. When a bit in this register is set to 1, then the corresponding interrupt line is released. If the user writes a 0 to a bit in this register, the value remains unchanged. The INTERRUPT STATUS ISR1 register is synchronous with the interface OCP clock.
Type	RW

7	6	5	4	3	2	1	0
RESERVED				USB_CHGSTOP_ISR1	USB_CHGSTART_ISR1	USB_ERROR_ISR1	WATCHDOG_TIMEOUT_ISR1

Bits	Field Name	Description	Type	Reset
7:4	RESERVED		RO R returns 0s	0x0
3	USB_CHGSTOP_ISR1	Write 0: No impact. Register keeps its value. Read 0: No interrupt set Read 1: Interrupt set Write 1: When set to 1, the corresponding interrupt line is released.	RW	0
2	USB_CHGSTART_ISR1	Write 0: No impact. Register keeps its value. Read 0: No interrupt set Read 1: Interrupt set Write 1: When set to 1, the corresponding interrupt line is released.	RW	0
1	USB_ERROR_ISR1	Write 0: No impact. Register keeps its value. Read 0: No interrupt set Read 1: Interrupt set Write 1: When set to 1, the corresponding interrupt line is released.	RW	0
0	WATCHDOG_TIMEOUT_ISR1	Write 0: No impact. Register keeps its value. Read 0: No interrupt set Read 1: Interrupt set Write 1: When set to 1, the corresponding interrupt line is released.	RW	0

Table 36. BCIIMR1

Address Offset	0xBA
Description	The INTERRUPT MASK IMR1 REGISTER allows the user to mask the expected transition on end of sequence from generating an interrupt request on PO_BCI_SIH_INT1_N. The interrupt mask registers are programmed synchronously with the interface OCP clock.
Type	RW

7	6	5	4	3	2	1	0
RESERVED				USB_CHGSTOP_IMR1	USB_CHGSTART_ISR1	USB_ERROR_IMR1	WATCHDOG_TIMEOUT_IMR1

Bits	Field Name	Description	Type	Reset
7:4	RESERVED		RO	0
3	USB_CHGSTOP_IMR1	0: Interrupt is not masked. 1: Interrupt is masked.	RW	1
2	USB_CHGSTART_IMR1	0: Interrupt is not masked. 1: Interrupt is masked.	RW	1
1	USB_ERROR_IMR1	0: Interrupt is not masked. 1: Interrupt is masked.	RW	1
0	WATCHDOG_TIMEOUT_IMR1	0: Interrupt is not masked. 1: Interrupt is masked.	RW	1

Table 37. BCISIR

Address Offset	0xBD
Description	For test purposes, the BCI SOFTWARE INTERRUPT register allows generating an interrupt event on the PO_BCI_SIH_INT1_N or PO_BCI_SIH_INT2_N request line by writing 1 to the targeted SIR bit in a specific test mode. An interrupt is generated if the corresponding BCI_EDR bit is set to edge (falling or rising) sensitive. External interrupt requests and internal software requests are merged before being sent to the PIH.
Type	RW

7	6	5	4	3	2	1	0
RESERVED				USB_CHGSTOP_SIR	USB_CHGSTART_SIR	USB_ERROR_SIR	WATCHDOG_TIMEOUT_SIR

Bits	Field Name	Description	Type	Reset
7:4	RESERVED		RO	0
3	USB_CHGSTOP_SIR	0: Software interrupt not set 1: Software interrupt set	RW	0
2	USB_CHGSTART_SIR	0: Software interrupt not set 1: Software interrupt set	RW	0
1	USB_ERROR_SIR	0: Software interrupt not set 1: Software interrupt set	RW	0
0	WATCHDOG_TIMEOUT_SIR	0: Software interrupt not set 1: Software interrupt set	RW	0

Table 38. BCIEDR1

Address Offset	0xBE
Description	The INTERRUPT EDGE DETECTION register bit BCI_EDR allows the user to define, for all incoming interrupt lines, the expected edge to trigger an interrupt request. The interrupt request can be generated either from a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions (bits are 11) accruing. To disable the edge detection capability, the relevant bits must be reset (00).
Type	RW

7	6	5	4	3	2	1	0
USB_CHGSTOP_EDRRISING	USB_CHGSTOP_EDRFALLING	USB_CHGSTART_EDRRISING	USB_CHGSTART_EDRFALLING	USB_ERROR_EDRRISING	USB_ERROR_EDRFALLING	WATCHDOG_TIMEOUT_EDRRISING	WATCHDOG_TIMEOUT_EDRFALLING

Bits	Field Name	Description	Type	Reset
7	USB_CHGSTOP_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	0
6	USB_CHGSTOP_EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	1
5	USB_CHGSTART_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	1
4	USB_CHGSTART_EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	0
3	USB_ERROR_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	1
2	USB_ERROR_EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	0
1	WATCHDOG_TIMEOUT_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	1
0	WATCHDOG_TIMEOUT_EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	0

Table 39. BCISIHCTRL

Address Offset	0xC0
Description	The BCI SIH control register allows the user to disable a pending event incoming during SW interrupt latency by programming 1 in the PENDDIS bit. By writing 0 in the EXCLEN bit, the user disables the exclusivity between the interrupt request line PO_BCI_SIH_INT1_N and PO_BCI_SIH_INT2_N. The ClearOnRead bit enables the clear-on-read feature. This means that any read access to the ISR clears this register and releases the associated interrupt line (default value). If disabled a read access to a specific address value will clear all ISR within the SIH.
Type	RW

7	6	5	4	3	2	1	0
RESERVED					COR	PENDDIS	EXCLEN

Bits	Field Name	Description	Type	Reset
7:3	RESERVED		RO R returns 0s	0x00
2	COR	0: Clear ISR on write 1: Clear ISR specific bit field when read access	RW	0
1	PENDDIS	0: Pending event enabled 1: Pending event disabled	RW	0
0	EXCLEN	0: Exclusivity disabled 1: Exclusivity enabled	RW	0

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