TPS65911 Layout Guidelines

User's Guide

Literature Number: SWCU080A
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TPS65911 Layout Guidelines

1 Introduction

This document describes constraints and points for special layout consideration when designing with the TPS65911. The TPS65911 is an analog chip containing several blocks which have different constraints when designing the board layout. The purpose of this document is to create a better understanding of some of these constraints and, through examples, to explain how good board layout can be achieved.

The document is built as a design process, starting with:

- Definition of the PCB
- Dividing the signals into groups; the requirements and constraints of each group are described.
- Placement of external components
- Use of tunnels for shielding

The design examples in this guide describe PCB build up.

2 Component Description, TPS65911

The TPS65911 is an integrated power management IC available in 98-pin 0.65-mm pitch BGA package and is dedicated to applications powered by one Li-Ion or Li-Ion polymer battery cell, 3-series Ni-MH cells, or a 5-V input, and which require multiple power rails. The device provides three step-down converters, one controller for external FETs to support high-current rail, eight LDOs, and is designed to be a flexible PMIC for supporting different processors and applications.

Figure 1 shows the block diagram of the TPS65911 PMIC.

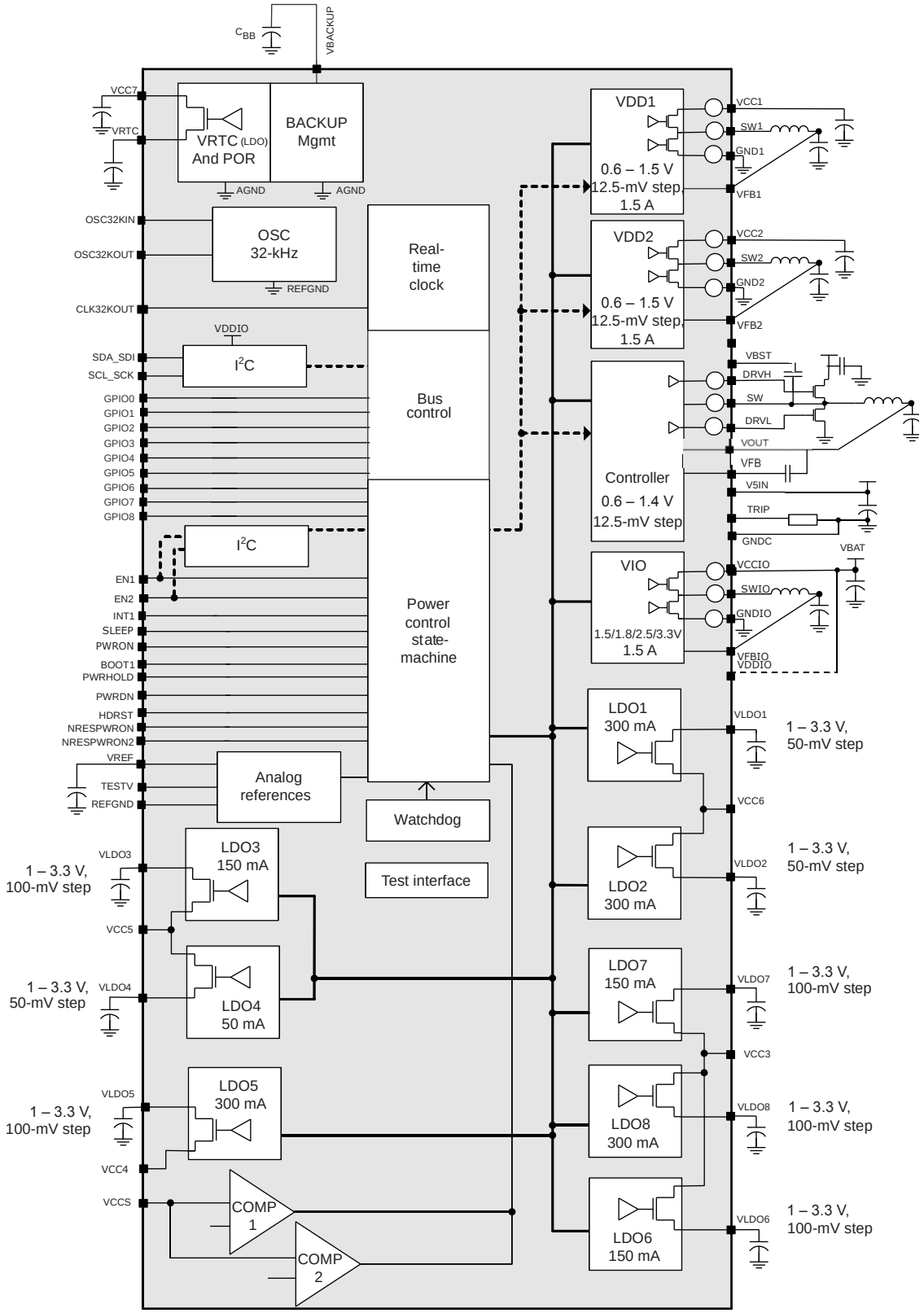

Figure 1. Block Diagram

3 PCB Build Up

Before the layout starts, the PCB build up is needed to determine a good strategy for which signal lines to place on each layer. There is a lot of theory to consider to achieve a good and proper design. Some theories are conflicting. Hence, the design of the PCB has trade-offs. A sound strategy is important to create the best possible design, even with the compromises.

3.1 Routing Strategy

Routing on different board layers is an advantage for the CAD designer, but some constraints still must be addressed to achieve a good design. Some signals (victims) are sensitive to influence from other signals (aggressors) and these victims must be kept a certain distance from the aggressors, even if the signals are on different layers. One of the biggest misconceptions is that a different layer for a victim with respect to an aggressor solves all problems (that is, the PCB does not shield for capacitive or inductive coupling between signals). The designer must pay special attention to these issues, especially when planning the ground paths from different circuits.

3.1.1 PCB Strategy

When deciding the PCB build up, a number of considerations must be taken into account:

- Number of layers
- Number of micro via layers
- Buried via
- Stacked via layers

All the options are related to cost and, hence, there will be trade-offs between the cost and the options chosen.

Figure 2 shows the TPS65911 ball placement. This sets the requirement for PCB build up to either have a number of levels of stackable vias or the possibility to have tracks between the balls. The absence of balls in certain places facilitates via placement under the package.

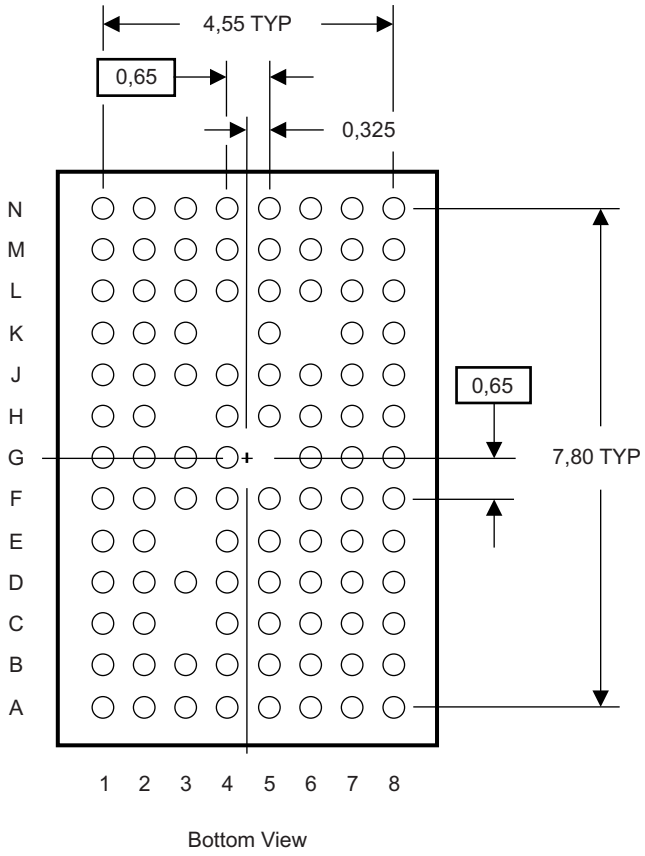

Figure 2. TPS65911 Ball Placement

The pitch of the package is 0.65 mm, which allows routing between balls. Tracks between the balls or routing to vias to access internal balls are possibly the most common solution for routing.

- The only pins not routed are TRAN, EN, and PGOOD of the DC/DC controller. These pins are not needed for application purposes.
- Minimum line width is 4 mils.
- Minimum space between lines is 4 mils.
- Minimum space for line to pad is 5 mils.
- Minimum space for via to pad is 5 mils.
- Minimum space for via to via is 4 mils.
- Minimum drill is 10 mils (20 mils total).
- No vias in pads
- Maximum ball size is 350 µm.

NOTE: Maximum ball pad size value taken is 80% of maximum. (350 µm × 80% = 280 µm)

Figure 3 shows a build up of the evaluation board.

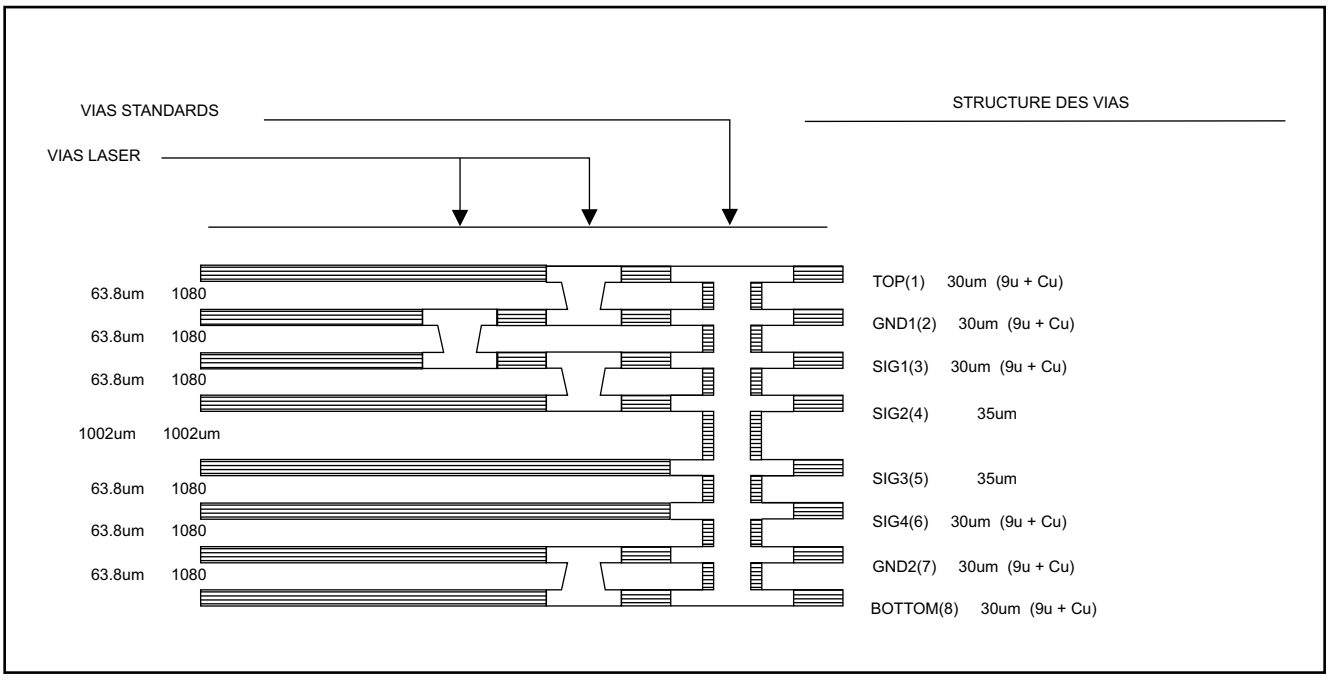

Figure 3. Evaluation Board PCB Layer Information

3.2 Layer Definition

Before the layout is started, the engineer and the PCB designer must determine the location of the signals. To understand this, the following can be used to understand the need for a routing strategy.

When dealing with sensitive signals and signals that can affect other signals in the vicinity, it becomes very practical to have a pre-study of where specific signals should be routed. A classic example is that the ground loop for high-power consumption devices surrounds some other signals which are not able to withstand the interference from these signals.

In Figure 4, signals are placed in the ground loop (layers 3–5). This is not recommended. The signals in the ground loop will be affected by the flux, which is generated by the current in the loop. This must be avoided, especially regarding sensitive signals such as oscillators, and so forth.

The supply line and the ground path are crucial when the layout is made; both are equally important. Supplies must be placed and calculated so that their flux does not affect any signals that cannot withstand it. The ground plane must be very solid, especially close to the supply trace. If this is not taken into account, the risk for noise pollution increases.

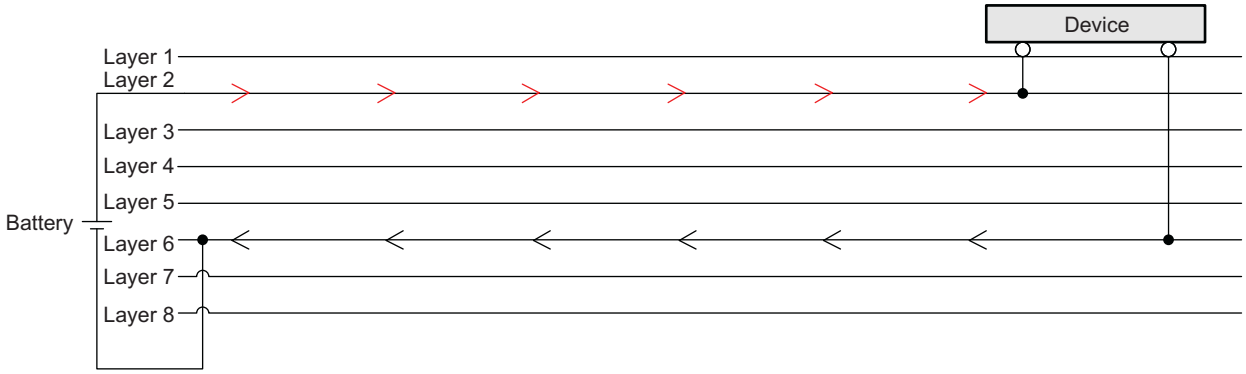

Figure 4. Incorrect Design: Signals Inside the Ground Loop

In Figure 5, the problem is solved by choosing other layers for supply and ground, with no signal layer between the ground loop. It must still be taken into account that no sensitive signals are in parallel with the supply line and the corresponding ground path.

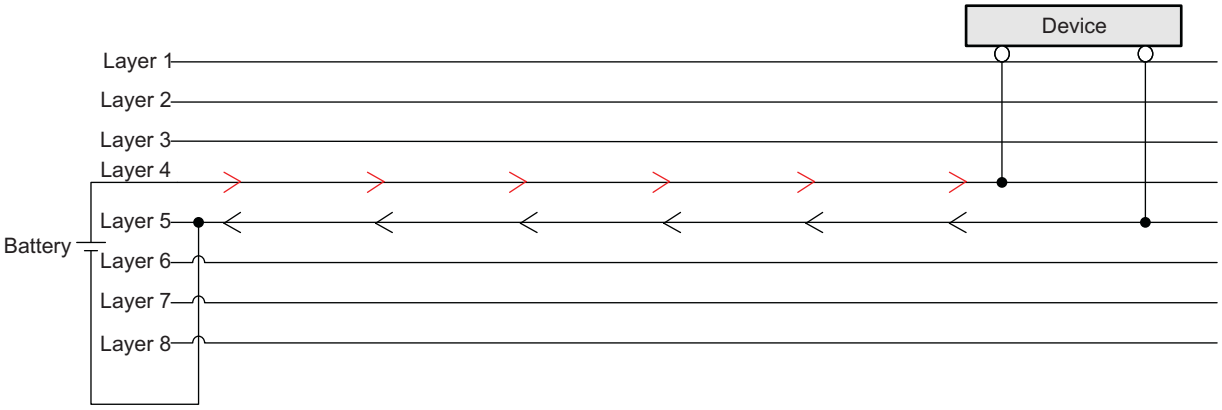

Figure 5. Correct Design: Signals Outside of the Ground Loop

4 Signal Grouping

4.1 Ground

4.1.1 Ground for Digital

Group	BGA Pin	Pin Name	Pin Type
GND digital	A1	DGND	Power
	B1	DGND	Power
	B2	DGND	Power

4.1.2 Ground for DC/DC Power (Short Thick Traces Required)

Group	BGA Pin	Pin Name	Pin Type
GND DCDC	J8	GNDIO	Power
	J7	GNDIO	Power
	D3	GND1	Power
	C2	GND1	Power
	C1	GND1	Power
	J1	GND2	Power
	J2	GND2	Power
	A7	GND_CTRL	Power
	A8	GND_CTRL	Power

4.1.3 Main Analog Ground Plane

Group	BGA Pin	Pin Name	Pin Type
GND power	D6	AGND	Power
	E5	AGND	Power
	E6	AGND	Power
	F5	AGND	Power
	G4	AGND	Power
	H5	AGND	Power
	H6	AGND	Power
	J3	AGND	Power
	J4	AGND	Power
	J6	AGND	Power
	K3	AGND	Power
	N8	AGND2	Power
	M8	AGND2	Power

4.1.4 Sensitive Ground (Isolate From Noisy Signals)

Group	BGA Pin	Pin Name	Pin Type
GND signal	G7	REFGND	Power

4.2 Power

4.2.1 Power Input Lines

Group	BGA Pin	Pin Name	Pin Type
Power input	E1	VCC1	Power
	F2	VCC1	Power
	F3	VCC1	Power
	G1	VCC2	Power
	G2	VCC2	Power
	N3	VCC3	Power
	L1	VCC4	Power
	D8	VCC5	Power
	N5	VCC6	Power
	B6	VCC7	Power
	L7	VCCIO	Power
	L8	VCCIO	Power
	A5	V5IN	Power
	A2	VBST	Power

4.2.2 Power Switching Output Lines (Aggressors – Careful Routing Required)

Group	BGA Pin	Pin Name	Pin Type
Power output	D1	SW1	Power
	D2	SW1	Power
	E2	SW1	Power
	H1	SW2	Power
	H2	SW2	Power
	K7	SWIO	Power
	K8	SWIO	Power
	A4	SW	Power
	A3	DRVH	Power
	A6	DRVL	Power

4.2.3 Power Passive Output Lines (IR Drops To Be Considered)

Group	BGA Pin	Pin Name	Pin Type
Power output	N6	LDO1	Power
	N4	LDO2	Power
	E7	LDO3	Power
	C8	LDO4	Power
	K1	LDO5	Power
	M2	LDO6	Power
	M3	LDO7	Power
	M1	LDO8	Power

4.2.4 Decoupling for Internal Functions

Group	BGA Pin	Pin Name	Pin Type
Power output	B5	VRTC	Power

4.3 Sensitive Signals

4.3.1 Clock Signals

Group	BGA Pin	Pin Name	Pin Type
Slow clock	F4	CLK32KOUT	Output
	F8	OSC32KIN	Input
	F7	OSC32KOUT	Output

4.3.2 Reference

Group	BGA Pin	Pin Name	Pin Type
Reference	G8	VREF	Output
	B3	TRIP	Output
	J5	BOOT1	Input

4.3.3 Voltage Sense

Group	BGA Pin	Pin Name	Pin Type
Voltage sense	E8	VCCS	Input
	D4	VFB1	Input
	K2	VFB2	Input
	H8	VFBIO	Input
	C5	VFB	Input
	B4	VOUT (DCDC_CTRL)	Input

4.4 Digital Signals

4.4.1 Dedicated Static I/Os

Group	BGA Pin	Pin Name	Pin Type
I/Os	N2	PWRDN	Input
	L6	HDRST	Input
	E4	PWRON	Input/Output
	N1	PWRHOLD	Input/Output
	M7	EN1	Input/Output
	M6	EN2	Input/Output
	F1	SLEEP	Input/Output
	H4	NRESPWRON	Output
	C7	NRESPWRON2	Output

4.4.2 Dedicated Dynamic I/Os

Group	BGA Pin	Pin Name	Pin Type
I/Os	M5	SDA	Input/Output
	M4	SCL	Input/Output
	L3	INT1	Output

4.4.3 GPIO Signals

Group	BGA Pin	Pin Name	Pin Type
GPIO	L5	GPIO0	Input/Output
	F6	GPIO1	Input/Output
	L2	GPIO2	Input/Output
	B7	GPIO3	Input/Output
	H7	GPIO4	Input/Output
	G6	GPIO5	Input/Output
	G3	GPIO6	Input/Output
	L4	GPIO7	Input/Output
	K5	GPIO8	Input/Output

5 External Components Placement

Placement of external components must be done using engineering techniques. The placement is expected to be affected by the mechanical dimension, and hereby also the placement of the TPS65911. Placement of the TPS65911 must consider the distance to supplied devices (for example, the processor). The placement has requirements to the placement of external components and also to the possibility to route power lines from integrated PMU to power consuming devices, such as processors, and so forth. When performing the calculation, consider that the tolerances on DC/DC converter outputs are ±4%.

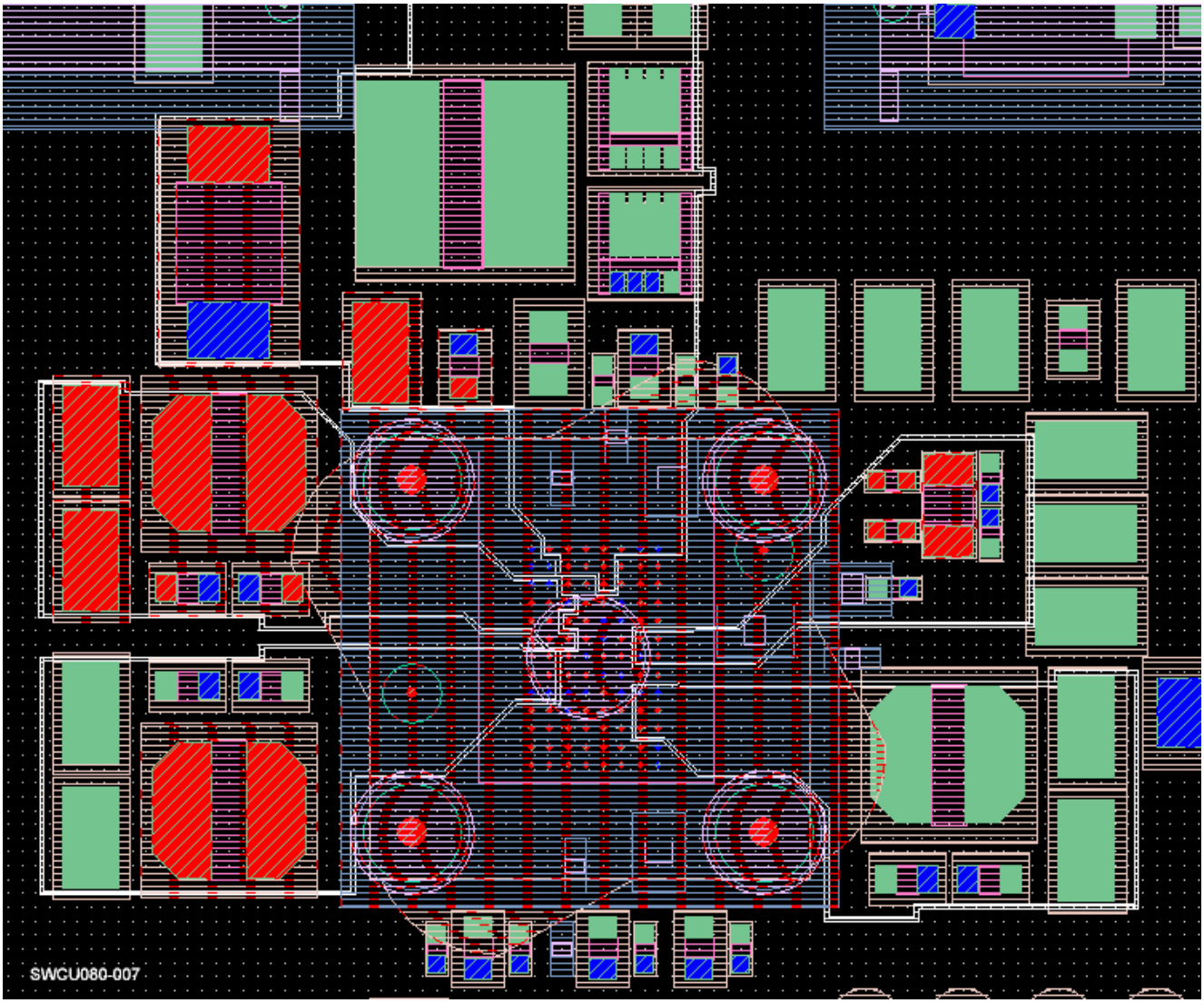

Figure 6. Example of Component Placement on a Socket Board

5.1 DC/DC Converter Outputs

As for all switching power supplies, the board layout is an important step in the design. High-speed operation of the TPS65911 device demands careful attention to PCB layout. Take care during board layout design to achieve the specified performance. If the layout is not done carefully, the regulator could show poor line and/or load regulation, stability issues, as well as EMI problems. It is critical to provide a low inductance-impedance ground path. Therefore, use wide and short traces for the main current paths, as indicated in bold red lines in Figure 7.

The input capacitor, output capacitor, and inductor should be placed as close as possible to the IC pins. Grounds can be separated between the control and the power devices to minimize the effects of ground noise. Connect these ground nodes together (star point) underneath the IC and make sure that small signal components returning to the AGND pin do not share the high current path of C1 and C2.

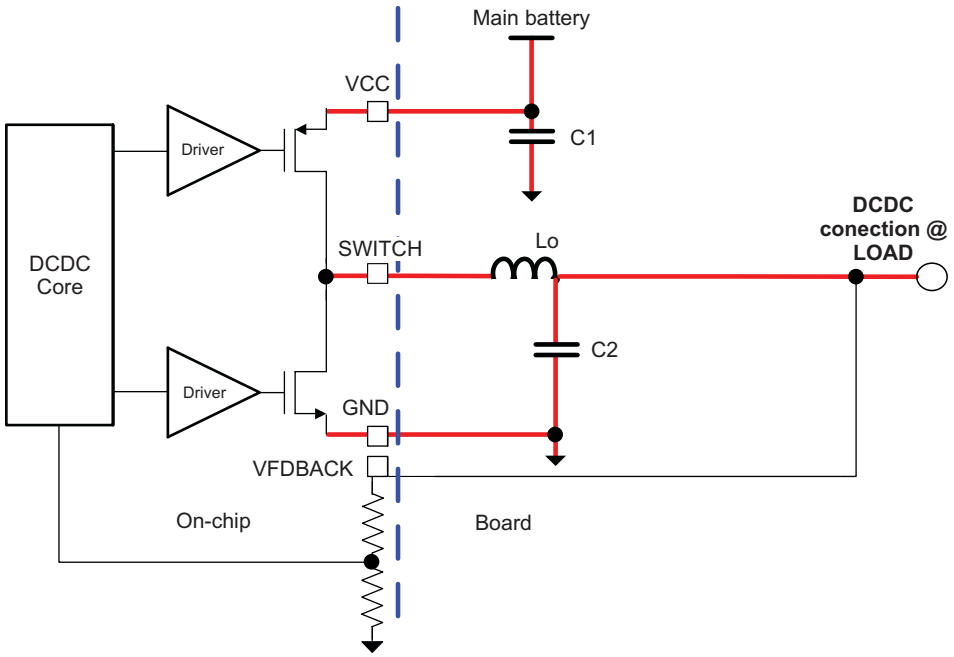

Figure 7. DC/DC Converter

One way to do this is to isolate the ground plane for the DC/DC on the first ground plane (GND layer 1) and then connect multiple vias to the main ground plane (GND layer 2).

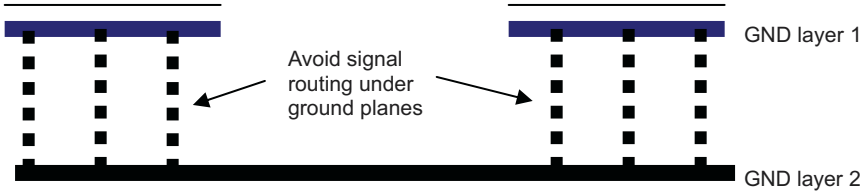

Figure 8. DC/DC Ground Routing

5.1.1 Sense Signal for DC/DC Converter

The output voltage sense line (VFBx) should be connected directly to the output capacitor and routed away from noisy components and traces (for example, the SWITCH line). Its trace should be minimized and placed in such a way that no signals can affect the voltage level, as it is used to adjust the output voltage from the DC/DC converter. Figure 10 is an example of a bad layout where the feedback line (highlighted in red) for the DC/DC converter is parallel to and on the same layer as the switching output (large green trace connected to the other side of L4).

5.1.2 Bad DC/DC Converter Design

Some design examples that have caused errors follow. All the design examples have required a redesign of the PCB.

5.1.2.1 Supply for DC/DC Converters

In the design example shown in Figure 9, the designer has connected VCC1, the supply input for VDD1, with a connection that is a very small. However, the real problem is that the designer has chosen to connect ball H15 and K15 to the same line. K15 and H15 supply sensitive circuits internally in this example, and these circuits are affected by the shifting current draw by VDD1. The inrush current for VDD1 is so high that a dip in the supply line occurs. This dip should be minimized and isolated from other circuits; this can be done by using the small impedances in the PCB and the decoupling capacitors.

TPS65911 application

If this layout was used for a single-cell solution and the input to the DC/DC was shared with VCCS, the design would have problems starting up due to the inrush current in VDD1.

Solution

Avoid sharing supply line routing for the DC/DC converters with other module inputs even if the source is the same. This is also called star topology.

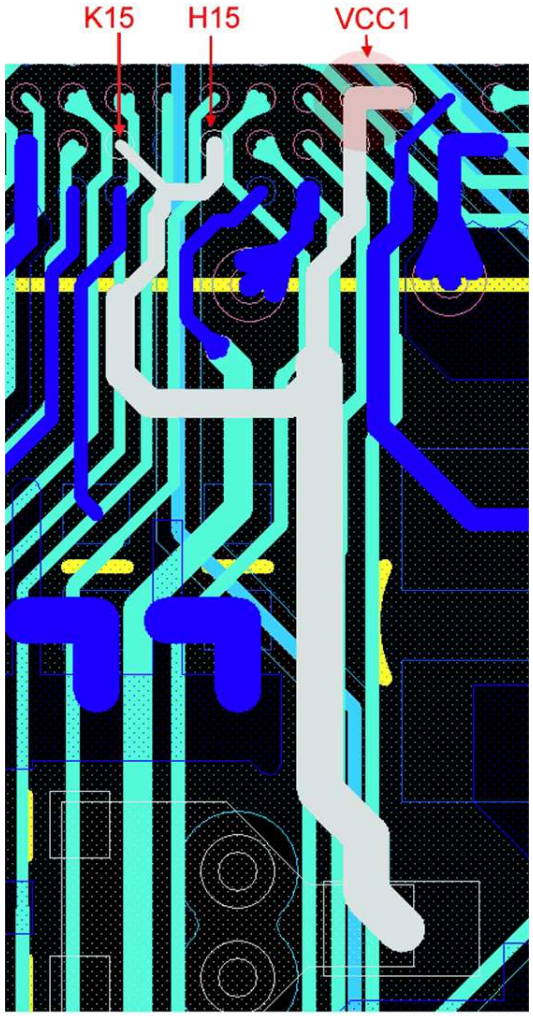

Figure 9. Badly Routed Supply Connections

5.1.2.2 Feedback to DC/DC Converter

The feedback for the DC/DC converter should be routed away from the switching node. In the example shown in Figure 10, the feedback line (highlighted in red) was routed on the same layer and parallel to the switching line introducing a capacitive coupling between the traces.

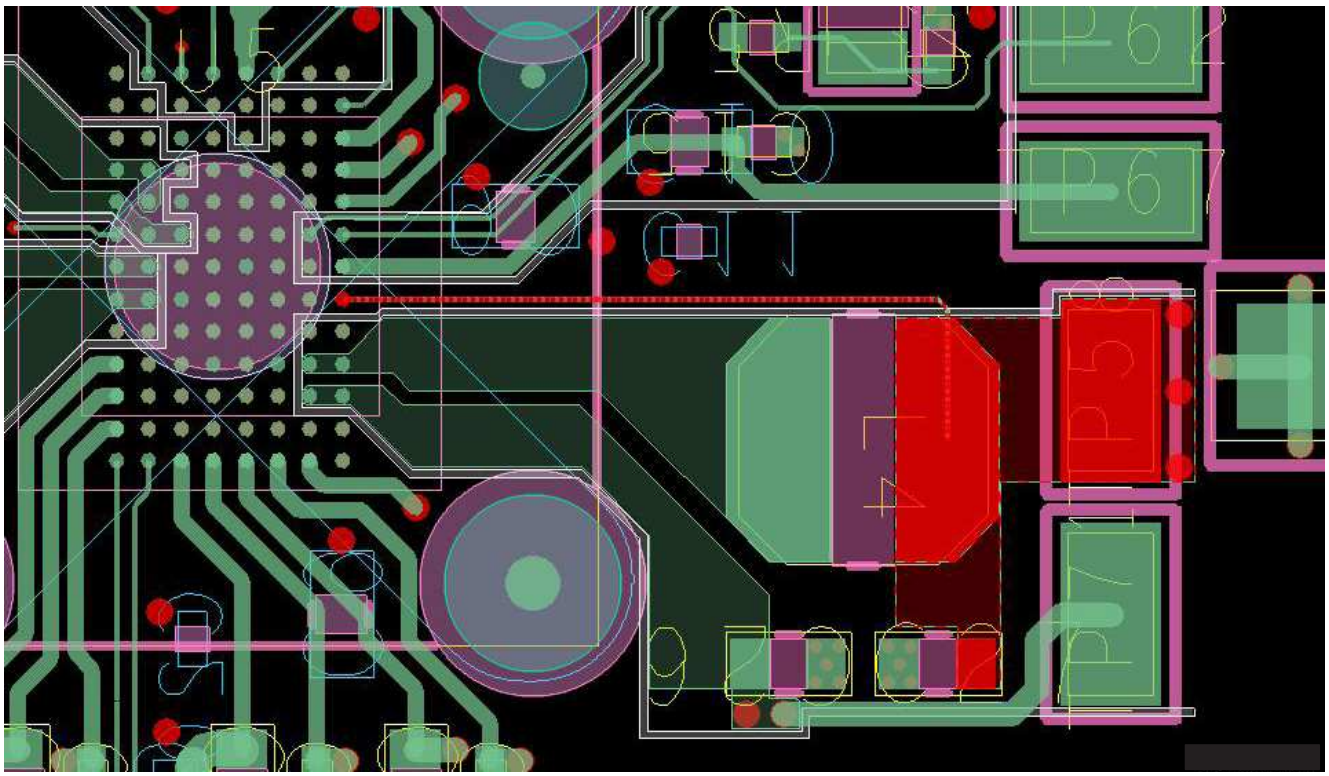

Figure 10. Badly Routed Feedback on DC/DC Converter

Solution

Route the feedback in a different layer and shield from the switching node, if possible.

5.1.2.3 Output From DC/DC Converters

See Figure 11.

The DC/DC switching output in this case is connected by three balls; this is to support the high current in the connection.

Here a board is made with a very narrow connection from SW1 to the coil. This connection was made only on the top layer. The impedance in the connection affects the efficiency on the DC/DC converter. After the coil a plane has been defined, which is sufficient for the load current drawn from the DC/DC. The narrow connection from SW1 to the inductor becomes a bottleneck for high current and causes an IR loss.

Solution

Improve the connection from output balls by widening the track as soon as possible. Otherwise make parallel tracks in layer 2 and layer 3 when possible.

The impedance in the connection from SW1 causes poor efficiency in VDD1.

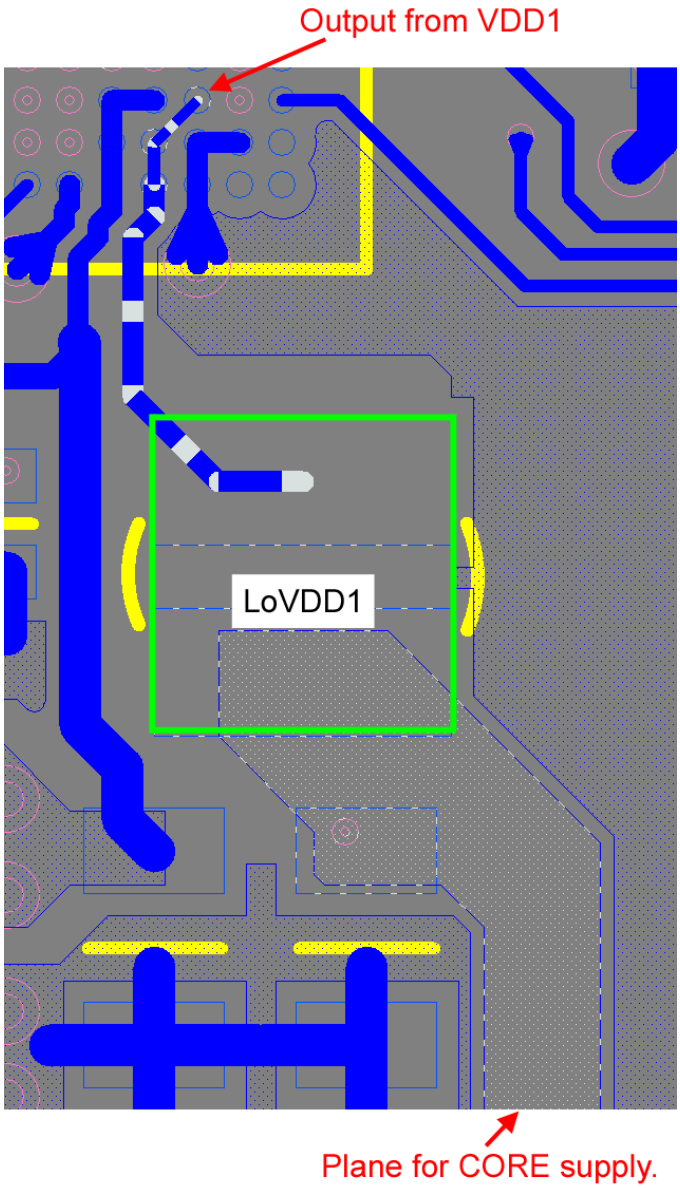

Figure 11. Badly Routed DC/DC Switching Load

5.2 Reference Voltage Routing

The reference voltage requires a clean ground. Hence, the REFGND ground is used as the ground connection for its filter capacitor.

5.3 BOOT1 Routing

BOOT1 can be connected to VRTC or to AGND depending on the boot mode required. Do not leave BOOT1 floating; doing so can risk noise coupling on the node and during boot mode configuration changes.

5.4 32-kHz Oscillator Circuit

The 32-kHz clock circuit is sensitive and certain considerations should be taken to prevent impact on the circuit performance.

The buffered 32-kHz output signal CLK32KOUT is also a signal to be considered for tunneling due to the fact that even though it is buffered this signal is the core to slow-clocking for the system when used. If noise impacts this signal, the system may not be able to do calibrations of the clock signal, and therefore the system will not enter deep sleep if the clock integrity is gating for this purpose. If the 32-kHz signal must be distributed to more than one device from the output pin F4, it is recommended to use star topology to avoid timing differences.

To prevent disturbances in the ground plane, a special restricted area should be defined. It is suggested that planes are placed in the layer directly under the components. This plane may refer only to the REFGND ball G7 on the TPS65911 and be connected to the main ground plane with via connections.

Figure 12 and Figure 13 show the ground layer isolation and the component layer, respectively.

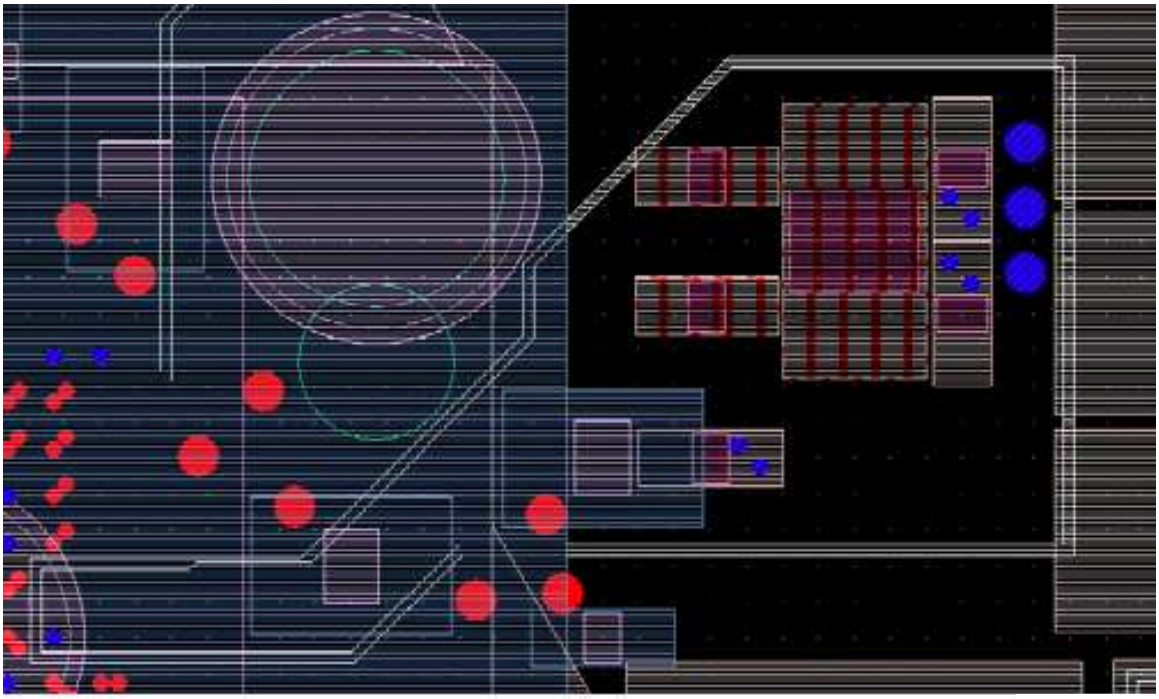

Figure 12. Ground Layer Isolated From Other Grounds

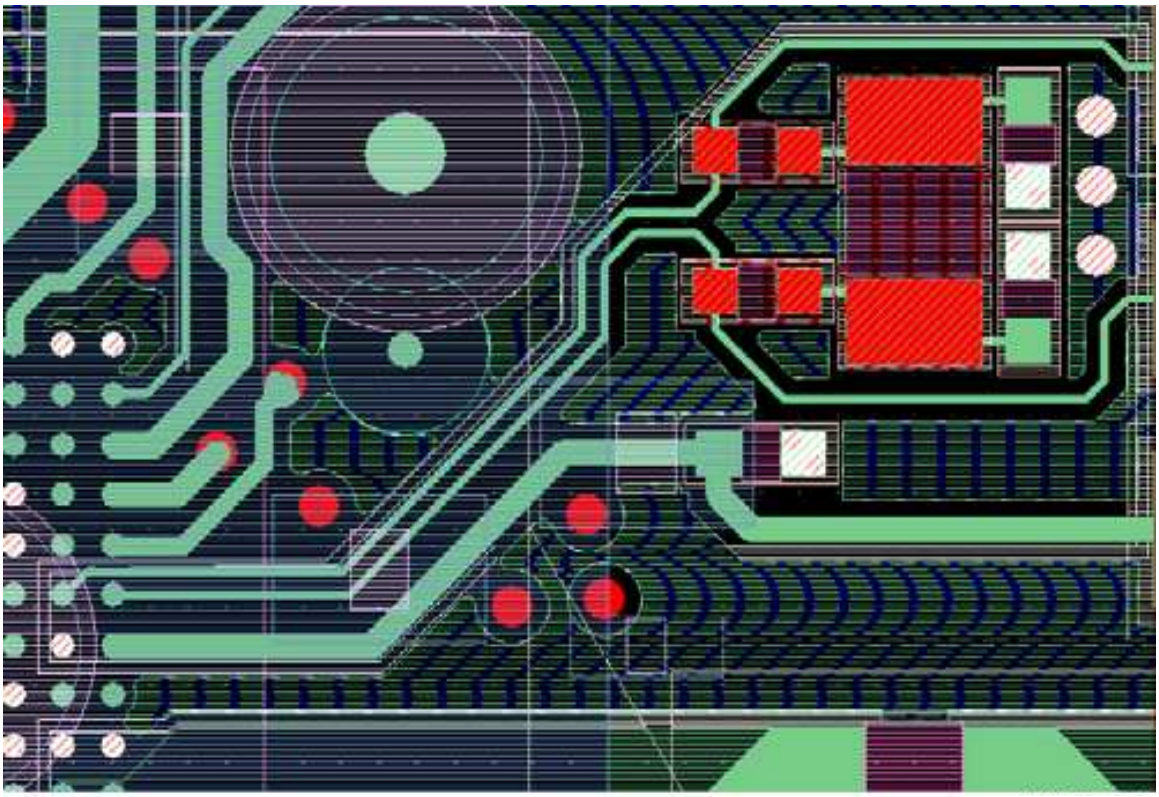

Figure 13. Component Layer

6 Routing of Parallel Balls

Routing of parallel balls can be divided into three scenarios:

- High-power outputs
- High-power inputs
- Multiple power inputs

6.1 High-Power Outputs

When routing high-power outputs, ensure low impedance in the tracks to ensure low IR drop. Furthermore, it is crucial that the routing of the paralleled balls ensures that power is distributed evenly between the balls. This can be done by connecting the paralleled balls to a power plane. To control the current distribution and hence the power distribution, consciously connect a well-planned distribution of via connections to the plane.

6.2 High-Power Inputs

High-power inputs must be routed with low-impedance tracks in order to meet requirements for IR drop. If decoupling capacitors are connected, these should be placed as close as possible to the inputs. To ensure good decoupling, the power first must pass the footprint of the decoupling capacitor and then on to the power input. Even the smallest stub from the power track to the capacitor significantly degrades the effect of the capacitor. Grounding the capacitor with a solid connection to the same ground as the high-power device is equally important to achieve good decoupling to ensure best possible performance from the capacitor.

6.3 Multiple Power Inputs

Multiple power inputs means that the same power source is distributed to multiple devices with multiple connections on a single device. In this case, select a point of distribution from which to branch out the power supply to various devices or to various locations on the same device.

6.3.1 Point of Distribution

A preferable point of distribution could be the decoupling capacitor of the device, which generates the power, or a similar point on the PCB where there is good decoupling of the power and low-impedance tracks from the power supply. From this point, power is distributed to the various locations where it is needed. When distributing the power this should be done using the point of distribution as a star point. **Do not distribute power in a daisy-chain manner because this causes the quality of the power to deteriorate as the chain moves from power consumer to power consumer.**

6.3.2 Connecting Multiple Devices

Use a star point approach when distributing power to multiple devices for the reasons mentioned in Section 6.3.1. Consider how much decoupling is necessary. To ensure good decoupling, the power first must pass the footprint of the decoupling capacitor and then on to the power input.

Even the smallest stub from the power track to the capacitor degrades the effect of the capacitor. Grounding the capacitor with a solid connection to the same ground as the high-power device is equally important to achieve good decoupling to ensure best possible performance from the capacitor.

6.3.3 Connecting Multiple Pins on a Single Device

When connecting multiple pins on a device, an assessment of the number of decoupling capacitors must be made. If in doubt, provide one capacitor per pin (although this is not possible in many cases). Find groups of pins that can share decoupling, route the power from the point of distribution to the decoupling capacitor, and route from the pins to the decoupling capacitor, thus, creating a common star connection at the decoupling capacitor. This prevents the different balls from affecting each other by injecting ripple and noise. Make interconnections between parallel balls only at the decoupling capacitor.

6.3.4 Routing of Balanced Signals

Signals that are made balanced must be routed in parallel, the same distance from start to end, with the same impedance for both signals.

Examples of balanced signals:

OSC32KIN – OSC32KOUT

7 Remote Sensing for the DCDC_CTRL

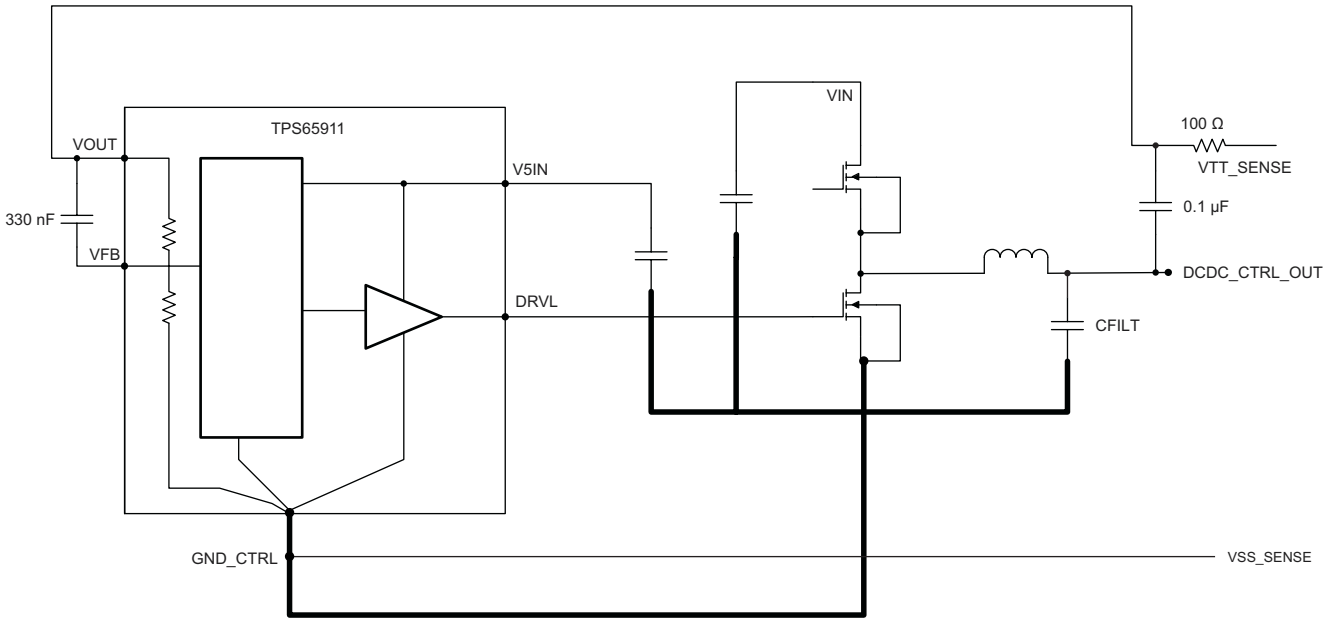

Figure 14. DC/DC Controller Remote Sensing

- Make a Kelvin connection to the load device.
- Run the feedback signals as a differential pair to the device. The distance of these parallel pairs should be as short as possible.
- Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible.
- 100-Ω resistance on VTT_SENSE is to act as a filter to reduce the AC component of the signal.
- 0.1-µF capacitance between DCDC_CTRL_OUT and VOUT is to add the AC component of the ripple to the feedback loop.

8 Use of Tunnels for Signal Isolation

The purpose of tunneling or shielding in the PCB is to ensure signal integrity on sensitive signals. Tunneling is extremely space consuming in a PCB and should only be used on signals for which it is necessary.

It is preferable to tunnel signals on a dedicated layer in the PCB on which the signals are routed. The signals are routed with unbroken ground on both sides, and the shield is formed by having ground on the PCB layers above and below the signals. It is important that the surrounding ground planes are firmly connected with vias to ensure connection between the ground layers and to the main ground in the PCB. When applying tunneling on signals, make sure that the signals do not accidentally get exposed to other signals; high-speed digital signals with frequent activity should be especially avoided at all costs.

8.1 Signals Requiring Tunneling

The signals that require tunneling where available are:

32K crystal: The connections to the 32-kHz crystal should be tunneled. The 32-kHz oscillator is a very low-power circuit, hence, the connections to the crystal should be protected against aggressors.

Revision History

Changes from Original (December 2010) to A Revision **Page**

- Update made to Section 3. 7
- Update was made in Section 4.1.1. 10
- Update made in Section 4.2.4. 12
- Updates were made to Section 4.4.3. 13
- Figure 9: Updates were made. 16

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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