TPS65086100 Non-Volatile Memory Programming Guide

The TPS65086100 power management integrated circuit (PMIC) provides the power of the TPS65086 family of devices and combines it with the ability to program the non-volatile memory to generate the desired voltages and sequencing for rapid prototyping and quick time to market. The TPS65086100 device has three controllers, three converters, three general purpose LDOs, one termination LDO, and three load switches which can be programmed with a variety of default voltages and sequences.

The TPS65086100 has two banks of non-volatile one-time programmable (OTP) memory which can be programmed in the BOOSTXL-TPS650861 BoosterPack™ plug-in module with an MSP430F5529 LaunchPad™ development kit, or directly on board during manufacturing.

For a detailed description of how to use the BOOSTXL-TPS650861 BoosterPack plug-in module with an MSP430F5529 LaunchPad development kit refer to the *BOOSTXL-TPS650861 EVM User's Guide*. Programming can be done with any I^2C interface and a 7V supply following the simple procedure described in this document. For large volume opportunities, please contact a local TI sales representative to determine if use of TI's manufacturing for a custom OTP is available. Third party distributors may also support programming of the TPS65086100.

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1 Introduction

The goal of this document is to provide guidelines for the programming of TPS65086100 OTP memory for prototyping as well as in-system programming. This should allow for rapid prototyping for quick time to market as well as an option to support many smaller projects with different OTP programs in a cost effective manner. Finalized OTP programs can be programmed into TPS65086100 units in the socket of a BOOSTXL-TPS650861 board, directly on customer board, using a third party vendor, or by sending the OTP file back to Texas Instruments to go through formal release to market process, depending on volume requirements. All OTP programmed settings should be validated during prototyping phase to ensure desired functionality because parts cannot be returned in case of incorrect programming. Report issues to http://support.ti.com.

2 TPS65086100 Memory Structure

TPS65086100 PMIC is intended to serve as the customer OTP programmable version of the TPS65086xxx family, which includes the TPS65086, TPS650861, and TPS650864 devices. It will come from factory fully trimmed, but with all user programmable OTP registers programmed to '0'. The OTP registers are EPROM, so values in an OTP bank can be changed from '0' to '1' but a '1' cannot be changed back to a '0'. The TPS65086100 has two banks of OTP memory, bank 0 and bank 1, so each part can programmed twice. Any changes from a '0' to a '1' can be written without changing banks for additional programming.

The TPS65086100 has two forms of storage: OTP memory and active registers. The active registers are what are interfaced with when using I^2C communication and there is an active register for every OTP bit. There are also active registers bits which do not have an equivalent OTP bit. For example, the IRQ register, which shows which interrupts are active, does not have an OTP register since there would be no value in starting with a default value other than '0'. At first power up and after any device resets, the OTP bits are loaded into the active registers. When programming the OTP, the active register bits with OTP registers are programmed into the selected OTP bank.

The TPS65086100 has two I^2C device addresses for two different sets of registers. The first is located at 0x5E by default and most of the registers in it are intended to be accessed by the processor during normal operation. These include the DEVICEID1 and DEVICEID2 values, the voltage setting of each regulator, the interrupts, and more. The I^2C address of this first set of registers can be changed, but it is generally recommended to keep it at 0x5E unless a change is necessary. The second register address is fixed to 0x38 and the registers in it are intended to be only accessed when setting up the OTP. Registers in 0x38 are complicated and designed for use with automated test equipment. An Excel OTP Generator file is provided to simplify the OTP setup process. By filling out the Excel form, a simple I^2C sequence is generated which can be run either in the IPG-UI or any I^2C capable device.

3 I^2C Protocol

The TPS65086100 uses I^2C protocol for communication. Further information on the I^2C interface in the device can be found in the *TPS650861 Programmable Multirail PMU for Multicore Processors, FPGAs, and Systems* data sheet.

4 Using the TPS65086100 OTP Generator

The TPS65086100 OTP Generator Excel based tool is provided to simplify the programming of the device OTP. It shows the available options and outputs the required register writes to achieve these settings. It is designed to work with the IPG-UI but also provides the raw output for alternate I2C communication options. The following sections will provide some guidance on using this tool. For more information on any of the settings mentioned in this section refer to the device datasheet.

The color coating in the document is used to indicate areas that can or cannot be modified. The yellow boxes indicate cells that should be modified to match the desired settings. Red boxes indicate that the current value is not valid and needs to be changed. This is most common when the voltage of BUCK1, BUCK2, or BUCK6 are outside the bounds of the chosen step size. White and grey boxes should not be changed. In general, the OTP Generator tool will prevent unexpected modification of cells.

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NOTE: It is highly recommended to use Microsoft Excel to access the TPS65086100 OTP Generator Excel based tool as other programs that can open Excel files may not include all of the functionality needed to ensure the tool works correctly.

4.1 Overview Sheet

The first sheet of the tool is the Overview sheet. It outlines the basic settings of the device.

4.1.1 OTP Description

The OTP Description box has four settings:

1. OTP Name: This field is provided for providing a description of the OTP stored in the Excel file. It could be a board name that the OTP program is being designed for, or a processor target. This is not used elsewhere in the OTP Generator tool, it is just for identification purposes.
2. Part Number: This value modifies the DEVICEID1 register contents and can be used to identify different OTP program variants. All parts shipped from TI will start with a default value of TPS65086**100**. If multiple OTP programs are being used, it is recommended to program each variant with a different Part Number so that the DEVICEID1 register can be read to determine which OTP is programmed in each part. This will help prevent installing parts programmed with the wrong OTP program.
3. OTP Version: This is similar to the Part Number field, it modifies the content of the OTP_Version bits in the DEVICEID2 register. A = 0x0, B = 0x1, C = 0x2, and D = 0x3. This is helpful if multiple revisions of a single program are used. 0x0 could be the first version of an OTP program and if changes are necessary, it could be updated to 0x1 and any parts with 0x0 in the OTP_Version bits can be replaced with units programmed with the new 0x1 program.
4. Purpose: This field is provided for providing any further description of the OTP stored in the Excel file if desired. It is not used elsewhere in the OTP Generator tool.

OTP Description	
OTP Name:	Programming
Part Number:	TPS65086100
OTP Version:	A
Purpose:	Programming
Test Revision:	0

Figure 1. OTP Description Box

4.1.2 Default Voltages

The second box contains the default voltages and step sizes for all of the voltage regulators. After selecting a voltage for BUCK1, BUCK2, or BUCK6, the step size options will populate with the available step sizes. For controllers, 10 mV step size supports from 0.41 V to 1.67 V and 25 mV step size supports 1 V to 3.575 V. For converters, the 25 mV step size supports the full 0.425 V to 3.575 V range.

If choosing to use BUCK1 to generate a 5 V supply, select "Ext FB" to indicate that external feedback resistors will be used. Step size and SLP_VID will no longer apply.

BUCK6 can support an additional fixed voltage of 1.2 V when using CTL2 as a voltage selection control pin. To enable this functionality either the "CTL2&CTL3" or "CTL2&CTL6" options have to be selected as the SLP_VID Selection Pin in the Sequencing tab. This can allow the support of multiple DDR voltages with a single OTP program if necessary. Generally, these additional voltage options can be ignored unless necessary. If the step size is set to 25 mV then the additional BUCK6 fixed voltage will be 2.4 V instead of 1.2 V.

If the alternate SLP_VID voltages are not going to be used then they can be set to any value. The "-" symbols for the SLP_VID values will use the same as the regular VID values.

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Default Voltages			
Rail	**Voltage (V)**	**Step Size:**	**Default VID**
BUCK1_VID	0.000	10 mV	0000000
BUCK1_SLP_VID	-		0000000
BUCK2_VID	0.000	10 mV	0000000
BUCK2_SLP_VID	-		0000000
BUCK3_VID	0.000	25 mV	0000000
BUCK3_SLP_VID	-		0000000
BUCK4_VID	0.000	25 mV	0000000
BUCK4_SLP_VID	-		0000000
BUCK5_VID	0.000	25 mV	0000000
BUCK5_SLP_VID	-		0000000
BUCK6_VID	0.000	10 mV	0000000
BUCK6_SLP_VID	-		0000000
BUCK6 (CTL2 Alternate)	1.200		
LDOA1_VID	1.35		0000
LDOA2_VID	0.7		0000
LDOA2_SLP_VID	-		0000
LDOA3_VID	0.7		0000
LDOA3_SLP_VID	-		0000

Figure 2. Default Voltages Box

4.1.3 LDOA1 and SWB2

The next box covers the use of LDOA1 and SWB2. LDOA1 can be configured as part of the sequence like the rest of the rails or it can be configured as an always on LDO. When LDOA1 is used as part of the sequence, SWB2 cannot be used in sequencing. SWB2 can be merged with SWB1 or it can be controlled by I2C separately. If LDOA1 is not used in the sequence, it can be set to be always on or off by default. If off by default, it can be turned on by I2C. The emergency shutdown behavior setting determines whether LDOA1 will turn off in the event of an emergency shutdown. If LDOA1 is always on and configured to turn off in the case of an emergency shutdown, the duration of the turn off can also be modified. These options become visible if they are required.

4.1.4 Load Switch Power Good Options

The fourth box provides the load switch power good options. The load switches can monitor their output voltage and report power good and power fault based on these values.

4.1.5 GPO Configuration

The final box describes the available options for the GPO. GPOs can be controlled in two ways, using the GPOx_CTL bit shown in Figure 5. When configured to "I2C" mode, a GPO is high or low based strictly on the setting of the corresponding GPOx_LVL bit in the I2C_RAIL_EN2 register. The default state of these bits is configured by the "Default state if I2C option". When configured to "Power good" mode, the GPO monitors the unmasked power good signals it is assigned in the Sequencing tab and goes high when all of the unmasked power good signals are high. The GPOx_LVL bits have no impact on a GPO configured to be in "Power good" mode. All four GPOs can operate in open drain mode. GPO1, GPO2, or GPO3 can alternatively be configured to push-pull output mode which uses the LDO3P3.

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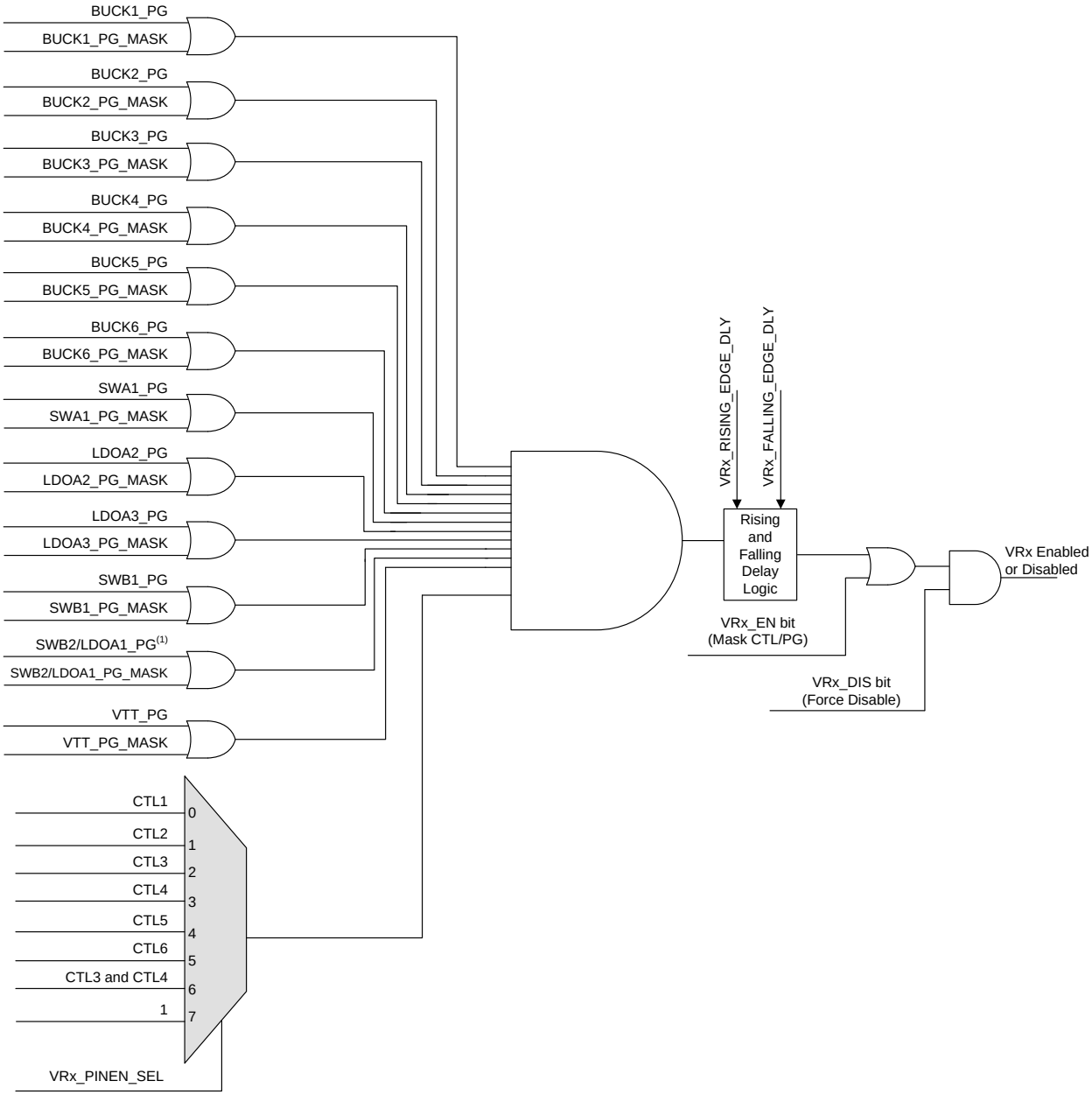
4.2 Sequencing Sheet

The sequencing sheet outlines the options for powering up and powering down the voltage regulators and GPOs. Each voltage regulator except VTT LDO and LDOA1 has the enable control circuit shown in Figure 3. In cases where LDOA1 is preferred to be in the sequence, it can use SWB2's sequencer.



(1) SWB2 sequencer can be used by LDOA1 instead.

Figure 3. Voltage Regulator Enable Control

VTT LDO has the enable control circuit shown in Figure 4.

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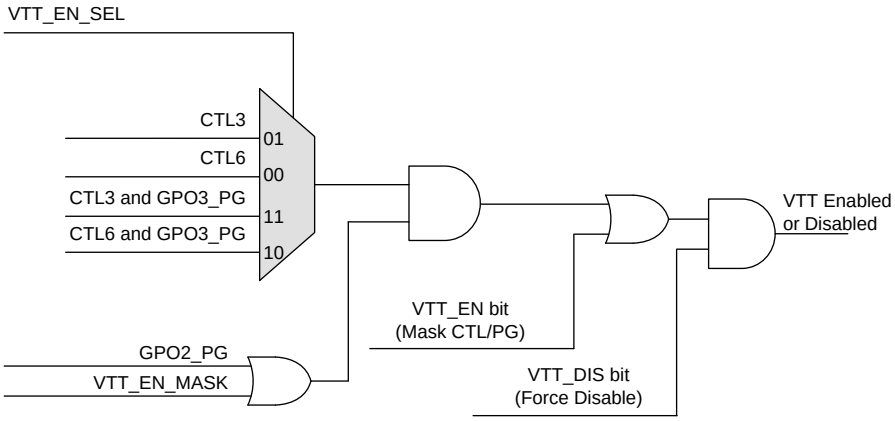

Figure 4. VTT Regulator Enable Control

GPOs have the enable control circuit shown in Figure 5, which is similar to the VRs.

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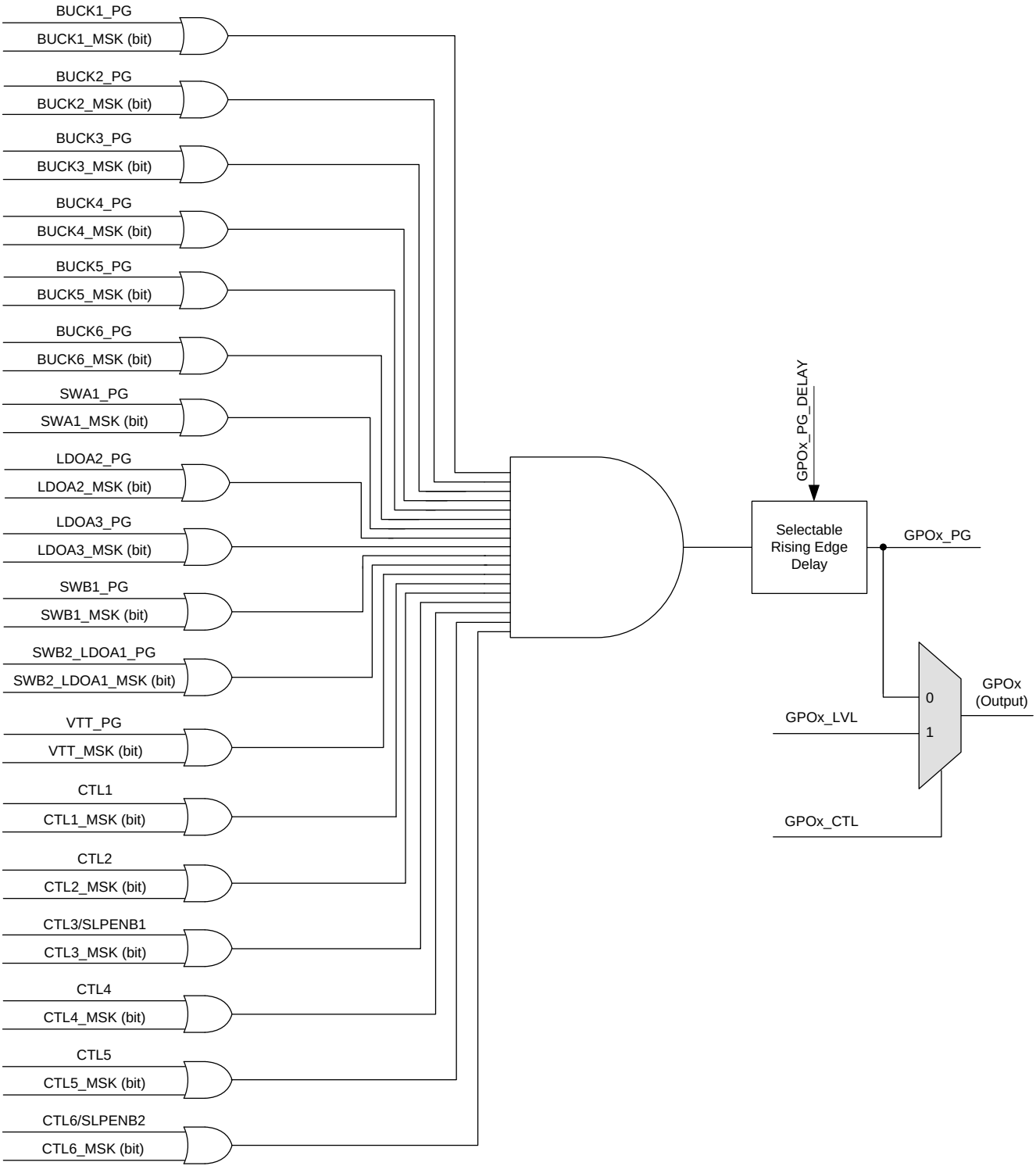

Figure 5. GPO Enable Control

4.2.1 Pin Assignments

The "Pin Assignments" box is used to set up the sequencing. The columns have the following meaning:

1. The "Assigned to which CTL pin?" input is used to determine the input to the multiplexor shown in Figure 3. Generally CTL4 should not be used as it is used for entering the programming state. An input

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of "-" results in a '1' being output from the multiplexor. This setting cannot be changed in the active (volatile) registers.

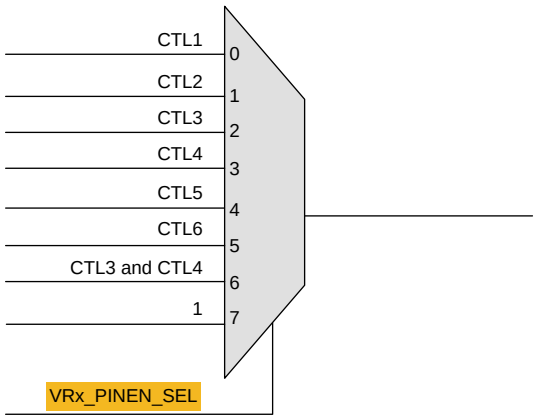

Figure 6. CTL Pin Assignment

2. The "Disabled by default?" input controls the regulator disable bit (BUCK1_DIS, BUCK2_DIS, etc.) and is one of the inputs to the final AND gate of the sequencer. As long as this is "Yes", the regulator will not turn on, so it is generally set to "No" if used in the sequence and "Yes" if planning to only enable by I^2C.

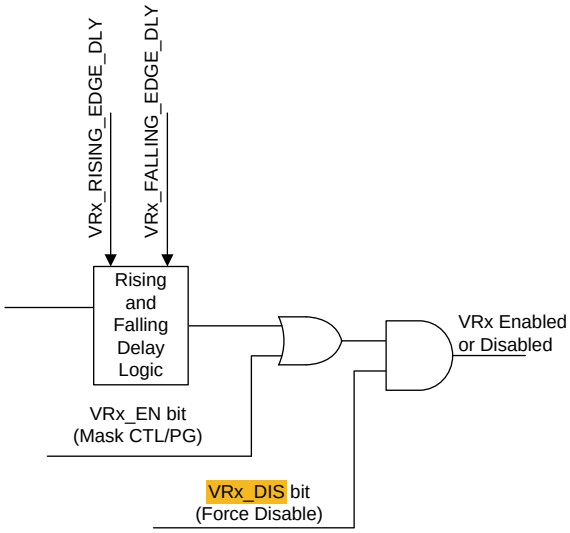

Figure 7. Disabled by Default

3. The "CTL/PG by default" input corresponds with the voltage regulator enable bit (BUCK1_EN, BUCK2_EN, etc.) and is one of the inputs to the final OR gate of the sequencer. As long as this is set to "Yes", the regulator will ignore the control pins and power good signals and turn on as long as the disable bit is not forcing the regulator off. It should be set to "No" if the regulator is used in the sequence and can be set to "Yes" if using the regulator disable bit to enable by I^2C.

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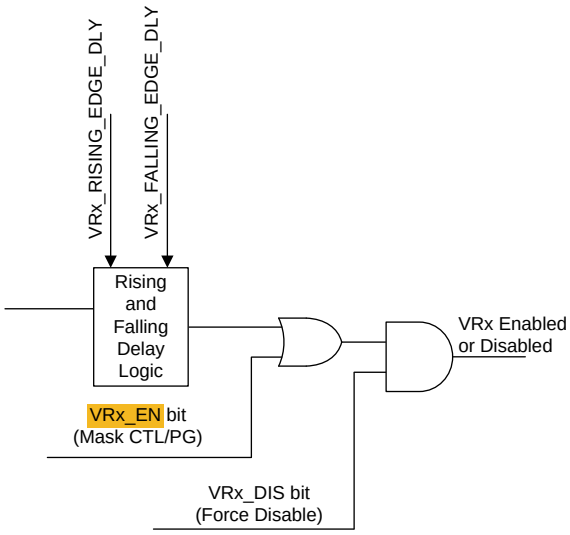

Figure 8. CTL_PG by Default

4. The "SLP_VID Selection Pin" input determines whether the regulator uses CTL3 or CTL6 to switch from the VID to SLP_VID setting. If SLP_VID is not needed, this selection does not matter as long as SLP_EN is set to "No" as well. This setting cannot be changed in the active (volatile) registers.
5. The "SLP_EN by default" input determines whether the regulator should mask the state of the assigned sleep CTL pin and instead always use VID. This should be "No" unless using SLP_VID to switch between voltages.

4.2.2 Inputs to Enable Logic

The "Inputs to Enable Logic" box controls the input to the first AND gate shown in Figure 3. The rail name on the left is the rail to be enabled / disabled and the columns indicate which power goods it is dependent on. The voltage regulators will depend on the CTL pin assigned in the "Pin Assignments" box in addition to those assigned in this box. Typically the easiest way to generate a sequence is to have each rail enabled by the power good of the previous rail. This will create a clean staggered power up. It is not recommended to enable multiple rails at the same time to minimize inrush current on the external supply. The simplest way to implement a power down sequence is to utilize the falling delays, though it may be necessary to merge some rail power down timings to ensure a timely shutdown. For example, to implement a sequence where BUCK1, and BUCK2 are first in the sequence, BUCK3 is second in the sequence, BUCK4 is third in the sequence, and GPO1 signals that all rails in the sequence are high, and it's equivalent reverse sequence, it is recommended to have BUCK1 not rely on any PG, BUCK2 rely on BUCK1_PG, BUCK3 on BUCK2_PG, and BUCK4 on BUCK3_PG. GPO1 would check all rail power goods and go high when all rails reach power good. Falling edge delays would be no delay for BUCK4, 2 ms for BUCK3, and 4 ms for BUCK1 and BUCK2. All should be assigned to one CTL pin, CTL1 for example. Table 1 shows a summary of this example in a table.

Table 1. Example of Sequence Control

Sequence #	Rails	CTL Pin Control	PG Control	Falling Edge Control
1	BUCK1, BUCK2	BUCK1 relies on CTL1. BUCK2 relies on CTL1.	BUCK1 relies on no PG signals. BUCK2 relies on BUCK1_PG.	BUCK1 & BUCK2 falling edge delay is 4ms.
2	BUCK3	BUCK3 relies on CTL1.	BUCK3 relies on BUCK2_PG.	BUCK3 falling edge delay is 2ms.
3	BUCK4	BUCK4 relies on CTL1.	BUCK4 relies on BUCK3_PG. GPO1 relies on BUCK1_PG through BUCK4_PG.	BUCK4 falling edge delay is 0ms.

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4.3 Additional Details Sheet

The "Additional Details" Sheet contains the remaining settings.

4.3.1 Force PWM or Auto

The "Force PWM or Auto" box allows the choice for each BUCK controller (BUCK1, 2, and 6) to operate in either Forced Pulse Width Modulation (PWM) mode or Auto mode which allows Pulse Frequency Modulation (PFM) at light loads. PWM mode is the recommended setting for any projects where light load efficiency is not important. It will result in a stable output frequency which typically generates less noise at light loads. Auto mode improves the light load efficiency but at the cost of more noise and higher output voltage ripple. Note that at high loads, both modes will be in PWM mode. This setting only affects light load behavior. The BUCK controllers (BUCK3, 4, and 5) only support forced PWM mode.

4.3.2 Discharge Resistor Default

The "Discharge Resistor Default" box provides the ability to set the discharge resistor on each output while the output is disabled. They help to provide a more controlled power down sequence by adding a fixed load. The lower the resistance, the faster the discharge.

4.3.3 Power Fault Masking

The "Power fault masked by default?" box determines whether the PMIC initiates emergency shutdown in case of a power fault of each specific voltage regulator. It is recommended to mask any unused voltage regulators. For load switches, if they are expected to use any voltage other than the fixed value on the "Overview" sheet, it is recommended to mask them also.

4.3.4 Decay or DVS

The "Decay or DVS Down" box allows for choosing between decay or dynamic voltage scaling (DVS) when changing from VID to SLP_VID. In general it should be left at "DVS" unless power savings due to rapid transitions between VID and SLP_VID are significant.

4.3.5 VTT ILIM

The "VTT ILIM" box allows for the choice of four nominal VTT LDO current limit settings. The actual current limit may vary slightly from this value.

4.3.6 I2C Address

The "I2C Address" box allows for changing the I2C address of the "Configuration Registers", which includes all the registers which are accessible when not in the programming state. It is highly recommended not to change from 0x5E unless there is a conflict with another IC on the I2C bus. Note that if trying to stay compliant with I2C specification, some addresses may not be available.

4.4 Programming Board Setup Sheet

The "Programming Board Setup" sheet provides some information on how to set up the BOOSTXL-TPS650861 programming board to allow for proper sequencing. While it is not required to use the BOOSTXL-TPS650861 BoosterPack plug-in module for programming it does provide an easy way to program the TPS65086100. This tab provides the possible input options for PVINLDOA2_A3, VIN_SWA1, VIN_SWB1_2, and VIN_345ANA nets in order to properly power the device. It only checks the voltages. It does not check that the sequence will work. For example if BUCK2 is providing 1.8V but it is enabled after LDOA2, it should not be used for PVINLDOA2_A3. This sheet also notes the necessary changes to modify a TPS650860EVM-116 to support 5 V output on BUCK1 if "Ext FB" is selected. It is not recommended to generate 5 V output on the BOOSTXL-TPS650861 board and instead just confirm that the output is regulating properly to 0.4 V.

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4.5 Script Generator Sheet

The final sheet is the "Script Generator" sheet which contains two sets of text. The first represents the necessary text to be copied to the TPS650861-Script-[revision].js to allow the IPG-UI to program the new OTP program. The cells highlighted in purple can be copied and pasted directly with a text editor. For more information on using the IPG-UI to program a TPS65086100 refer to the *BOOSTXL-TPS650861 EVM User's Guide*. The second table shows the raw commands necessary to program a part without the IPG-UI to perform the I2C communication. These commands will set the active registers to the desired program settings. One key item to note is that the contents of the register which contains VTT ILIM need to be preserved. In order to do this, the data should be read first, then bits 1 and 2 changed and the result written back to the PMIC. Any register writes generated with the value 0x00 can be omitted, as the OTP memory will already have a value of 0x00 in that register.

5 Entering Programming Mode

In order to access the registers in device address 0x38 the TPS65086100 must first be put into programming mode by writing the PROGRAMMING_STATE bit in the OTP_CTRL1 register to 1b. In order to access this register, 7V must be placed on the CTL4 pin. Once the PROGRAMMING_STATE bit in the OTP_CTRL1 register is set to 1b, remove the 7V from the CTRL4 pin. Once this is done all of the registers in the device can be accessed.

NOTE: When applying 7V for programming ambient temperature must remain below 50 °C, and total time must be less than one minute.

6 Burning in the OTP

After all of the active registers are set to the desired program settings, the contents need to be burned into the OTP memory. To burn the contents of the active registers to OTP memory the PROGRAM_OTP bit in the OTP_CTRL1 register must be set to 1b, while a 7 V supply of at least 10mA is placed on the IRQB pin. Once the PROGRAM_OTP bit in the OTP_CTRL1 register is set to 1b, remove the 7V from the IRQB pin.

NOTE: When applying 7V for programming ambient temperature must remain below 50 °C, and total time must be less than one minute.

7 Tips and Tricks

1. GPOs don't have falling edge sequencing, so sometimes unused LDOs and load switches are more effective for external sequencing.
2. If the IRQB pin is not used by the processor, then it can be used strictly as a programming pin and does not need to have a pull-up or connection to the processor.
3. It is recommended to not assign anything to CTL4 and to use it strictly as a programming pin. Otherwise going into programming state can cause rails to turn on unexpectedly. This should not be a problem for initial programming, but can be an issue for reprogramming or debugging. If CTL4 must be used to enable a rail, then using the "CTL3&CTL4" option can help mitigate this risk.
4. GPO2 power good tree is usually reserved for VTT LDO enable to ensure that it isn't enabled prior to BUCK6 being turned on. GPO2 can be set to I2C control and used independently as well.
5. GPO3 minimum delay is 2.5 ms, it is generally used as the final GPO if it is used at all.

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