CC2533 Silicon Errata

Errata

Literature Number: SWRZ034A
June 2010–Revised October 2014

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1 Introduction

This document describes the known exceptions to functional specifications of the indicated devices.

The advisory numbers in this document may not be sequential. Some advisories may not be numbered. Some advisories may be moved to the next revision and others may have been removed and documented in the data sheet. When items are moved or deleted, the remaining numbers remain the same and are not resequenced.

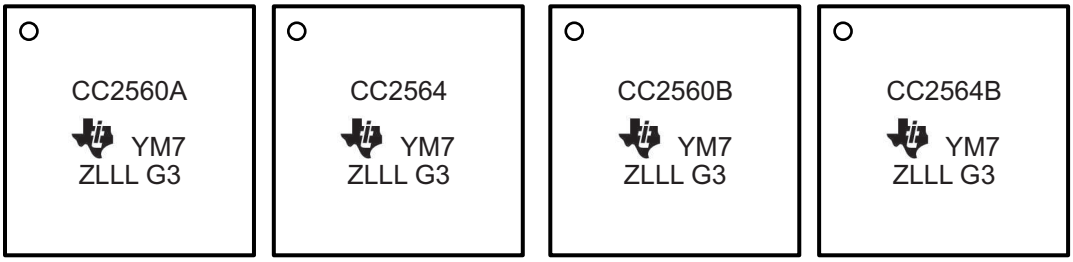
1.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices

X...	Experimental, preproduction, sample or prototype device. Device may not meet all product qualification conditions and may not fully comply with TI specifications. Experimental/Prototype devices are shipped against the following disclaimer: “ This product is still in development and is intended for internal evaluation purposes. ” Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.
null...	Device is qualified and released to production. TI ’ s standard warranty applies to production devices.

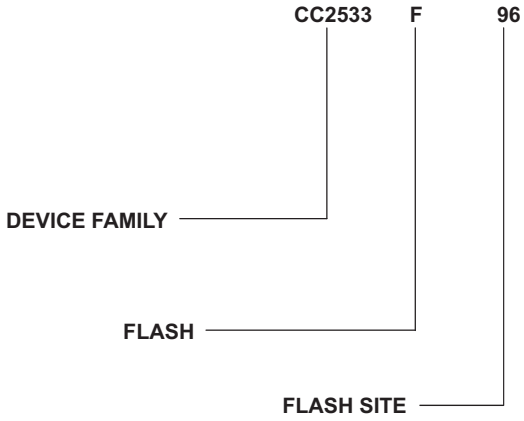
1.2 Device Markings

Figure 1 provides an example of the Concerto device markings and defines each of the markings. The device revision can be determined by the symbols marked on the top of the package as shown in Figure 1. Some prototype devices may have markings different from those illustrated. Figure 2 shows an example of the device nomenclature.



Y = Last digit of the year
M = Month in hex number, 1-C for Jan-Dec
7 = Primary site code for ANM
Z = Secondary site code for ANM
LLL = Assembly lot code
○ = Pin 1 indicator

Figure 1. Example of Device Markings



A The additional 256KB is added to the Cortex™-M3 core (Connectivity Devices) or to the C28x™ core (Base Devices).

Figure 2. Example of Device Nomenclature

2 Known Design Exceptions to Functional Specifications

Table 1. Advisory List

Issue 1 *DMA Variable Transfer Length with Length 0 or 1*

Revision(s) Affected All revisions affected

Details Depending on which VLEN mode is used, attempting a variable length transfer with length 0 or 1 can lead to erroneous behavior by the DMA. The failing conditions will not occur naturally in an application as they do not transfer useful data, but may occur as the result of an error condition at the source of the DMA transfer. The DMA is generally set up with variable transfer length to transfer packets that come in over USART or RF. If there is an error in the medium, these packets may be malformatted. If they for example contain a length byte of 0, using the DMA to transfer those packets automatically without taking the described precautions may lead to a buffer overrun. The two VLEN modes that are affected are VLEN values 001 and 010. VLEN values 000, 011 and 100 work without restrictions.

In VLEN modes VLEN = 001 and VLEN = 010, the DMA transfers a number of bytes/words based on the value of the first byte/word it reads from the source (the length byte/word). In the event that a transfer is started with a length byte/word of 0 or 1, the wrong number of bytes will be transferred and the DMA interrupt may be lost. The failure mode depends on whether byte or word mode is selected for the transfer as described in DMA Variable Lenght Restrictions .

DMA Variable Lenght Restrictions

VLEN	Byte Mode	Word Mode	Comment
000	OK	OK	
001	Two bytes transferred when length byte is 0	Two words transferred when length word is 0	Can be used if contents of length byte/word in source buffer can be checked not to be 0 or 1 before DMA is triggered, or if an extra transfer to destination is acceptable.
010	Excessive number of bytes transferred when length byte is 0 Extra transfer when length byte is 1	Two transfers executed when length word is 0 or 1 Interrupt not raised when length word is 0.	Byte mode can be used if contents of length byte in source buffer can be checked not to be 0 or 1 before DMA is triggered.Word mode can be used if contents of length word in source buffer can be checked not to be 0 or 1 before DMA is triggered, or if an extra transfer to destination is acceptable.
011	OK	OK	
100	OK	OK	

Workaround(s) Please observe the comments for each of the affected modes in order to use them without issues. Alternatively, any of the unaffected VLEN modes can be used if the buffer sizes are adjusted accordingly.

Issue 2 *Timer 2 (MAC Timer) Read Latching*

Revision(s) Affected All revisions affected

Details In Timer 2, the value of T2M1 is latched when T2M0 is read, and the values of T2MOVF1 and T2MOVF2 are latched when T2MOVF0 is read. This does not work as expected when the least significant byte read is 0xFF. When the timer is read on the cycle where the least significant byte is about to wrap around, the latched values are captured one cycle later. This means that the latched registers are incremented while the register that was read first (T2M0 or T2MOVF0) is not.

Workaround(s) To read Timer 2 overflow: Use T2CTRL.LATCH_MODE = 1 and read T2M0 to trigger latching. Then read the overflow counter and ignore the result of the T2M0 read. To read Timer 2 counter: Read T2M0 first. If T2M0 == 0xFF, read timer once more to confirm its state.

Issue 3 *Watchdog Timer Counts Too Fast when System Clock Division is Enabled*

Revision(s) Affected All revisions affected

Details If system clock division is used (CLKCONCMD.CLKSPD ≠ CLKCONCMD.OSC) the Watchdog timer will count too fast. If clock division is used, for each 32 kHz clock cycle, the Watchdog timer will count more than one period. The number of periods counted is proportional to the amount of division.

Workaround(s) If clock division is used, a proportionally larger WDT timeout should be used if possible.

Issue 4 *Leaving PM2/3 can produce glitches on the SCL and SDA pins*

Revision(s) Affected All revisions affected

Details Glitches can occur on the SCL and SDA pins when leaving PM2/3.The I2C pins SCL and SDA should be high impedance with pull-up when not transmitting on the I2C bus. This issue can cause a low pulse for approximately 250 ns when going from PM2/3 to Active Mode. This is due to an insufficient reset of the I2C module when exiting PM2/3.

Workaround(s) To prevent these glitches, the I2C pin override bit (I2CWC.OVR) can be set before entering PM2. This bit overrides the I2C module's control of the I/O lines and sets them to the state defined in I2CWC. They should then be left in the reset state for I2CWC which is input with pull-up enabled. The I2CWC.OVR bit can be cleared just after returning to Active mode. This prevents any glitches from propagating to the pins.

Revision History

Changes from June 1, 2014 to October 3, 2014 **Page**

- Added Updated to new standards 7
- Added Issue 4, Leaving PM2/3 can produce glitches on the SCL and SDA pins 7

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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