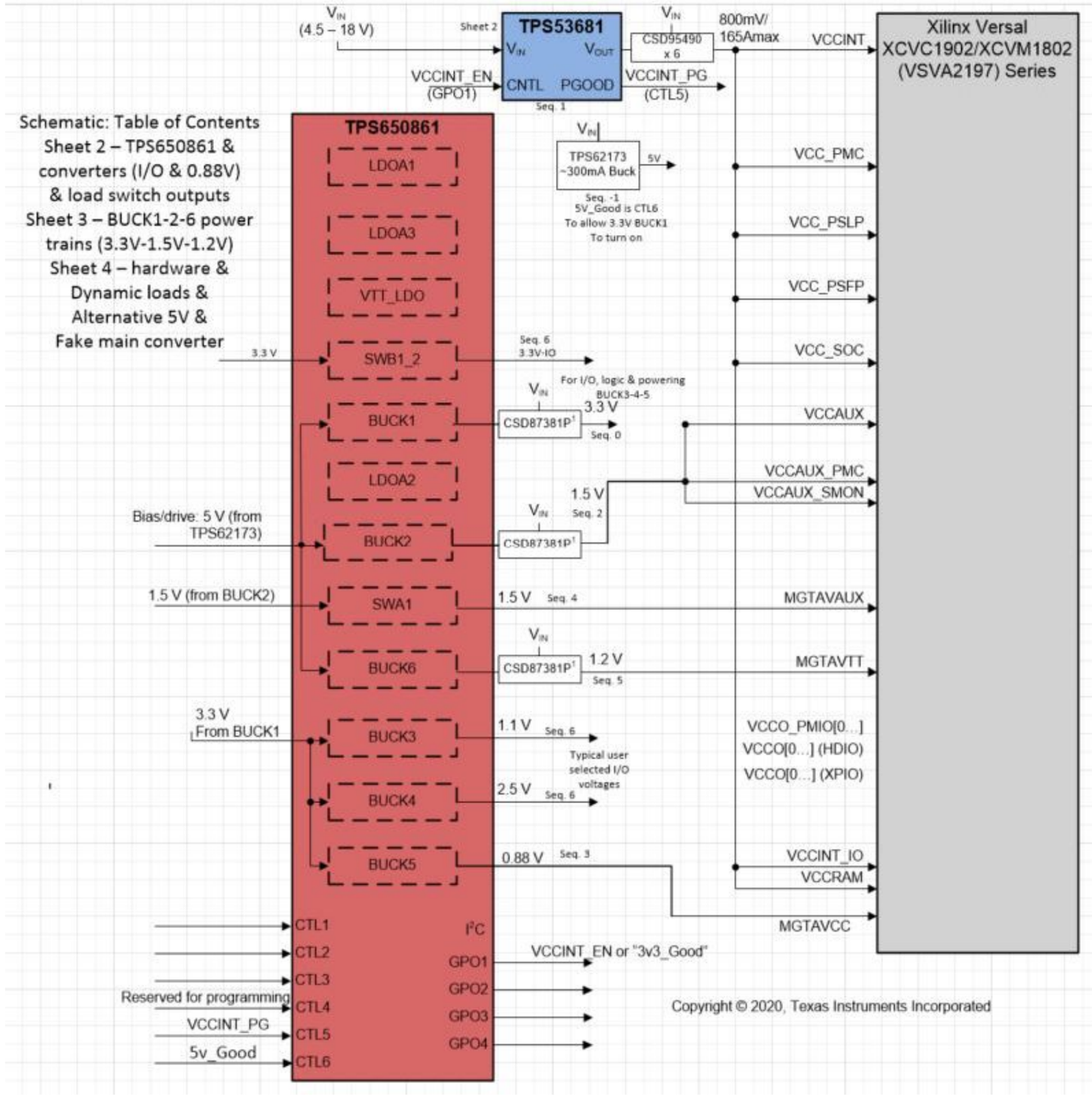
Main 0.8V (6 phases) and 5V TPS62173 provided on TPS53681EVM-002

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A



Target Application

TPS650861&Outputs.SchDoc

TPS650861_Bucks.SchDoc

PMP22165_Hardware.SchDoc

Table 9: **Power Supply Groupings for Minimum Rails, Mid-/High-Voltage Scenario**

Rail Group/ Sequence Order	Combined Rails	Nominal Voltage (V)	DC VRM Tolerance[1]	AC Ripple Noise[1]
1	VCCINT, VCC_PMC, VCC_PSLP, VCC_PSFP, VCC_IO, VCC_RAM, VCC_SOC	0.78 or 0.88 **now 0.8V**	1%	2%, ±25 mV (VCCINT)
2	VCCAUX, VCCAUX_PMC, VCCAUX_SMON (filtered)	1.50	1%	2%

Table 9: **Power Supply Groupings for Minimum Rails, Mid-/High-Voltage Scenario** *(cont'd)*

Rail Group/ Sequence Order	Combined Rails	Nominal Voltage (V)	DC VRM Tolerance[1]	AC Ripple Noise[1]
3	MGTYAVCC	0.88	3%	10mV pk-pk[2]
4	MGTYVCCAUX	1.50	3%	10mV pk-pk[2]
5	MGTYAVTT	1.20	3%	10mV pk-pk[2]
6	VCCO (multiple rails)	1 to 3.3	1%	4%

Notes:
1. Expressed as ±% from nominal voltage.
2. 10 kHz to 80 MHz.

Was tested along with

TPS53681EVM-002 providing 5V startup & main 0.8V

Items in maroon block along with test dynamic loads on this PMP22165 board

Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 4/21/2020	
TID #: N/A	Project Title: Versal Power Delivery		
Number: PMP22165 Rev: A	Sheet Title:		
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 1 of 4	
Drawn By:	File: PMP22165_CoverSheet.SchDoc	Size: B	
Engineer: Josh Mandelcorn	Contact: http://www.ti.com/support		

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for rev A PCB's
add C218 & C219 on bottom side of board from 3v3 feedthrus near U50 pins 21 & 18 to ground near ground feedthrus under U50

These caps must provide close bypass between U50 pin 21 and U50 powerpad

3v3 — X7S 1206 C218 6.3V 47uF — X7S 1206 C219 6.3V 47uF — GND

C50 2.2uF
C51 2.2uF
C52 10uF — C52 not needed if VTT not used
C53 10uF
C54 10uF
C55 10uF
R52 0
C56 1uF
C63 1uF

1v5 — 3v3 — 1v2 — 5v

R50 0 — not yet used
R51 0

U50

8	DRV5V_2_A1	BOOT1	35
38	DRV5V_1_6	DRVH1	33
46	PVINVTT	SW1	34
11	PVIN3	DRVL1	37
24	PVIN4	FBVOUT1	29
21	PVIN5	PGNDSNS1	36
50	PVINLDOA2_A3	ILIM1	30
32	PVINSWA1	BOOT2	5
18	PVINSWB1_B2	DRVH2	3
13	CTL1	SW2	4
62	CTL4	DRVL2	7
63	CTL5	FBVOUT2	2
61	CTL3/SLPENB1	PGNDSNS2	6
14	CTL6/SLPENB2	FBGND2	1
60	CTL2	ILIM2	64
58	CLK	LX3	10
59	DATA	FB3	12
15	IRQB	LX4	25
27	GPO3	FB4	23
16	GPO1	LX5	20
26	GPO2	FB5	22
28	GPO4	BOOT6	41
9	LDOA1	DRVH6	43
47	VTT	SW6	42
48	VTTFB	DRVL6	39
51	LDOA2	FBVOUT6	44
49	LDOA3	PGNDSNS6	40
31	SWA1	ILIM6	45
17	SWB1	AGND	52
19	SWB2	PAD	65
55	VSYS		
53	VREF		
56	LDO5P0		
54	LDO3P3		
57	V5ANA		

TPS65086100RSKR

BOOT1 BOOT2 DRVH1 DRVH2 SW1 SW2 DRVL1 DRVL2 FBVOUT1 FBVOUT2 ILIM1 ILIM2 FBGND2 — GND

Power Sequence Zero - always on

to BUCK1 3.3V next page

power seq. 2

to BUCK2 1.5V next page

0v78_Good called "VCCINT_PG" at system level

CTL1 CTL4 0v78_Good CTL3/SLPENB1 5v_Good CTL2 PMB_CLK PMB_DIO IRQB GPO3 3v3_Good GPO2 GPO4

TP99 5002 — GPO3 — "All Outputs Good"

Nov. 22: R65 changed from 100k to 10k

R57 100k R58 100k R59 100k R60 100k R61 100k R62 100k
3v3_SU R63 100k R64 100k R65 10.0k R66 100k R67 100k

pullups for GPOx pins needed

reserve CTL4 for programming

CTL6: 5v_Good turns on BUCK1 3v3

GPO1: BUCK1 good (3v3) turns on main TPS53681 0.8V output

CTL5: 0.8V good from TPS53681 allows BUCK2 1v5 to turn on

BUCK2 1v5 being good allows BUCK5 0v88 to turn on

BUCK5 0v88 being good allows SWA1 1v5 MGTAVAUX to turn on

SWA1 1v5 MGTAVAUX beibf good allows BUCK6 1v2 to turn on

BUCK6 1v2 being good allows I/O voltages to turn on: BUCK3 1v1, BUCK4 2v5 and SWB1/2 3v3_IO to turn on

April 20, 2020: C472 increased from 0.1uF to 4.7uF 0603 to reduce dynamic undershoot

R54 0 — not yet used — not yet used — not yet used — not yet used — GND

25% load step & +/-3% window

max ripple 10mV p-p 10 kHz to 80 MHz

1v5_MGTAVAUX — TP221 — TP211 — TP212

200mA max — J221 — 691214110002 — C472 4.7uF 25V — C57 1uF — TP222 — GND

12V_B — R55 0 — 3v3-IO — C64 0.1uF — 4% ripple / noise OK — J211 — 691214110002

power seq. 4 — **power seq. 6**

C58 1uF — GND

1.25V bandgap ref.

C59 0.1uF
C60 4.7uF
C61 4.7uF

3v3 — R56 0 — C62 1uF — 3v3_SU — GND

Apply 7V to CTL4 for programming

and also 7V to IRQB for "burn-in" of program

CONTROL I/O's for Programming

IRQB — CTL4 — J50 — TSW-103-07-G-S — C65 1uF — GND

Power Sequence Zero - always on: 5V_SU, 3v3_SU, 5v and 3v3

These internal voltages will always come up first with 3v3 being last of this group to come up

TPS53681 converter for 0.8V and 5V TPS62173 are on TPS53681EVM-002

Interface to TPS53681EVM-002

J481 — TSW-105-07-G-S — called "VCCINT_PG" at system level — U3-12 on EVM 0v78_Good — U2-8 on EVM 5v_Good — 3v3_Good to U3-13 on EVM — 5v to 5V_INT at C7 on EVM — GND to GND at C7 on EVM

BAT54C-7-F D99 — BAT54-7-F D488 — J99 — TSW-102-07-G-S — CTL1

On rev A PCBs add D488 by hand

jumper to power down and for programming

March 2020: 0v78_Good is now 0.8V_Good as main voltage now 800mV

BUCK3

L230 470nH — R230 0 — C230 6.3V 47uF — C231 4.7uF — C232 0.1uF — TP430 1v1_IO — J430 — 691214110002 — GND — TP431

4% ripple / noise OK

power seq. 6 I/O

BUCK4

L240 470nH — R240 0 — C240 6.3V 47uF — C241 4.7uF — C242 0.1uF — TP440 2v5_IO — J440 — 691214110002 — C243 6.3V 47uF — GND — TP441

4% ripple / noise OK

power seq. 6 I/O

for rev A PCB's
add C243 by hand each size "0805" English ok

effective cap of 47uF size 0805 at 2.5V bias ~26uF

max ripple 10mV p-p 10 kHz to 80 MHz

BUCK5

L250 470nH — R250 0 — C250 6.3V 47uF — C251 6.3V 47uF — C252 6.3V 47uF — C253 4.7uF — C255 6.3V 47uF — C254 0.1uF — C256 6.3V 47uF — TP450 0v88 — J450 — ED120/2DS — TP451 — GND

power seq. 3

25% load step & +/-3% window

Decoupling Capacitors

3.08A max

for rev A PCB's

piggyback C255 & C256 on top of C251 & C252

to BUCK6 1.2V

power seq. 5

Do not connect AGND pin 52 to powerpad in top layer.

must go first to return side of VREF bypass cap

BUCK3-4-5 converters switch at about 2 MHz off 3.3V
470 nF inductors recommended

TPS650861 multiple output converter / controller

Controls 3 outputs with power train next page

Buck converters for 0.88V and two I/O rails

1.5V & 3.3V load switches and 5V & 3.3V Startup LDOs

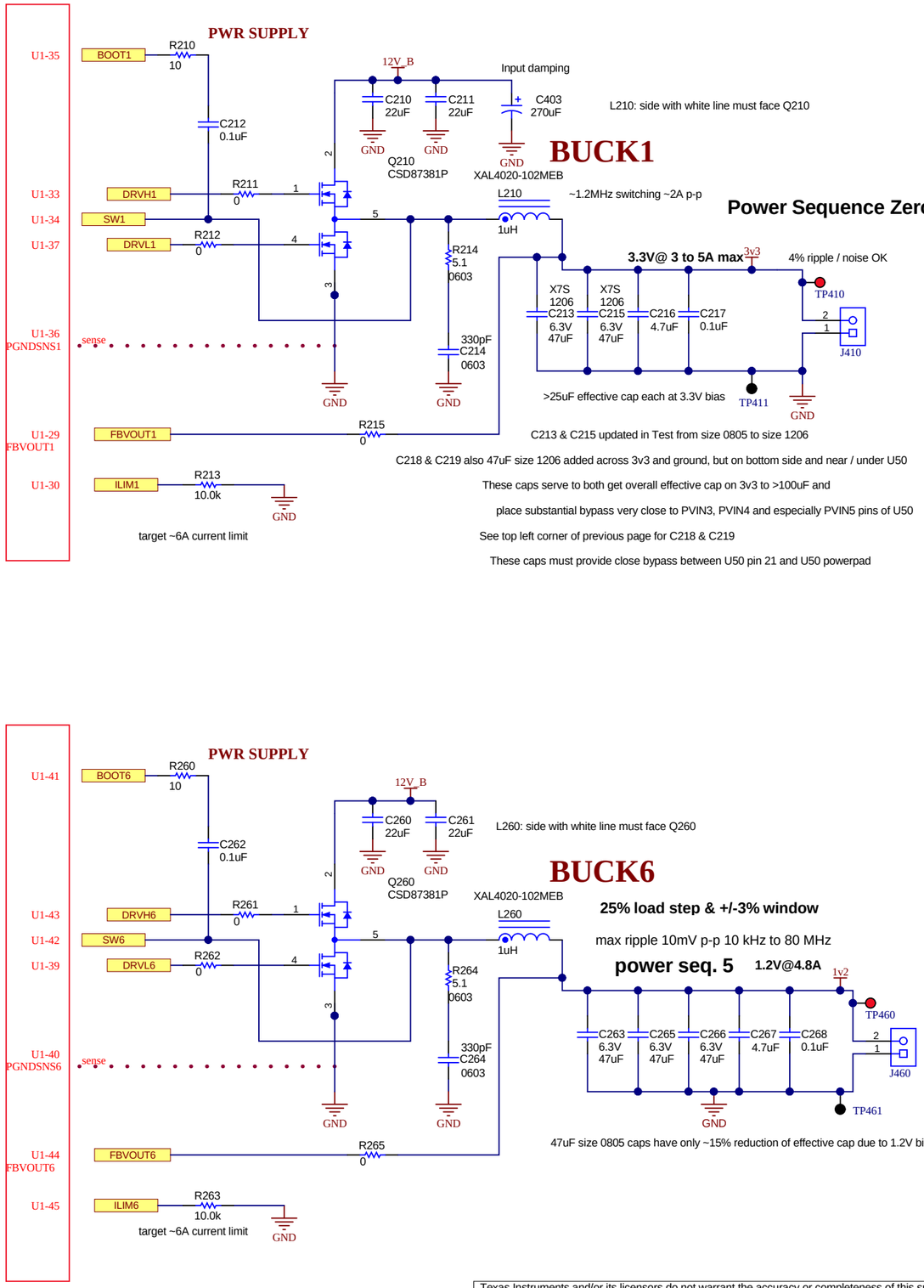
Orderable: ChangeMe in variant		Designed for: Public Release	Mod. Date: 4/21/2020
TID #: N/A		Project Title: Versal Power Delivery	
Number: PMP22165	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 2 of 4
Drawn By:		File: TPS650861&Outputs.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

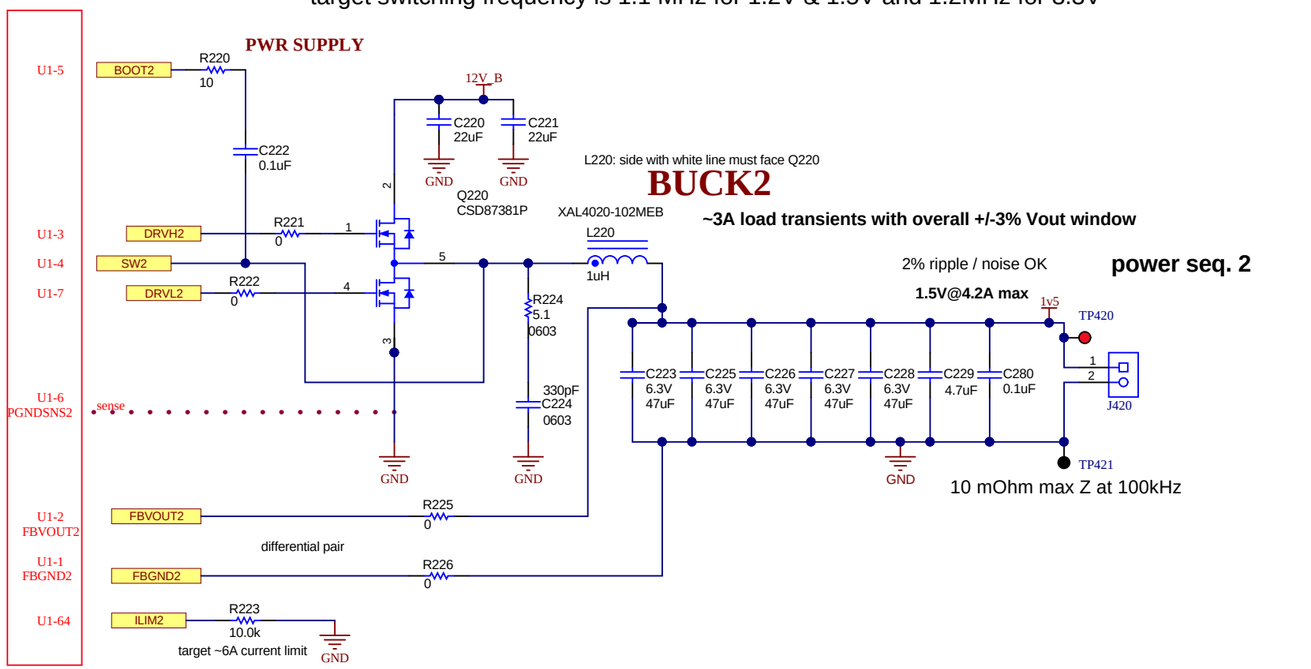
Power Trains of TPS650861 Bucks each ~5A max and

Powered off main Vin: 3.3V, 1.5V and 1.2V

Power Sequence Zero - always on

target switching frequency is 1.1 MHz for 1.2V & 1.5V and 1.2MHz for 3.3V





Orderable: ChangeMe in variant		Designed for: Public Release	Mod. Date: 2/17/2020
TID #: N/A		Project Title: Versal Power Delivery	
Number: PMP22165	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 3 of 4
Drawn By:		File: TPS650861_Bucks.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

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H1 NY PMS 440 0025 PH
H2 NY PMS 440 0025 PH
H3 NY PMS 440 0025 PH
H4 NY PMS 440 0025 PH

H5 1902C
H6 1902C
H7 1902C
H8 1902C

DNP FID1 DNP FID2 DNP FID3

PCB Number: PMP22165
PCB Rev: A

PCB LOGO
Texas Instruments

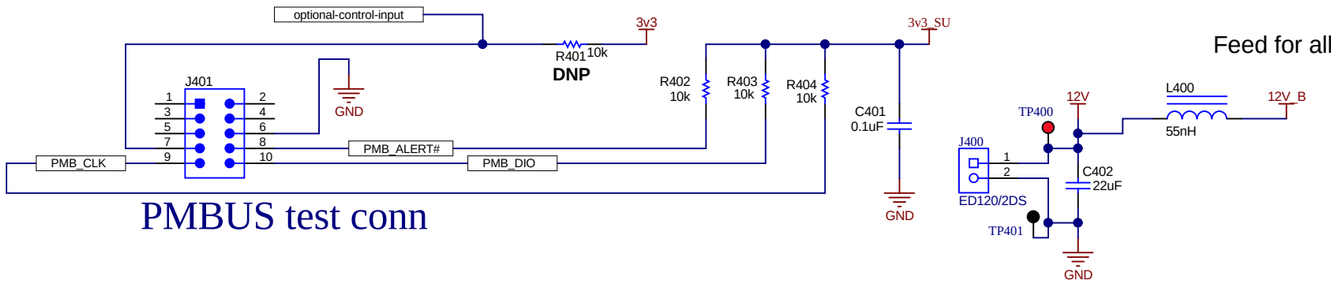
CE Mark

PCB LOGO
WEEE logo

with Rev A PCBs: C401, R402-3-4

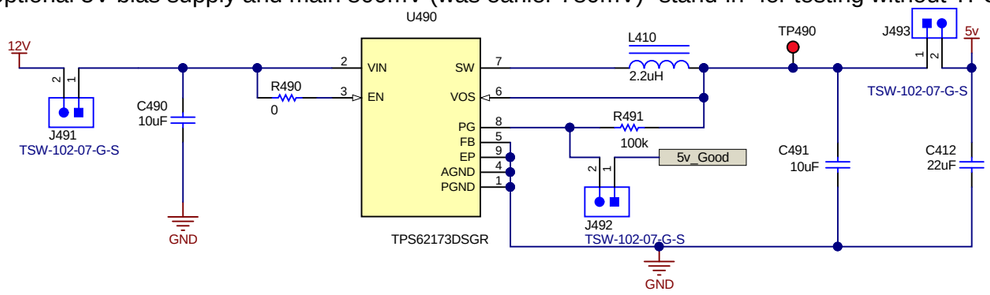
need to be cut from 3v3 and jumpered to 3v3_SU

Feed for all other outputs



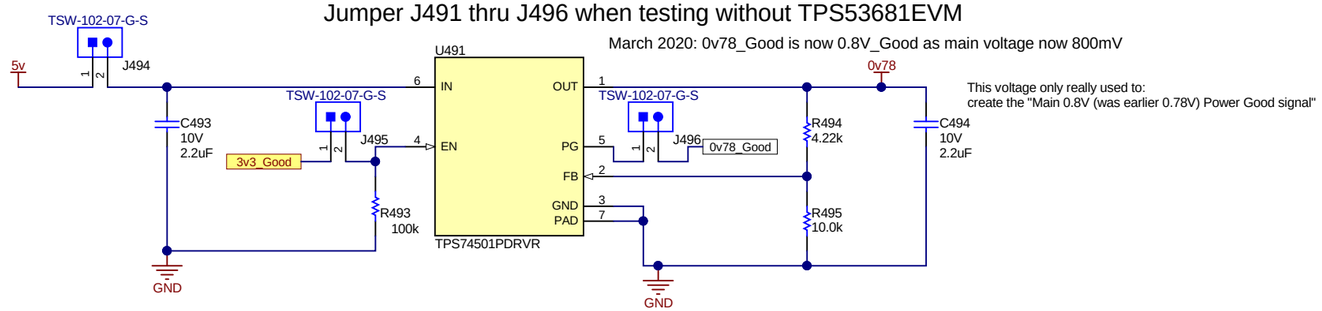
PMBUS test conn

optional 5V bias supply and main 800mV (was earlier 780mV) "stand-in" for testing without TPS53681EVM

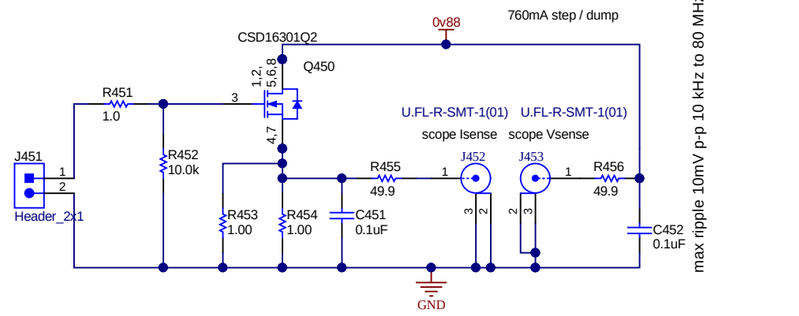


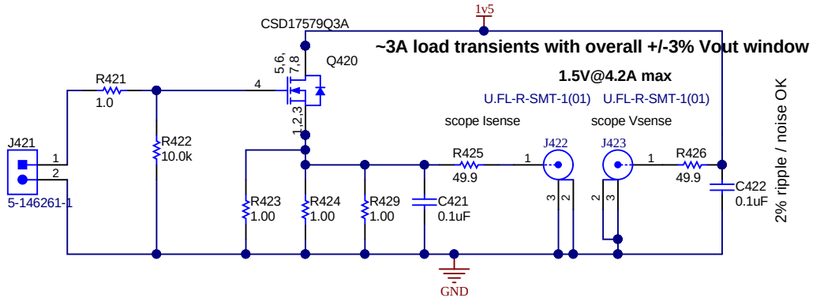
Jumper J491 thru J496 when testing without TPS53681EVM

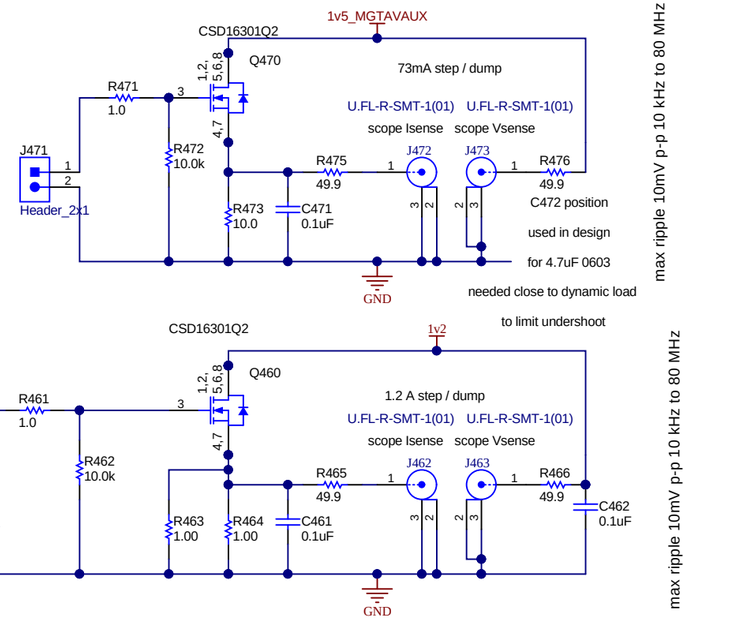
March 2020: 0v78_Good is now 0.8V_Good as main voltage now 800mV



This voltage only really used to:
create the "Main 0.8V (was earlier 0.78V) Power Good signal"







ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

Orderable: ChangeMe in variant		Designed for: Public Release	Mod. Date: 4/21/2020
TID #: N/A		Project Title: Versal Power Delivery	
Number: PMP22165	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 4 of 4
Drawn By:		File: PMP22165_Hardware.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

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