

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR-4 High Tg	5.00mil	4.2	
2	Signal Layer 1		1.40mil		
	Dielectric 2	FR-4 High Tg	5.00mil	4.2	
3	Signal Layer 2		1.40mil		
	Dielectric 3	FR-4 High Tg	5.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	

DESIGN INFORMATION

MIN. TRACE WIDTH: 10 MIL  
MIN. CLEARANCE: 8.9 MIL  
MIN. VIA SIZE: 18 MIL  
MINIMUM ANNIELING RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C  
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL  
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

FR-408  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  40 MIL (1.0mm) +/-10%  OTHER \_\_\_\_\_

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

DRILLING:

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

BOARD FINISH:

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_

SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

SURFACE FINISH:  IMMERSION GOLD (ENIG)  ENEPIG  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

ARRAY/PANEL:  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS ->  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION:  YES

BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER

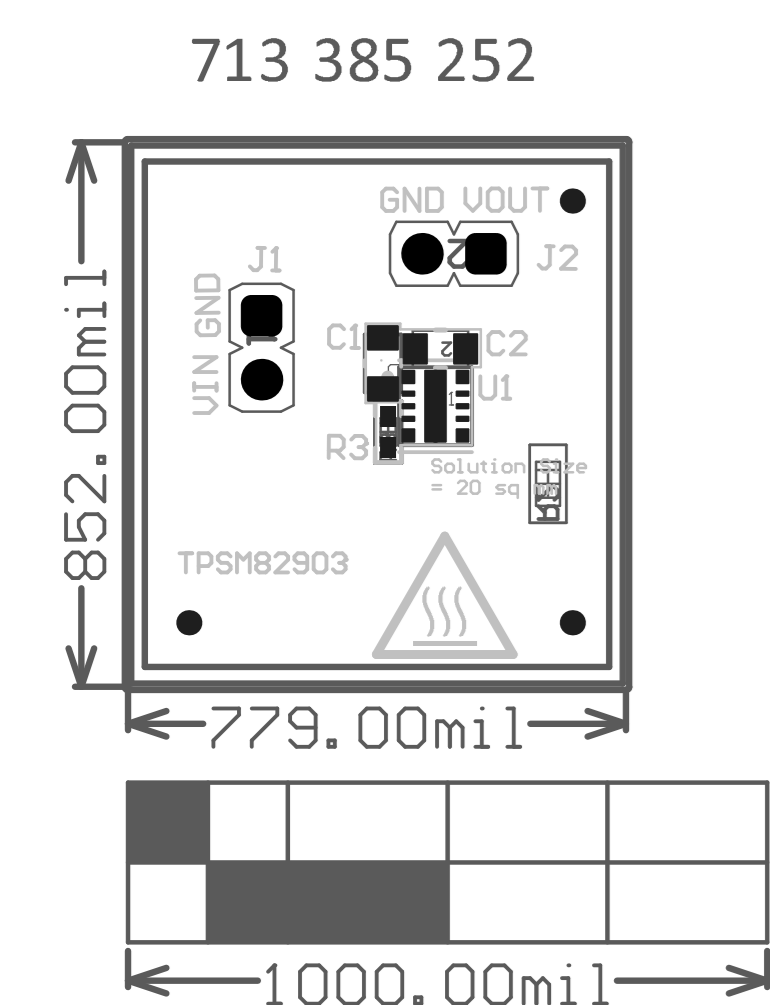
6.1MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.  
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.  
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.  
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED 'DNP' SHOULD NOT BE OBTAINED FROM THE BOARD MANUFACTURER.  
ASSEMBLY VARIANT: 001

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ENGINEER: Tahar Allag  
LAYOUT BY: Fred Illguth  
SCALE: 1.00  
ALTIUM DESIGNER VERSION: 22.7.1.60

BOARD NAME: TPS82903	BOARD: A	DATE: 08/22/2023	DESIGNER: A	DATE: 08/22/2023
LAYER NAME = TOP	TID #: .TIDGIT.	# DIT		
PLTNAME: TIDGIT	GENS: 001	DATE: 08/22/2023	DATE: 08/22/2023	DATE: 08/22/2023

Layer	Name	Material	Thickness	Constant	Board Layer Stack
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	Top Solder	Solder Resist	0.40mil	3.5	
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DESIGN INFORMATION

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MIN. VIA SIZE: 18 MIL

MINIMUM ANNIELING RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

FR-408  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  40 MIL (1.0mm) +/-10%  OTHER \_\_\_\_\_

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2

OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2

OTHER +/- \_\_\_\_\_

DRILLING:

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

BOARD FINISH:

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_

SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_

MATTE  SEMI-GLOSS

SURFACE FINISH:  IMMERSION GOLD (ENIG)  ENEPIG

IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

ARRAY/PANEL:  CUT AND TRIM PER M1 BOARD OUTLINE

N.C. ROUTE  V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS ->  1  2  3

RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION:  YES

BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER

6.1MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE

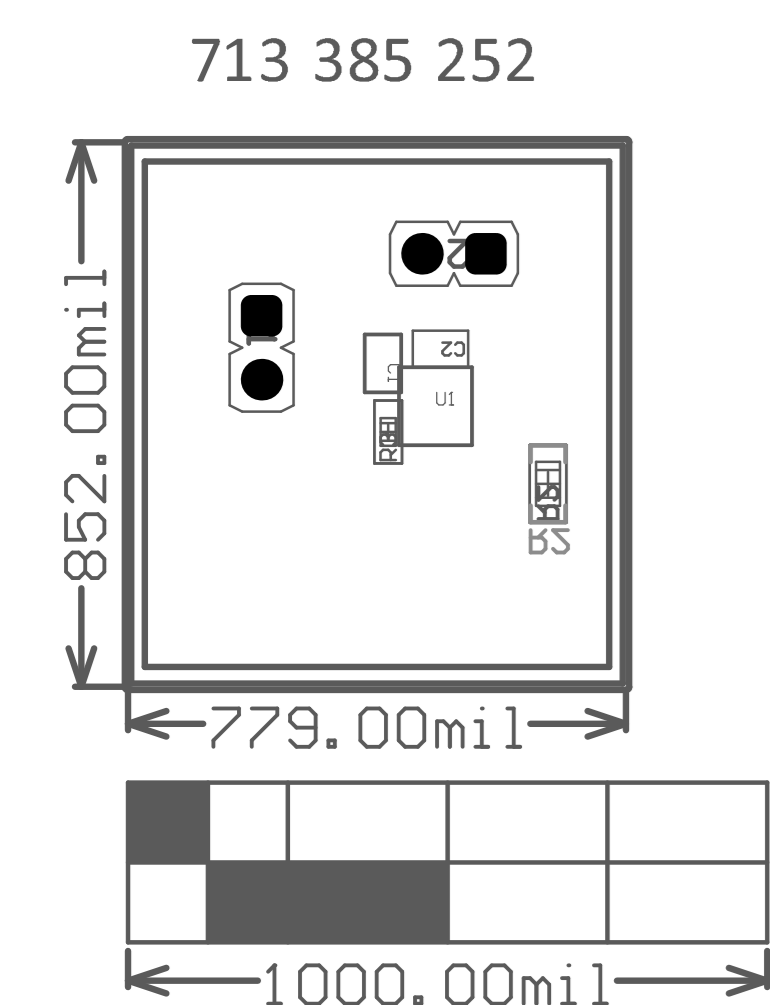
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

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ENGINEER: Tahar Allag

LAYOUT BY: Fred Illguth

SCALE: 1.00

ALTIUM DESIGNER VERSION: 22.7.1.60

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PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION:  YES

BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER

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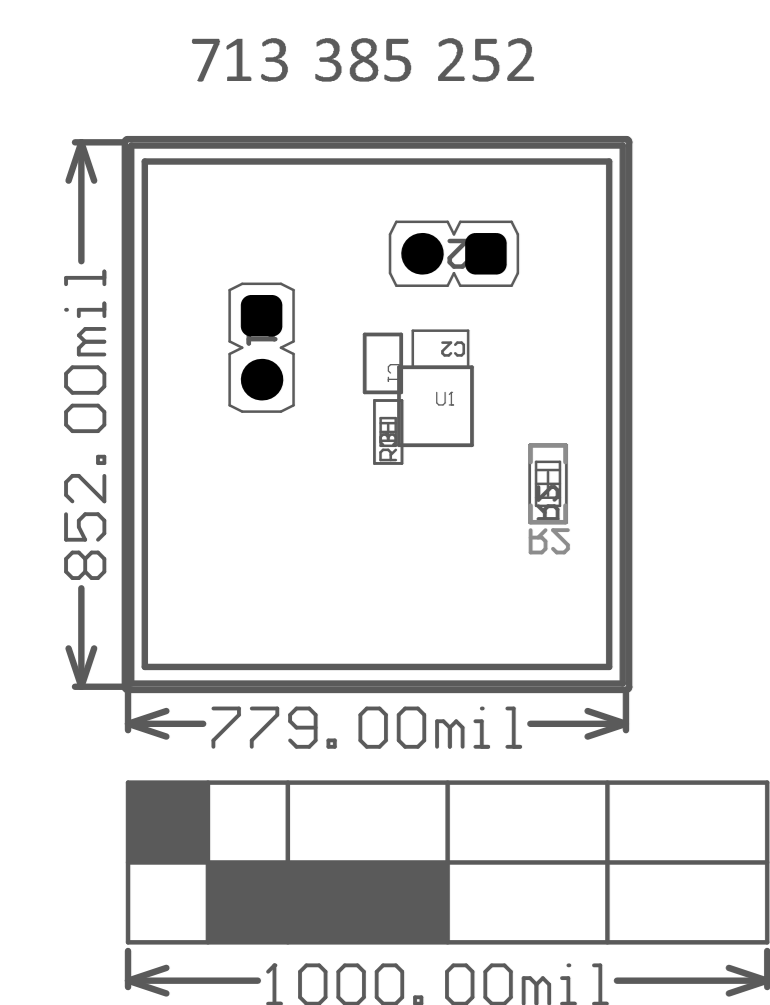
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LAYOUT BY: Fred Illguth

SCALE: 1.00

ALTIUM DESIGNER VERSION: 22.7.1.60

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BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
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DRILLING:

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PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

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ADDITIONAL REQUIREMENTS:

MICROSECTION:  YES

BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER

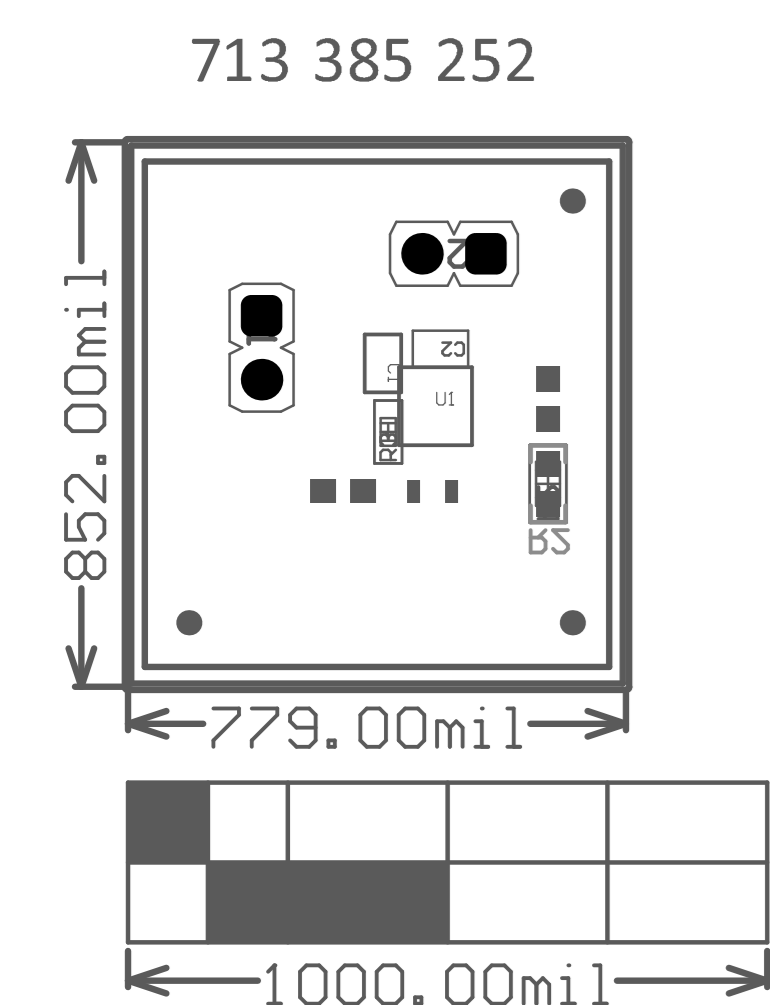
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ASSEMBLY VARIANT: 001

713 385 252	BOARD	20070A05055	DATE:	A	SUN 3000: N00T08 M00E: 1.00.00.00
LAYER NAME =	FR-4 High Tg	TID #:	.TIDDIT.	#	DIT
PLTNAME =	Layer Assembly	DATE:	8/27/2007	TIME:	11:22:19

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ENGINEER:	Tahar Allag	LAYOUT BY:	Fred Illguth
SCALE:	1.00	ALTIUM DESIGNER VERSION:	22.7.1.60

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