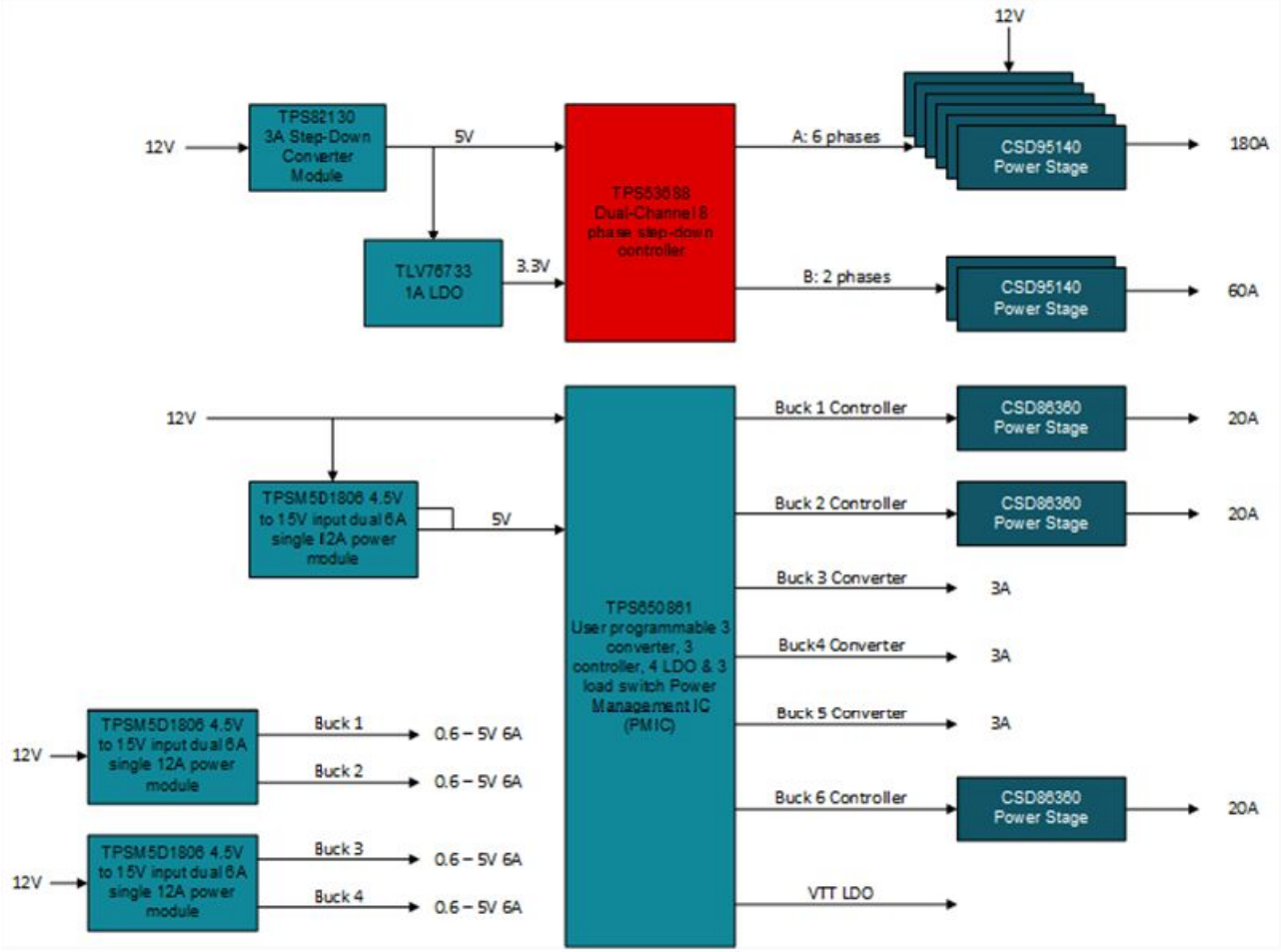
Block Diagram



Orderable:	Designed for: Public Release	Mod. Date: 8/31/2022
TID #: TIDA-010241	Project Title: Flexible FPGA Power	
Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 1 of 17
Drawn By:	File: Block Diagram.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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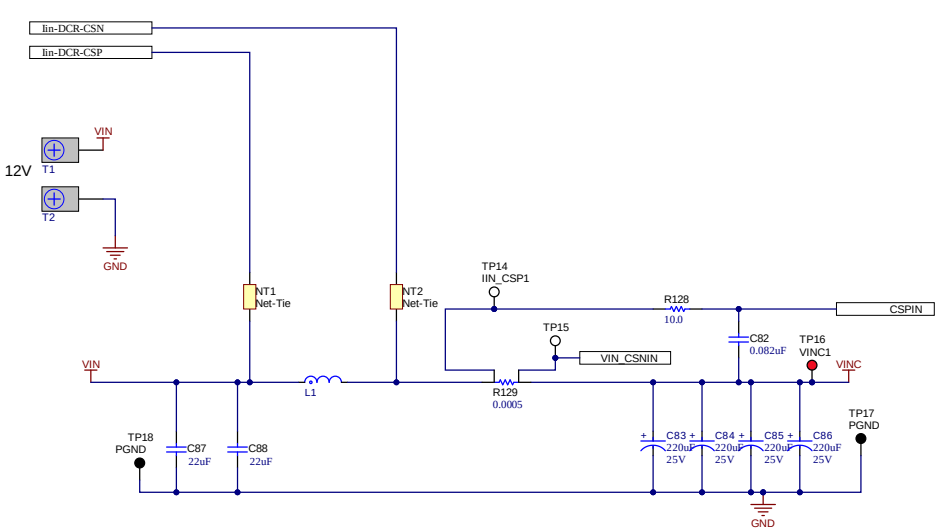
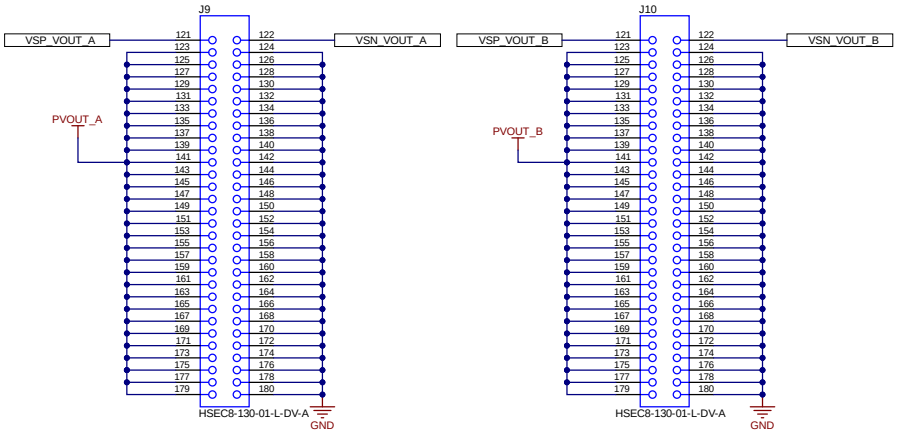
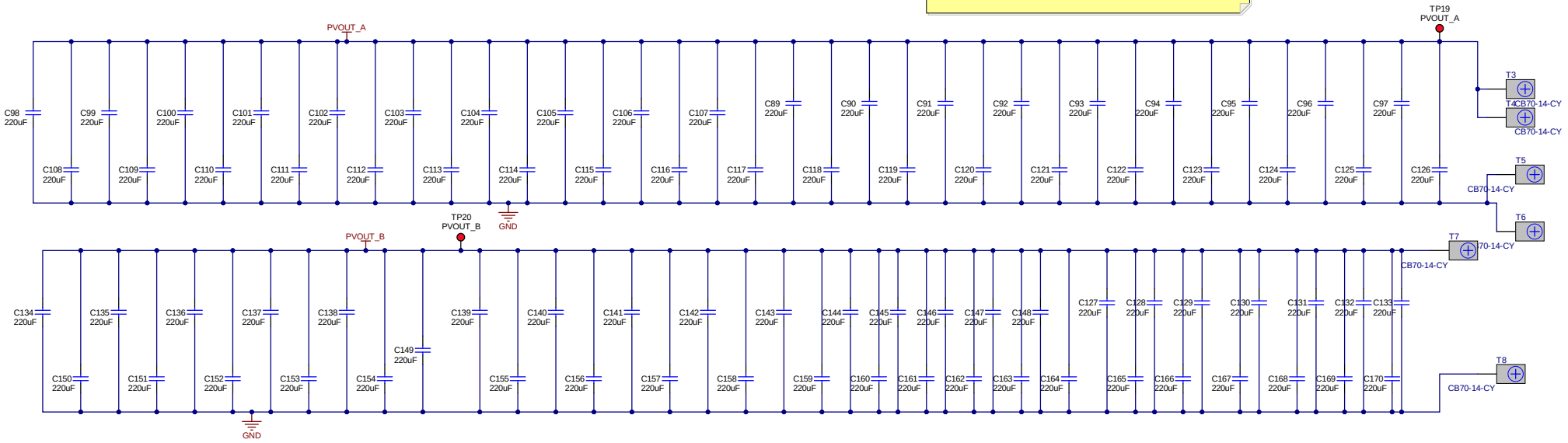




Theses headers and capacitors are not necssary. They were used for the load slammer circuit. The ony thing that is needed on this page is the input filter stage.

VOUTA: 0.88V

IOUTA: 320Adc Max. for 8ph



VOUTB: 1V IOUTB: 160Adc Max. for 4ph

Orderable:	Designed for: Public Release	Mod. Date: 1/26/2022
TID #: TIDA-010241	Project Title: Flexible FPGA Power	
Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 2 of 17
Drawn By:	File: EVRHC008_Filters.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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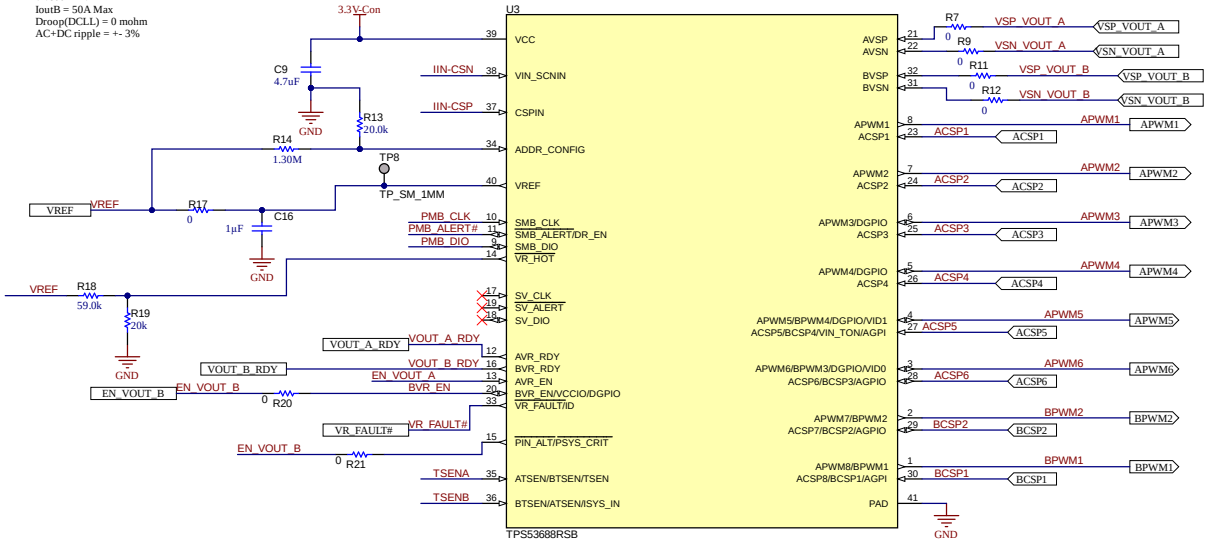
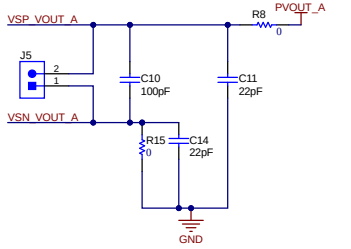
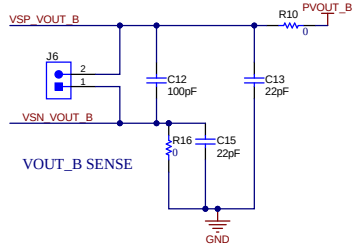
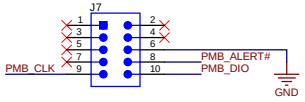
RAILA: VoutA=0.85V
Iout = 180A Max
Load step = 75-100
Droop(DCLL) = 0 mohm
AC+DC ripple = +- 3%
Boot voltgae = 0.85V
RAILA: VoutB=1V
IoutB = 50A Max
Droop(DCLL) = 0 mohm
AC+DC ripple = +- 3%

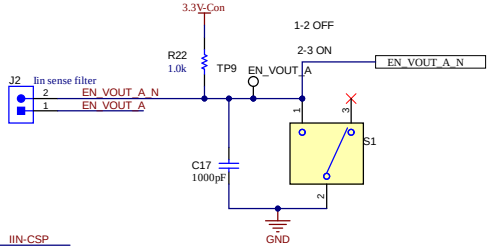


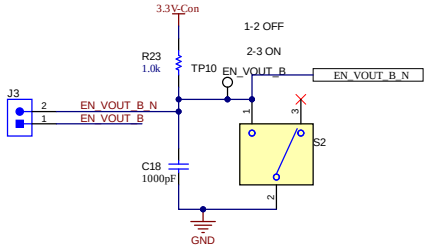




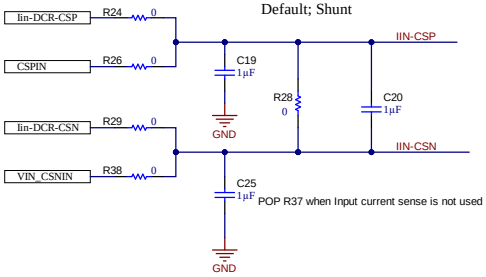


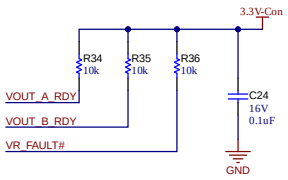
Only one current sense is needed. Either from the Inductor or from the Shunt Resistor.

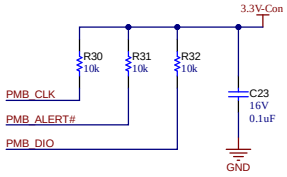


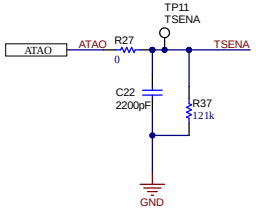


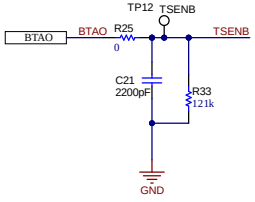
These are switches that are not need for enable. This can be driven by a digital pin.











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TID #: TIDA-010241	Project Title: Flexible FPGA Power	
Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 3 of 17
Drawn By:	File: EVRHC008_CONTROLLER_6X6.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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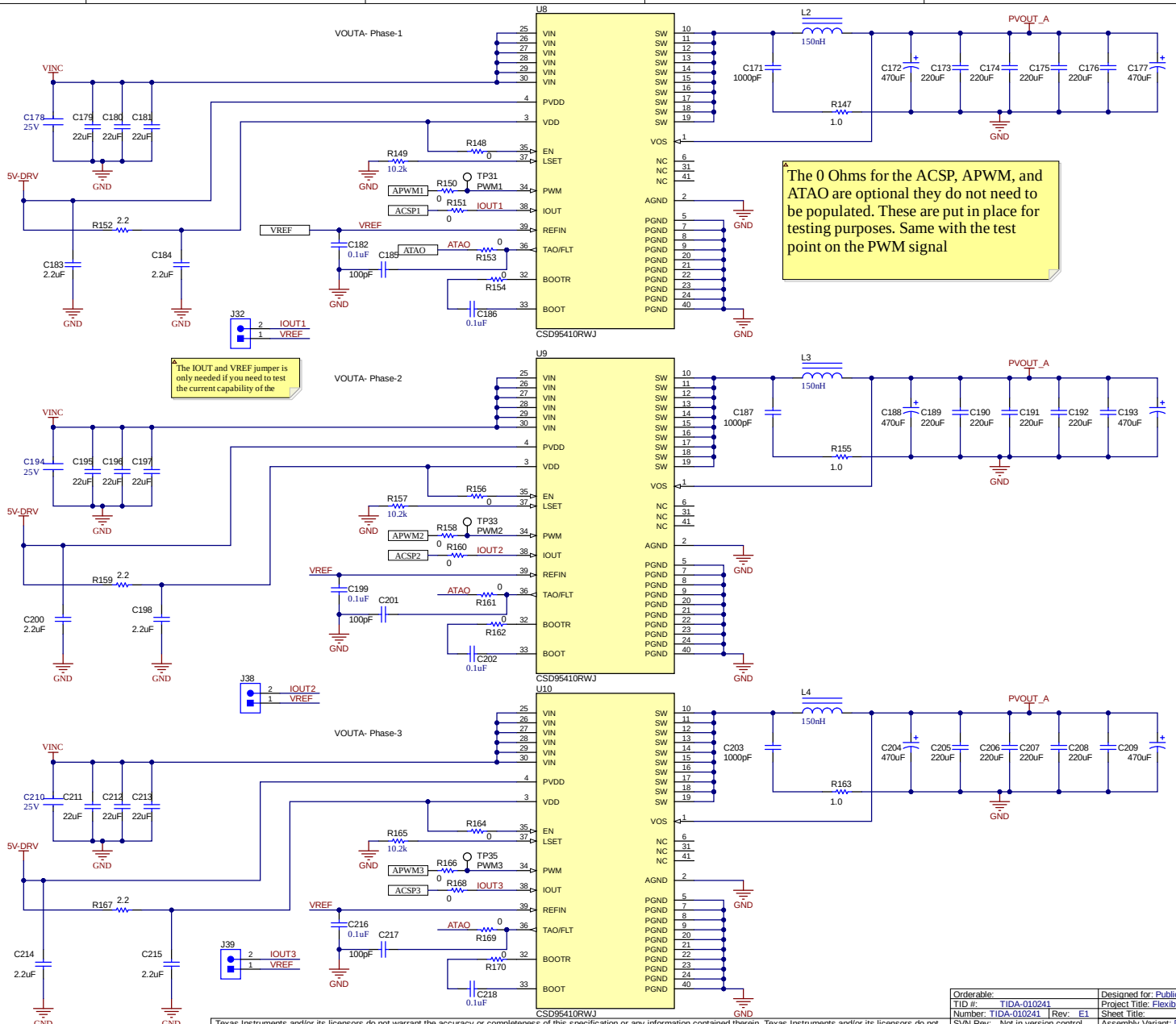

Orderable:	Designed for: Public Release	Mod. Date: 1/26/2022
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Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 4 of 17
Drawn By:	File: EVRHC008_VOUT_A_Phases 1-2-3.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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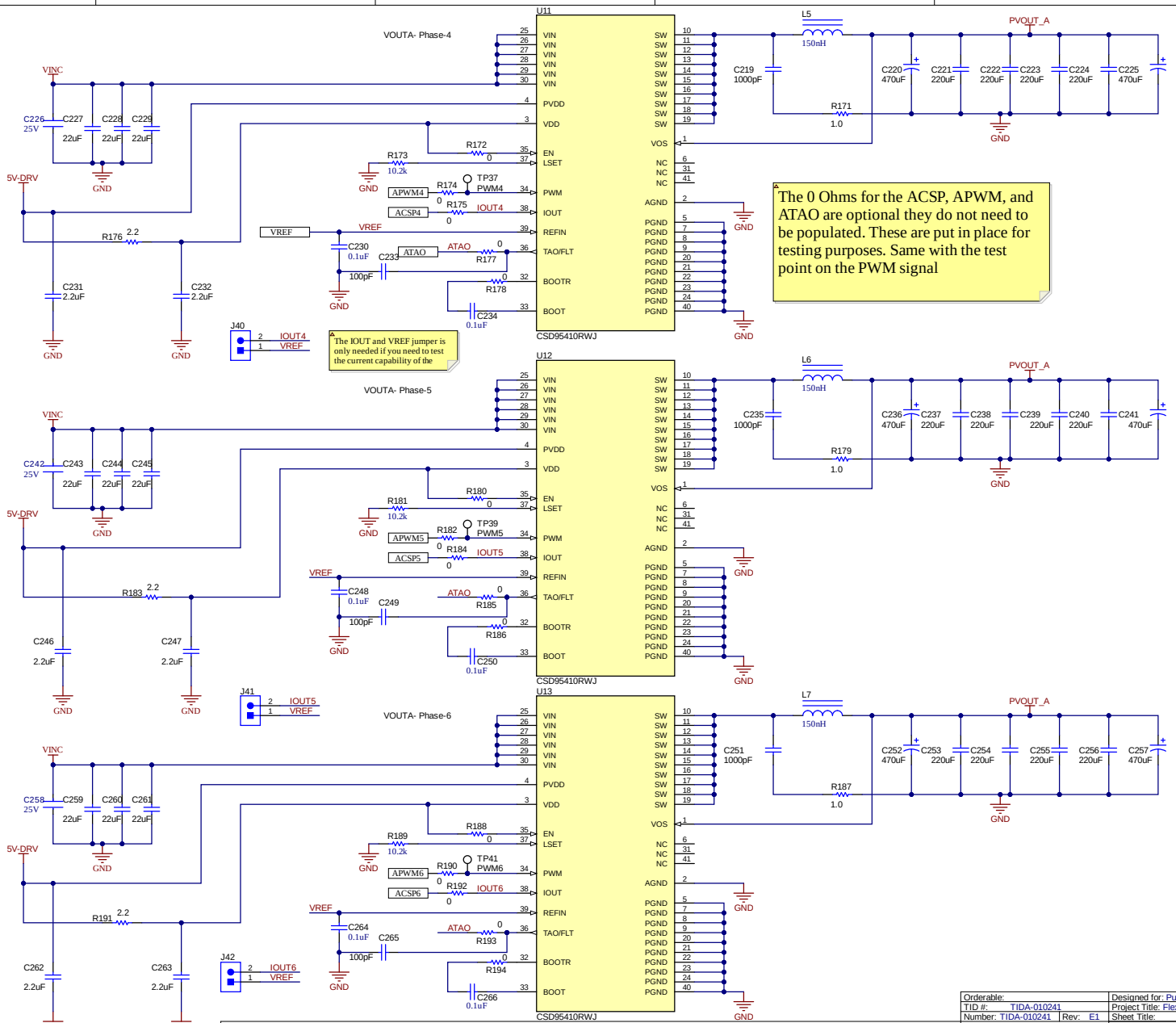

Orderable:	Designed for: Public Release	Mod. Date: 1/26/2022
TID #: TIDA-010241	Project Title: Flexible FPGA Power	
Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 5 of 17
Drawn By:	File: EVRHC008_VOUT_A_Phases 4-5-6.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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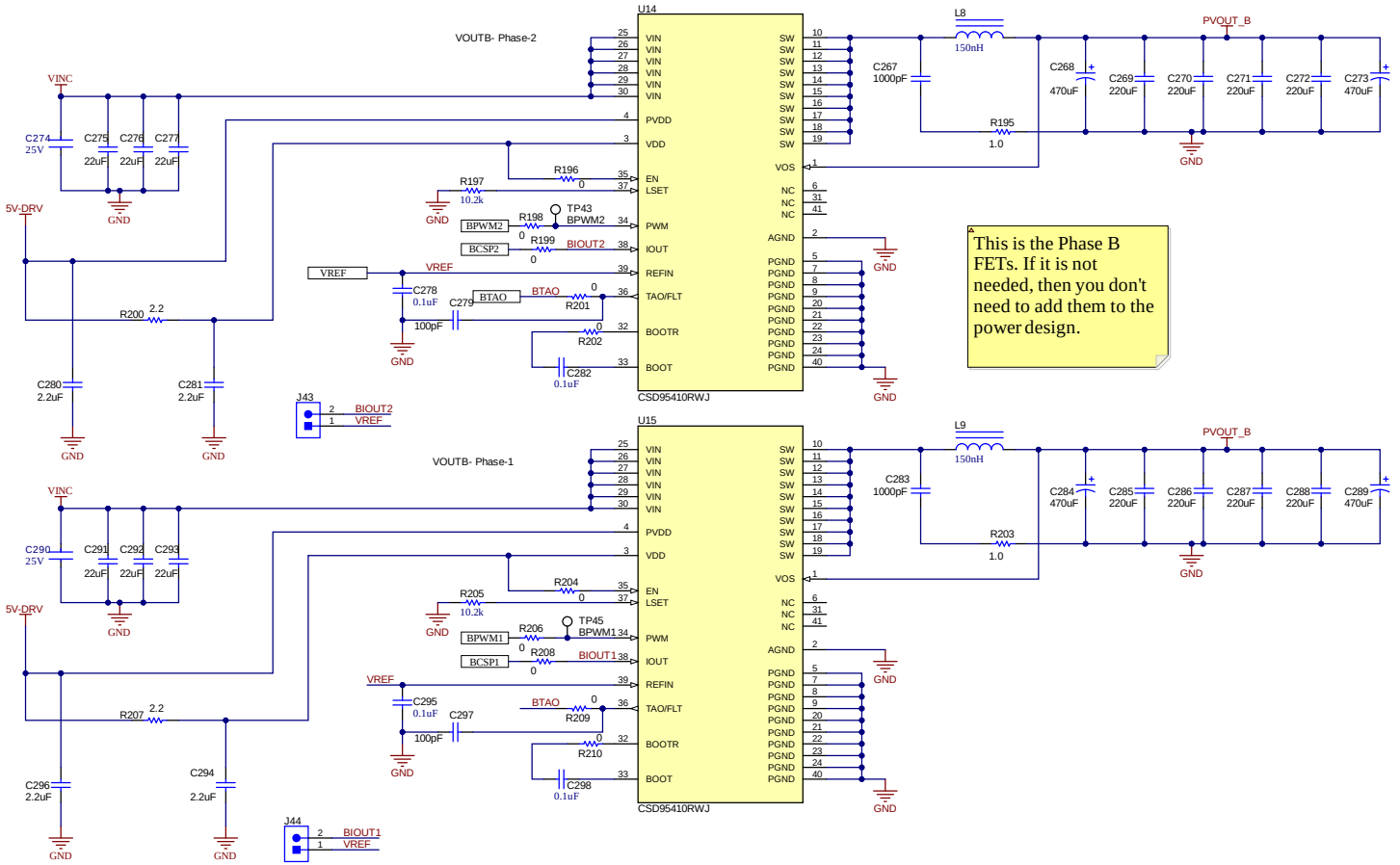

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Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 6 of 17
Drawn By:	File: EVRHC008_VOUT_B_Phases 1-2.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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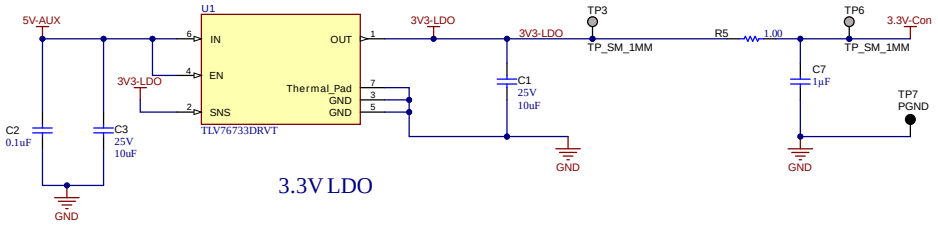
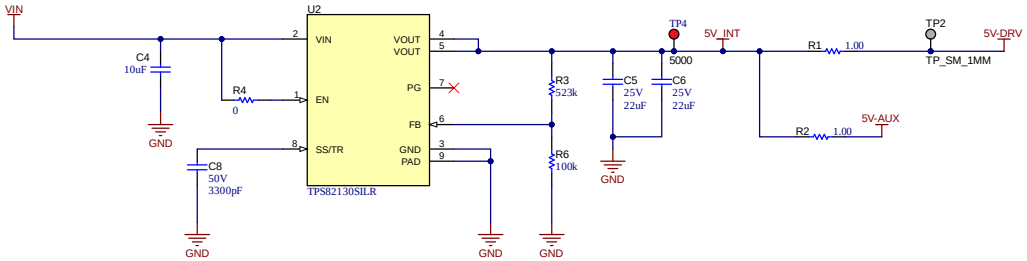


3.3V LDO



5V Module

Orderable:	Designed for: Public Release	Mod. Date: 1/26/2022
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Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 7 of 17
Drawn By:	File: EVRHC008_Aux Power.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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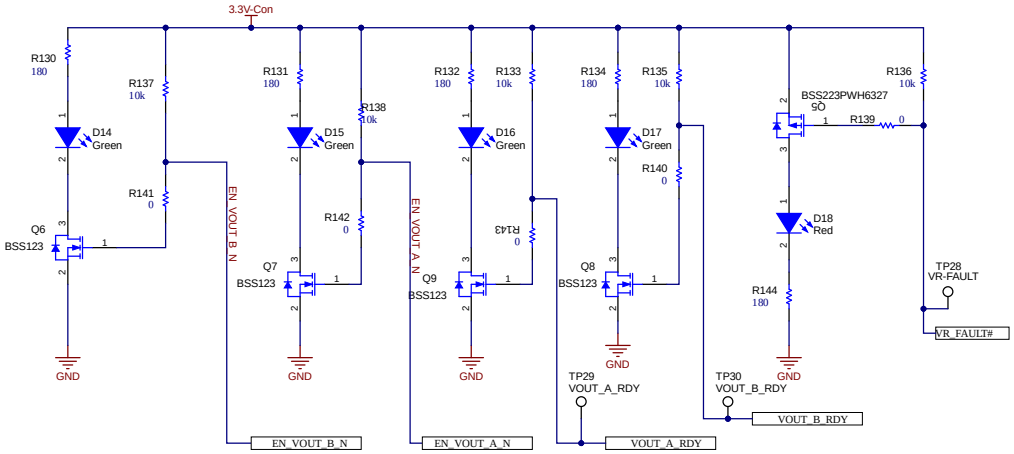
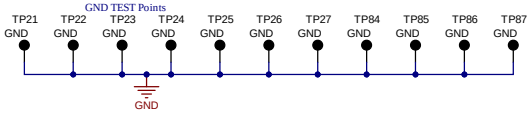
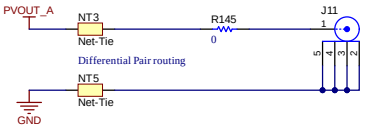
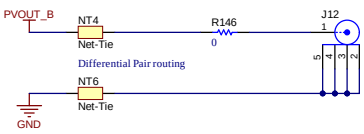






Everything on this page is not needed only if you want indicators for enable and PGOOD sginals.



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TID #: TIDA-010241	Project Title: Flexible FPGA Power	
Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 8 of 17
Drawn By:	File: EVRHC008_HelperCkts and Indicators.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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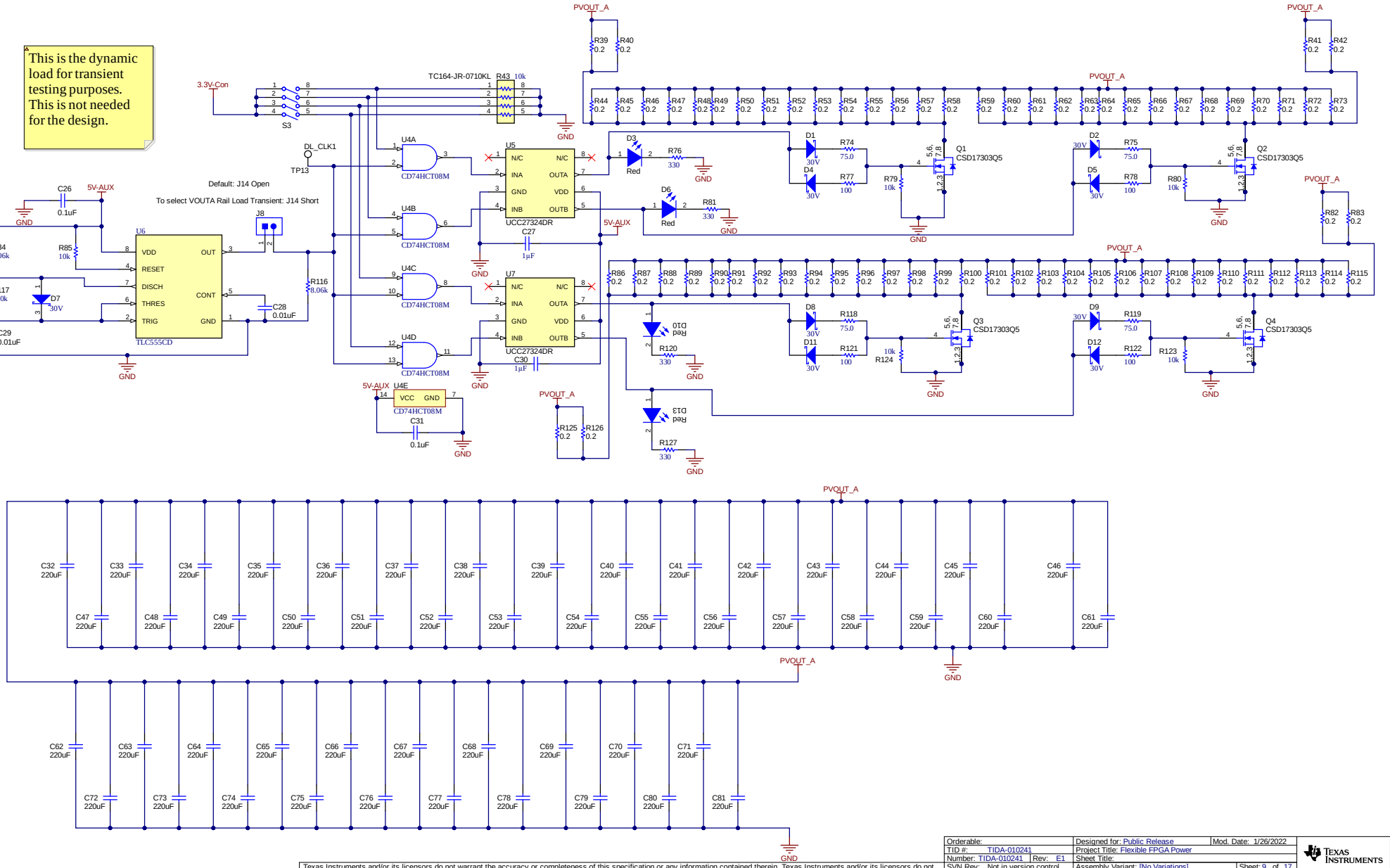
This is the dynamic load for transient testing purposes. This is not needed for the design.



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TID #: TIDA-010241	Project Title: Flexible FPGA Power	
Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 9 of 17
Drawn By:	File: EVRHC008_ Dynamic Load.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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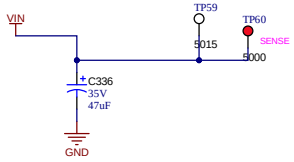
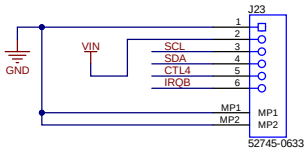
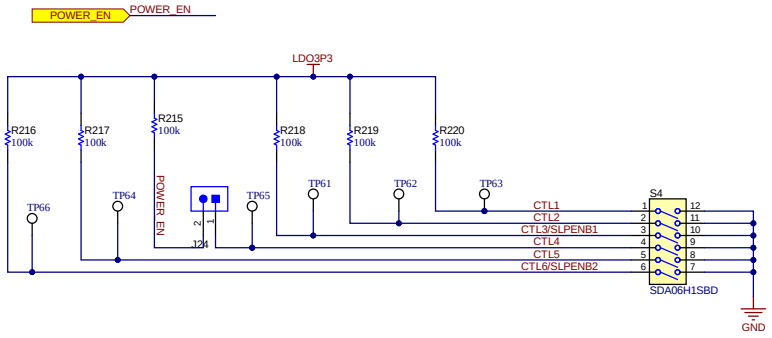
System Input

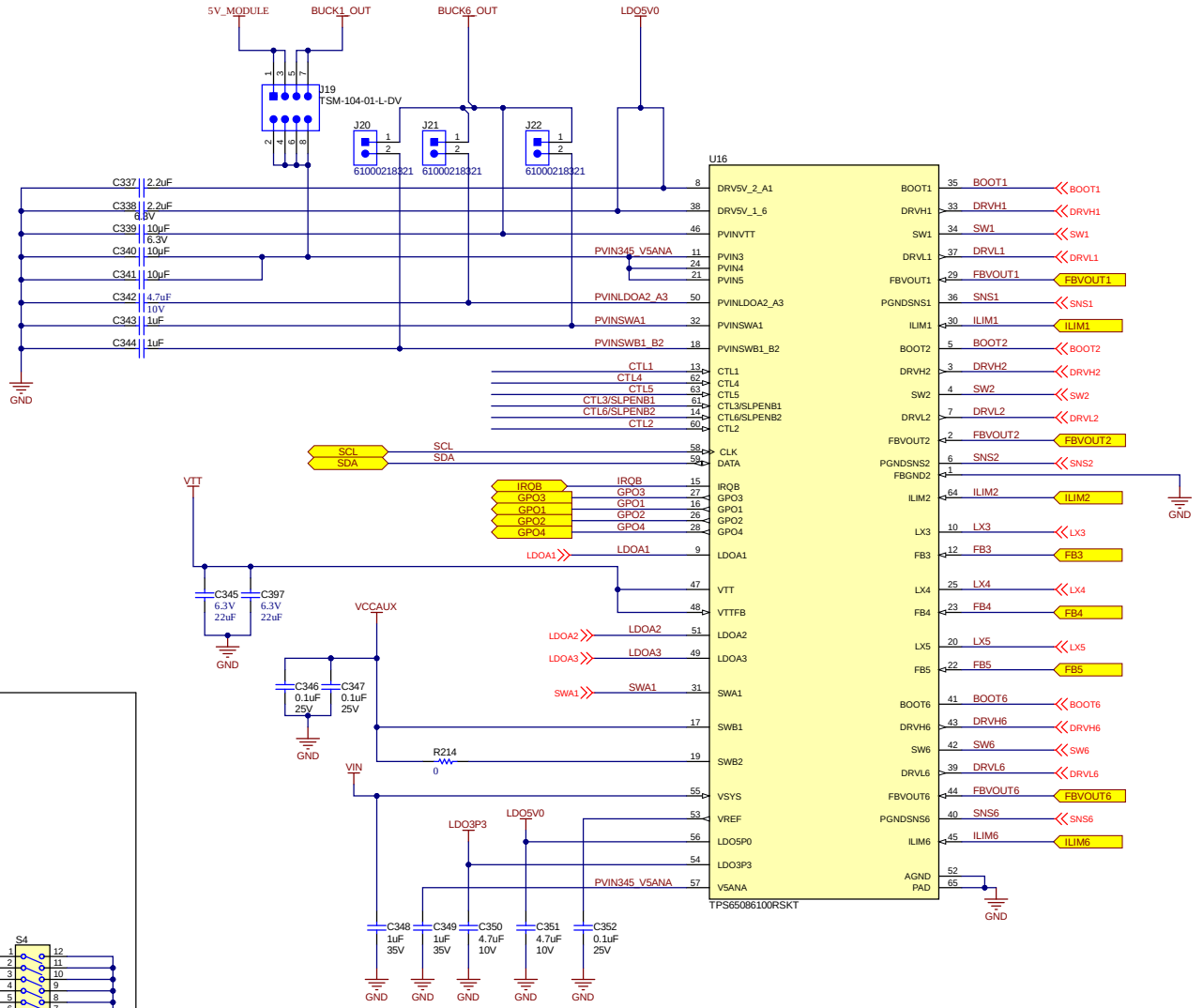


Programming Ribbon Connector



CTL Inputs





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Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 10 of 17
Drawn By:	File: TPS650841_Project_TPS65086.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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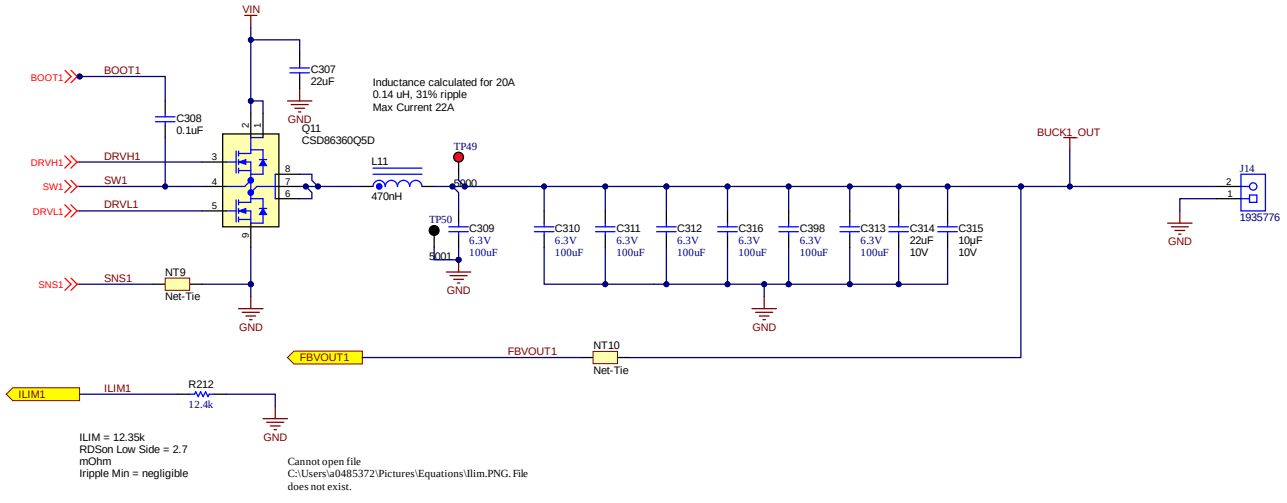
BUCK1



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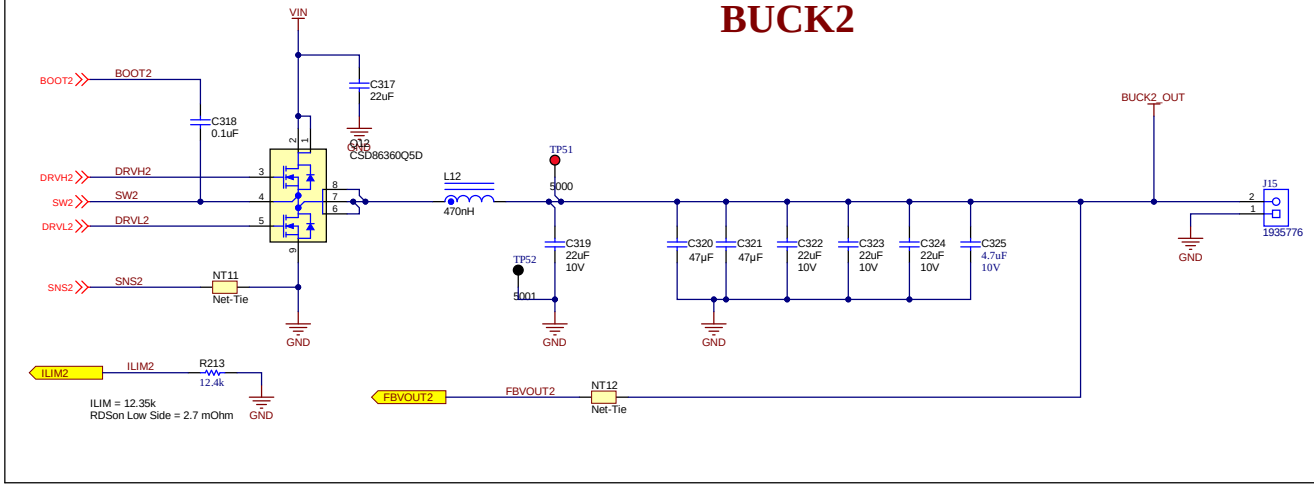

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Number: TIDA-010241 Rev: E1	Sheet Title:	
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Drawn By:	File: TPS6508641_Project_Buck12.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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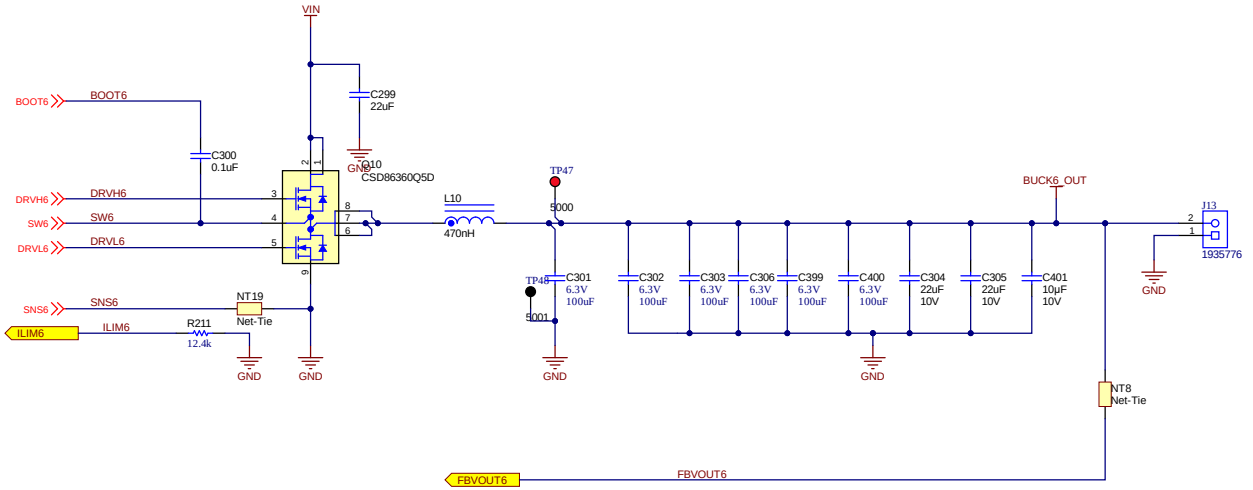
BUCK6



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Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 12 of 17
Drawn By:	File: TPS6508641_Project_Buck6.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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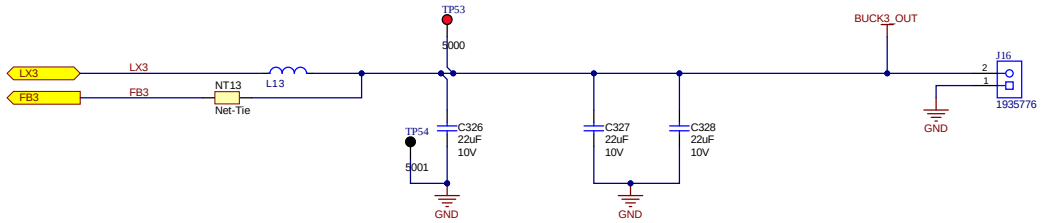
BUCK3



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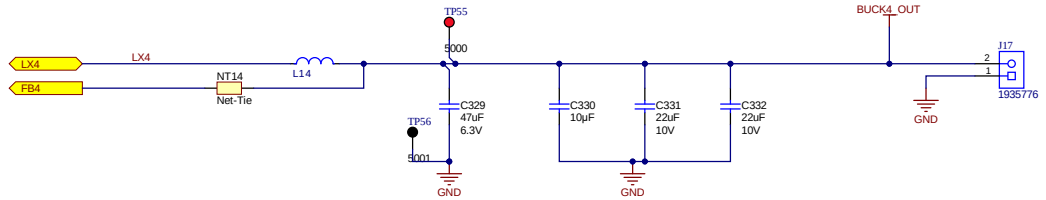
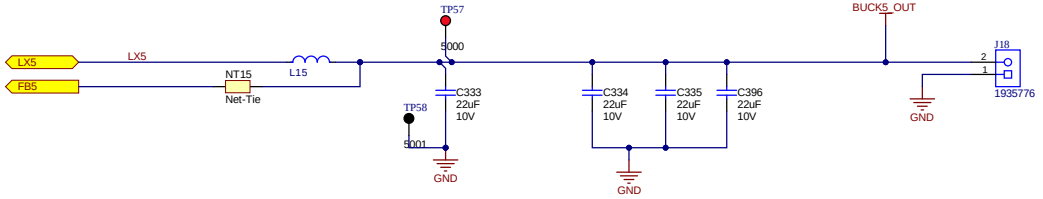


BUCK5



Orderable:	Designed for: Public Release	Mod. Date: 9/8/2021
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Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 13 of 17
Drawn By:	File: TPS6508641_Project_Buck345.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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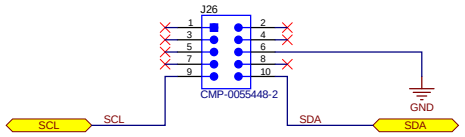
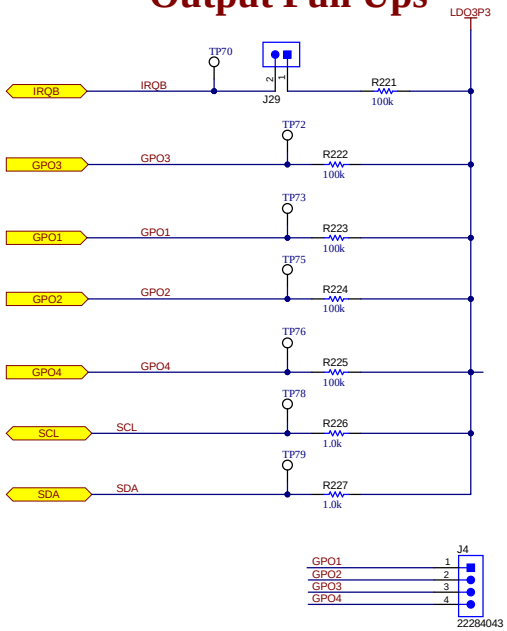
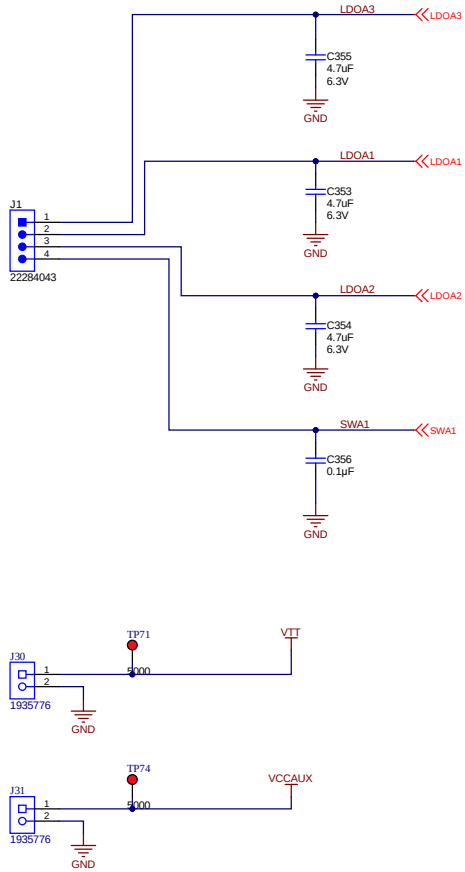
USB2ANY



Output Pull Ups



LDO/SW Out



Orderable:	Designed for: Public Release	Mod. Date: 9/8/2021
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Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 14 of 17
Drawn By:	File: TPS6508641_Support_Devices.SchDoc	Size: B
Engineer: Albert Lo	Contact: http://www.ti.com/support	

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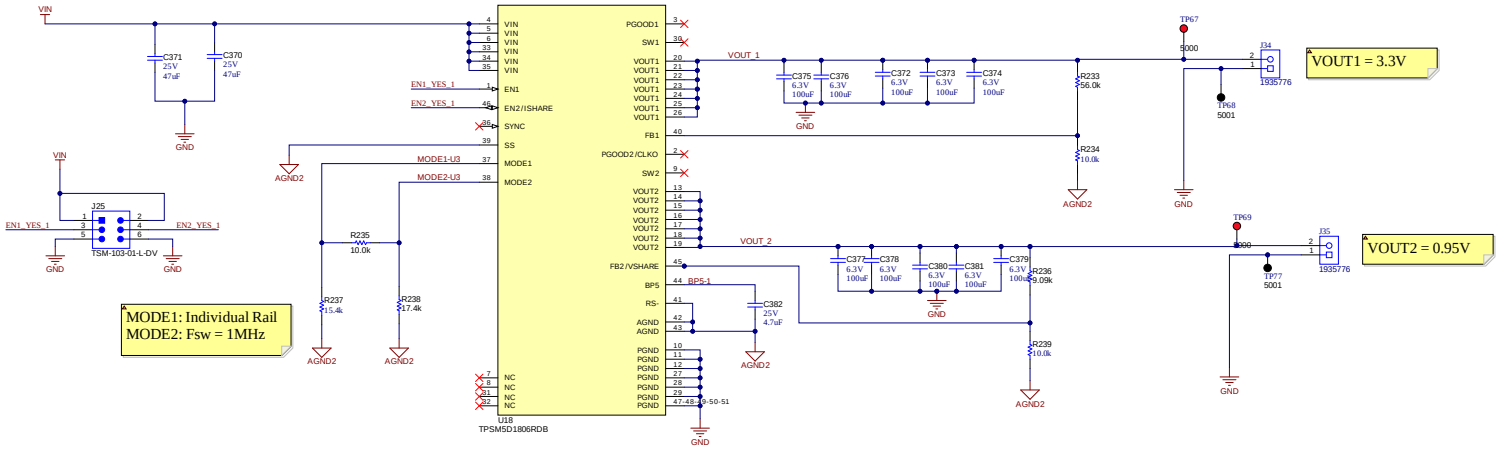
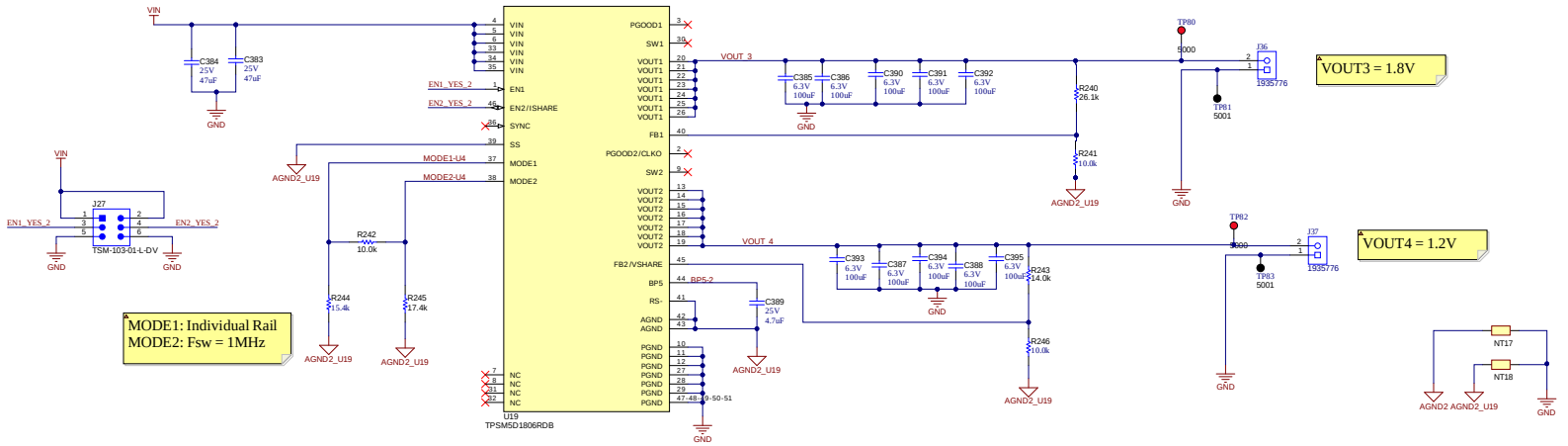
TPS5MD1806: 3.3V and 0.9V output



TPS5MD1806: 1.8V and 1.2V output



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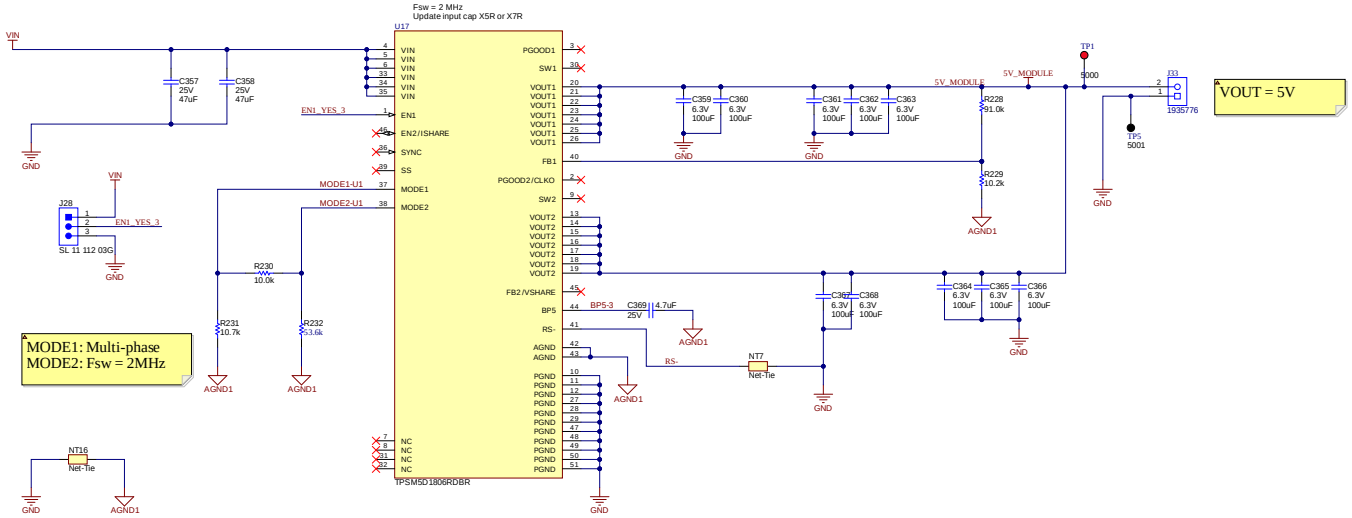
Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 15 of 17
Drawn By:	File: TPSM5D1806IND.SchDoc	Size: A2
Engineer: Albert Lo	Contact: http://www.ti.com/support	http://www.ti.com

TPS5MD1806: Multiphase 5V Output



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Number: TIDA-010241 Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 16 of 17
Drawn By:	File: TPSM5D1806 Multi Phase.SchDoc	Size: A2
Engineer: Albert Lo	Contact: http://www.ti.com/support	http://www.ti.com

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LOGO
Texas Instruments


CE Mark

PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo

H1
NY PMS 440 0025 PH

H3
NY PMS 440 0025 PH

H5
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SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 17 of 17
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