

Layout Notes:

- * Label all the Nets & Connections on the Silkscreen
- * Place all input and output capacitors as close to the device as possible on the top and bottom side of the board

Layer Stackup:

Top: PWR & Device Signals

L2: GND

L3: +5V_USB & BATT+

L4: Kelvin & measurement signals

L5: GND


L6: Kelvin & measurement signals

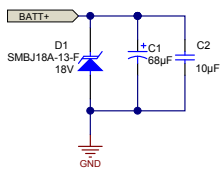
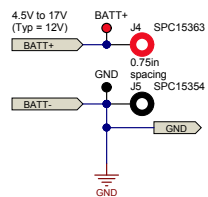
L7: GND

Bottom: PWR & Device Signals

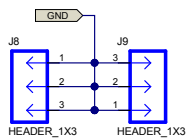
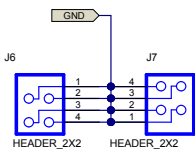
- * Place all the Power resistors, TPS22929D and current limiting resistor for LED's on the bottom side of the board
- * Place LEDs and Test Points on the top side of the board around the board
- * Place Banan connectors on the Top center of the board and USB2ANY connector on the left bottom center of the board
- * Compact the design on the top side with active and passive components (excluding LEDs, headers, Test Points & Connectors) such that it will fit in 3inx2in size
- * Make the total board size, including connectors, headers, test points etc as 4inx3in
- * Make the Power & Force lines as thick copper pour with multiple vias and sense lines as thin traces
- * Check each device foot print matches with it's Datasheet to ensure that pinout is correct
- * Match trace resistance on VIN & VOUT of TPS22993 for better RON
- * Place Rectangle box (Ex: 3inx2in) on the silk screen
- * Place box on silk screen around each DC-DC and TPS22993 including input and output caps
- * Place Banan Connectors at standard 0.75in spacing at Top center of the board
- * Place USB2ANY connector at the Left bottom center of the board

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SVN Rev: Not in version control	Assembly Variant: Variant name not interpreted	Project Title: TI Design-Capistrano	Sheet Title:
Drawn By: Sathish Vallamkonda	File: SkyLake_LayoutNotes_SchDoc	Sheet: 1 of 9	Size: B
Engineer: Sathish Vallamkonda	Contact: http://www.ti.com/support	 TEXAS INSTRUMENTS http://www.ti.com © Texas Instruments 2014	



Place these GND TPs on the top corners of the board



Place these GND TPs on the bottom corners of the board



PCB Number: TIDA-00194
PCB Rev: E2

PCB LOGO
Texas Instruments



Z21

Label Assembly Note

This Assembly Note is for PCB labels only

Z22

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

Z23

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Z24

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2., unless otherwise specified.

Z25

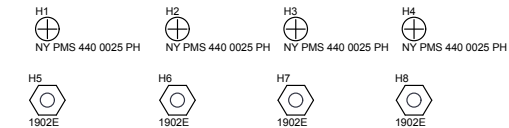
Assembly Note

Install TPS2294R1W at the locations U1&U2.

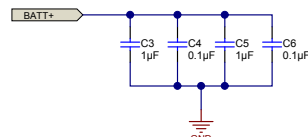
Z26

Assembly Note

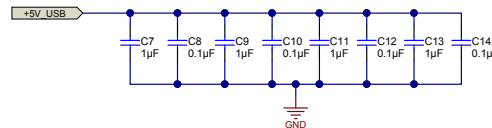
Install TPS2293R1W at the locations U3-U7.



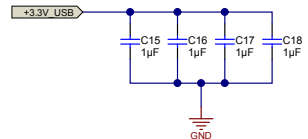
De-coupling Caps:



Layout Note: Place these caps at the border of 3inx2in rectangle



Layout Note: Place these combination of caps at 4 corners of the board



Layout Note: Place these caps at 4 corners of the board

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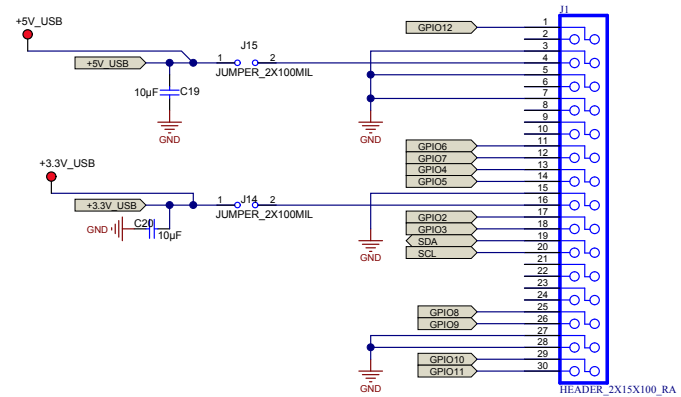
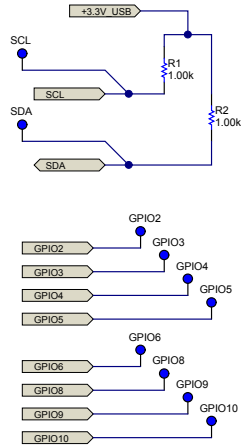
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Engineer: Sathish Vallamkonda	Contact: http://www.ti.com/support	Size: B	© Texas Instruments 2014



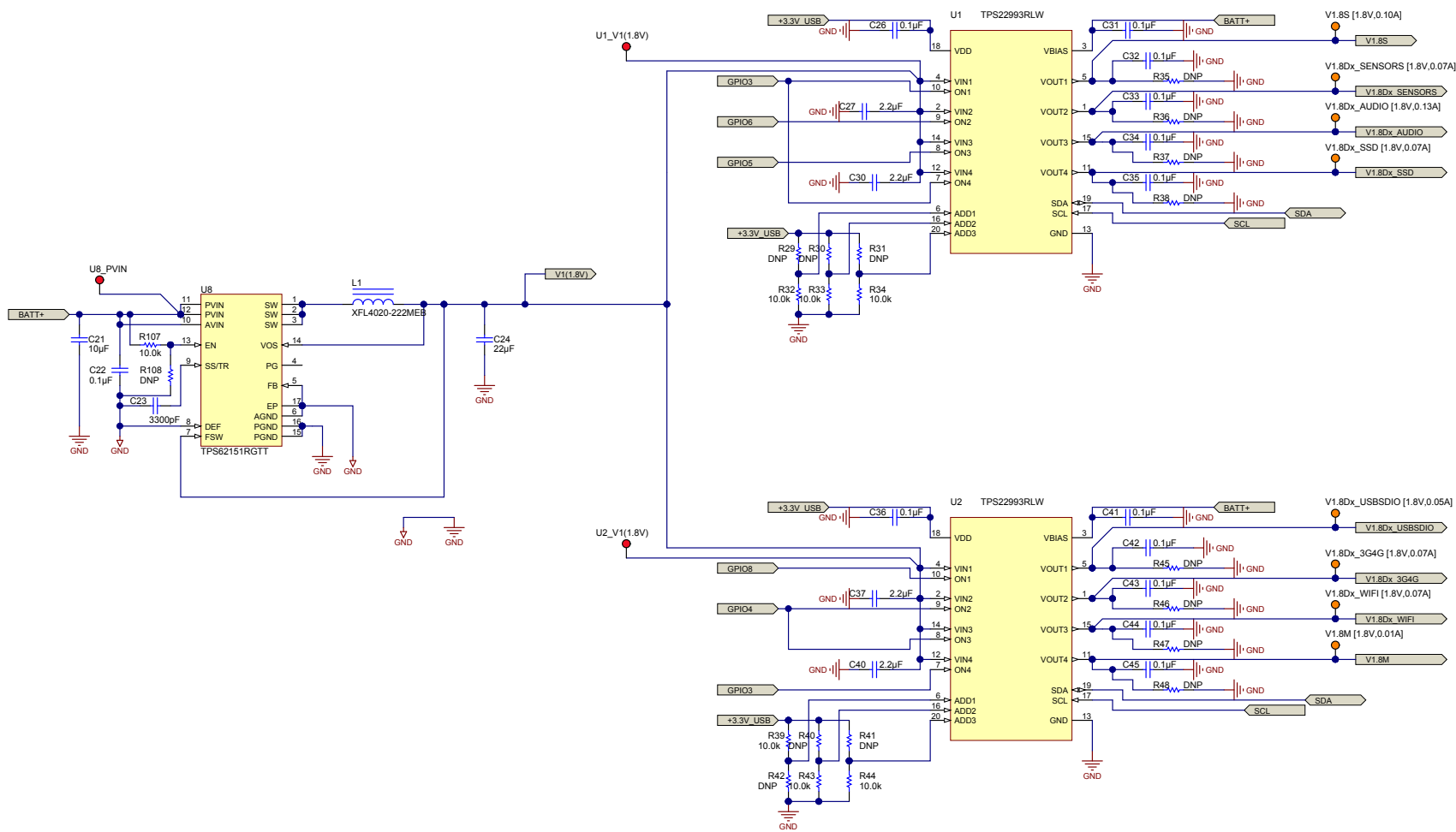
USB2ANY EXTERNAL CONNECTIONS

Important Layout Note: The USB2ANY is a right angle connector, need to make sure the connections are oriented correctly so the board will mate correctly with the USB2ANY
 Important Layout Note: Vertical and Horizontal spacing is exactly the same as the USB2ANY board. We can refer to the USB2ANY board layout to insure this is correct.

Important Layout Note: Place USB2ANY connector at the bottom of the board such that it connects in only one direction



TPS22993 U1 & U2 with TPS62151 U8 CONNECTIONS

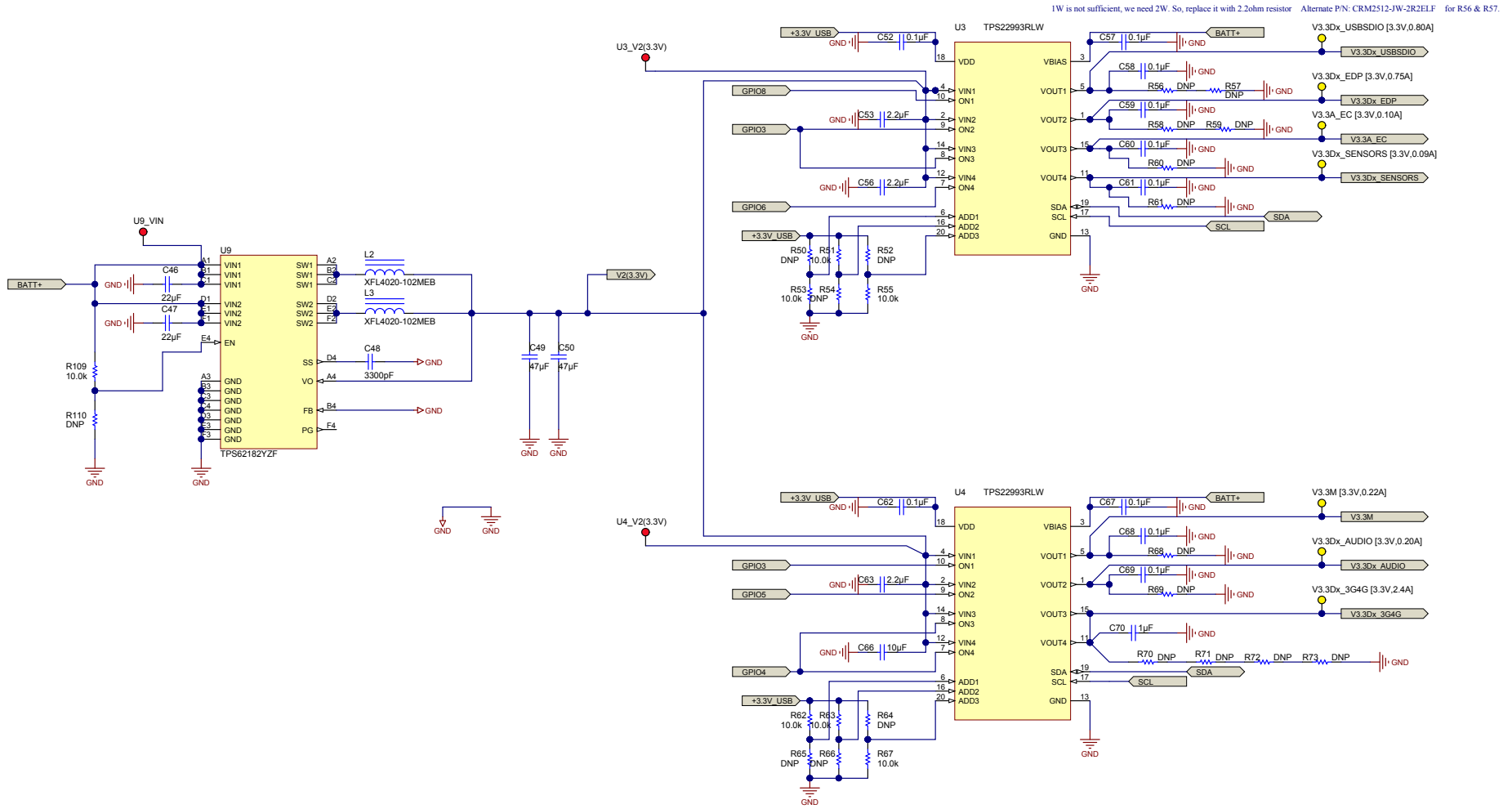


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Engineer: Sathish Vallamkonda	Contact: http://www.ti.com/support	Sheet 4 of 9	Size: B

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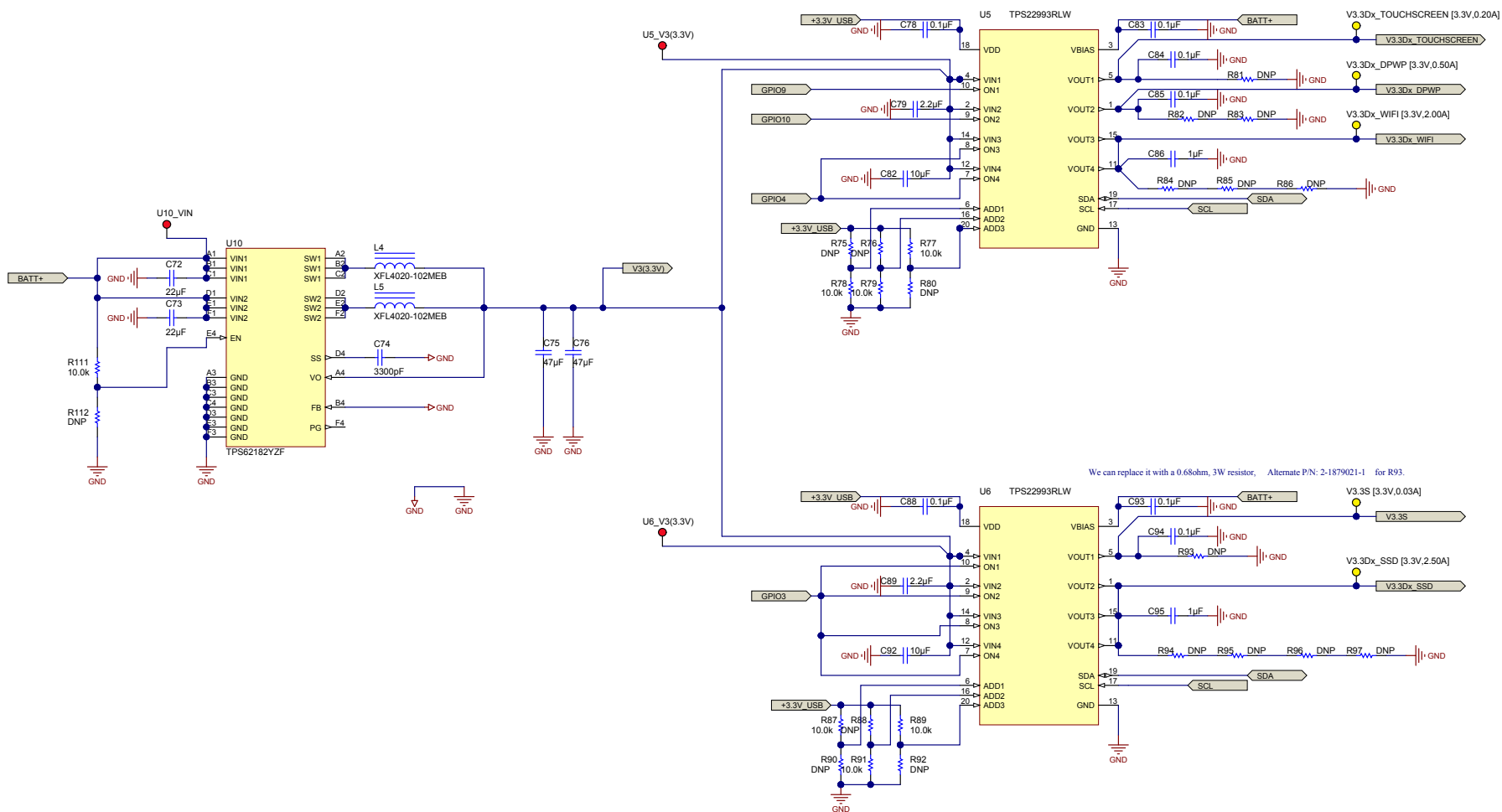
TPS22993 U3 & U4 with TPS62182 U9 CONNECTIONS



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Drawn By: Sathish Vallamkonda	File: SkyLake_TPS22993_U3_U4_SchDoc	Sheet 5 of 9	Size: B
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TPS22993 U5 & U6 with TPS62182 U10 CONNECTIONS

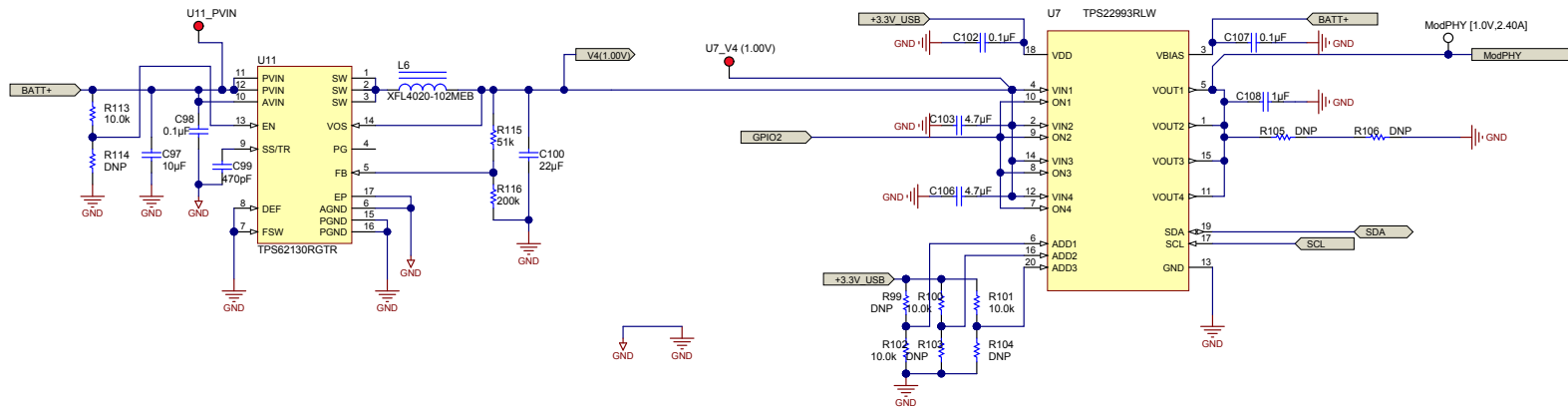


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Drawn By: Sathish Vallamkonda	File: Skylake_TPS22993_U5_U6.SchDoc	Size: B	
Engineer: Sathish Vallamkonda	Contact: http://www.ti.com/support	http://www.ti.com	

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TPS22993 U7 with TPS62130 U11 CONNECTIONS



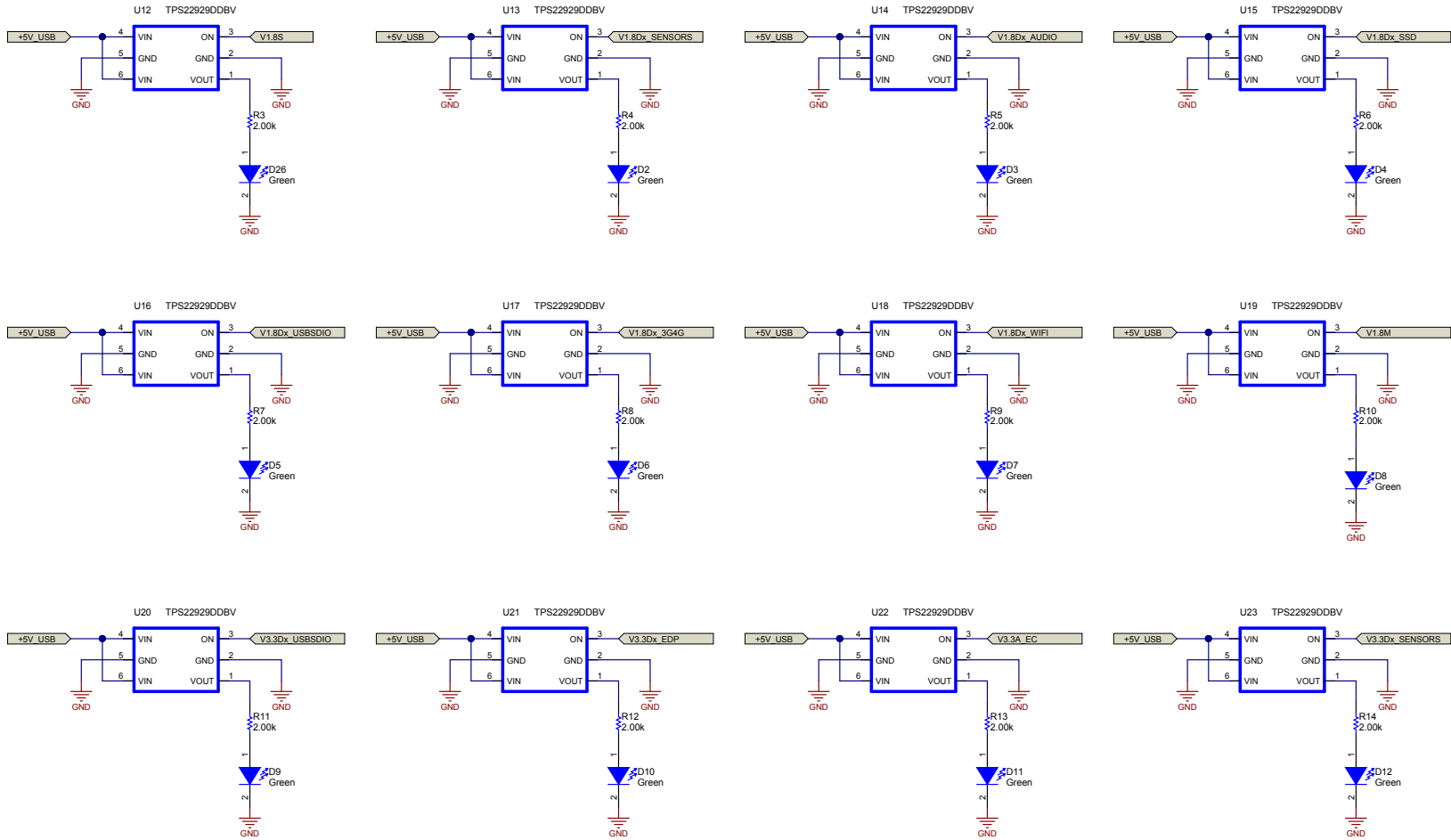
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Drawn By: Sathish Vallamkonda	File: SkyLake TPS22993_U7_SchDoc		Sheet: 7 of 9
Engineer: Sathish Vallamkonda	Contact: http://www.ti.com/support		Size: B



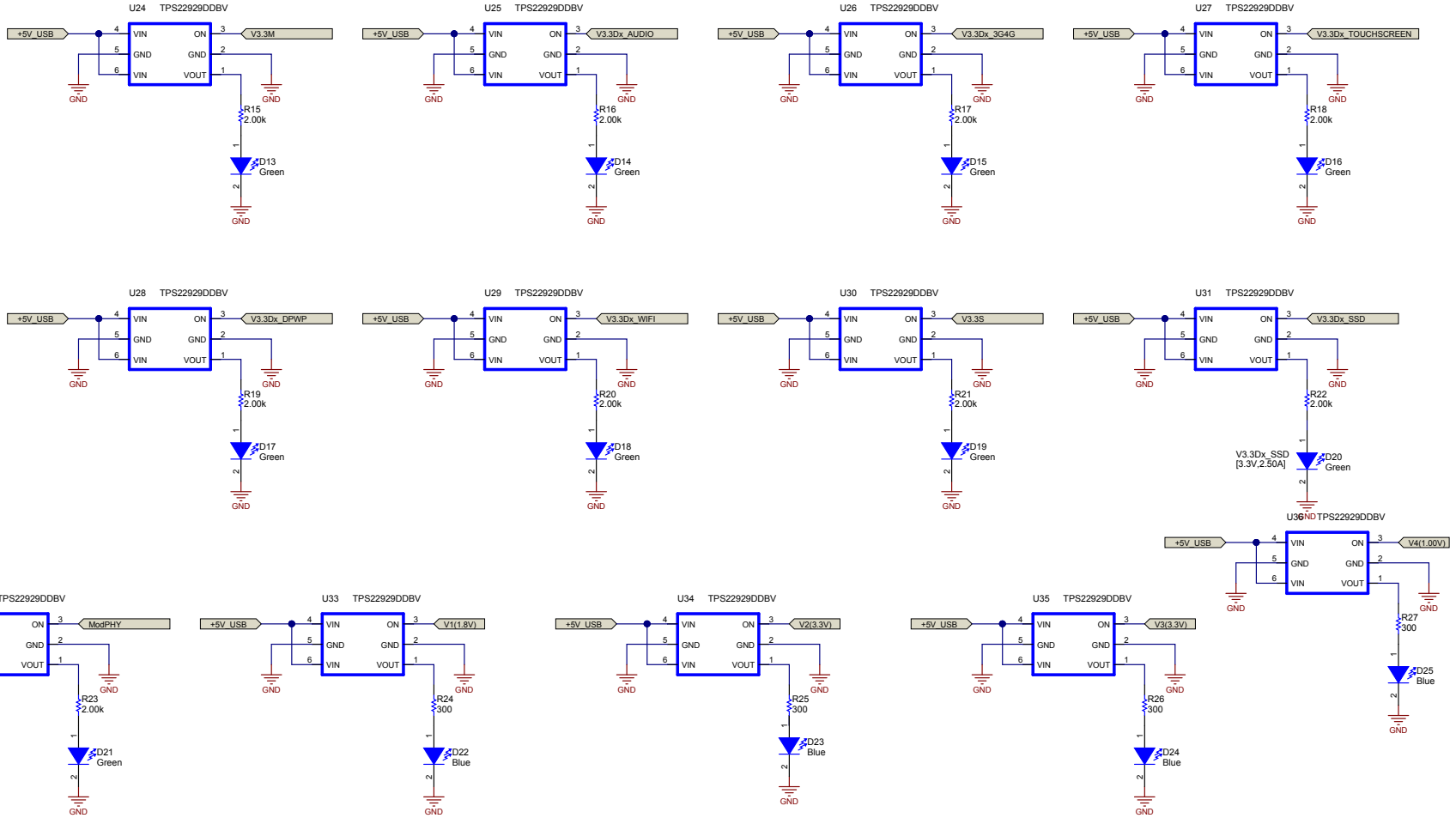
TPS22993 VOUTx pins LED INDICATORS

Layout Note: Place all TPS22929D parts & series current limiting resistors on the bottom side of the board



TPS22993 VOUTx pins and DC-DC Vout LED INDICATORS

Layout Note: Place all TPS22993 parts & series current limiting resistors on the bottom side of the board



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Drawn By: Sathish Vallamkonda	Contact: http://www.ti.com/support	Assembly Variant: Variant name not interpreted	Sheet 9 of 9
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