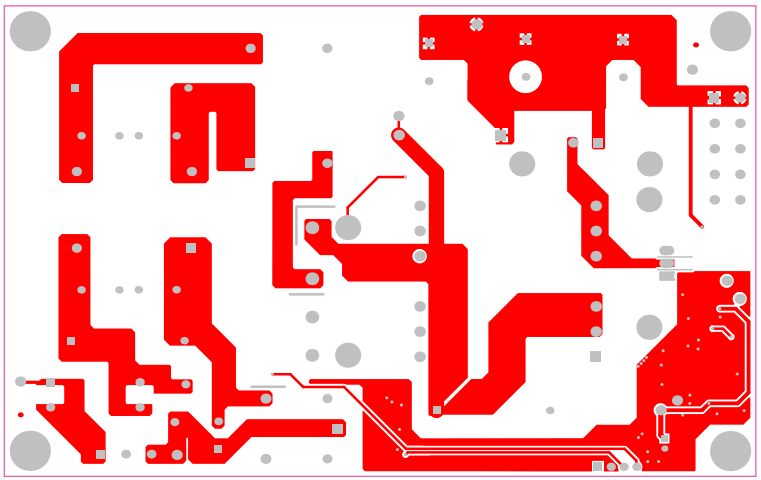
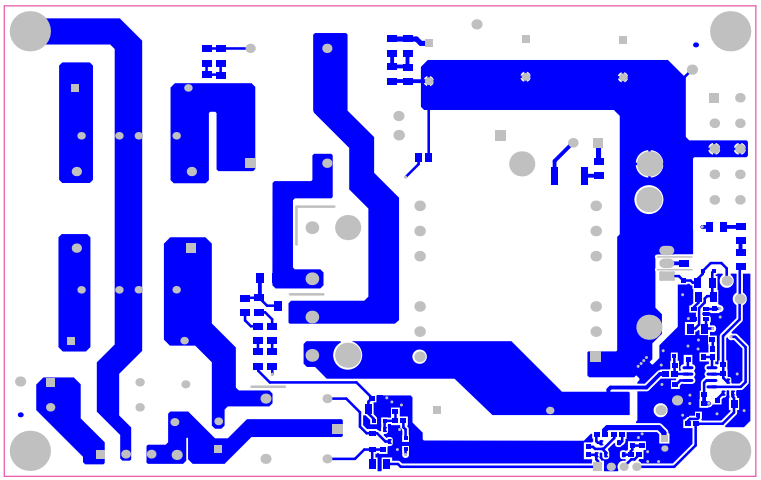
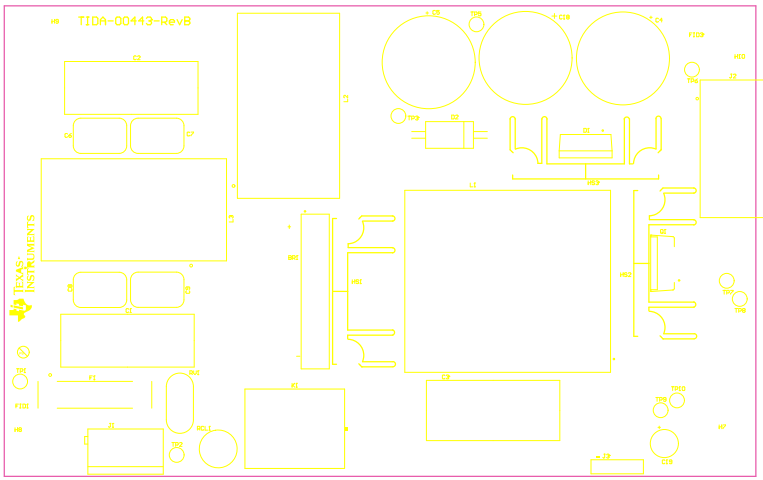


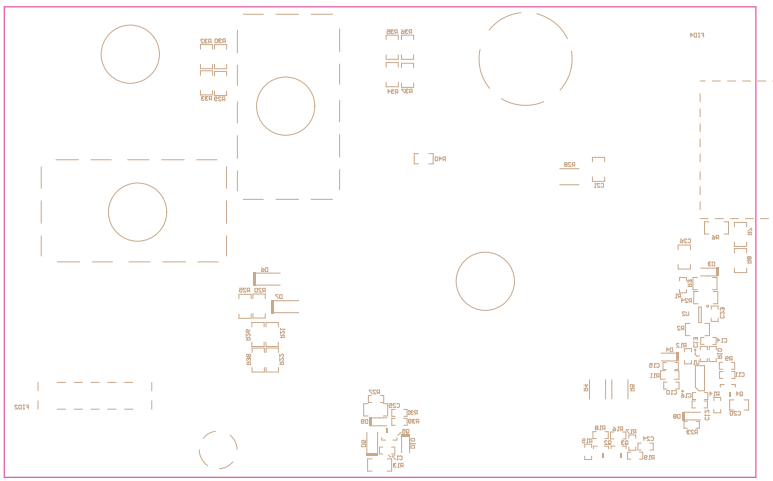
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00443	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Top Layer			
PLOT NAME = Top Layer	GENERATED : 6/1/2015 4:57:51 PM		TEXAS INSTRUMENTS



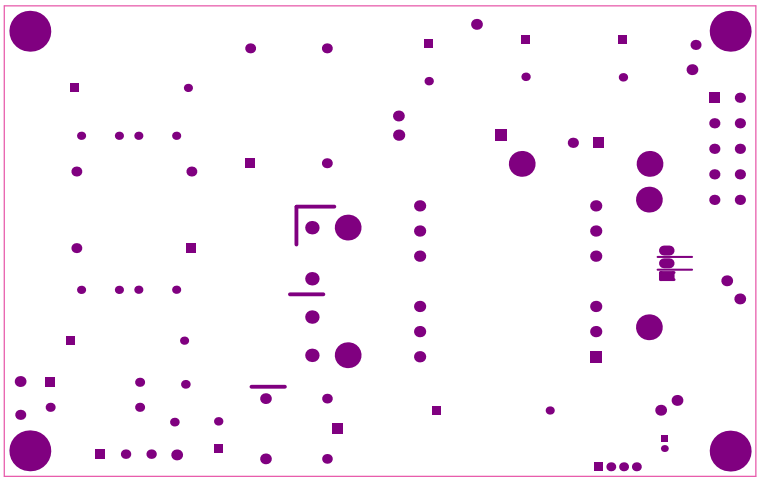
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00443	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Bottom Layer			
PLOT NAME = Bottom layer	GENERATED : 6/1/2015 4:57:52 PM		TEXAS INSTRUMENTS



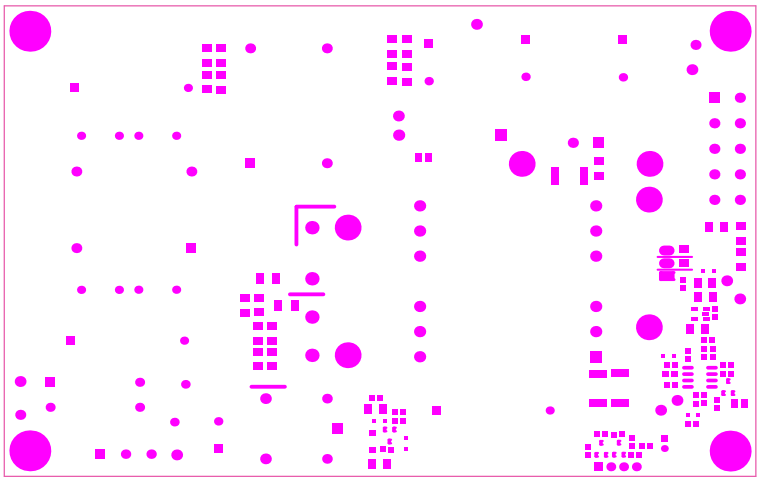
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00443	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Top Overlay			
PLOT NAME = Top Overlay	GENERATED : 6/1/2015 4:57:52 PM		TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00443	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Bottom Overlay			
PLOT NAME = Bottom overlay	GENERATED : 6/1/2015 4:57:53 PM		TEXAS INSTRUMENTS

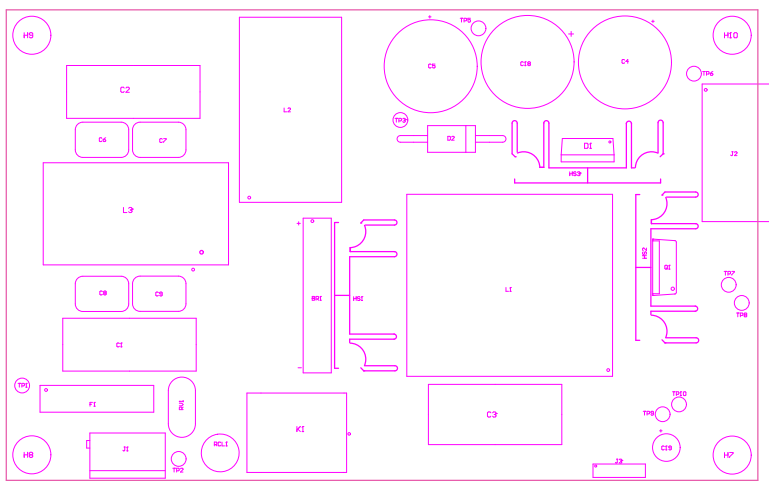


ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00443	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Top Solder			
PLOT NAME = Top Solder	GENERATED : 6/1/2015 4:57:54 PM		TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00443	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Bottom Solder			
PLOT NAME = Bottom Solder	GENERATED : 6/1/2015 4:57:54 PM		TEXAS INSTRUMENTS

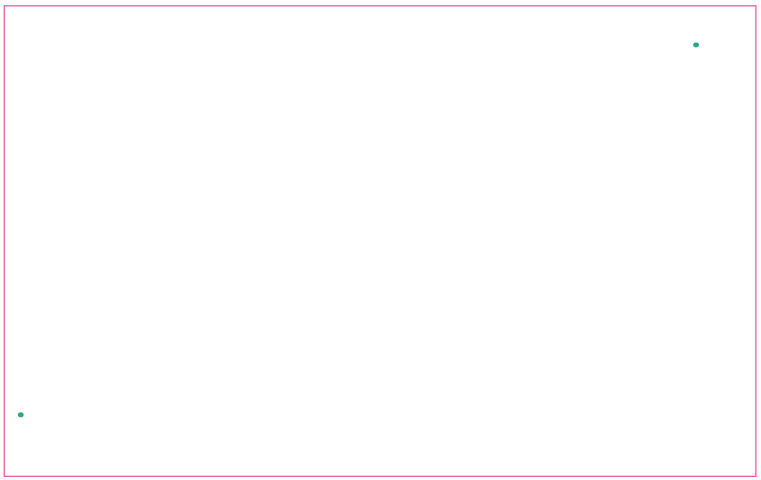
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANTS [No Variations]

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-00449	REVs E2	SVN REVs Not In VersionControl
M5 Assembly Top			
PLOT NAME = M5 Assembly Top	GENERATED : 6/1/2015	4:57:54 PM	TEXAS INSTRUMENTS

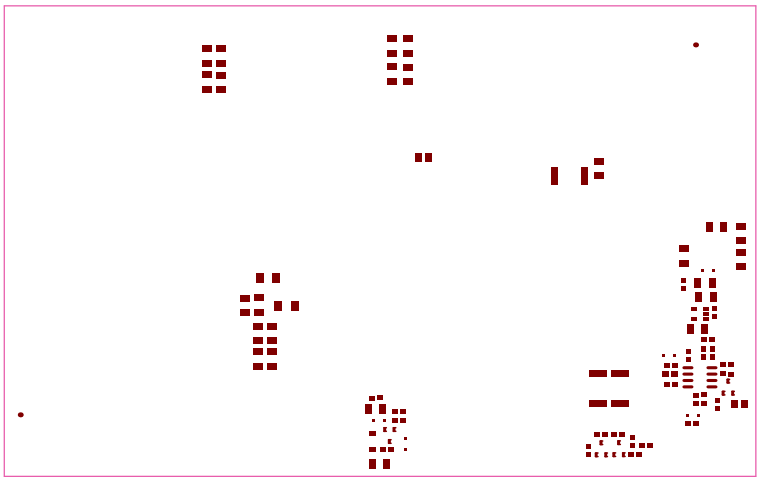


ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00443	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Top Paste			
PLOT NAME = Top Paste	GENERATED : 6/1/2015 4:57:55 PM		TEXAS INSTRUMENTS

ASSEMBLY VARIANTS: This Variation1

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

PCB VIDEO FROM BOTTOM SIDE			
M6 Assembly Bottom			
PLOT NAME = M6 Assembly Bottom	DERIVATED : 6-1-2018	4525/65 PM	TEXAS INSTRUMENTS
BOARD ID: TIDA-00443	REV: E2	SVN REV: Not In VersionControl	

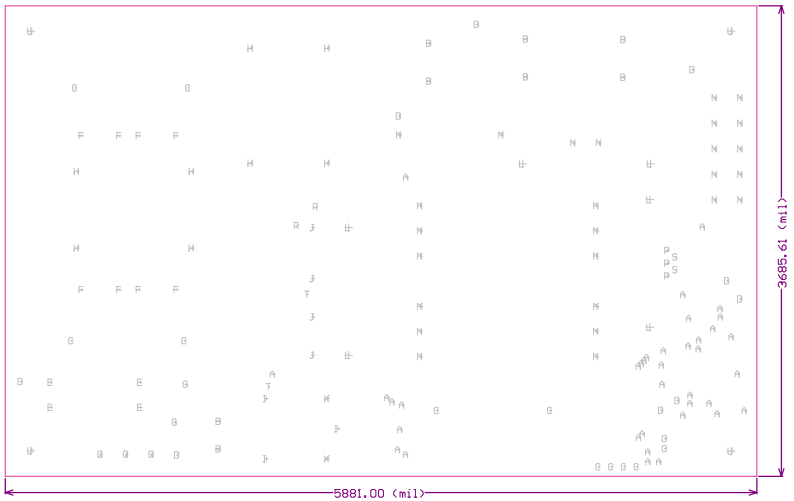


ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00443	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Bottom Paste			
PLOT NAME = Bottom Paste	GENERATED : 6/1/2015 4:57:56 PM		TEXAS INSTRUMENTS

Symbol	Hit Count	Tool Size	Physical Length	Rout Path Length	Plated	Hole Type
A	37	12mil (0.305mm)			PTH	Round
O	2	28mil (0.711mm)			PTH	Round
F	8	35mil (0.889mm)			PTH	Round
C	10	39.37mil (1mm)			PTH	Round
D	9	40mil (1.016mm)			PTH	Round
B	8	41.496mil (1.054mm)			PTH	Round
G	2	43.307mil (1.1mm)			PTH	Round
E	4	46.063mil (1.17mm)			PTH	Round
Q	3	49.213mil (1.25mm)			PTH	Round
P	3	50mil (1.27mm)			PTH	Round
K	2	51.181mil (1.3mm)			PTH	Round
H	8	53.15mil (1.35mm)			PTH	Round
N	12	55.118mil (1.4mm)			PTH	Round
J	4	57mil (1.448mm)			PTH	Round
I	3	59.055mil (1.5mm)			PTH	Round
M	14	62.992mil (1.6mm)			PTH	Round
L	6	118.11mil (3mm)			PTH	Round
U	4	125.984mil (3.2mm)			PTH	Round
S	2	12mil (0.305mm)	282mil (7.163mm)	270mil (6.858mm)	NPTH	Slot
T	2	20mil (0.508mm)	282mil (7.163mm)	262mil (6.655mm)	NPTH	Slot
R	2	20mil (0.508mm)	317mil (8.052mm)	297mil (7.544mm)	NPTH	Slot
	145 Total					

Slot definitions : **Rout Path Length** = Calculated from tool start centre position to tool end centre position.
Physical Length = Rout Path Length + Tool Size = Slot length as defined in the PCB layout

Drill Table
DRILL TOLERANCE
FOR PTH +/- 3MIL
12mil drill:+0/-12mil
FOR NPTH +/- 2MIL



Layer Stack Up Detail for: TIDA-00443-RevB

Layer Name	Gerber Document	Copper Thickness	Dielectric Height	Dielectric Material	Dielectric Constant	Dielectric Type
Top Solder Mask	(.GTS)		0.4mil	Solder Resist	3.50	
Top Layer	(.GTL)	1.4mil				
			59.2mil	FR-4 High Tg	4.80	Core
Bottom Layer	(.GBL)	1.4mil				
Bottom Solder Mask	(.GBS)		0.4mil	Solder Resist	3.50	

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
5881 MIL X 3685.61 MIL
Number of Layers : 2
MIN. TRACK WIDTH: 20 MIL
MIN. CLEARANCE: 8 MIL
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.152mm (6MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
IMPEDENCE CONTROLLED BOARD:NO

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62.99 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR:
[X] GREEN [ ] BLUE [ ] OTHER
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER MECH LAYER 1
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK
VIA'S TO BE TENTED: YES

Texas Instruments

PROJECT TITLE: 900W PFC Pre-Regulator for Inverter Fed Drives
DESIGNED FOR: Public Release
FILE NAME: TIDA-00443-RevB.PcbDoc
ENGINEER: Latif Ameer
LAYOUT BY: Avinash
SCALE: 0.67
ALTIUM DESIGNER VERSION: 10.0.0.27009

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00443	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Drill Guide			
PLOT NAME = Drill Drawing	GENERATED : 6/1/2015 4:57:57 PM		TEXAS INSTRUMENTS

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