Main Controller, Driver and Power Stage

VBAT Conversion Voltage Input

SVIDAdd=0(R7=DNP)
ZeroLoadLine(R29=Open)
Vboot=1V(R4=DNP)
SlewRate=10mV/us(R8=30k)
Imax=6.4A(R5=5826k)

FSW=1MHz(R14=150k)
OCL=11A(R12=75k)
USR Level8(LeastSensitive)
(R6=9.37k)
OSRLevel8(LeastSensitive)
(R15=150k)
RAMP=100mV(R13=39k)

TIDA-00572

Intel® Pentium™ N3700 VCC0+VCC1 Rail

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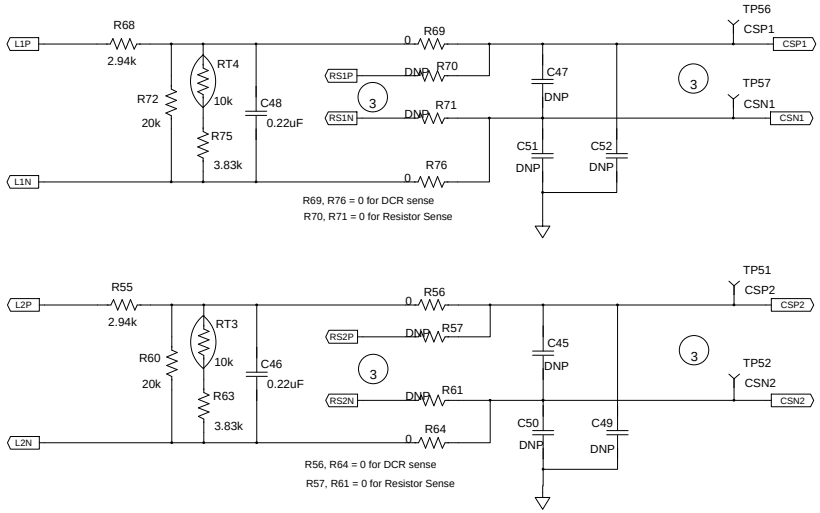
Notes:

1. A "*" before a component value indicates this component is not populated in the standard configuration.
2. These connections require kelvin connections to the component
3. These connections are to be run as differential pairs.

Title	Evaluation Schematic, TPS51631, VR12.5		
Size	C	Number	Rev A
Date	5/6/2015	Drawn by	Bo Wang
Engineer	Bo Wang	Filename	PR2110_TPS53625_EVM_Schematic_VCCP_Avoton-Rangley.sch
		Sheet	1 of 7

Current Feedback Selection (DCR Sense/ Res Sense) and Filtering



Notes:

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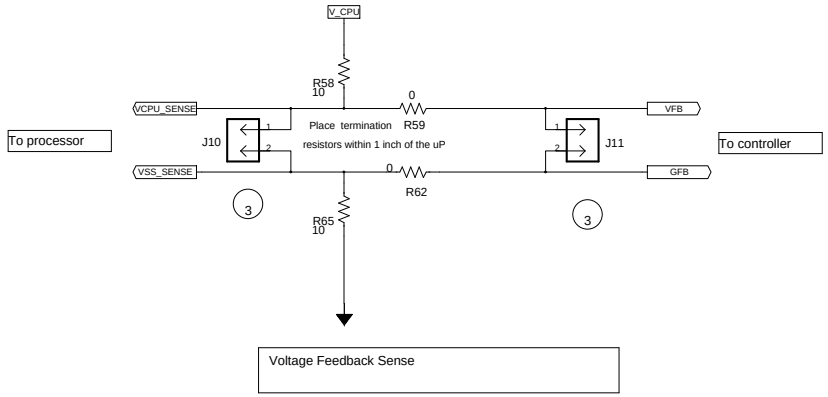
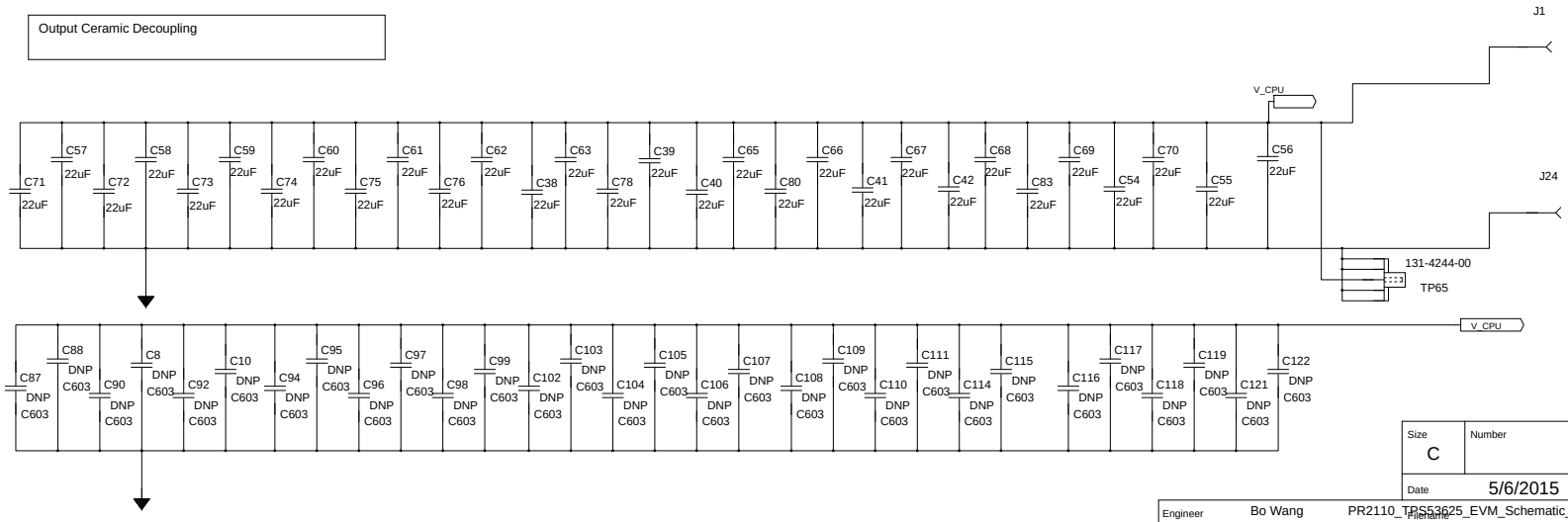


Output Ceramic Decoupling



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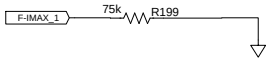
Frequency, OCP, OSR, SLEW, RAMP SELECTIONS

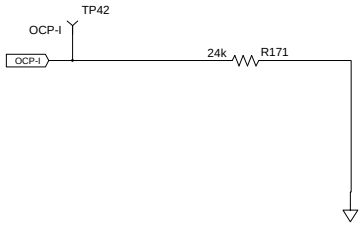
Note: ONLY TEST CIRCUITRY, NOT PART OF REFERENCE DESIGN

SWITCHING FREQUENCY SELECTION

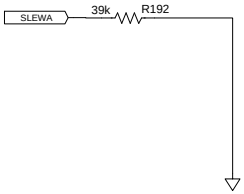


R199	Fsw
150K	1MHz
100K	900kHz
75K	800kHz
56k	700kHz
39k	600kHz
30k	500kHz
24k	400kHz
20k	300kHz

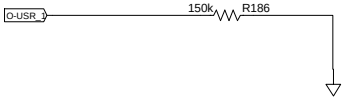
OVER-CURRENT PROTECTION SELECTION



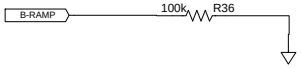
SLEW RATE SELECTION



OSR SELECTION



RAMP SELECTION



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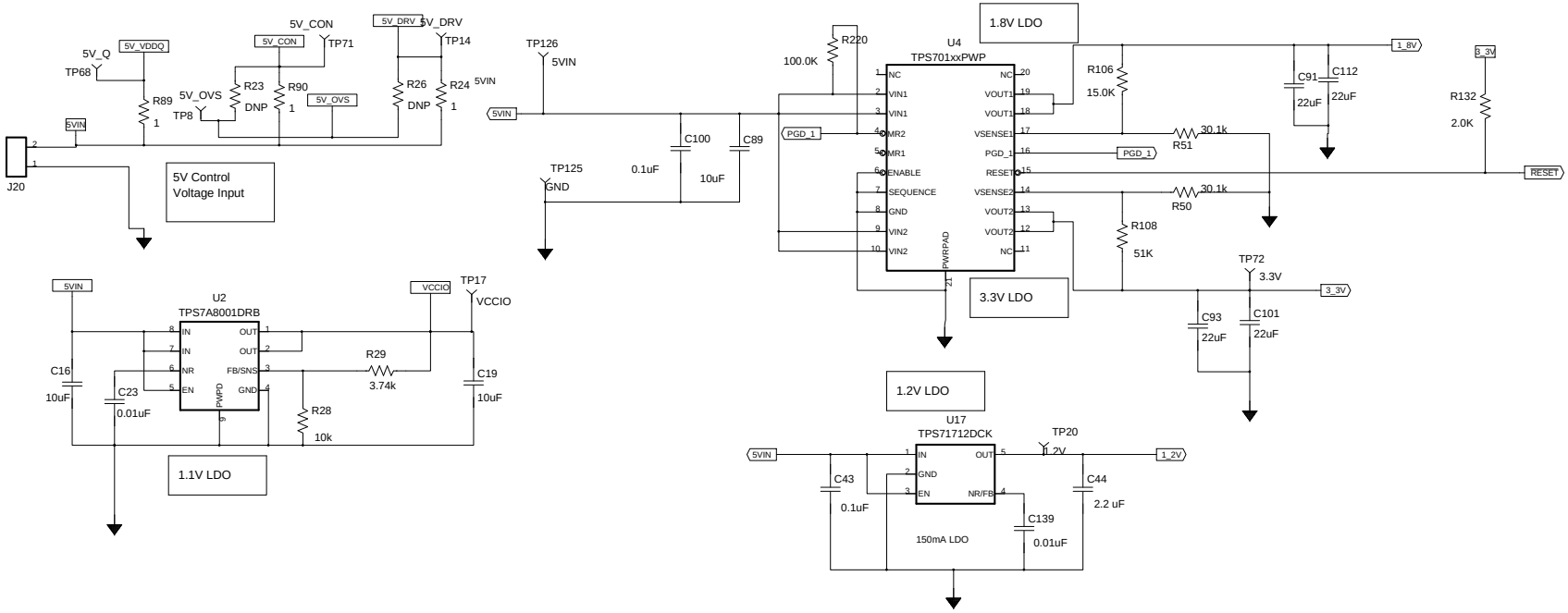
LDOs



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DSP BOARD Connector

Default Trim
R117 = DNP, R116 = 1k

Jumper to enter
I2C Mode

I2C Terminal

Logic Signal Termination and
Status LED's
LED is ON when the logic
signal is in the ACTIVE state

CONN_0442060007

CONN_0039299042

TLV3404PW

TS5A23157DGS

BSS123

BSS83P

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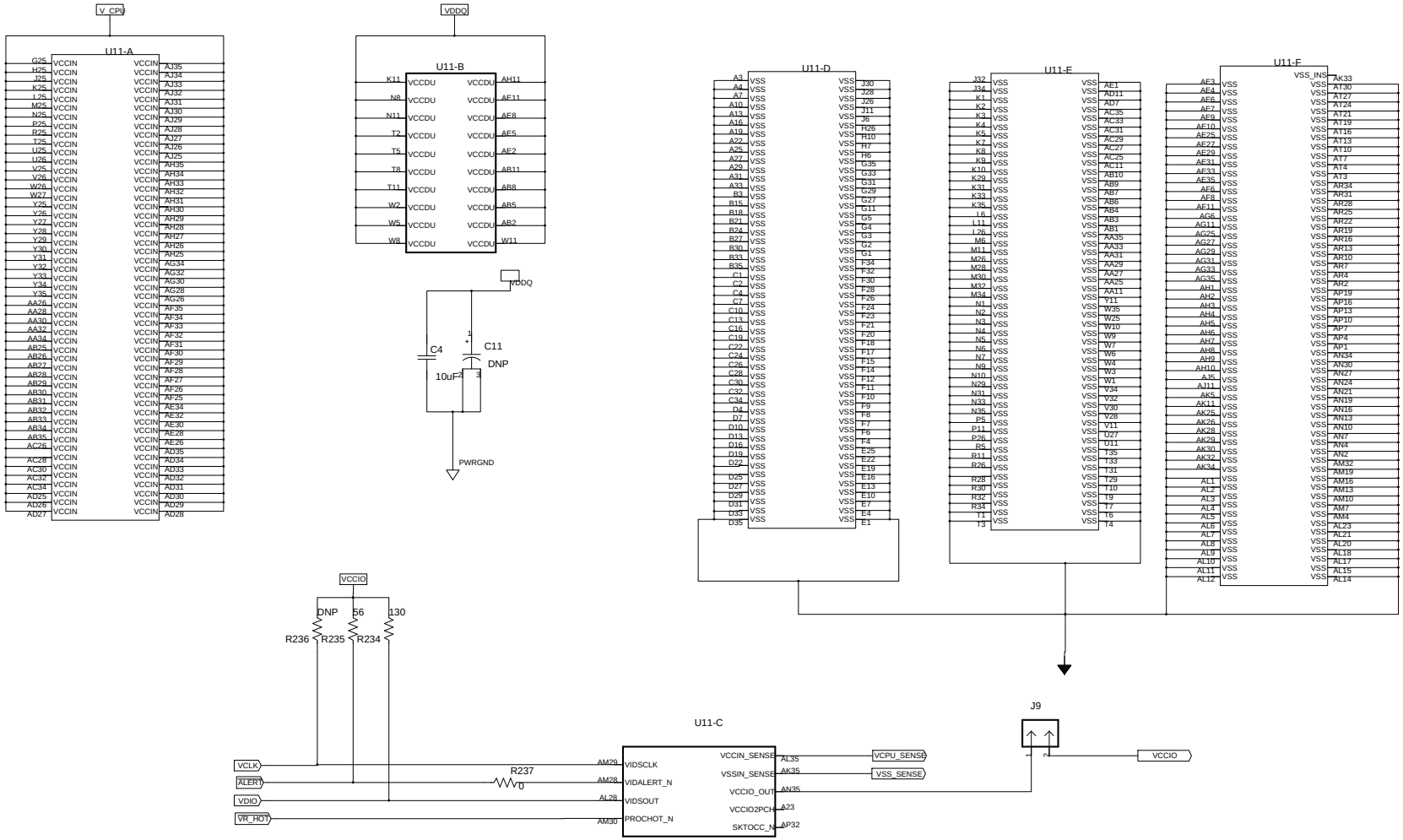

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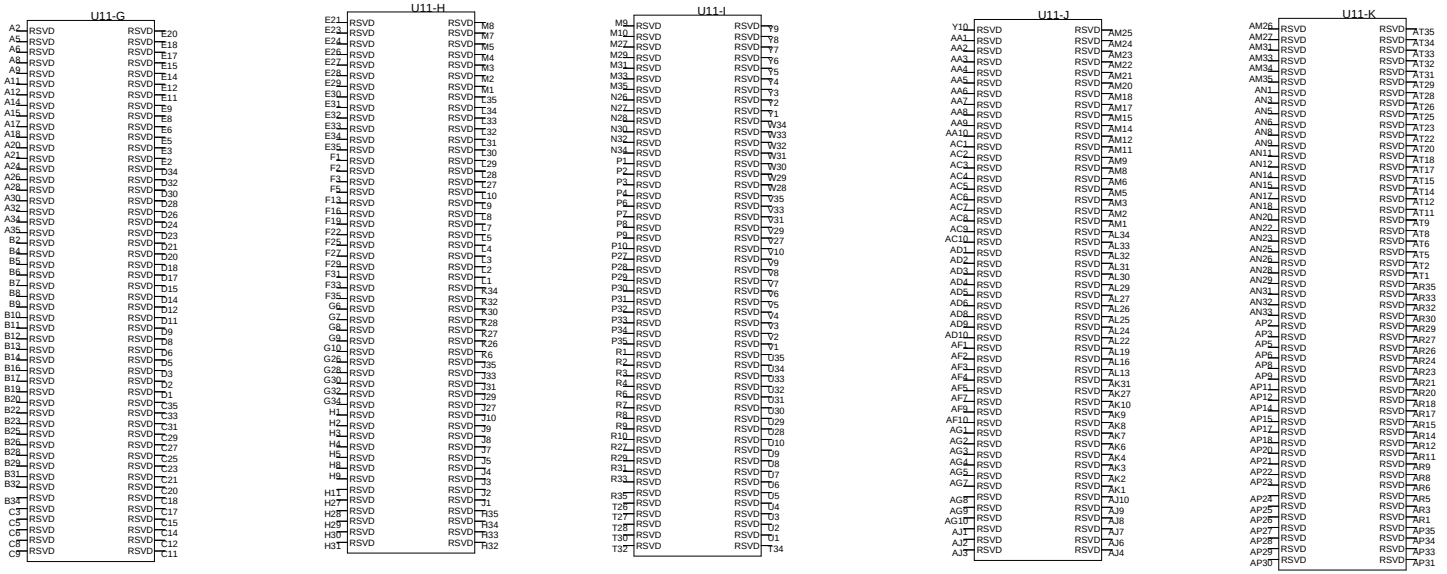

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5/6/2015

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