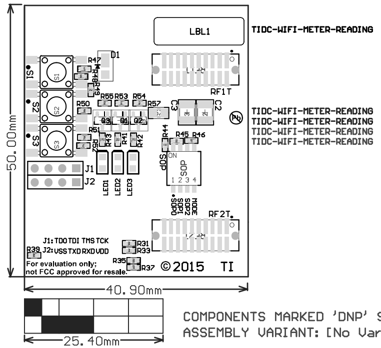
The Stackup Legend below this is static.
If you change the stackup, update the Legend.

Layer Stack Up Detail for: Ref_Design.PcbDoc

Layer Name	Gerber Document	Copper Thickness	Dielectric Material
Top Solder Mask	(.GTS)		Solder Resist
Top Layer	(.GTL)	1.4mil	FR-4
Bottom Layer	(.GBL)	1.4mil	
Bottom Solder Mask	(.GBS)		Solder Resist

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.
ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDC-WIFI-METER-READING	SVN REV: Not in version control
LAYER NAME = Top Overlay		
PLOT NAME = Top Layer Assembly Drawing	GENERATED : 10/26/2015 18:08:18	TEXAS INSTRUMENTS

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DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER ________
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER ________
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ________
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ________

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH MIN COPPER THICKNESS: ☒ 1MIL ☐ OTHER ________

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER ________
SOLDER RESIST COLOR:
☒ GREEN ☐ BLUE ☐ OTHER ________

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER ________

ARRAY/PANEL: ☐ CUT AND TRIM PER MECH LAYER 1
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ UL 94V-0 ☒ RoHS ☐ OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
MANUFACTURER'S UL: ☐ RAIL ☐ METAL ☒ SILK

TEXAS INSTRUMENTS

PROJECT TITLE:
Change in menu Project|Project Options|Parameters

DESIGNED FOR:
Public Release

FILE NAME:
CC3200MOD_CONV.PcbDoc

ENGINEER: Mars Leung	LAYOUT BY: Mars Leung
SCALE: 0.72	ALTIUM DESIGNER VERSION: 14.3.18.45973

The Stackup Legend below this is static.
If you change the stackup, update the Legend.

Layer Stack Up Detail for: Ref_Design.PcbDoc

Layer Name	Gerber Document	Copper Thickness	Dielectric Material
Top Solder Mask	(.GTS)		Solder Resist
Top Layer	(.GTL)	1.4mil	FR-4
Bottom Layer	(.GBL)	1.4mil	
Bottom Solder Mask	(.GBS)		Solder Resist

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER ____
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER ____
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH MIN COPPER THICKNESS: ☒ 1MIL ☐ OTHER ____

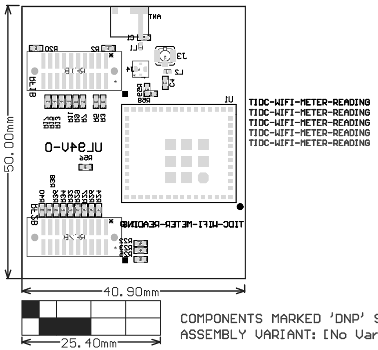
BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER ____
SOLDER RESIST COLOR:
☒ GREEN ☐ BLUE ☐ OTHER ____

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER ____

ARRAY/PANEL: ☐ CUT AND TRIM PER MECH LAYER 1
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ UL 94V-0 ☒ RoHS ☐ OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
MANUFACTURER'S UL: ☐ RAIL ☐ METAL ☒ SILK



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDC-WIFI-METER-READING	REV: Not in VersionControl
LAYER NAME = Bottom Overlay	IGNORE	
PLOT NAME = Altium LayerAssemblyDrawing	GENERATED : 10/27/2015 18:08:07	TEXAS INSTRUMENTS

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PROJECT TITLE: Change in menu Project|Project Options|Parameter	
DESIGNED FOR: Public Release	
FILE NAME: CC3200MOD_CONV.PcbDoc	
ENGINEER: Mars Leung	LAYOUT BY: Mars Leung
SCALE: 0.72	ALTIUM DESIGNER VERSION: 14.3.18.45973

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