

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4	59.20mil	4.8	
5	Internal Plane 1	Copper	1.42mil		
6	Dielectric 3		5.00mil	4.2	
7	Internal Plane 2	Copper	1.42mil		
8	Dielectric 2		10.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

221 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.  
 222 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.  
 223 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 8 ML  
 MIN. CLEARANCE: 0.2 mm  
 MIN. VIA PAD SIZE: 24 ML  
 MINIMUM ANNULAR RING: 0.05mm (2ML) EXTERNAL  
 PER IPC-D-275 CLASS 2 LEVEL C  
 REGISTRATION TOLERANCES: METAL +/- 5 ML HOLES +/- 3 ML

**MATERIAL:**  
 FR-408  FR-4 High Tg  OTHER \_\_\_\_\_  
 THICKNESS:  62 ML (1.6mm) +/-10%  OTHER \_\_\_\_\_  
 TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/- \_\_\_\_\_  
 BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/- \_\_\_\_\_

**DRILLING:**  
 REFERENCE:  AS SHOWN  NC\_DRILL FILES  
 PTH MIN COPPER THICKNESS:  1ML  OTHER \_\_\_\_\_

**BOARD FINISH:**  
 SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  BLUE  OTHER \_\_\_\_\_

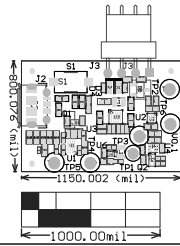
**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

**ARRAY/PANEL:**  CUT AND TRM PER MECH LAYER 1  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS -> 1  2  3  
 UL 94V-0  RoHS  OTHER PER ORDER

ADDITIONAL REQUIREMENTS:  
 MICROSECTION:  YES  
 BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER  
 MANUFACTURER'S UL:  RAL  METAL  SLK



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.  
 ASSEMBLY VARIANT: [No Variations]

PCB BOARD NUMBER: 13	BOARD #: 13	TID #: CHANGELIST	# OF REV: 1	EL:	SUN REV: No Change	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	ENGINEER: [Name]	LAYOUT BY: [Name]
LAYER NAME = [Name]	TID #: CHANGELIST	# OF REV: 1	EL:	SUN REV: No Change	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	ENGINEER: [Name]	LAYOUT BY: [Name]	
PLOT NAME: [Name]	GENERATED: 9/22/2015 10:38 AM	SCALE: 0.72	ALTIM DESIGNER VERSION: 14.3.18.4593					

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				✓
2	Top Solder	Solder Resist	0.40mil	3.5	✓
3	Top Layer	Copper	1.40mil		✓
4	Dielectric 1	FR-4	59.20mil	4.8	✓
5	Internal Plane 1	Copper	1.42mil		✓
6	Dielectric 3		5.00mil	4.2	✓
7	Internal Plane 2	Copper	1.42mil		✓
8	Dielectric 2		10.00mil	4.2	✓
9	Bottom Layer	Copper	1.40mil		✓
10	Bottom Solder	Solder Resist	0.40mil	3.5	✓
11	Bottom Overlay				✓

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 PER IPC-D-275 CLASS 2 LEVEL C  
 REGISTRATION TOLERANCES: METAL +/- 5 ML HOLES +/- 3 ML

MATERIAL:  
 FR-408  FR-4 High Tg  OTHER \_\_\_\_\_  
 THICKNESS:  62 ML (1.6mm) +/-10%  OTHER \_\_\_\_\_  
 TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_  
 BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_


DRILLING:  
 REFERENCE:  AS SHOWN  NC\_DRILL FILES  
 PTH MIN COPPER THICKNESS:  1ML  OTHER \_\_\_\_\_

BOARD FINISH:  
 SILKSCREEN COLOR:  TOP  BOTTOM  
 WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  
 GREEN  BLUE  OTHER \_\_\_\_\_

SURFACE FINISH:  IMMERSION GOLD (ENIG)  ENERP  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

ARRAY/PANEL:  CUT AND TRM PER MECH LAYER 1  
 N.C. ROUTE  V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs  
 TO MEET OR EXCEED THE REQUIREMENTS OF:



PROJECT TITLE:  
Change in menu Project\Project Options\Parameters

DESIGNED FOR:  
Public Release

FILE NAME:  
TIDN-00712-Smart Watch BMS PCB V0.3\_PcbDoc

ENGINEER:  
Enter name of project lead

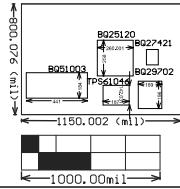
LAYOUT BY:  
Who did the Layout?

SCALE: 0.72

ALTIM DESIGNER VERSION:  
14.3.18.45973

ANSI IPC-A-600F CLASS -> 1  2  3  
 UL 94V-0  RoHS  OTHER PER ORDER

ADDITIONAL REQUIREMENTS:  
 MICROSECTION:  YES  
 BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER  
 MANUFACTURER'S UL:  RAL  METAL  SLK



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. ASSEMBLY VARIANT: [No Variations]

COMPOUND COMPONENTS SHOULD BE POPULATED IN THE BOARD LAYER. ASSEMBLY VARIANT: [No Variations]

PCB BOARD NAME: BMS PCB V0.3_PcbDoc	REV: 13	TITLE: BMS PCB V0.3_PcbDoc	DATE: 09/22/2015	DESIGNER: [Name]	DATE: 09/22/2015	TIME: 14:48	PROJECT: BMS PCB V0.3_PcbDoc	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = BMS PCB V0.3_PcbDoc	TID #:	CHANGE #:	DATE:					
PLOT NAME: BMS PCB V0.3_PcbDoc	GENERATED:	DATE:	TIME:					

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