

## NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P1P1V" represents connection to the +1.1V FPGA power plane
2. The netname "P1P1V\_FIL" represents connection to the +1.1V filtered FPGA power plane
3. The netname "P1P1V\_M" represents connection to the +1.1V Master ASIC power plane
4. The netname "P1P1V\_S" represents connection to the +1.1V Slave ASIC power plane
5. The netname "P1P15V" represents connection to the +1.15V FPGA power plane
6. The netname "P1P15V" represents connection to the +1.15V filtered FPGA power plane
7. The netname "P1P5V" represents connection to the +1.5V FPGA power plane
8. The netname "P1P5V\_FIL" represents connection to the +1.5V filtered FPGA power plane
9. The netname "P1P8V\_M" represents connection to the +1.8V Master ASIC power plane
10. The netname "P1P8V\_S" represents connection to the +1.8V Slave ASIC power plane
11. The netname "A1P8V\_M" represents connection to the +1.8V Master ASIC power plane for the PLLs
12. The netname "A1P8V\_S" represents connection to the +1.8V Slave ASIC power plane for the PLLs
13. The netname "P2P5V" represents connection to the +2.5V FPGA power plane
14. The netname "P2P5V\_FIL" represents connection to the +2.5V filtered FPGA power plane
15. The netname "P2P5V\_M" represents connection to the +2.5V Master ASIC power plane
16. The netname "P2P5V\_S" represents connection to the +2.5V Slave ASIC power plane
17. The netname "P3P3V" represents connection to the +3.3V FPGA power plane
18. The netname "P3P3V\_M" represents connection to the +3.3V Master ASIC power plane
19. The netname "P3P3V\_S" represents connection to the +3.3V Slave ASIC power plane
20. The netname "P5V\_M" represents connection to the +5V Master ASIC power plane
21. The netname "P5V\_S" represents connection to the +5V Slave ASIC power plane
22. The netname "P12V" represents the connection to the +12.0V power plane.
23. The netname "GND" represents connection to the ground plane
24. A "Z" suffix on a signal name indicates an active low signal
25. All components with designators "U\*", "Q\*", "D\*" are electrostatic discharge sensitive.
26. All components with designators above 500 are mounted on the bottom side of the board.
27. All resistor values are in ohms.

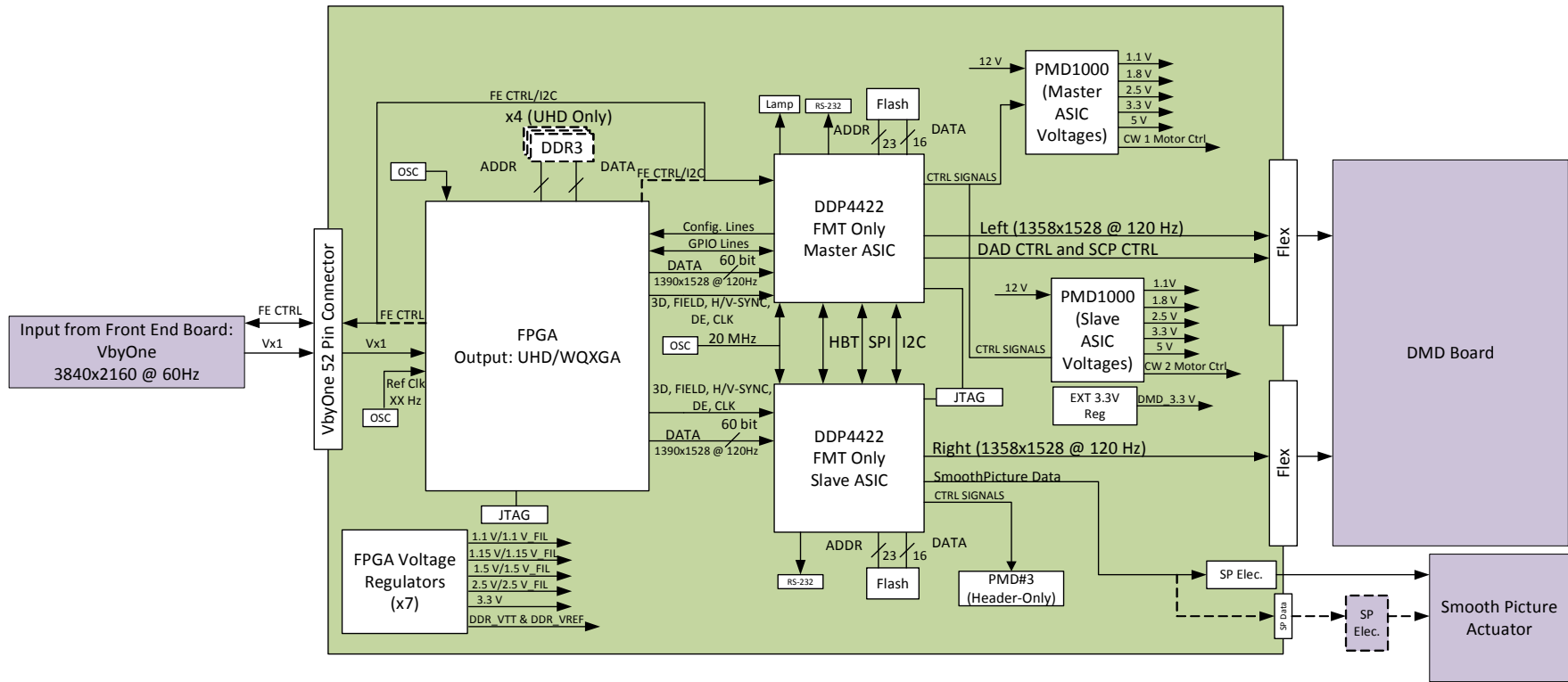
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2149913: Initial Release	4/13/2015	DH
B	ECO 2150627	5/15/2015	DH
C	ECO 2150877	6/25/2015	DH
D	ECO 2153403	9/15/2015	DH

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 Sheet 31: Smooth Picture Electronics  
 Sheet 32: Master Power and Bypass Caps  
 Sheet 33: Slave Power and Bypass Caps  
 Sheet 34: Revisions

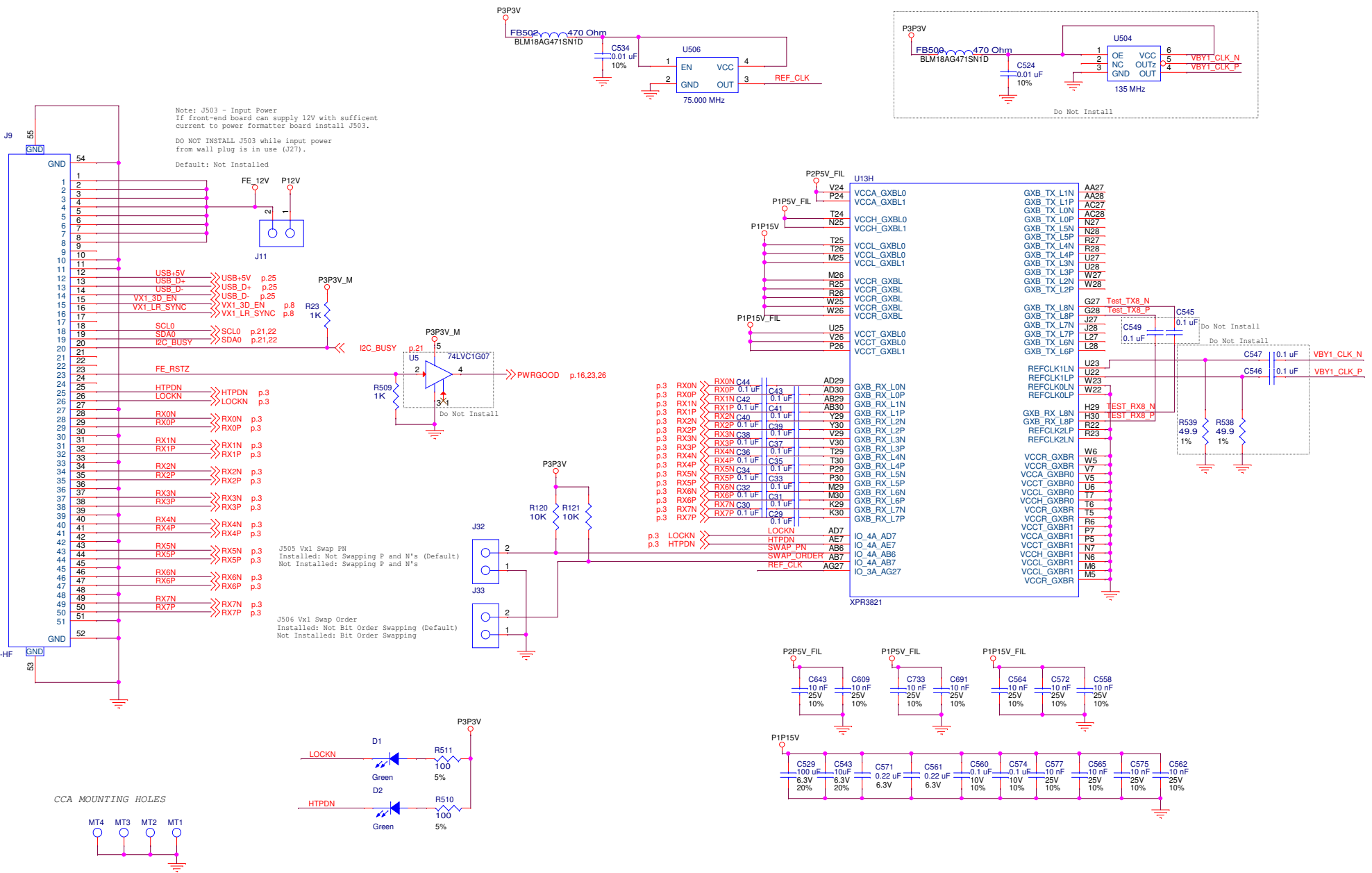
		DWN	Ben Uhing	DATE	9/30/2016	<b>TEXAS INSTRUMENTS</b> (C) COPYRIGHT 2015 TEXAS INSTRUMENTS ALL RIGHTS RESERVED
		ENGR	Scott Vestal		4/9/2015	
		APVD				
		MFG				
		QA				
NEXT ASSY	USED ON					TITLE TIDA-01347 P66 4KUHD Formatter Board
APPLICATION		SW	Cadence 16.6			<b>A3</b> DRAWING NO 2514423 REV E
				SCALE		SHEET 1 of 34

# Block Diagram



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	ISSUE DATE 3/18/2015	SCALE			



Note: J503 - Input Power  
 If front-end board can supply 12V with sufficient current to power formatter board install J503.  
 DO NOT INSTALL J503 while input power from wall plug is in use (J27).  
 Default: Not Installed

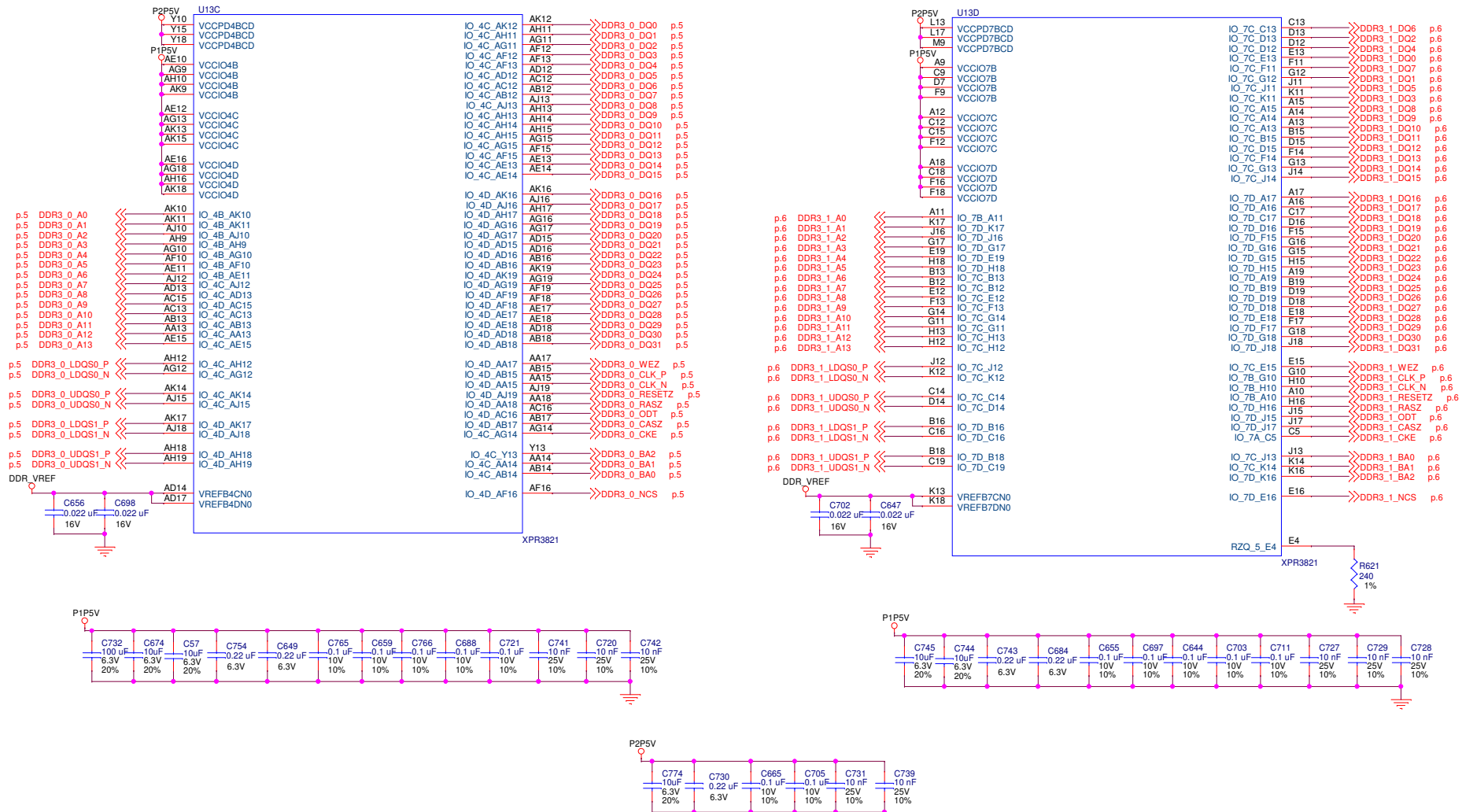
J505 Vx1 Swap PN  
 Installed: Not Swapping P and N's (Default)  
 Not Installed: Swapping P and N's

J506 Vx1 Swap Order  
 Installed: Not Bit Order Swapping (Default)  
 Not Installed: Bit Order Swapping

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FPGA - Front-End I/F

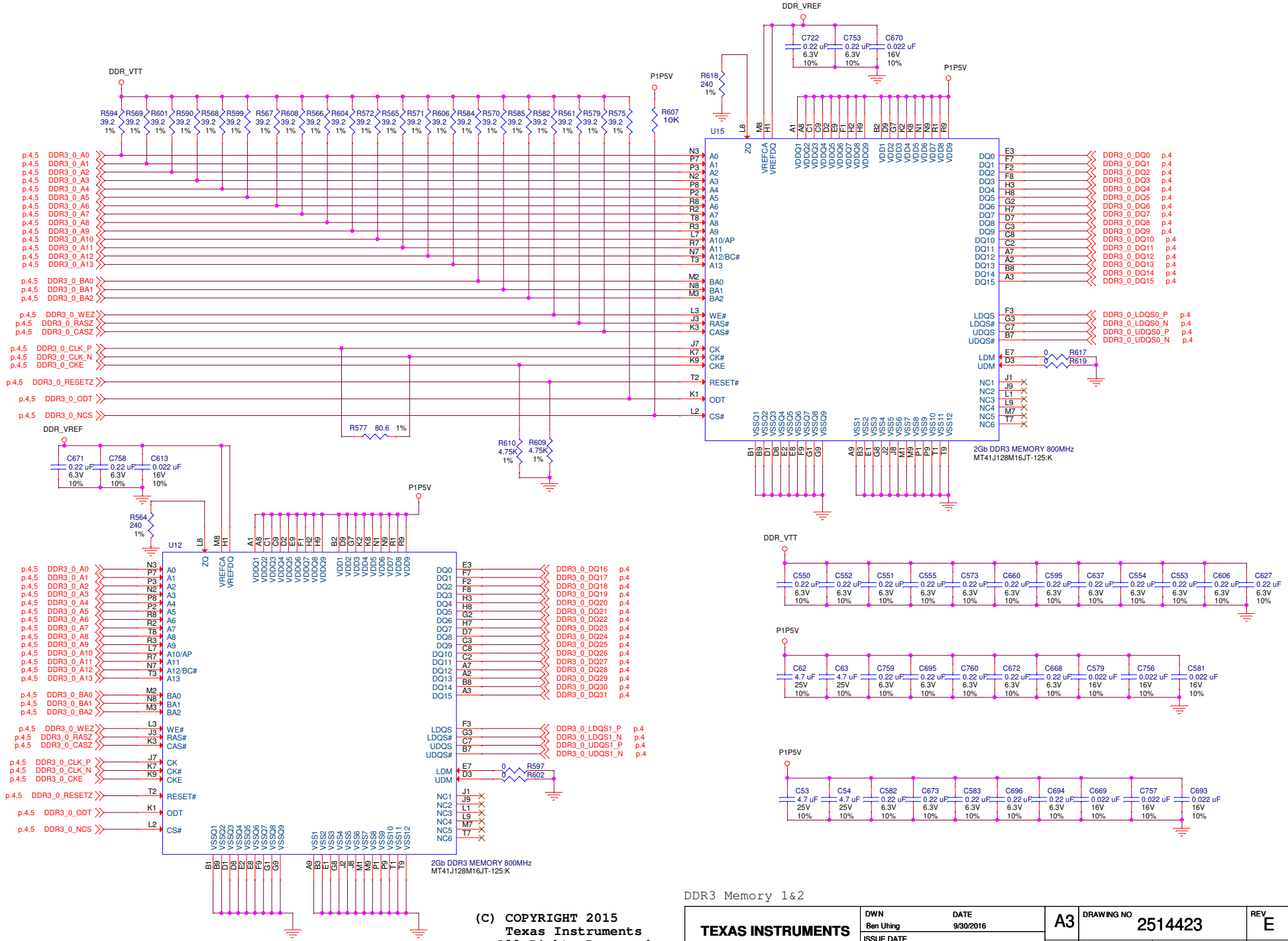
<b>TEXAS INSTRUMENTS</b>	DWN Ben Uhing	DATE 9/30/2016	<b>A3</b>	DRAWING NO <b>2514423</b>	REV <b>E</b>
	ISSUE DATE 1/31/2017	SCALE			



FPGA - DDR3 Interface

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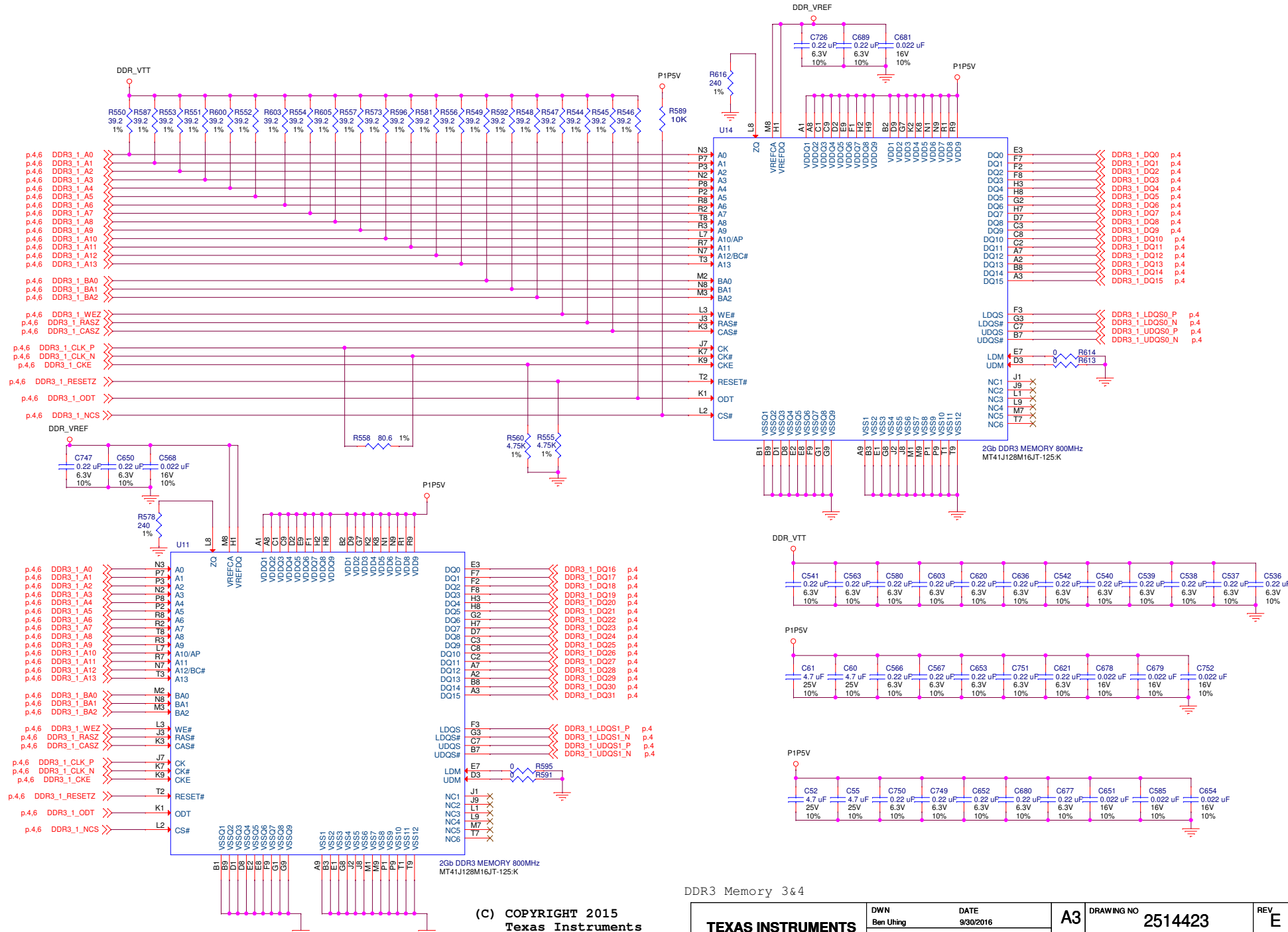
<b>TEXAS INSTRUMENTS</b> DWN Ben Uhling ISSUE DATE 1/31/2017	DATE 9/30/2016	<b>A3</b>	DRAWING NO 2514423	REV E
	SCALE	SHEET 4 OF 34		



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DDR3 Memory 1&2

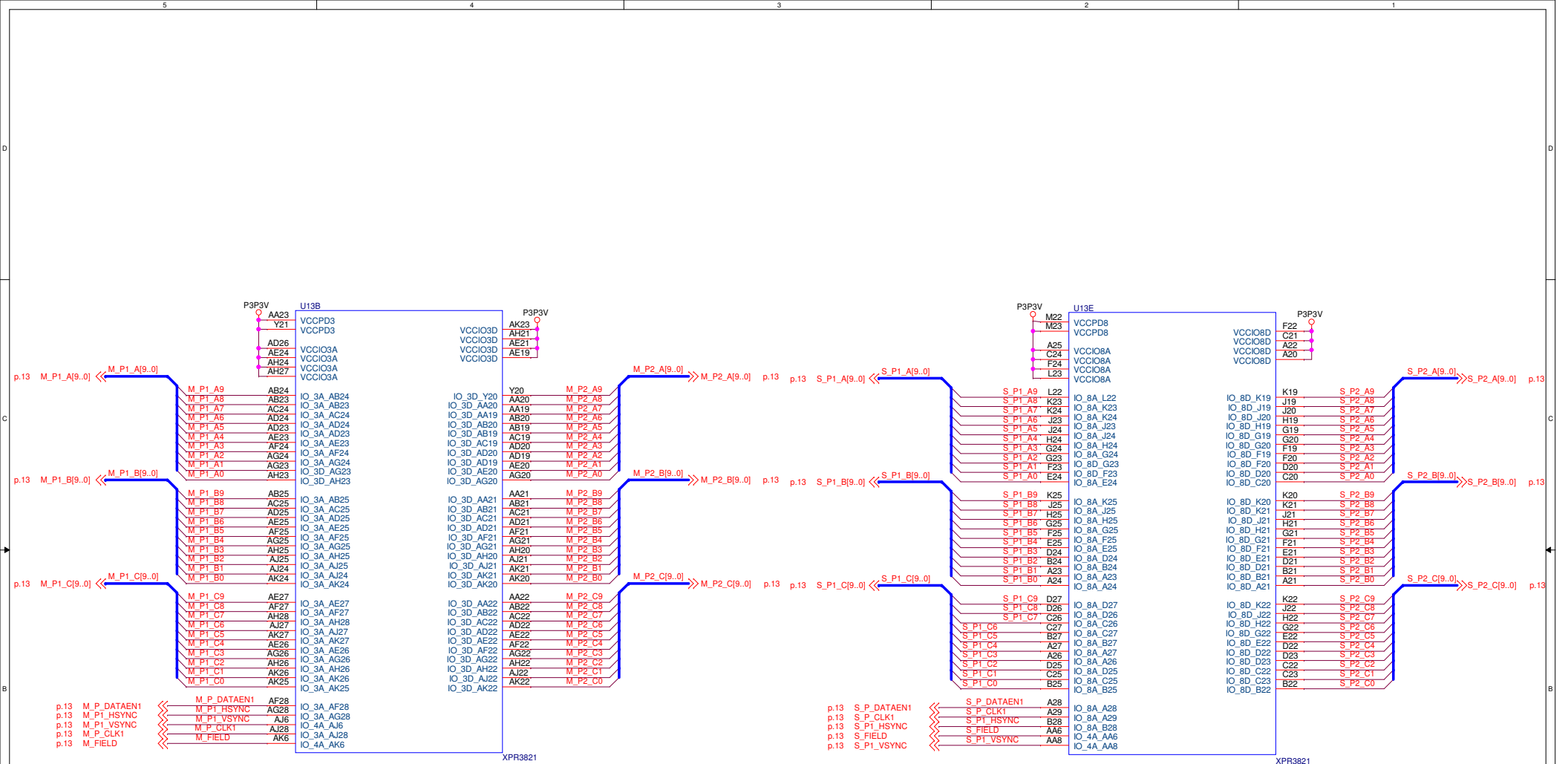
<b>TEXAS INSTRUMENTS</b> DWN Ben Uthing ISSUE DATE 1/31/2017	DATE 9/30/2016	<b>A3</b>	DRAWING NO <b>2514423</b>	REV <b>E</b>
	SCALE	SHEET 5 OF 34		



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DDR3 Memory 3&4

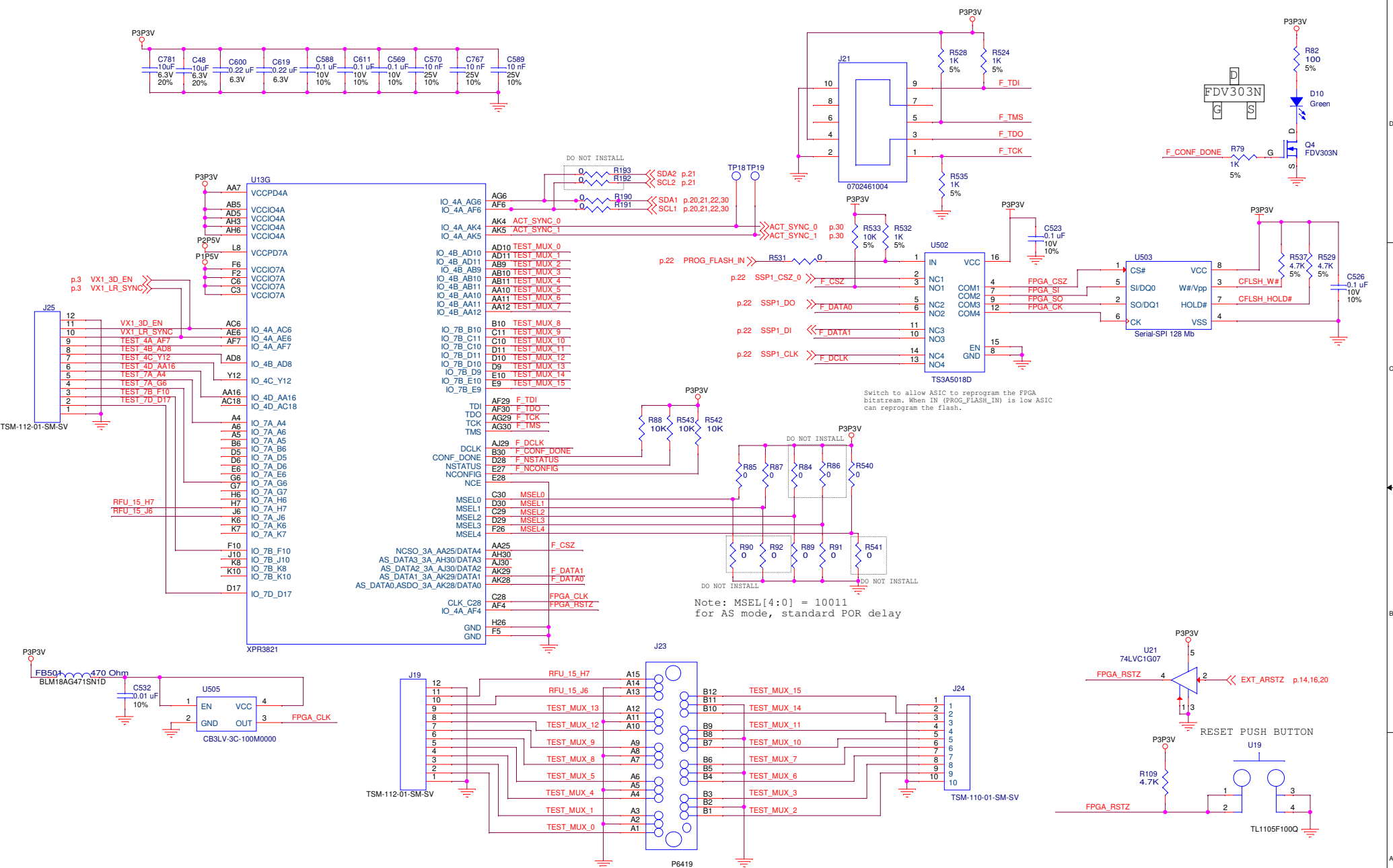
<b>TEXAS INSTRUMENTS</b> DWN Ben Ulling ISSUE DATE 1/31/2017	DATE 9/30/2016	<b>A3</b> DRAWING NO <b>2514423</b>	REV <b>E</b>
	SCALE		SHEET 6 OF 34



FPGA - Video I/F

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	SCALE		



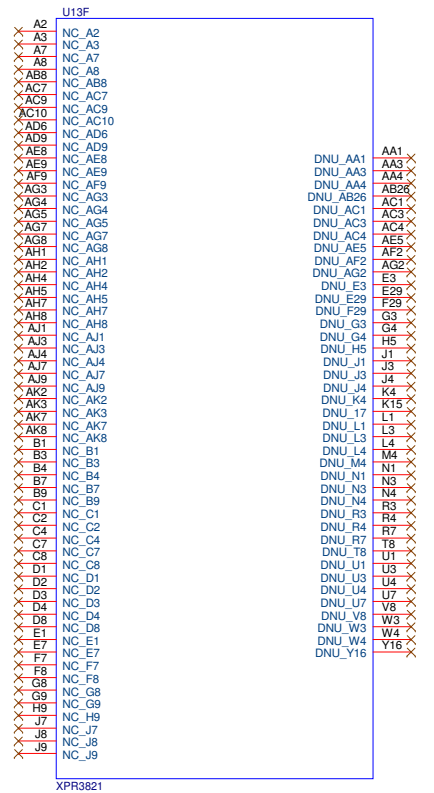
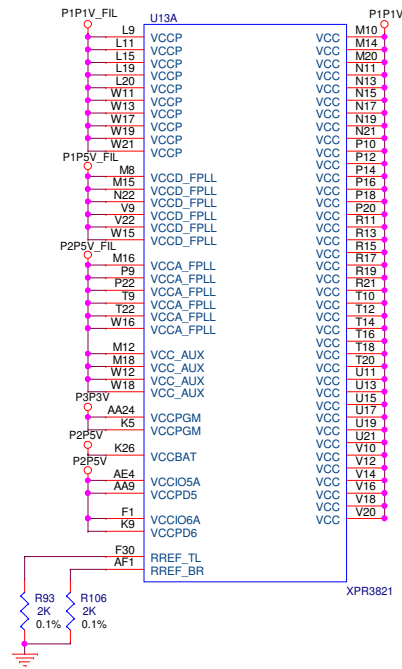
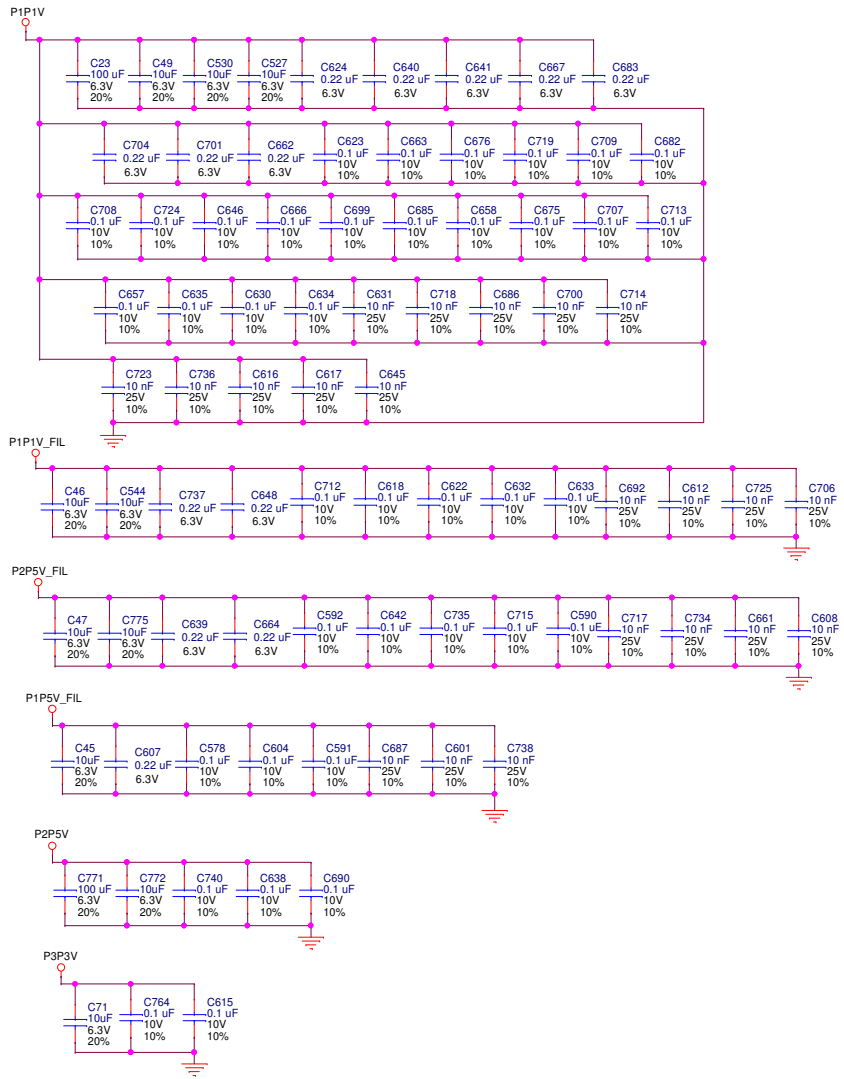
Note: MSEL[4:0] = 10111 for AS mode, standard POR delay

FPGA - Programming and Test Mux

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	ISSUE DATE 1/31/2017	SCALE			



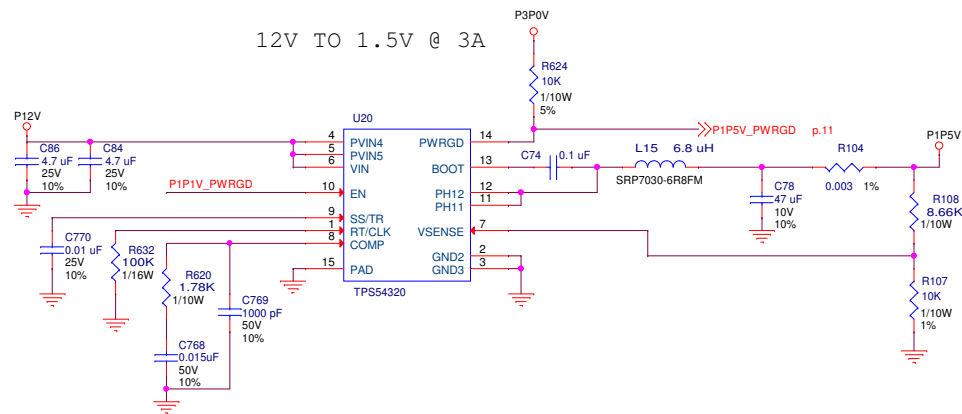
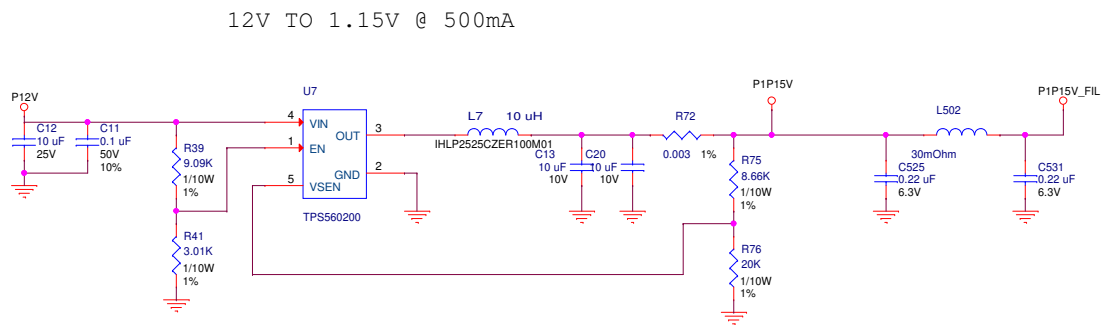
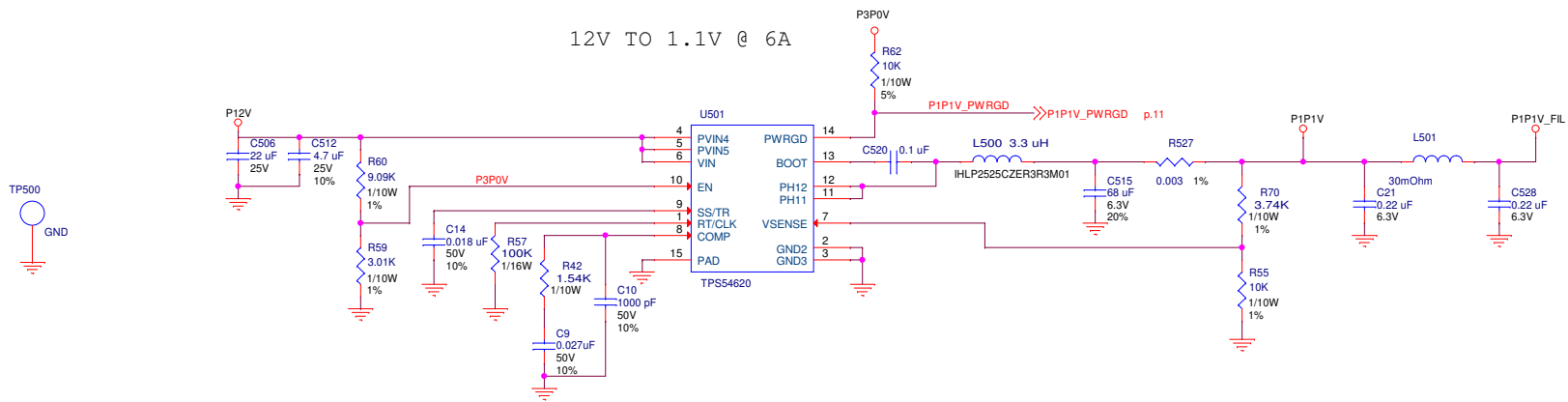


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FPGA - Power

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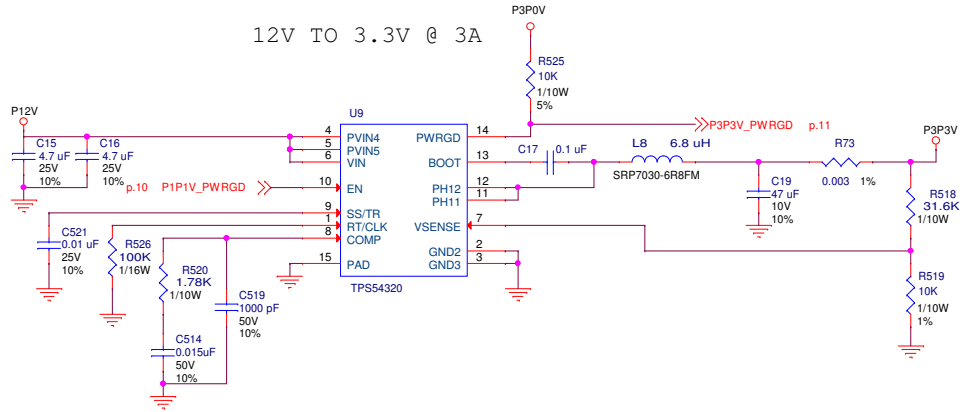
DWN Ben Uthing	DATE 9/30/2016	A3	DRAWING NO 2514423	REV E
ISSUE DATE 1/31/2017	SCALE	SHEET 9 OF 34		



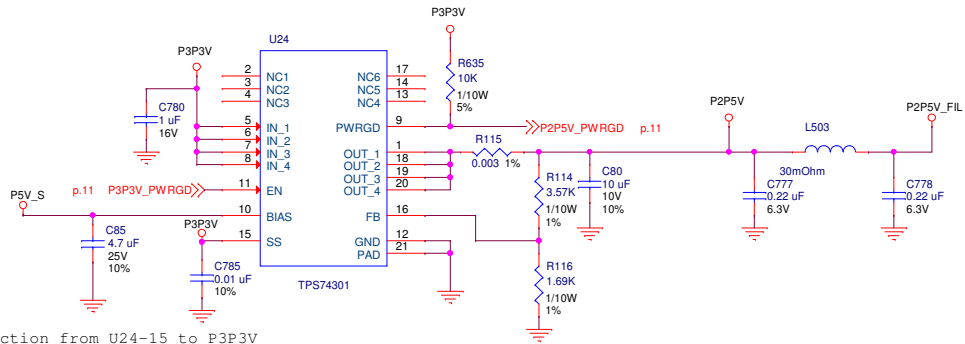
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12V TO 3.3V @ 3A

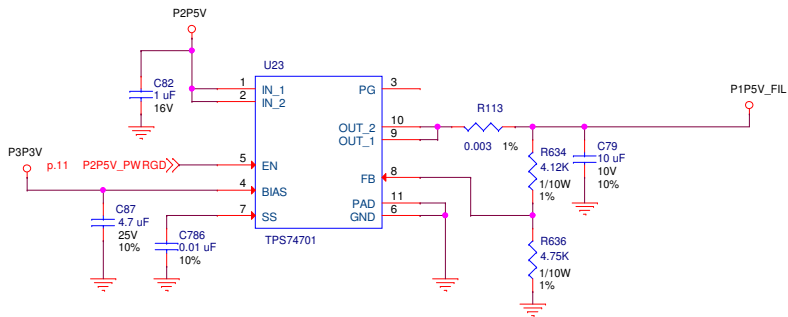


3.3V TO 2.5V @ 1.5A

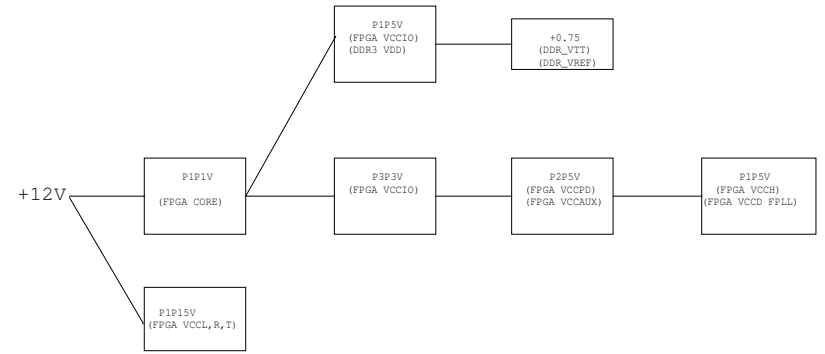


The connection from U24-15 to P3P3V is a blue wire on existing Rev A pwb's.

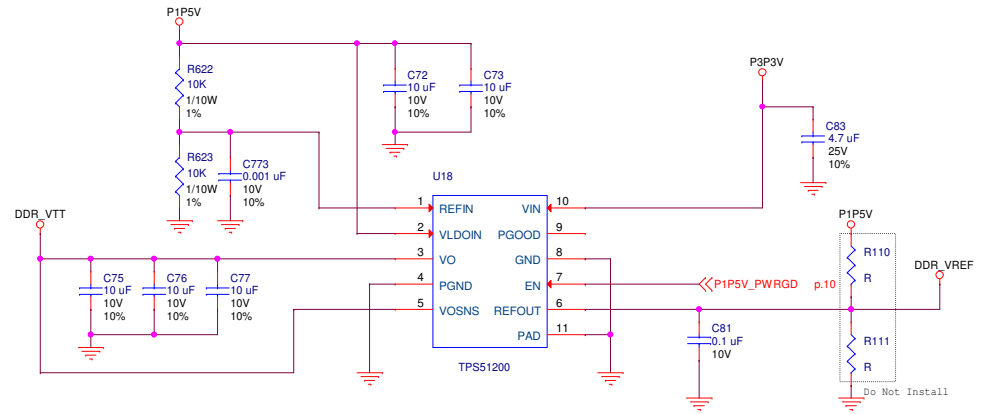
2.5V TO 1.5V @ 500mA



Power Sequence



1.5V TO 0.75V DDR\_VTT & DDR\_VREF



DDR TERMINATION VOLTAGE

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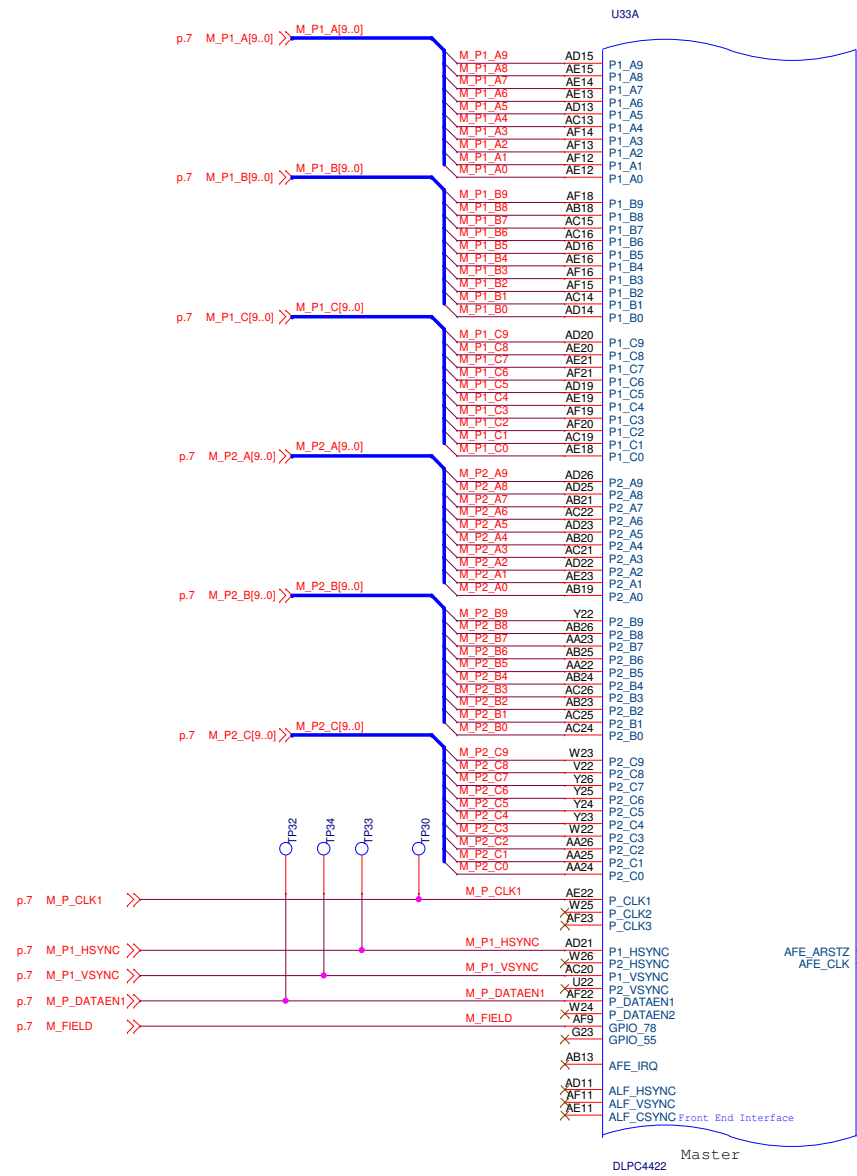


XPR3821

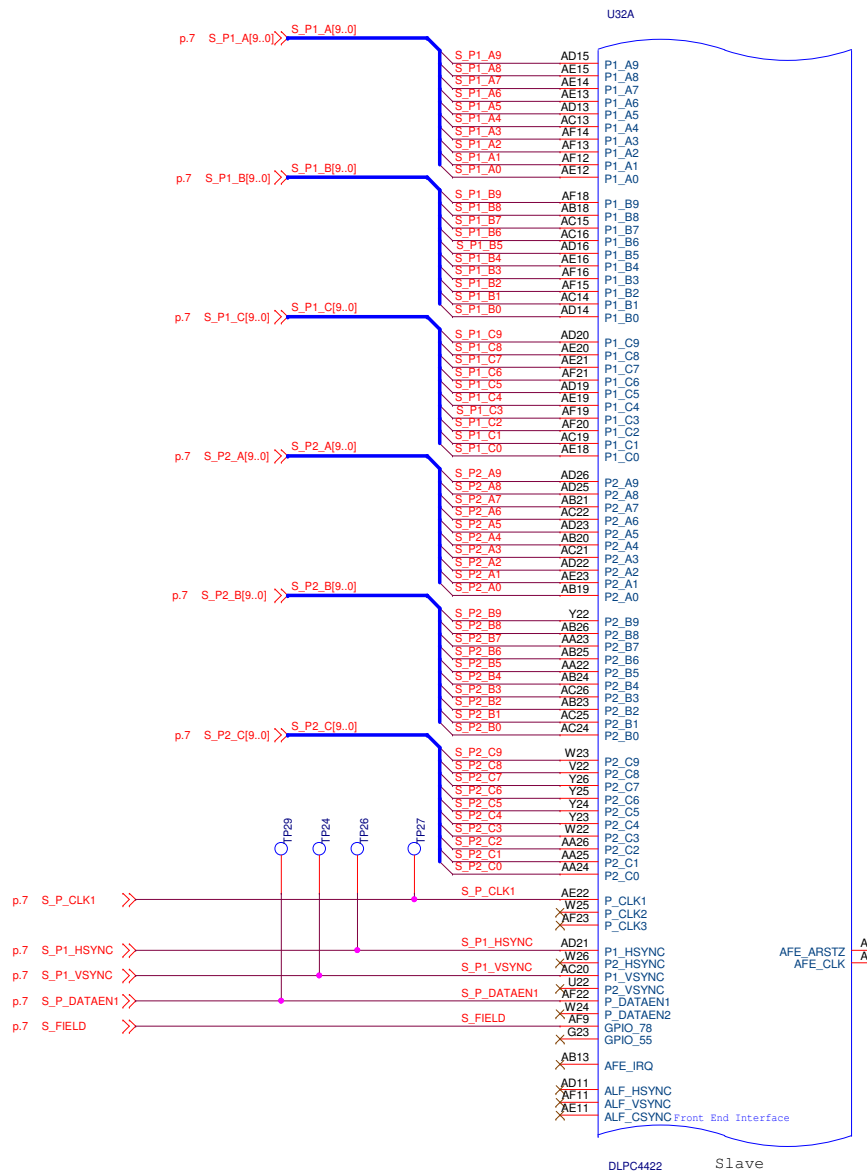
FPGA - GND

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AFE\_ARSTZ  
AFE\_CLK



AFE\_ARSTZ  
AFE\_CLK

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Master and Slave Front End Interface

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U33B

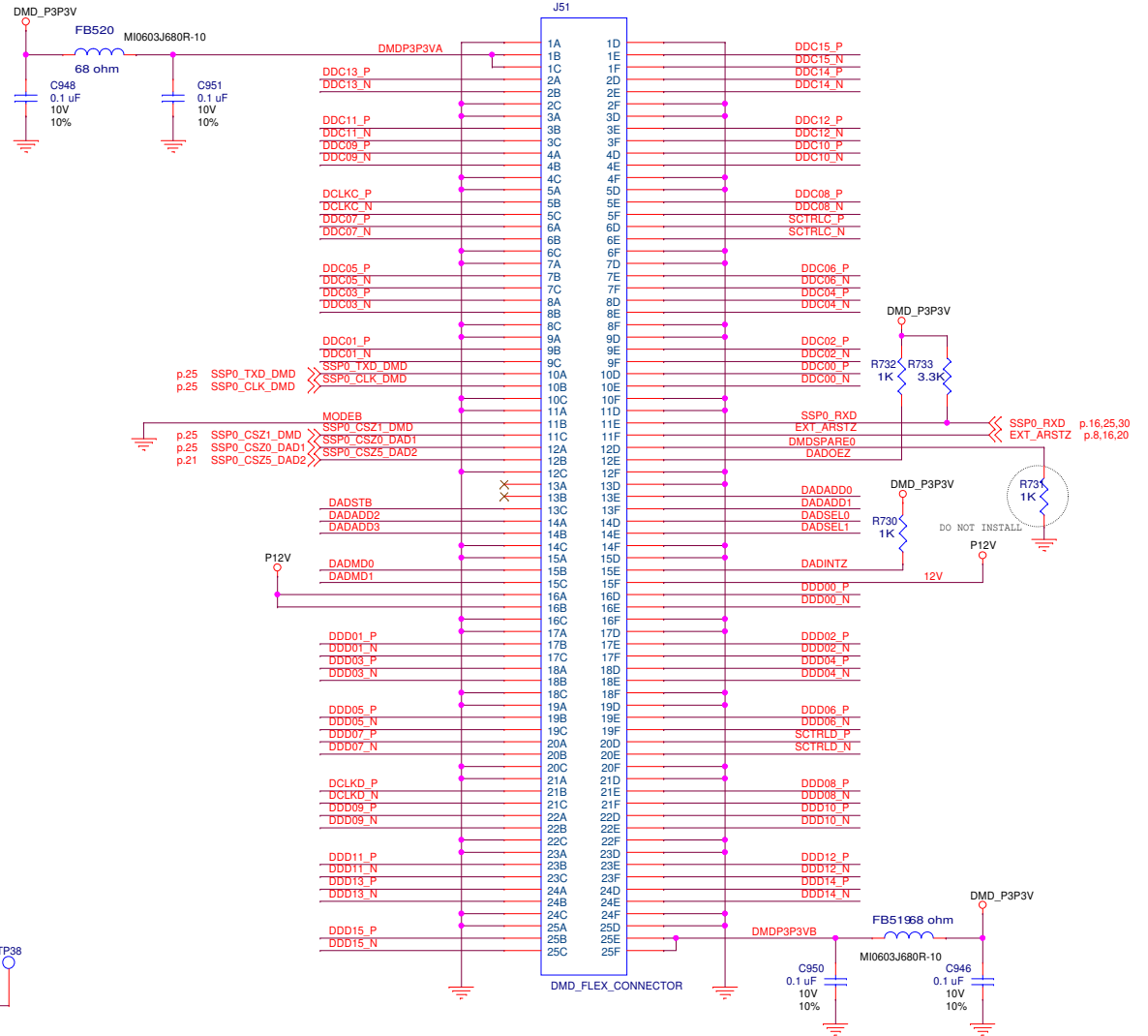
- DDB\_P\_15 N1 DDC00\_P
- DDB\_N\_15 N2 DDC00\_N
- DDB\_P\_14 N3 DDC01\_P
- DDB\_N\_14 N4 DDC01\_N
- DDB\_P\_13 M2 DDC02\_P
- DDB\_N\_13 M1 DDC02\_N
- DDB\_P\_12 N3 DDC03\_P
- DDB\_N\_12 M4 DDC03\_N
- DDB\_P\_11 L1 DDC04\_P
- DDB\_N\_11 L2 DDC04\_N
- DDB\_P\_10 L3 DDC05\_P
- DDB\_N\_10 L4 DDC05\_N
- DDB\_P\_9 K1 DDC06\_P
- DDB\_N\_9 K2 DDC06\_N
- DDB\_P\_8 K3 DDC07\_P
- DDB\_N\_8 K4 DDC07\_N
- DDB\_P\_7 H1 DDC08\_P
- DDB\_N\_7 H2 DDC08\_N
- DDB\_P\_6 H3 DDC09\_P
- DDB\_N\_6 H4 DDC09\_N
- DDB\_P\_5 G1 DDC10\_P
- DDB\_N\_5 G2 DDC10\_N
- DDB\_P\_4 G3 DDC11\_P
- DDB\_N\_4 G4 DDC11\_N
- DDB\_P\_3 F1 DDC12\_P
- DDB\_N\_3 F2 DDC12\_N
- DDB\_P\_2 F3 DDC13\_P
- DDB\_N\_2 F4 DDC13\_N
- DDB\_P\_1 E1 DDC14\_P
- DDB\_N\_1 E2 DDC14\_N
- DDB\_P\_0 D1 DDC15\_P
- DDB\_N\_0 D2 DDC15\_N

- DDA\_P\_15 P4 DDD00\_P
- DDA\_N\_15 P3 DDD00\_N
- DDA\_P\_14 P1 DDD01\_P
- DDA\_N\_14 R4 DDD02\_P
- DDA\_P\_13 R3 DDD02\_N
- DDA\_N\_13 R2 DDD03\_P
- DDA\_P\_12 R1 DDD03\_N
- DDA\_N\_12 T4 DDD04\_P
- DDA\_P\_11 T3 DDD04\_N
- DDA\_N\_11 T2 DDD05\_P
- DDA\_P\_10 T1 DDD05\_N
- DDA\_N\_10 U4 DDD06\_P
- DDA\_P\_9 U3 DDD06\_N
- DDA\_N\_9 U2 DDD07\_P
- DDA\_P\_8 U1 DDD07\_N
- DDA\_N\_8 W4 DDD08\_P
- DDA\_P\_7 W3 DDD08\_N
- DDA\_N\_7 W2 DDD09\_P
- DDA\_P\_6 W1 DDD09\_N
- DDA\_N\_6 Y2 DDD10\_P
- DDA\_P\_5 Y1 DDD10\_N
- DDA\_N\_5 Y4 DDD11\_P
- DDA\_P\_4 Y3 DDD11\_N
- DDA\_N\_4 AA2 DDD12\_P
- DDA\_P\_3 AA1 DDD12\_N
- DDA\_N\_3 AA4 DDD13\_P
- DDA\_P\_2 AA3 DDD13\_N
- DDA\_N\_2 AB2 DDD14\_P
- DDA\_P\_1 AB1 DDD14\_N
- DDA\_N\_0 AC2 DDD15\_P
- DDA\_P\_0 AC1 DDD15\_N

- DCKB\_P J3 DCLK\_P
- DCKB\_N J4 DCLK\_N
- DCKA\_P V3 DCLKD\_P
- DCKA\_N J1 SCTRLC\_P
- SCB\_P J2 SCTRLC\_N
- SCB\_N V2 SCTRLD\_P
- SCA\_P V1 SCTRLD\_N
- SCA\_N

- DADADDR\_0 AB8 DA0 R689 22 DADADD0
- DADADDR\_1 AF4 DA1 R153 22 DADADD1
- DADADDR\_2 AE5 DA2 R151 22 DADADD2
- DADADDR\_3 AD6 DA3 R761 22 DADADD3
- DADMODE\_0 AE6 DM0 R148 22 DADMD0
- DADMODE\_1 AD7 DM1 R899 22 DADMD1
- DADSEL\_0 AC7 DS0 R700 22 DADSELO
- DADSEL\_1 AE4 DS1 R156 22 DADSEL1
- DADSTRB AE5 DSTB R150 22 DADSTRB
- DADDOEZ AE7 DOEZ R698 22 DADDOEZ
- DADINTZ AC8 DINTZ R686 22 DADINTZ

DLPC4422 Master



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Master DLPC4422 DMD Flex Interface

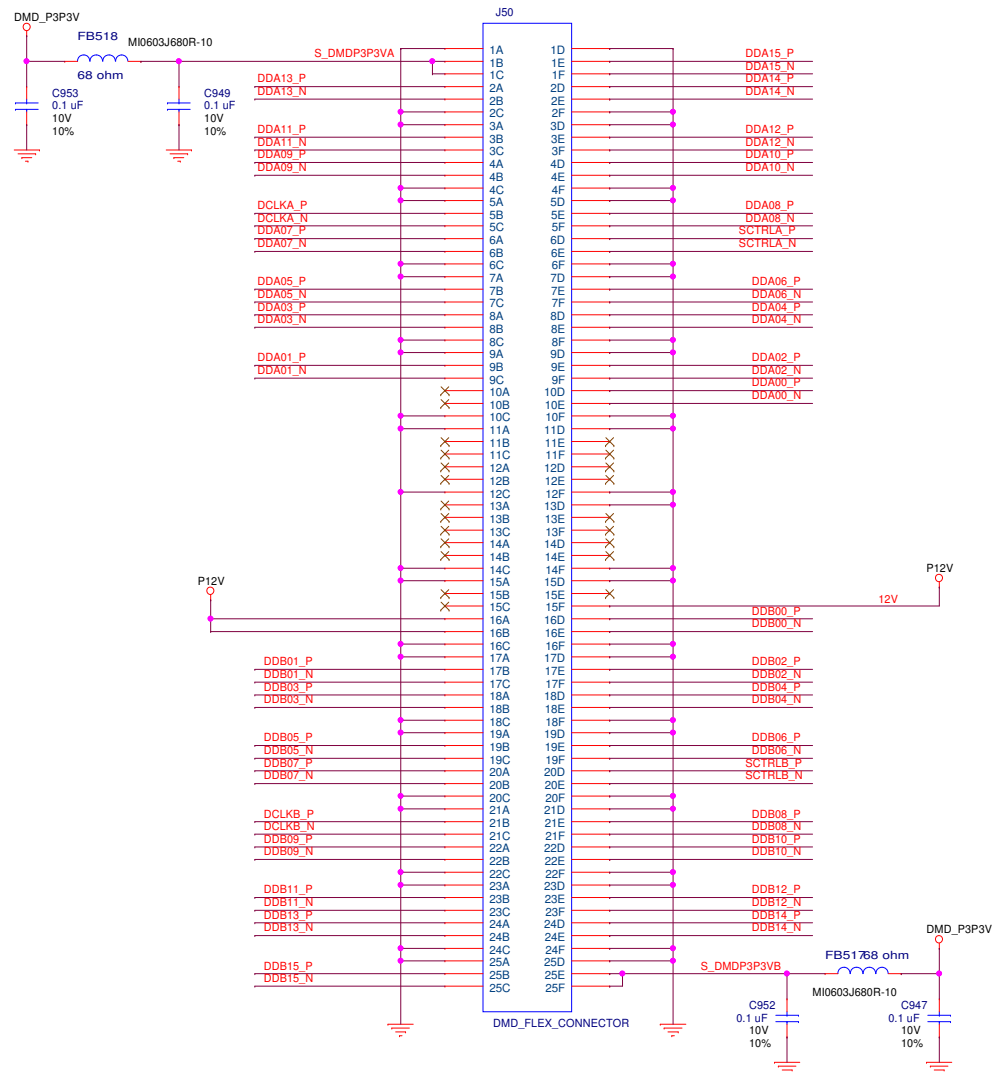
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	ISSUE DATE 1/31/2017	SCALE		SHEET 14 OF 34	

U32B

- N1 DDA00\_P
- N2 DDA00\_N
- N3 DDA01\_P
- N4 DDA01\_N
- M2 DDA02\_P
- M1 DDA02\_N
- M3 DDA03\_P
- M4 DDA03\_N
- L1 DDA04\_P
- L2 DDA04\_N
- L3 DDA05\_P
- L4 DDA05\_N
- K1 DDA06\_P
- K2 DDA06\_N
- K3 DDA07\_P
- K4 DDA07\_N
- H1 DDA08\_P
- H2 DDA08\_N
- H3 DDA09\_P
- H4 DDA09\_N
- G1 DDA10\_P
- G2 DDA10\_N
- G3 DDA11\_P
- G4 DDA11\_N
- F1 DDA12\_P
- F2 DDA12\_N
- F3 DDA13\_P
- F4 DDA13\_N
- E1 DDA14\_P
- E2 DDA14\_N
- D1 DDA15\_P
- D2 DDA15\_N
- P4 DDB00\_P
- P3 DDB00\_N
- P2 DDB01\_P
- P1 DDB01\_N
- R4 DDB02\_P
- R3 DDB02\_N
- R2 DDB03\_P
- R1 DDB03\_N
- Y4 DDB04\_P
- Y3 DDB04\_N
- T3 DDB05\_P
- T2 DDB05\_N
- U4 DDB06\_P
- U3 DDB06\_N
- U2 DDB07\_P
- U1 DDB07\_N
- W4 DDB08\_P
- W3 DDB08\_N
- W2 DDB09\_P
- W1 DDB09\_N
- Y2 DDB10\_P
- Y1 DDB10\_N
- Y4 DDB11\_P
- Y3 DDB11\_N
- AA2 DDB12\_P
- AA1 DDB12\_N
- AA4 DDB13\_P
- AA3 DDB13\_N
- AB2 DDB14\_P
- AB1 DDB14\_N
- AC2 DDB15\_P
- AC1 DDB15\_N
- J3 DCLKA\_P
- J4 DCLKA\_N
- V4 DCLKB\_P
- V3 DCLKB\_N
- J1 SCTRLA\_P
- J2 SCTRLA\_N
- V2 SCTRLB\_P
- V1 SCTRLB\_N
- AB8
- AF4
- AE5
- AD6
- AE6
- AD7
- AC7
- AE4
- AE5
- AE7
- AC8

DMD INTERFACE

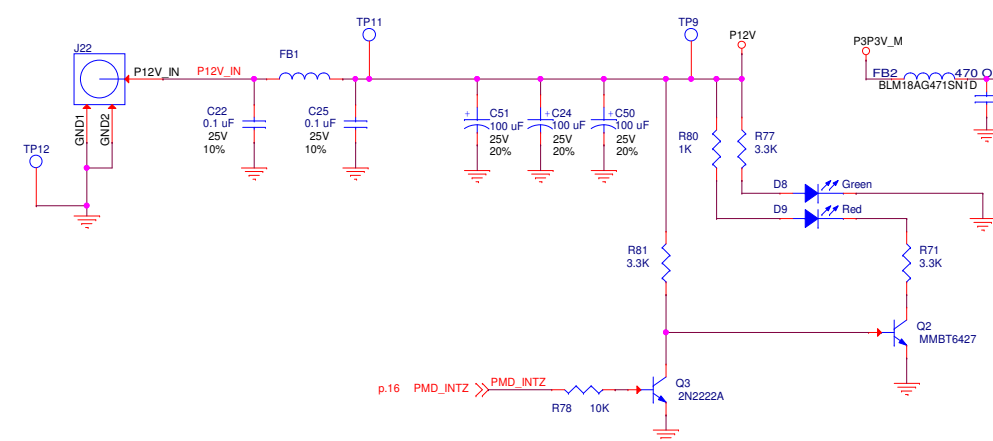
DLPC4422 Slave



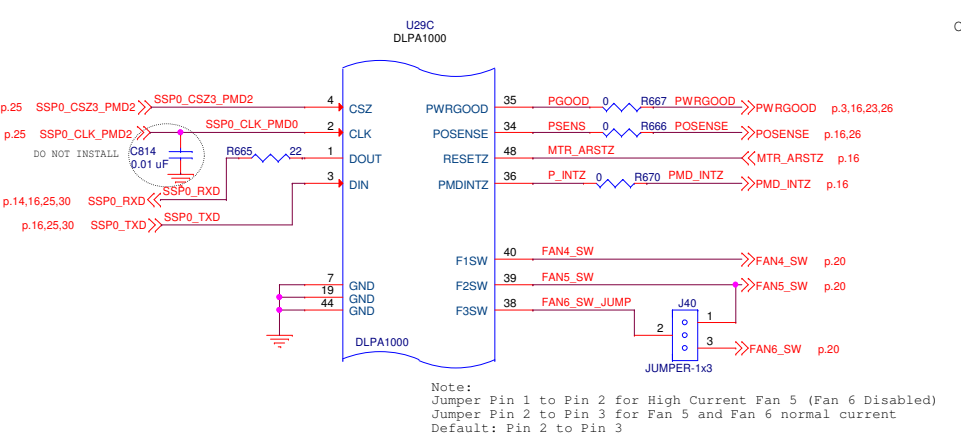
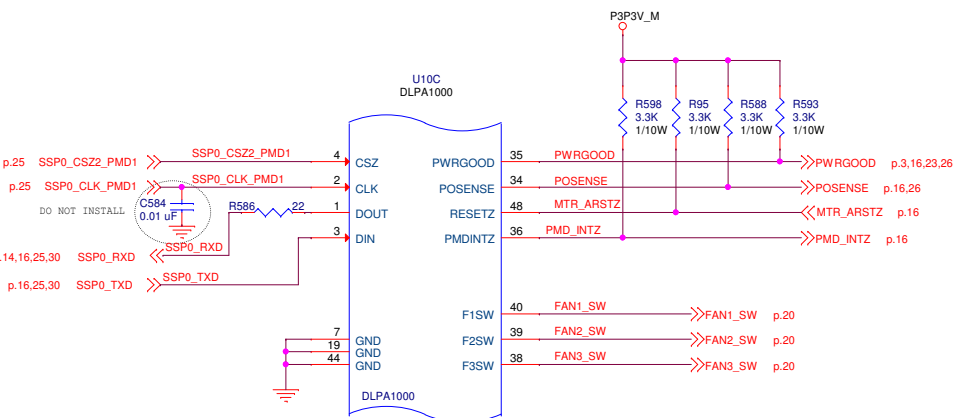
Slave DLPC4422 DMD Flex Interface

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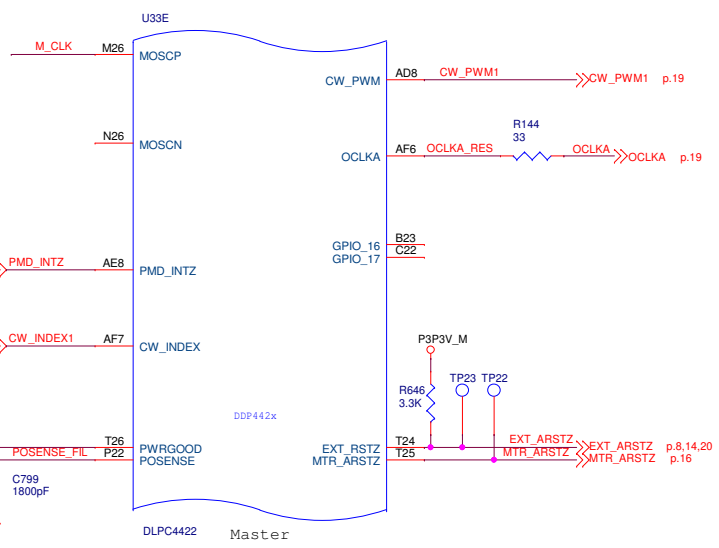
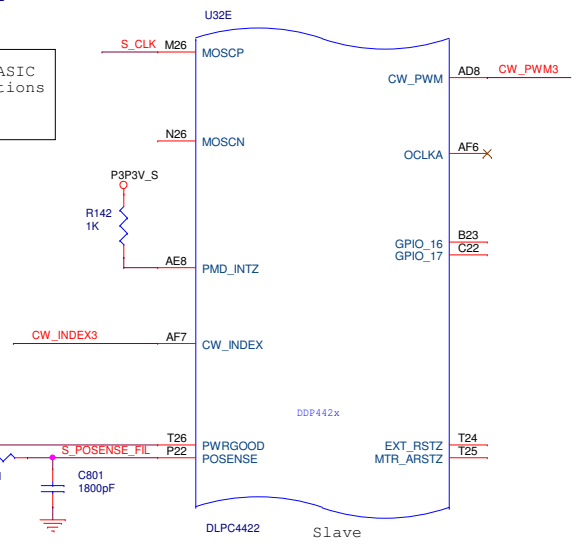
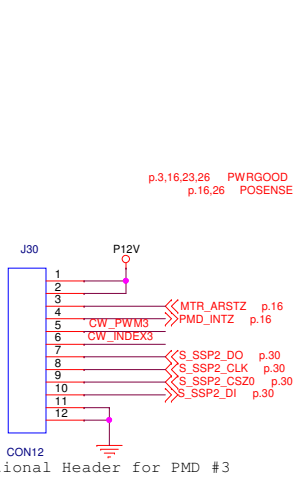
<b>TEXAS INSTRUMENTS</b>	DWN Ben Uihing	DATE 9/30/2016	<b>A3</b>	DRAWING NO <b>2514423</b>	REV <b>E</b>
	ISSUE DATE 1/31/2017	SCALE			



Note: See ASIC datasheet for Dual ASIC oscillator requirements on applications using DynamicBlack or BrightSync



Note:  
 Jumper Pin 1 to Pin 2 for High Current Fan 5 (Fan 6 Disabled)  
 Jumper Pin 2 to Pin 3 for Fan 5 and Fan 6 normal current  
 Default: Pin 2 to Pin 3



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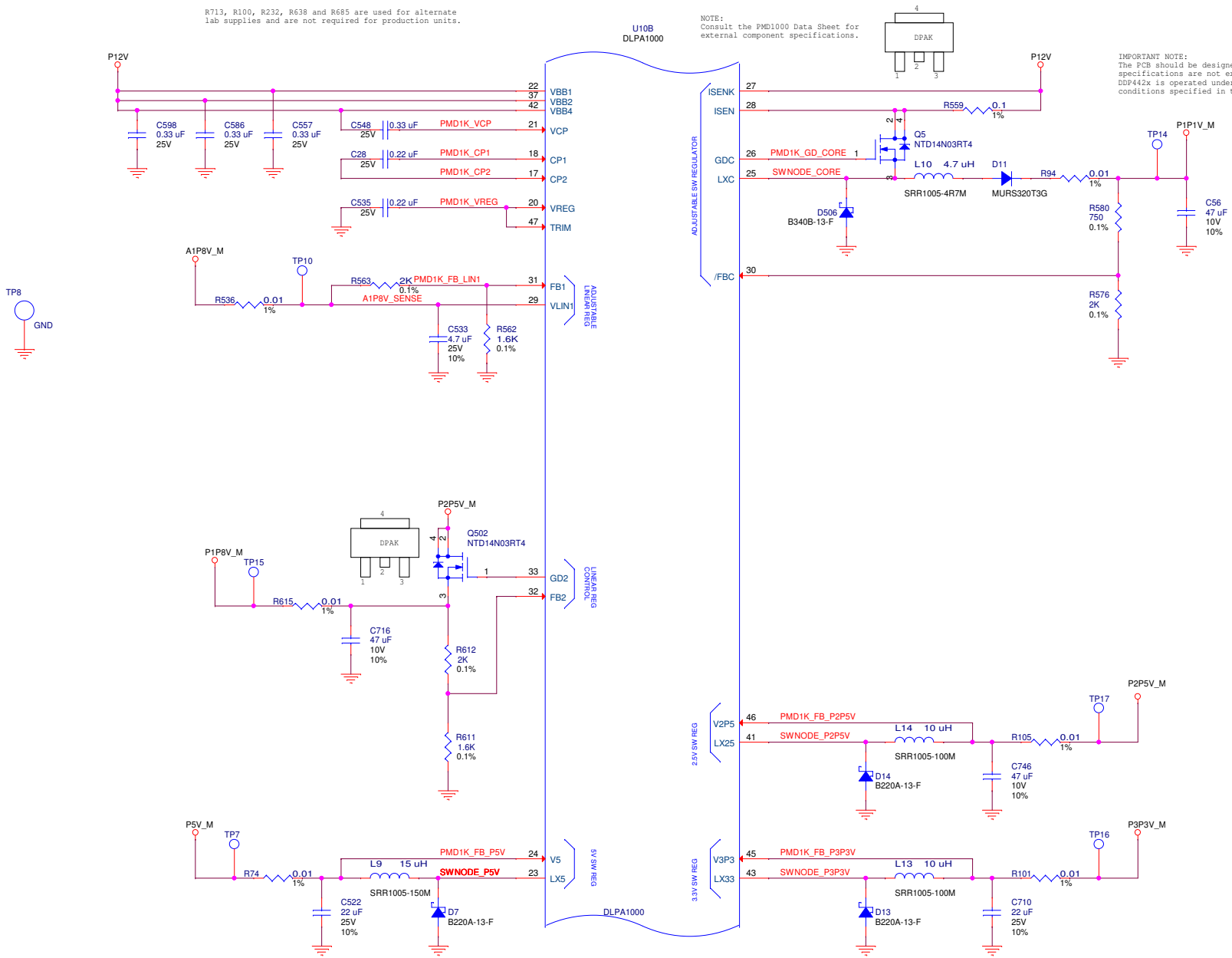
Input Power and PMD1000 / DDP442x Interface



NOTE:  
 R620, R634, R69, R102, R131, R85 are used  
 for current measurement and are not required for  
 production units.  
 R713, R100, R232, R638 and R685 are used for alternate  
 lab supplies and are not required for production units.

NOTE:  
 Consult the PMD1000 Data Sheet for  
 external component specifications.

IMPORTANT NOTE:  
 The PCB should be designed such that the  
 specifications are not exceeded when the  
 DDP442x is operated under the maximum current  
 conditions specified in the DDP442x datasheet.



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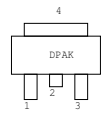
Primary DLPA1000 Power Supplies

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	ISSUE DATE 1/31/2017	SCALE			

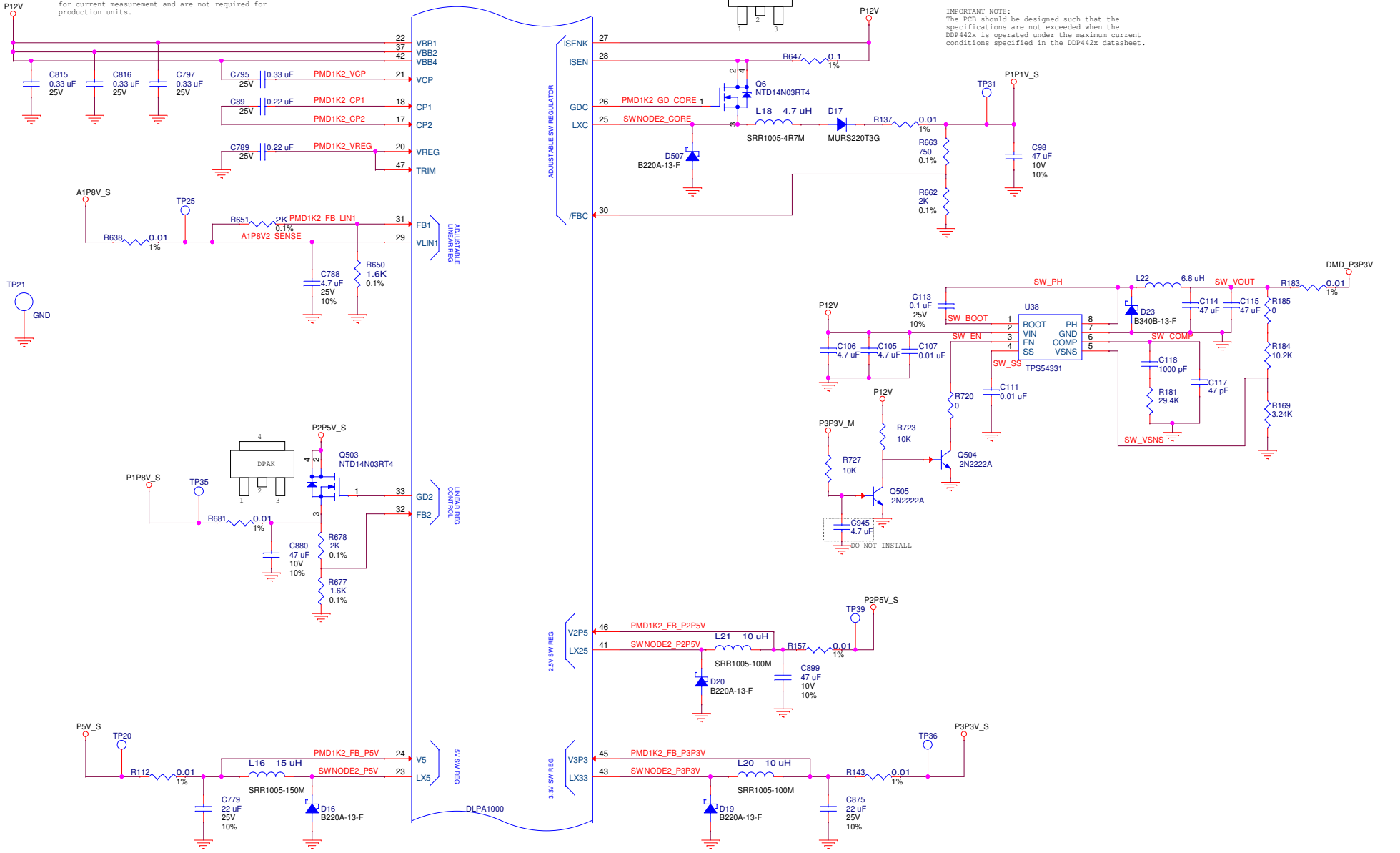
NOTE:  
R587, R525, R46, R576, R14 are used  
for current measurement and are not required for  
production units.

U29B  
DLPA1000

NOTE:  
Consult the PMD1000 Data Sheet for  
external component specifications.



IMPORTANT NOTE:  
The PCB should be designed such that the  
specifications are not exceeded when the  
DDP442x is operated under the maximum current  
conditions specified in the DDP442x datasheet.

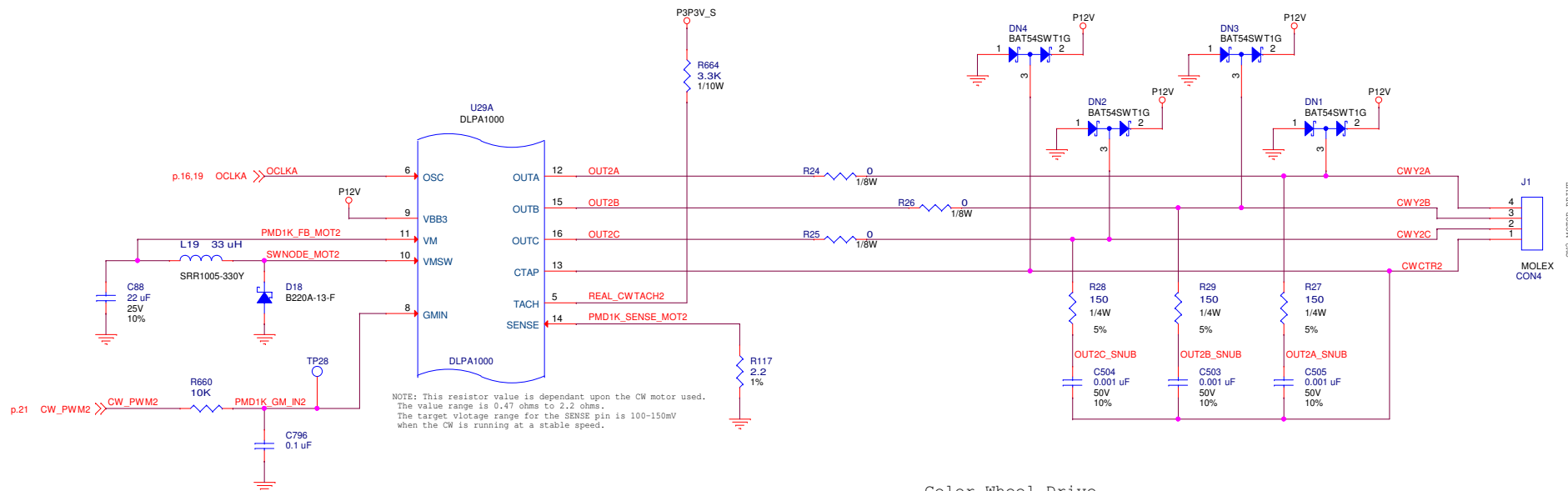
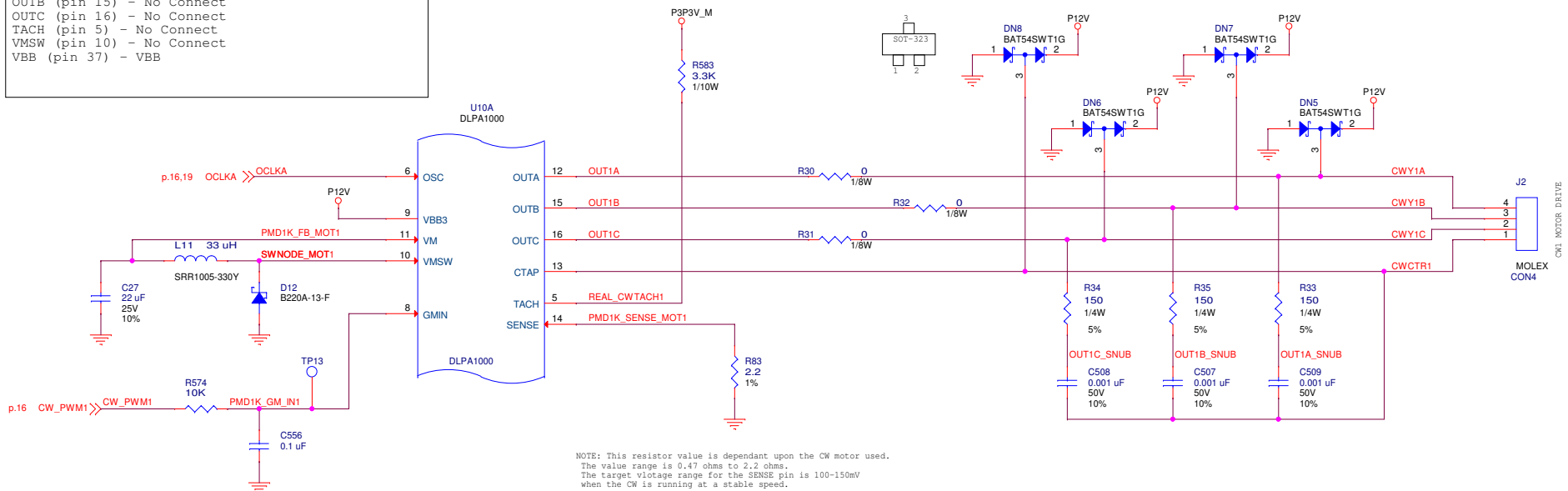


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Secondary DLPA1000 Supplies

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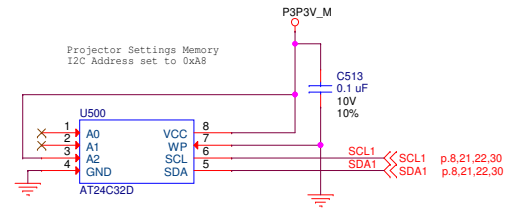
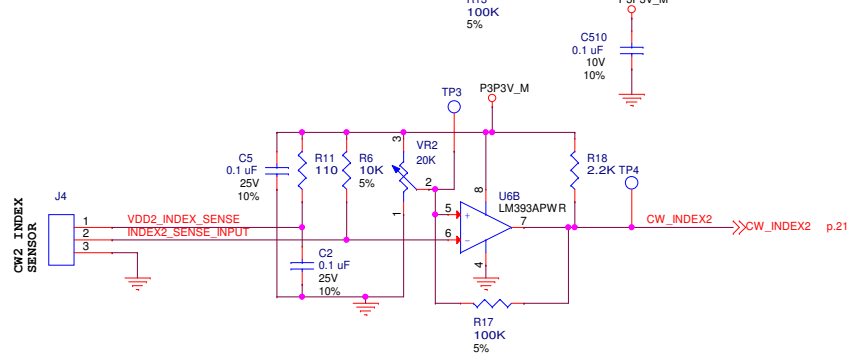
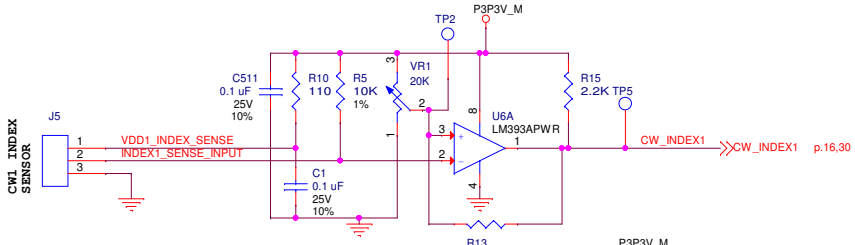
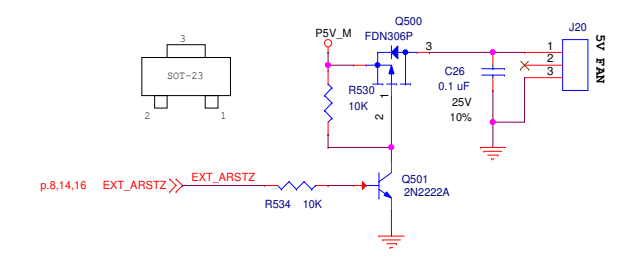
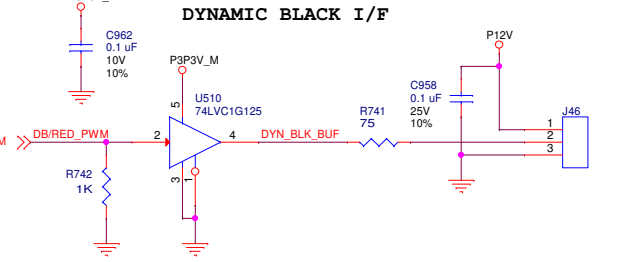
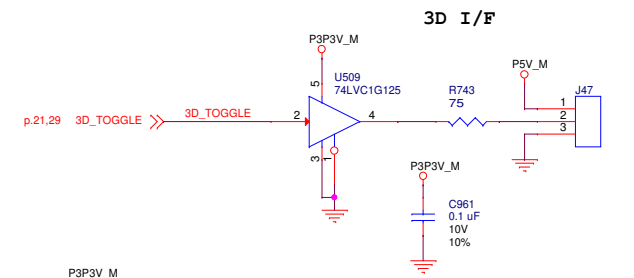
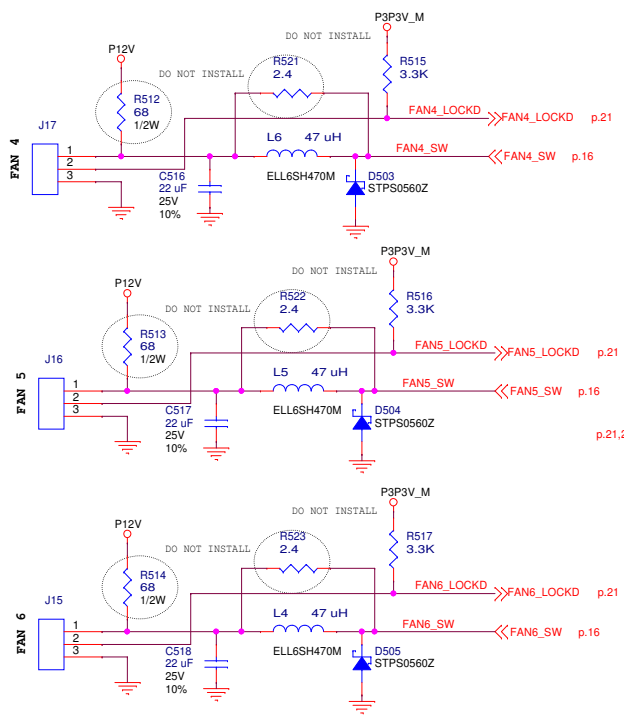
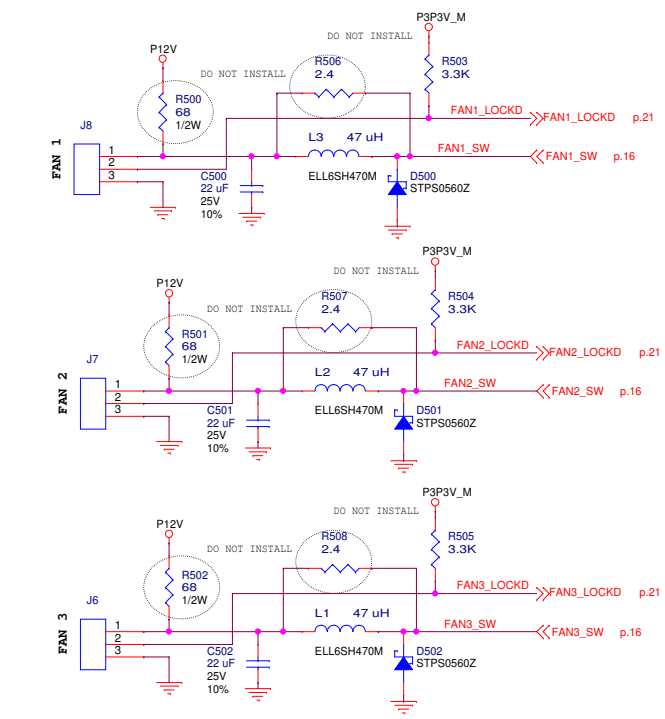
Note: If not using the motor driver on the DLPA1000 follow these guidelines for unused pins:  
 GMIN (pin 8) - Ground  
 OSC (pin 6) - Ground  
 SENSE (pin 14) - Ground  
 CTAP (pin 13) - VBB  
 VM (pin 11) - VBB  
 OUTA (pin 12) - No Connect  
 OUTB (pin 15) - No Connect  
 OUTC (pin 16) - No Connect  
 TACH (pin 5) - No Connect  
 VMSW (pin 10) - No Connect  
 VBB (pin 37) - VBB



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Color Wheel Drive

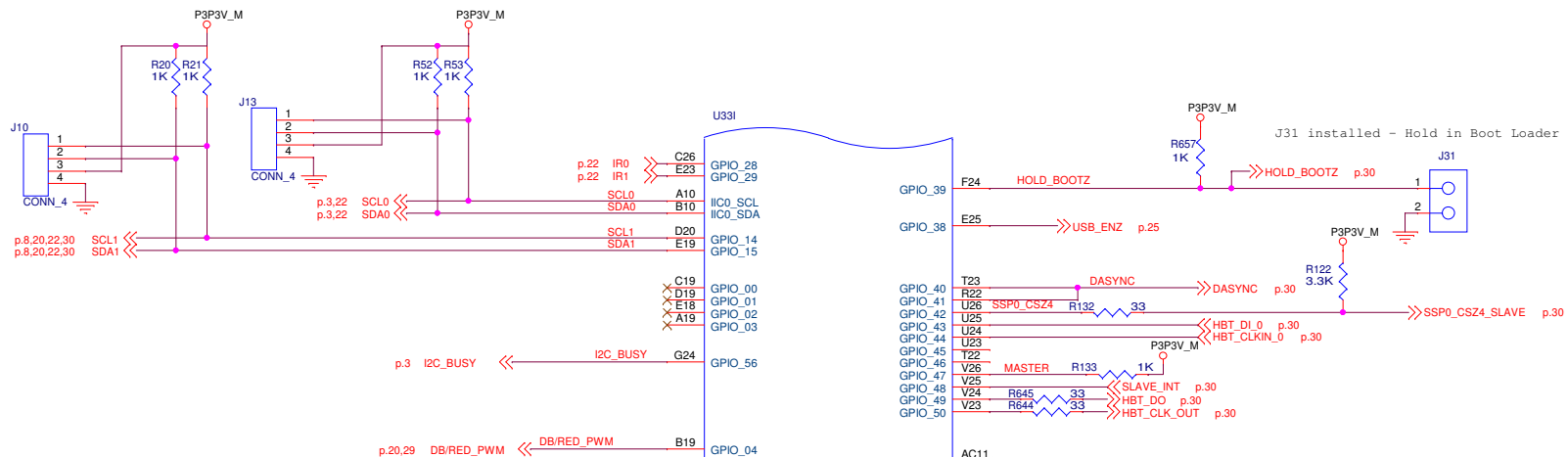
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	ISSUE DATE 1/31/2017	SCALE			



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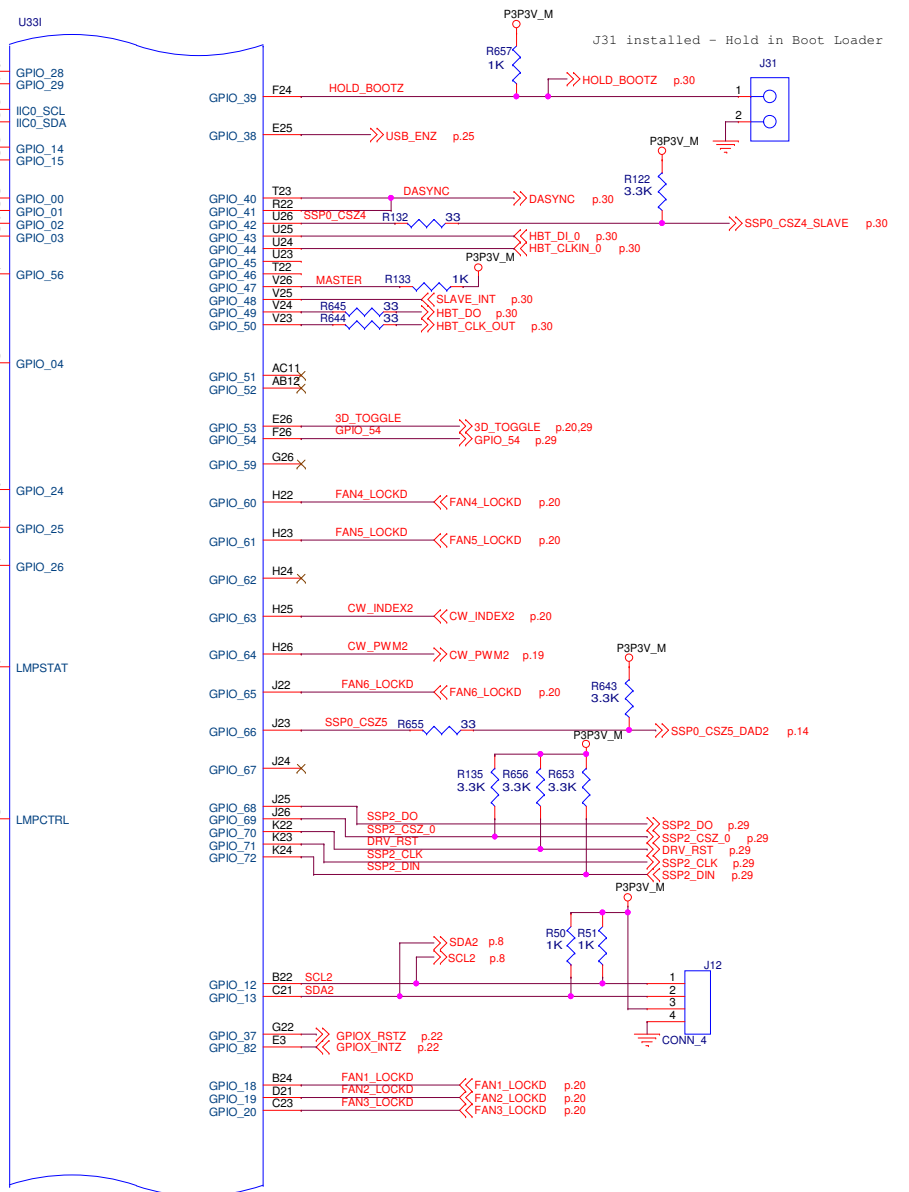
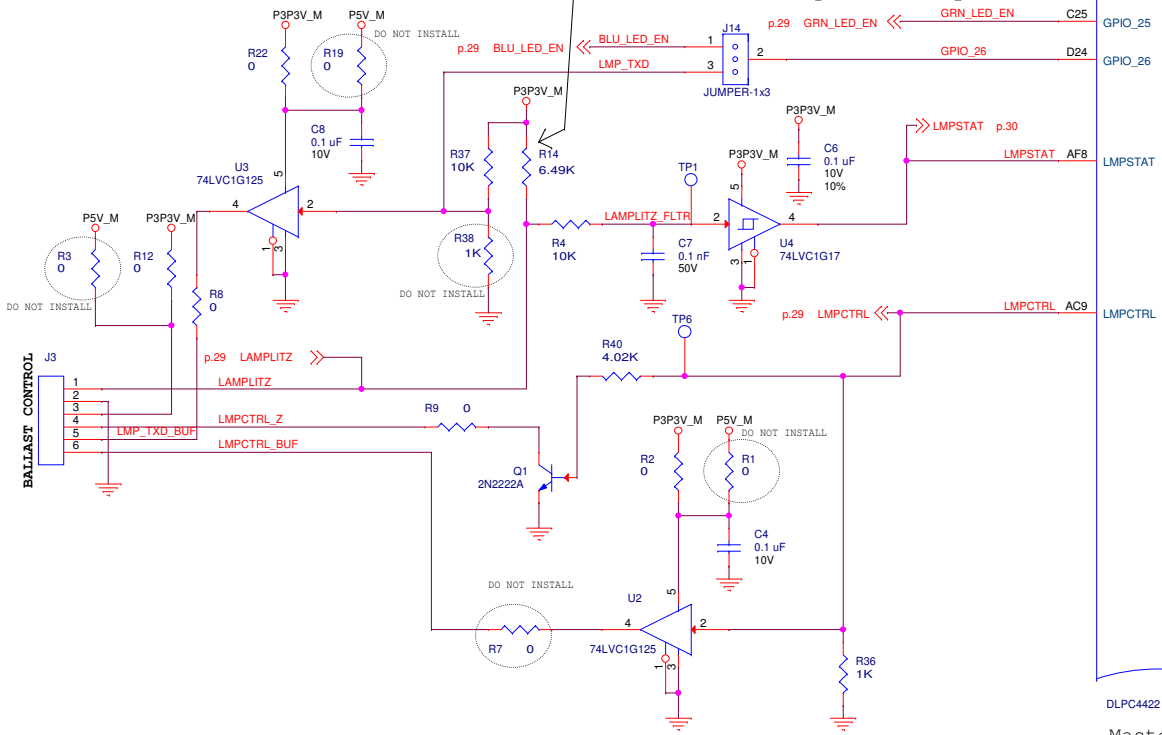
Fan, Color Wheel Interface and Peripherals

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Some ballast may require a different value of R14 for robust communication. Some ballast may require a value of 1.5k. See ballast data sheet for more information.

Note: GPIO\_25 can be used as LAMP\_SYNC if needed

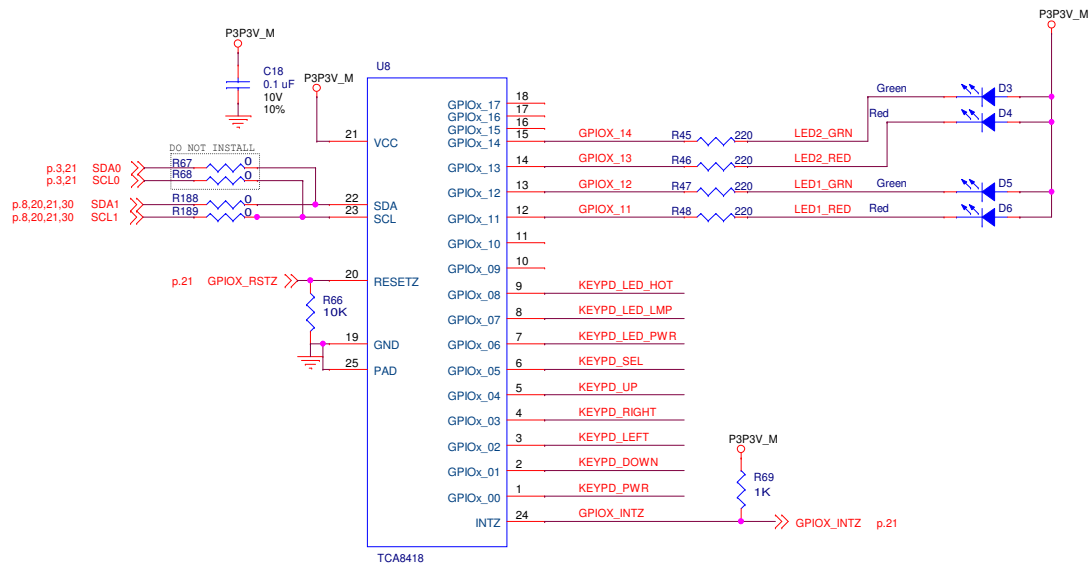


DLPC4422 Master

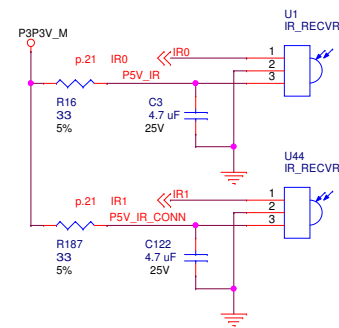
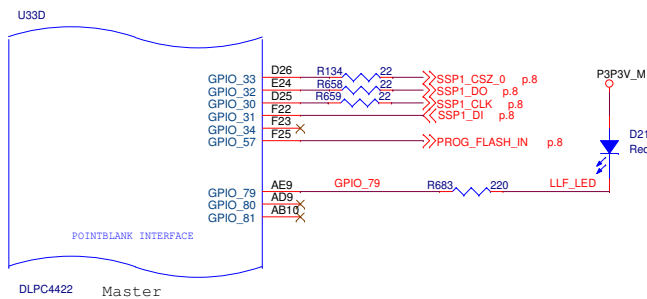
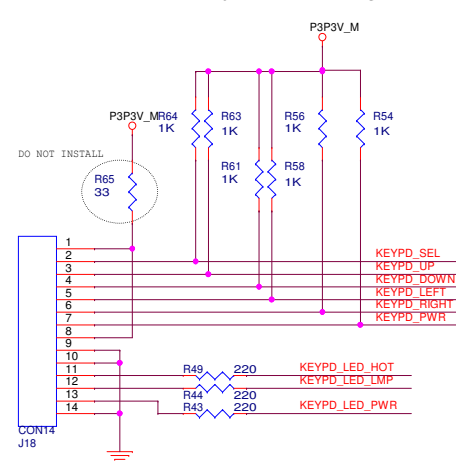
Master ASIC GPIO, I2C, and Ballast Control

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			2514423	E
SCALE		SHEET 21 OF 34		



### KEYBOARD INTERFACE

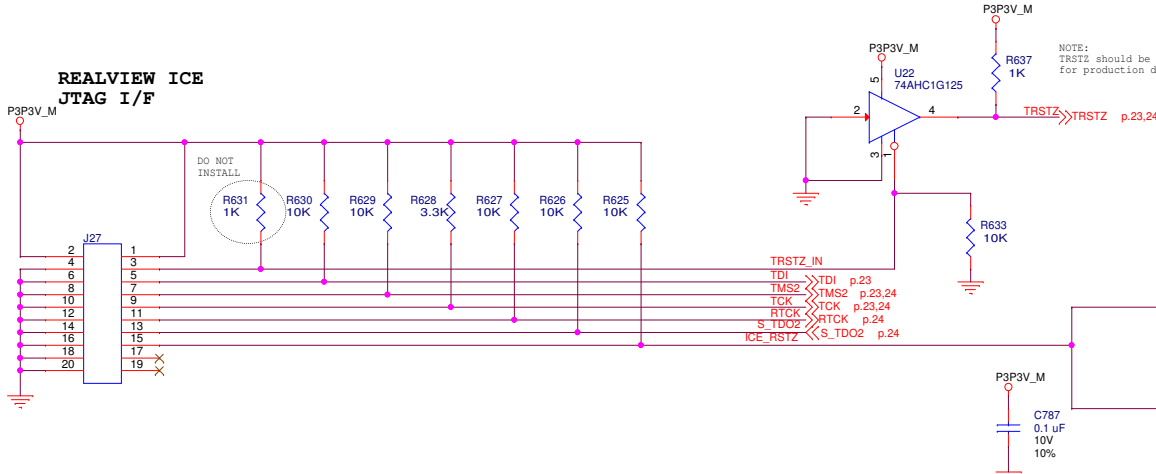


### GPIO Expander, Keypad Interface and IR Interface

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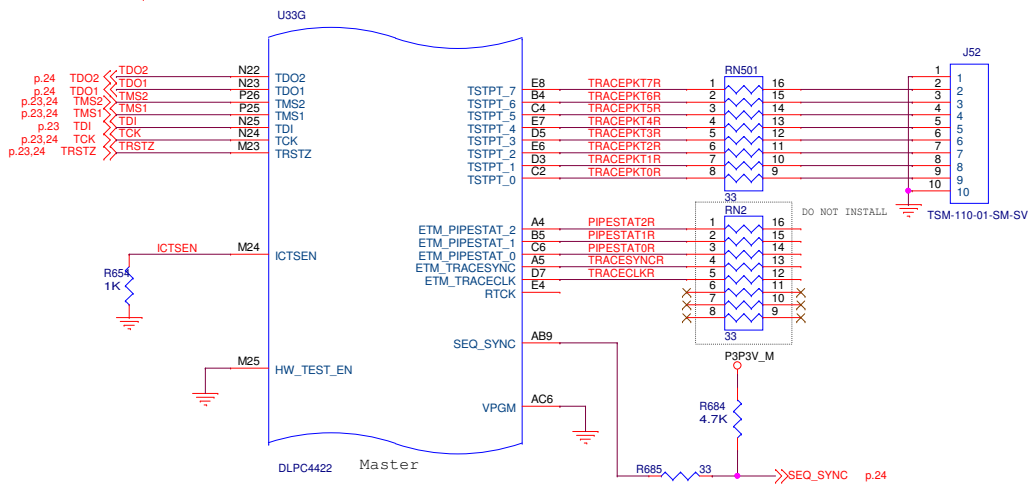
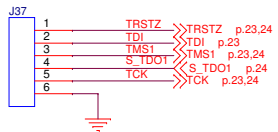
TEXAS INSTRUMENTS	DWN Ben Ulling	DATE 9/30/2016	A3	DRAWING NO 2514423	REV E
	ISSUE DATE 1/31/2017	SCALE			

**REALVIEW ICE  
JTAG I/F**



MANUAL RESET JUMPER	
INSTALLED	HOLD IN RESET
NOT INSTALLED	NORMAL OPERATION (DEFAULT)

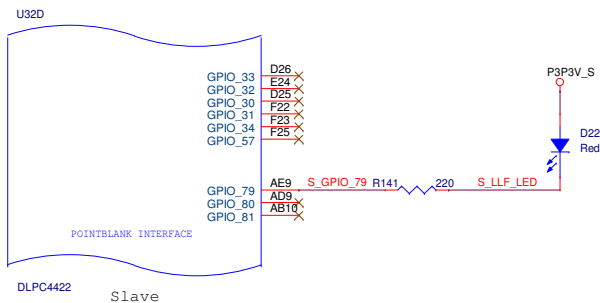
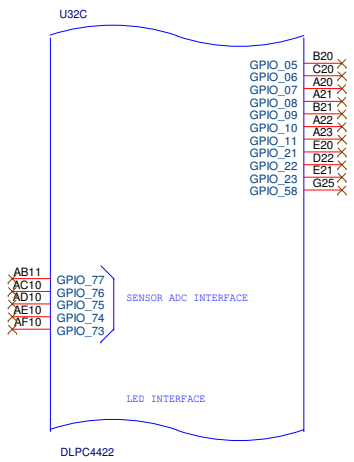
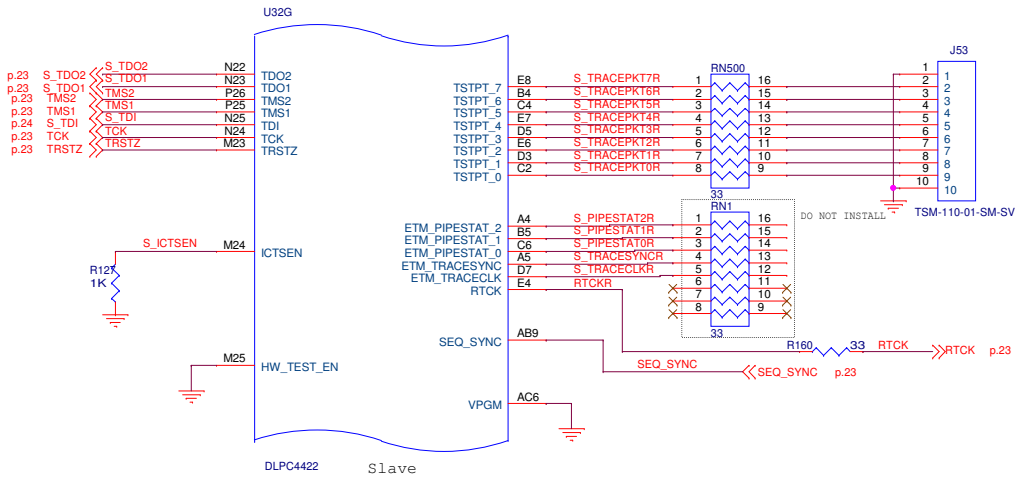
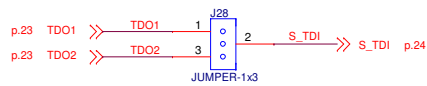
**JTAG BOUNDARY SCAN**



Master ASIC Test Points, ARM Trace, JTAG, and Reset

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	ISSUE DATE 1/31/2017	SCALE		

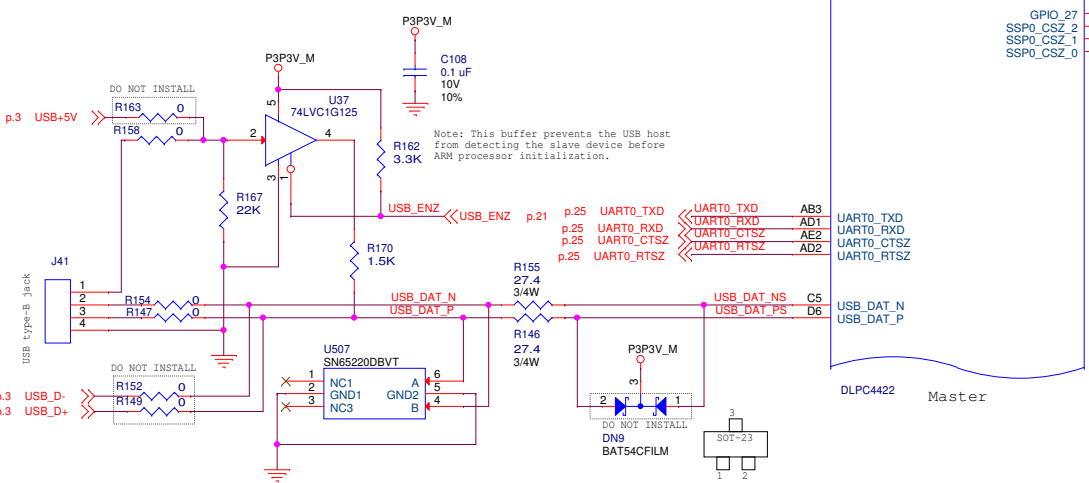
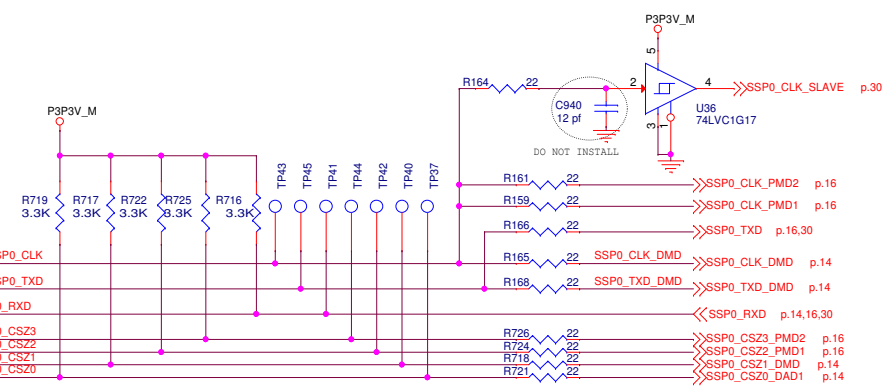
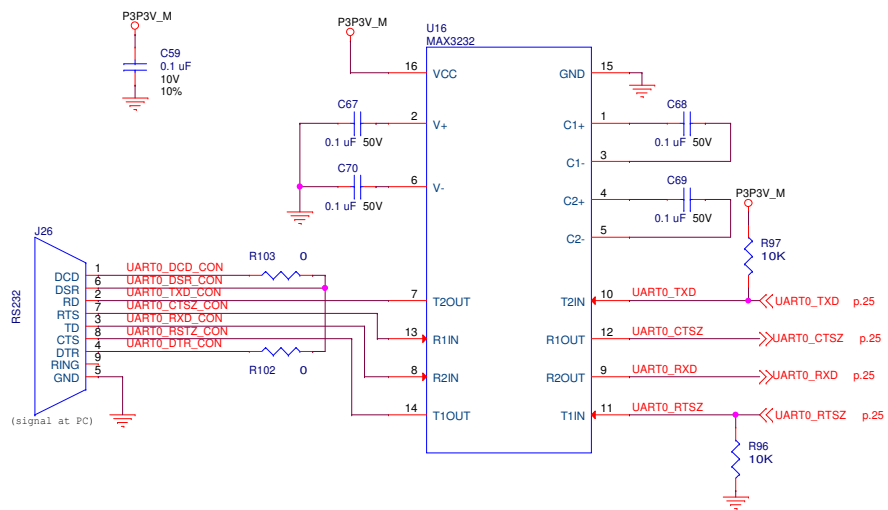


Slave ASIC Test Points, ARM Trace, and JTAG

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	ISSUE DATE 1/31/2017	SCALE		SHEET 24 OF 34	



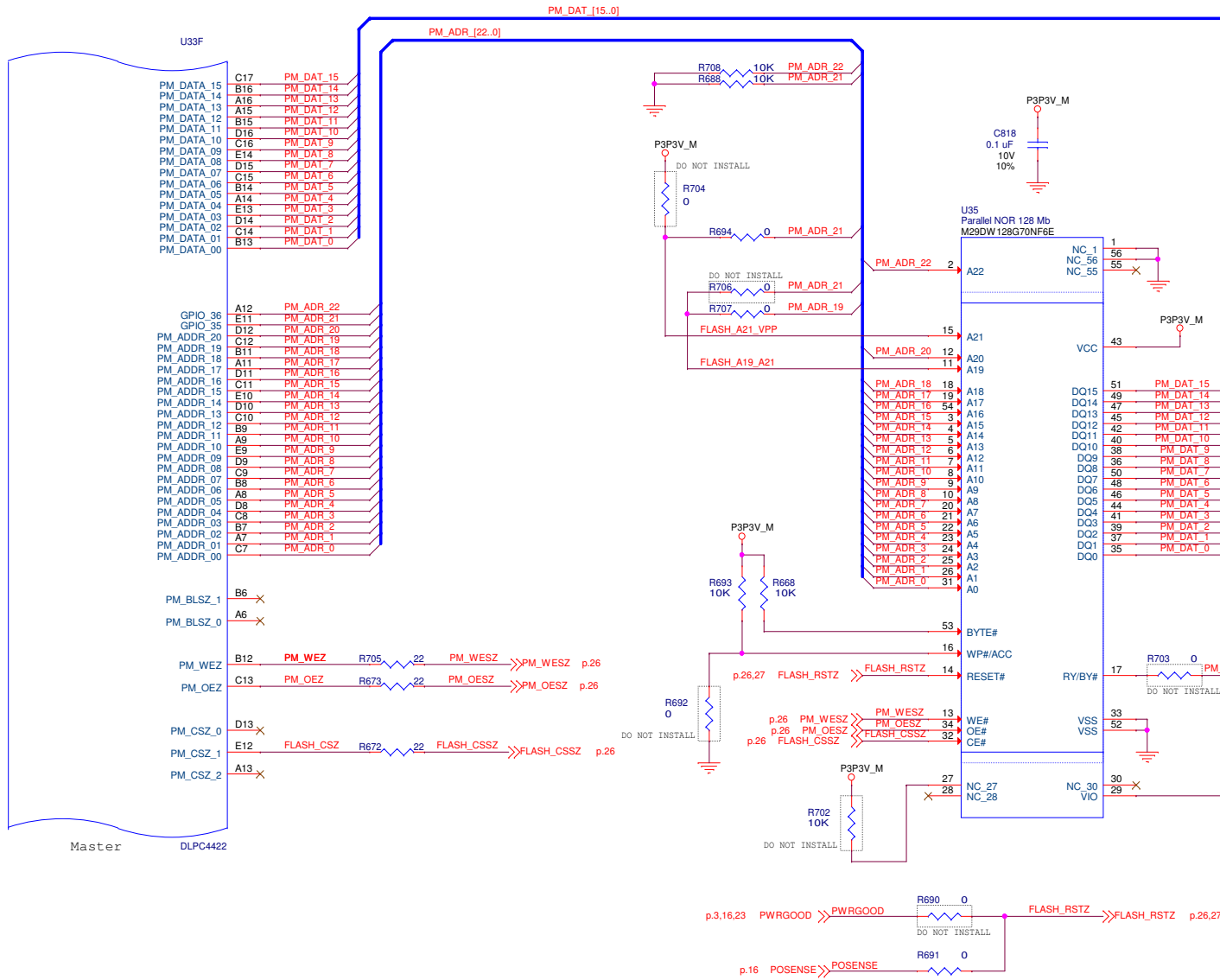


Note: TI recommends signal integrity analysis be performed for the SPI bus to determine the optimum buffering and termination.

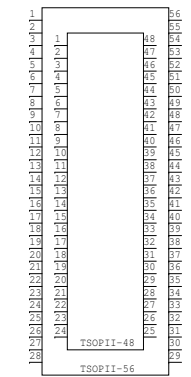
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Master ASIC RS-232, Synchronous Serial Port, and USB

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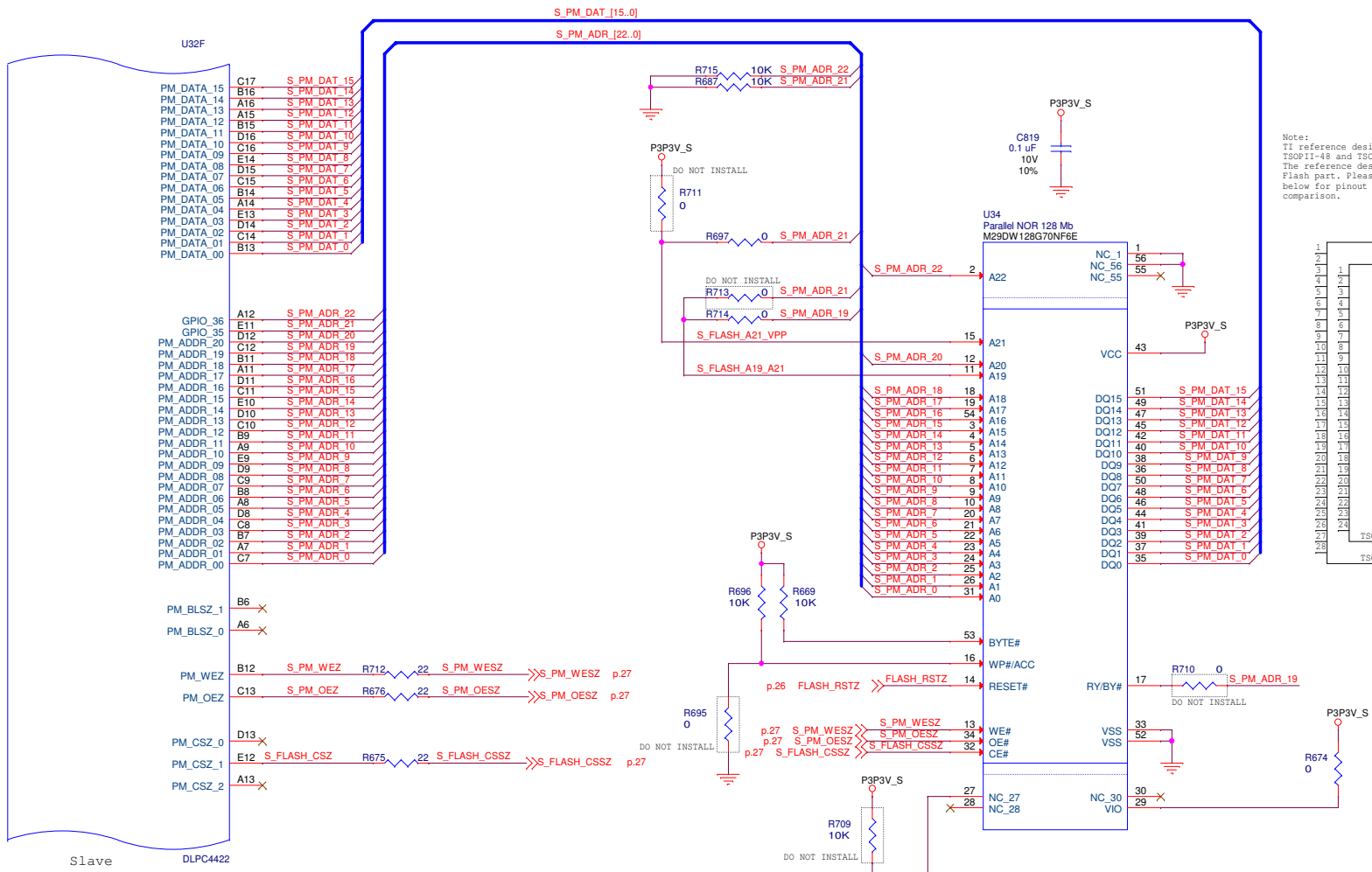
Note:  
 TI reference design supports both  
 TSOP11-48 and TSOP11-56 Flash types.  
 The reference design uses a TSOP11-48  
 Flash part. Please refer to diagram  
 below for pinout and footprint  
 comparison.



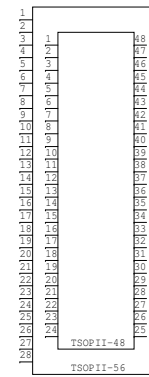
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Master ASIC Flash Memory Interface

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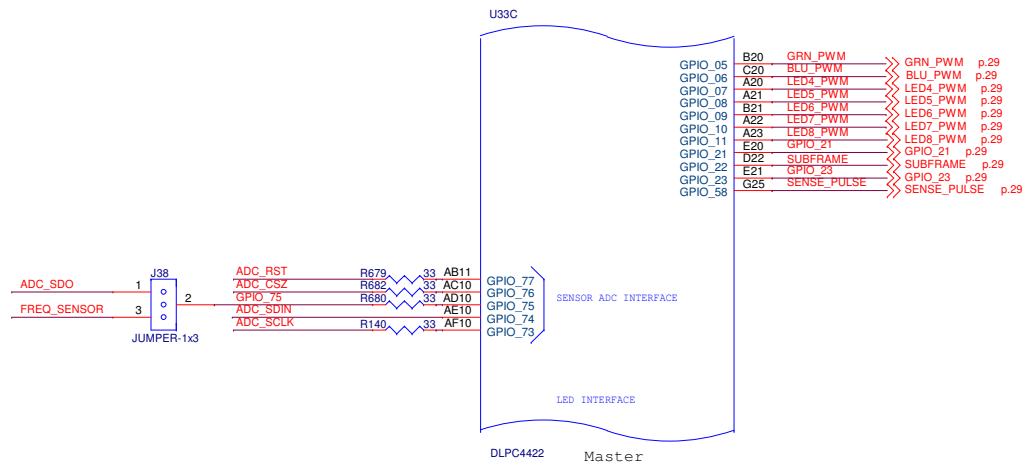


Note:  
 TI reference design supports both  
 TSOP11-48 and TSOP11-56 Flash types.  
 The reference design uses a TSOP11-48  
 Flash part. Please refer to diagram  
 below for pinout and footprint  
 comparison.

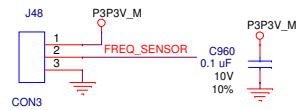


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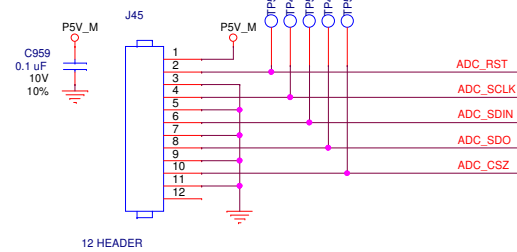
TEXAS INSTRUMENTS		DWN Ben Ulling	DATE 9/30/2016	A3	DRAWING NO 2514423	REV E
		ISSUE DATE 1/31/2017	SCALE			



LIGHT TO FREQUENCY SENSOR I/F



ADC INTEGRATING SENSOR BOARD I/F

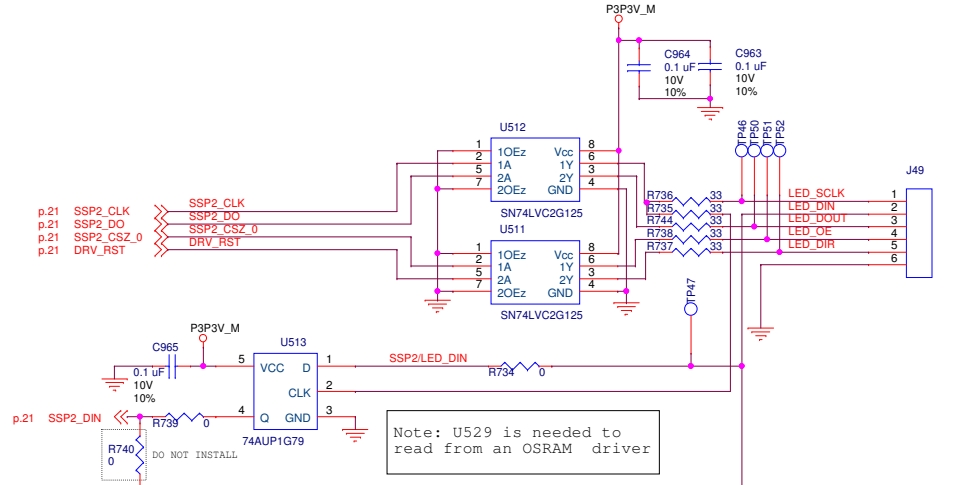
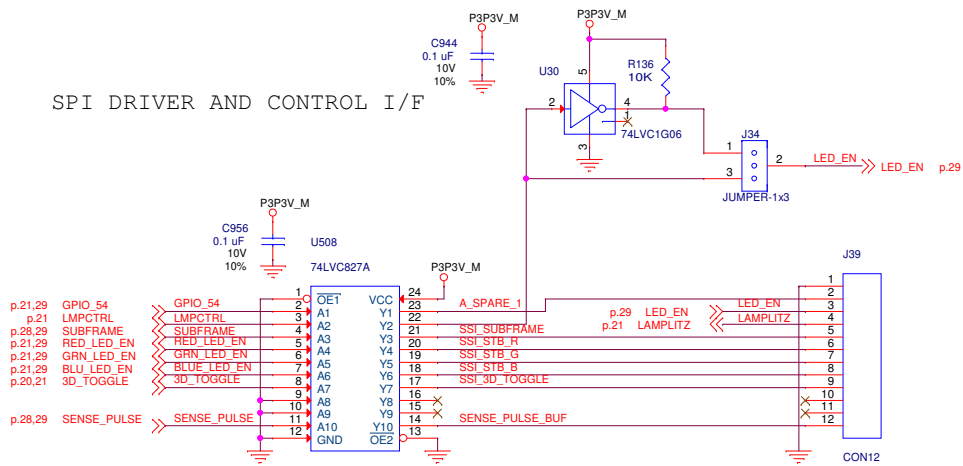


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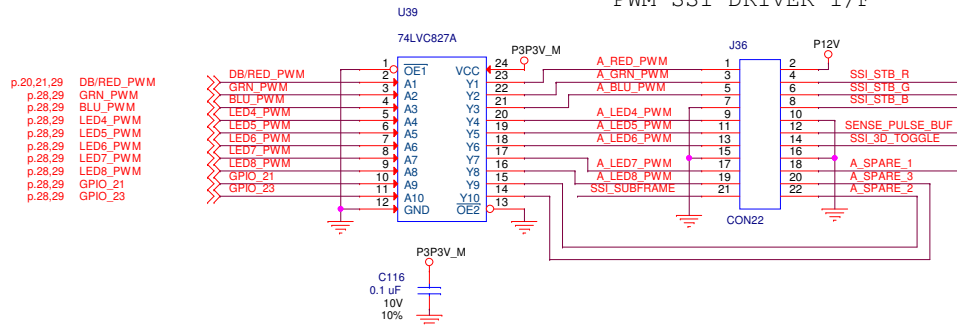
Master ASIC SSI Sensor Interface

TEXAS INSTRUMENTS	DWN Ben Uthing	DATE 9/30/2016	A3	DRAWING NO 2514423	REV E
	ISSUE DATE 1/31/2017	SCALE			

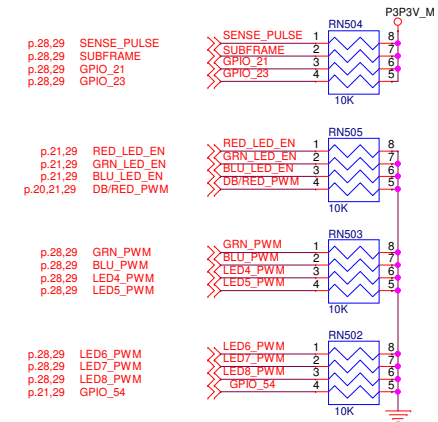
### SPI DRIVER AND CONTROL I/F



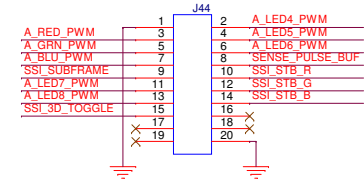
### PWM SSI DRIVER I/F



### PULL-UP/PULL-DOWN RESISTORS



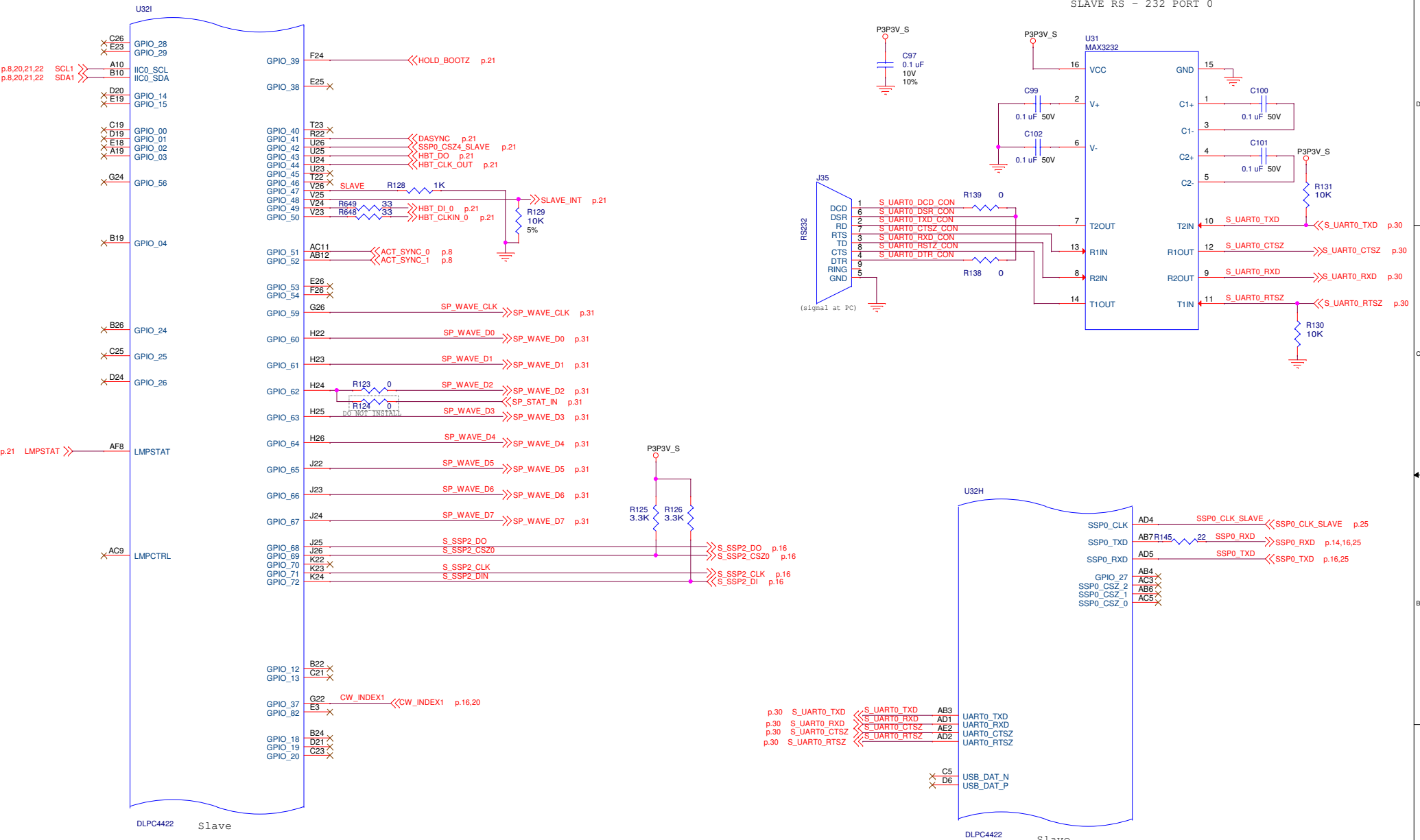
### TESTPOINTS



### SSI Driver Interfaces

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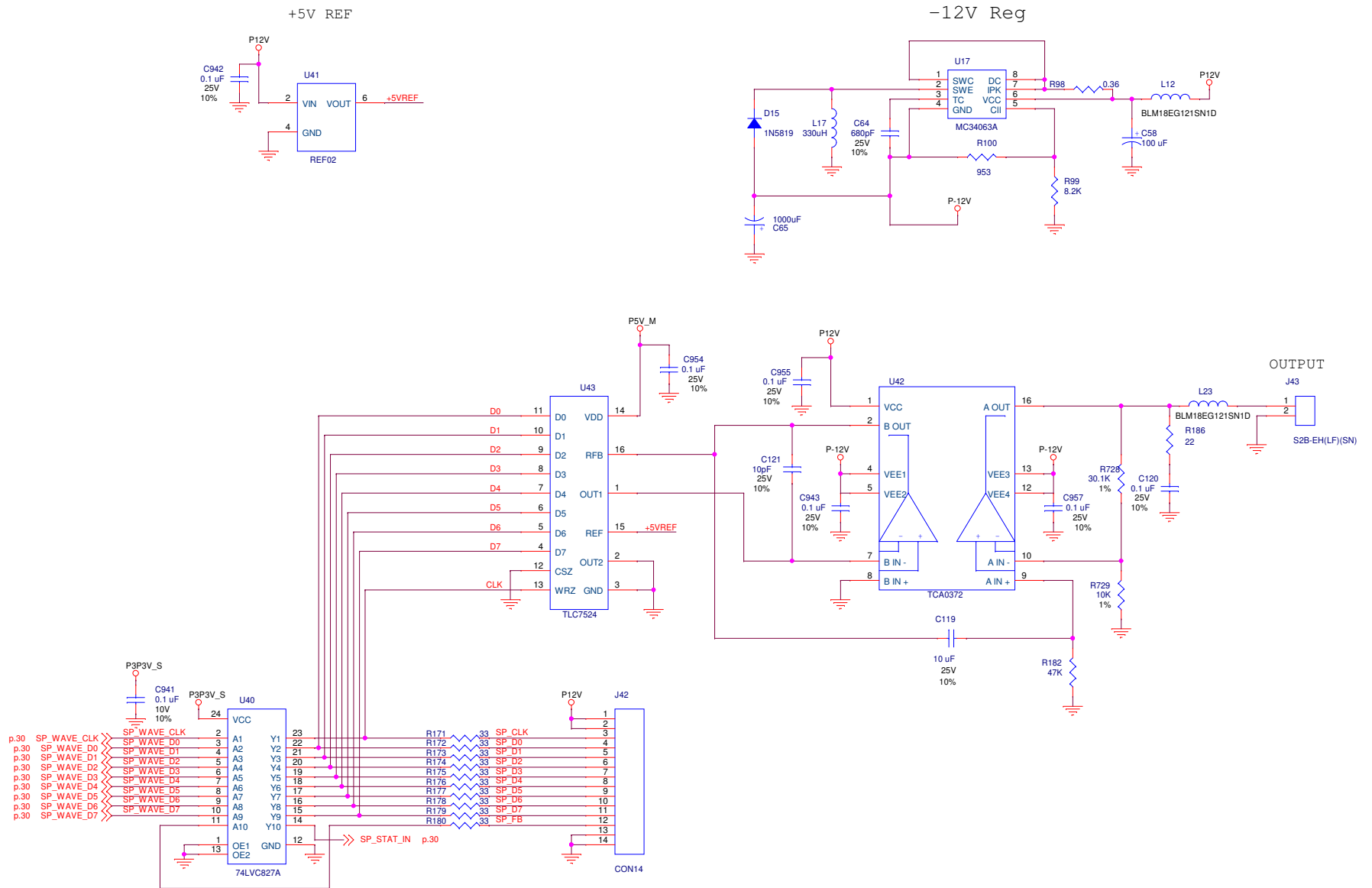
TEXAS INSTRUMENTS	DWN Ben Ulling	DATE 9/30/2016	A3	DRAWING NO 2514423	REV E
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Slave ASIC GPIO and Smooth Picture I/F

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Actuator I/F

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Revision B:

All Pages: Resequenced reference designators to align with layout

Page 1: Updated notes with correct voltage names  
Updated index

Page 4: Rearranged DDR3\_1\_DQ[15:0] for routability

Revision C:

Page 3: Change U5 to Do Not Install  
Updated C545 and C549 as Do Not Install  
Changed U506 to 75 Mhz

Page 11: Added Note Connecting pin 15 of U24 to P3P3V

Page 8: Changed R89, R90, R91, R92, and R541 to 0 ohms.

Revision D:

Page 3: Changed net name TEST\_4A\_AC6 to VX1\_3D\_EN.  
Changed net name TEST\_4A\_AE6 to VX1\_LR\_SYNC.

Page 8: Added R190, R191, R192, and R193.  
Changed net name TEST\_4A\_AC6 to VX1\_3D\_EN.  
Changed net name TEST\_4A\_AE6 to VX1\_LR\_SYNC.

Page 11: Connected pin 15 of U24 to P3P3V.

Page 16: Changed C799 and C801 to 1800pF.

Page 21: Added note to ballast circuit.

Page 22: Added R188 and R189.

Page 23: Changed RN501 to Install, added J52 header.

Page 24: Changed RN500 to Install, added J53 header.

Revision E:

Page 11: Changed U24-10, C85 connection from P3P3V to P5V\_S.

<b>TEXAS INSTRUMENTS</b>	DWN Ben Uting	DATE 9/30/2016	<b>A3</b>	DRAWING NO <b>2514423</b>	REV <b>E</b>
	ISSUE DATE 1/31/2017	SCALE			

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