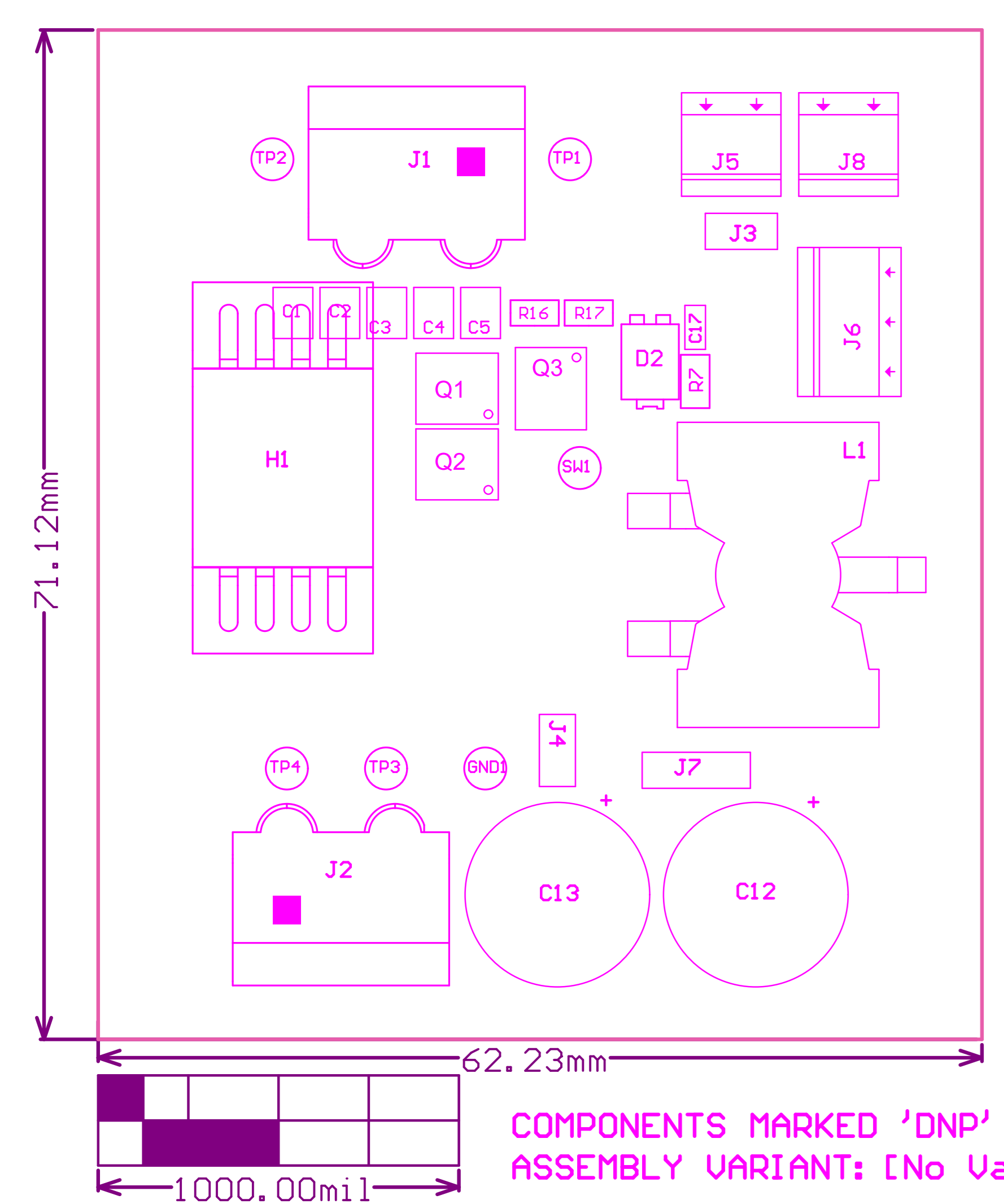
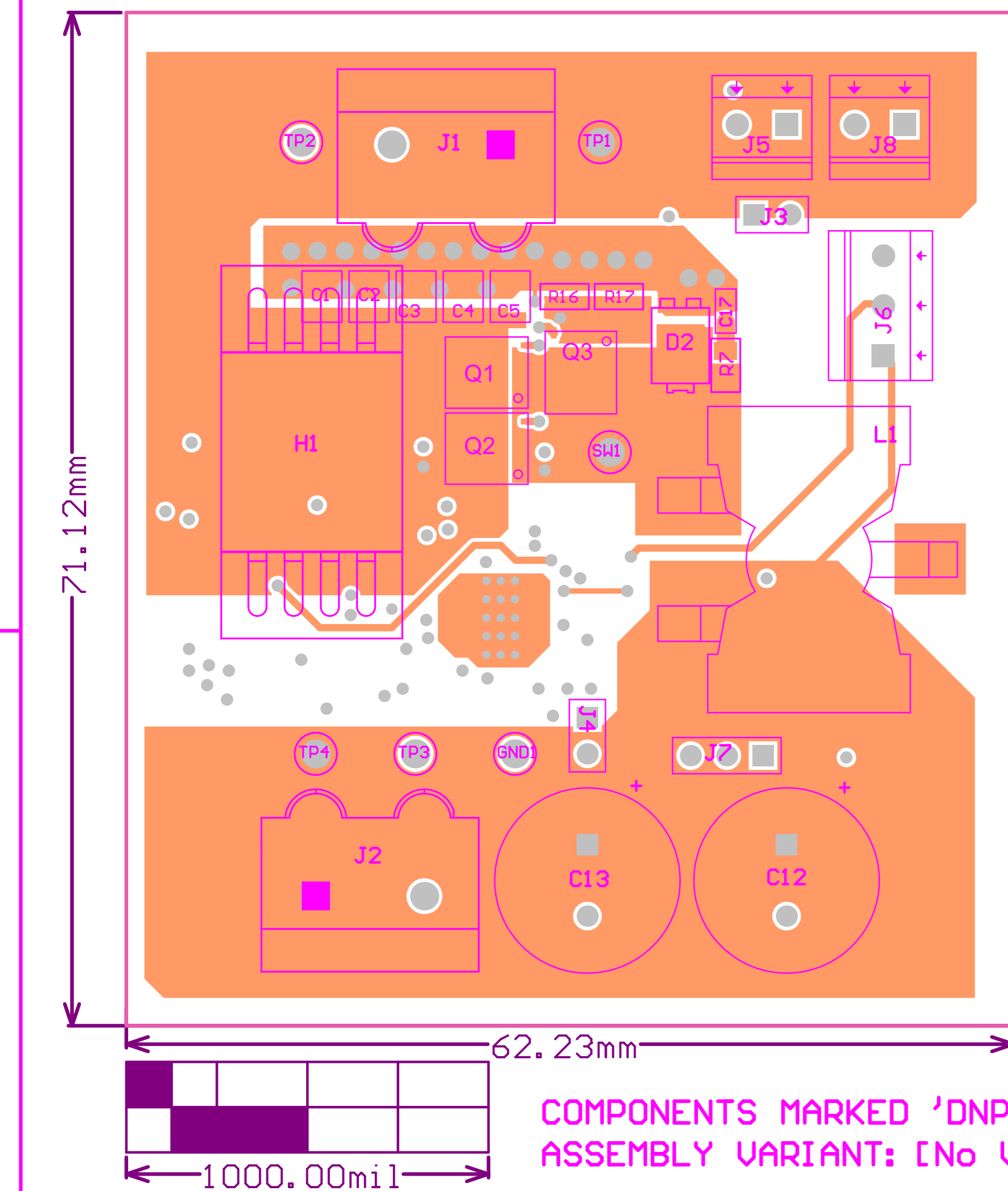


The reference design PMP30301 Rev\_A has been built on PMP30189 Rev\_B PCB



PROJECT TITLE: 27U...29Uin to 24U@11A Synch. Buck with OVP	
DESIGNED FOR: Public Release	
FILE NAME: PMP30189 Rev_B PCB.PcbDoc	
ENGINEER: R. Scibilia	LAYOUT BY: R. Scibilia
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.0.9.368

BOARD #: PMP30189		REV: B	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	
TID #:					
PLOT NAME = Assembly Layer Top		GENERATED : 6/26/2017 12:39:35 PM	TEXAS INSTRUMENTS		



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.  
 ASSEMBLY VARIANT: [No Variations]

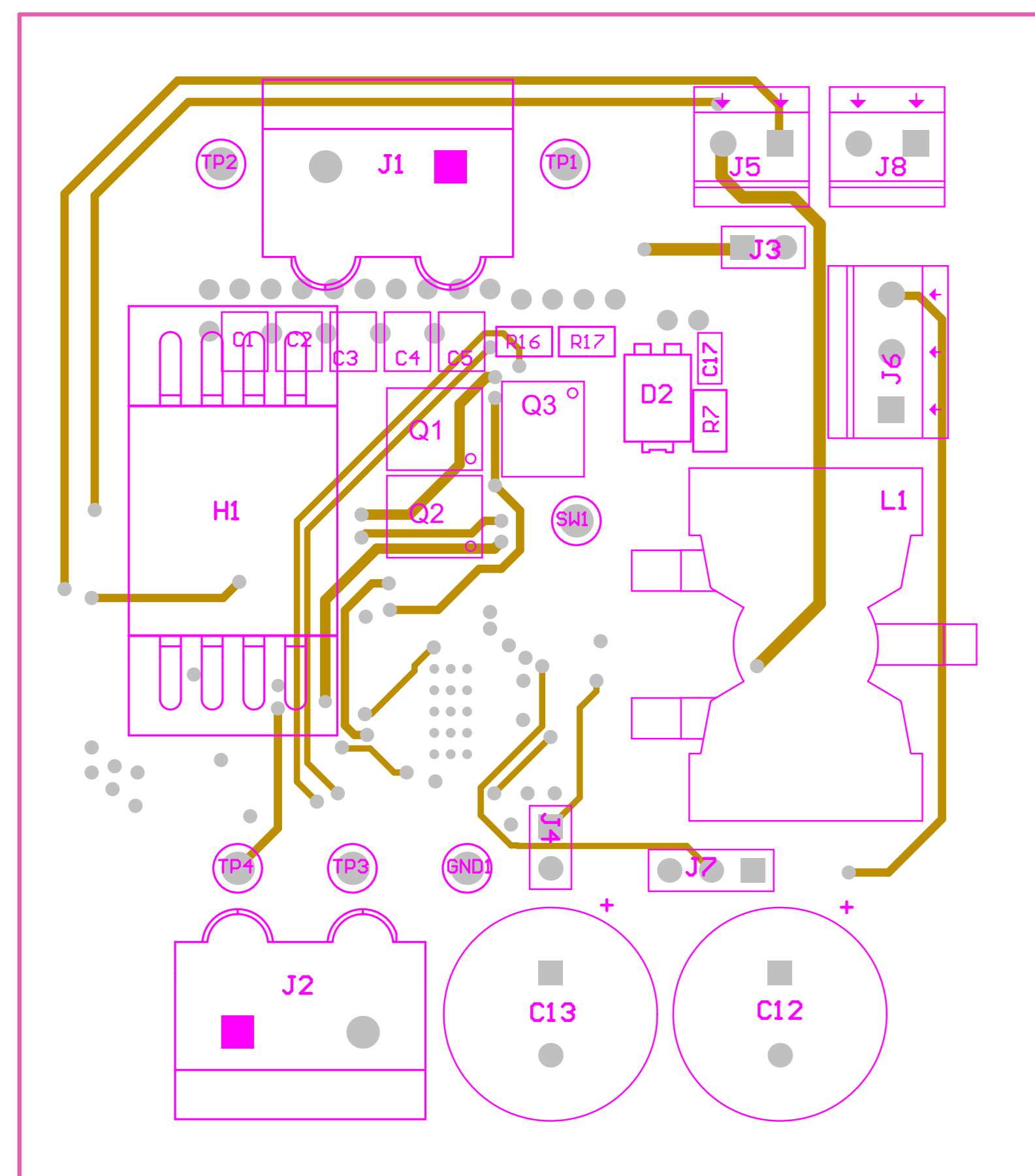


PROJECT TITLE:  
27U...29Uin to 24U@11A Synch. Buck with OVP

DESIGNED FOR:  
Public Release

FILE NAME:  
PMP30189 Rev\_B PCB.PcbDoc

BOARD #: PMP30189		REV: B	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	
TID #:					
PLOT NAME = Copper Top		GENERATED : 6/26/2017 12:39:36 PM	TEXAS INSTRUMENTS	ENGINEER: R. Scibilia	LAYOUT BY: R. Scibilia
				SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.0.9.368

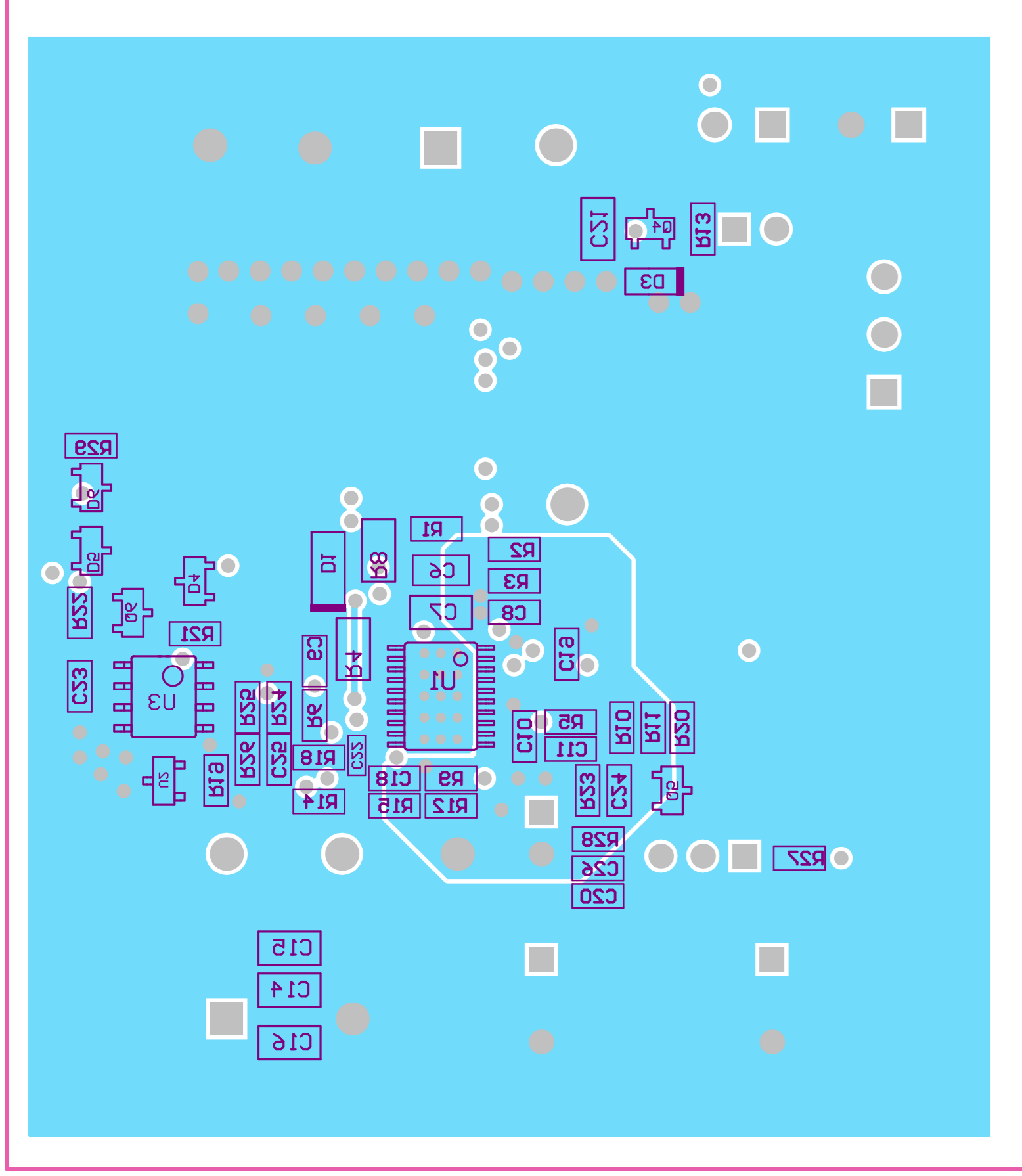


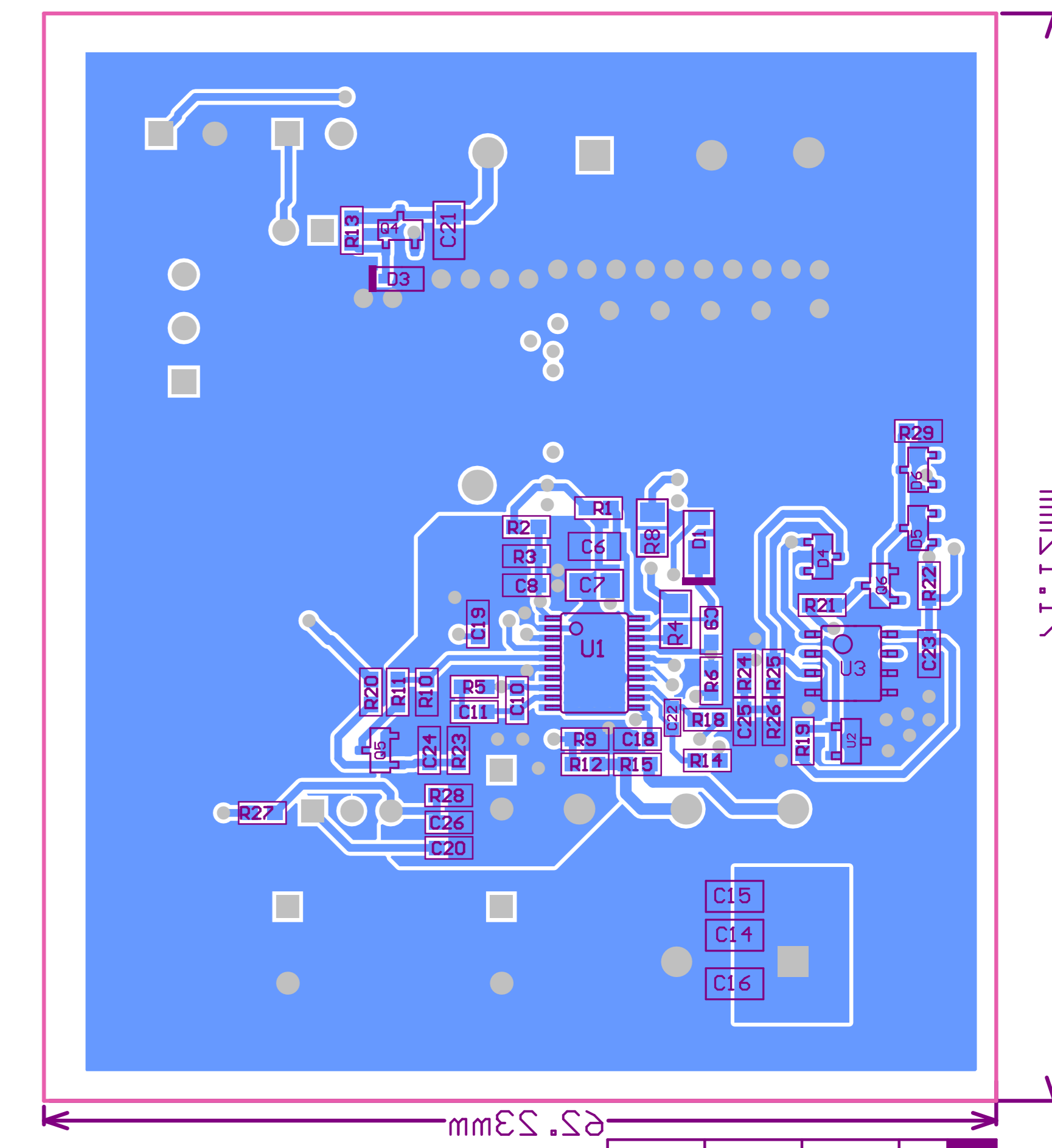
COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.  
 ASSEMBLY VARIANT: [No Variations]

	BOARD #: PMP30189	REV: B	SUN REV: Not In VersionControl
	TID #:		
PLOT NAME = Inner Layer 1	GENERATED : 6/26/2017 12:39:36 PM	TEXAS INSTRUMENTS	


ASSEMBLY VARIANT: [No Variations]  
COMPONENTS MARKED 'DNP', SHOULD NOT BE POPULATED.

PCB VIEWED FROM BOTTOM SIDE	BOARD # : PMP3018A	REV: B
PLOT NAME = Inner Layer 3	GENERATED : 8/28/2015 12:38:36 PM	TEXAS INSTRUMENTS





COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.  
 ASSEMBLY VARIANT: [No Variations]

	
PROJECT TITLE: ZVU...Zavin to Z4UG1A Synch. Buck with OVP	
DESIGNED FOR: Public Release	
FILE NAME: PMP30189 Rev_B PCB.PcbDoc	
LAYOUT BY: R. Scidilia	ENGINEER: R. Scidilia
ALTIM DESIGNER VERSION: 16.0.9.368	SCALE: 1.00

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PCB VIEWED FROM BOTTOM SIDE	BOARD #: PMP30189	REV: B	
	TID #:		
PLOT NAME = Copper Bottom	GENERATED : 6/26/2017 12:39:37 PM	TEXAS INSTRUMENTS	

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