Test Report: PMP22151

70-W Flyback and 37-W Boost Power Reference Design

Description

This reference design uses two LM5155 devices to make a flyback and boost power stage. The flyback creates an isolated 28 Vdc bus from a 24 +/-10% Vdc bus and the boost creates a 37 Vdc bus from the output of the flyback. The flyback can be loaded up to 70-W and the boost can be loaded up to 37-W. All components are placed on one side of the board to reduce assembly complexity and cost. Both power stages achieve over 90% efficiency across output conditions.

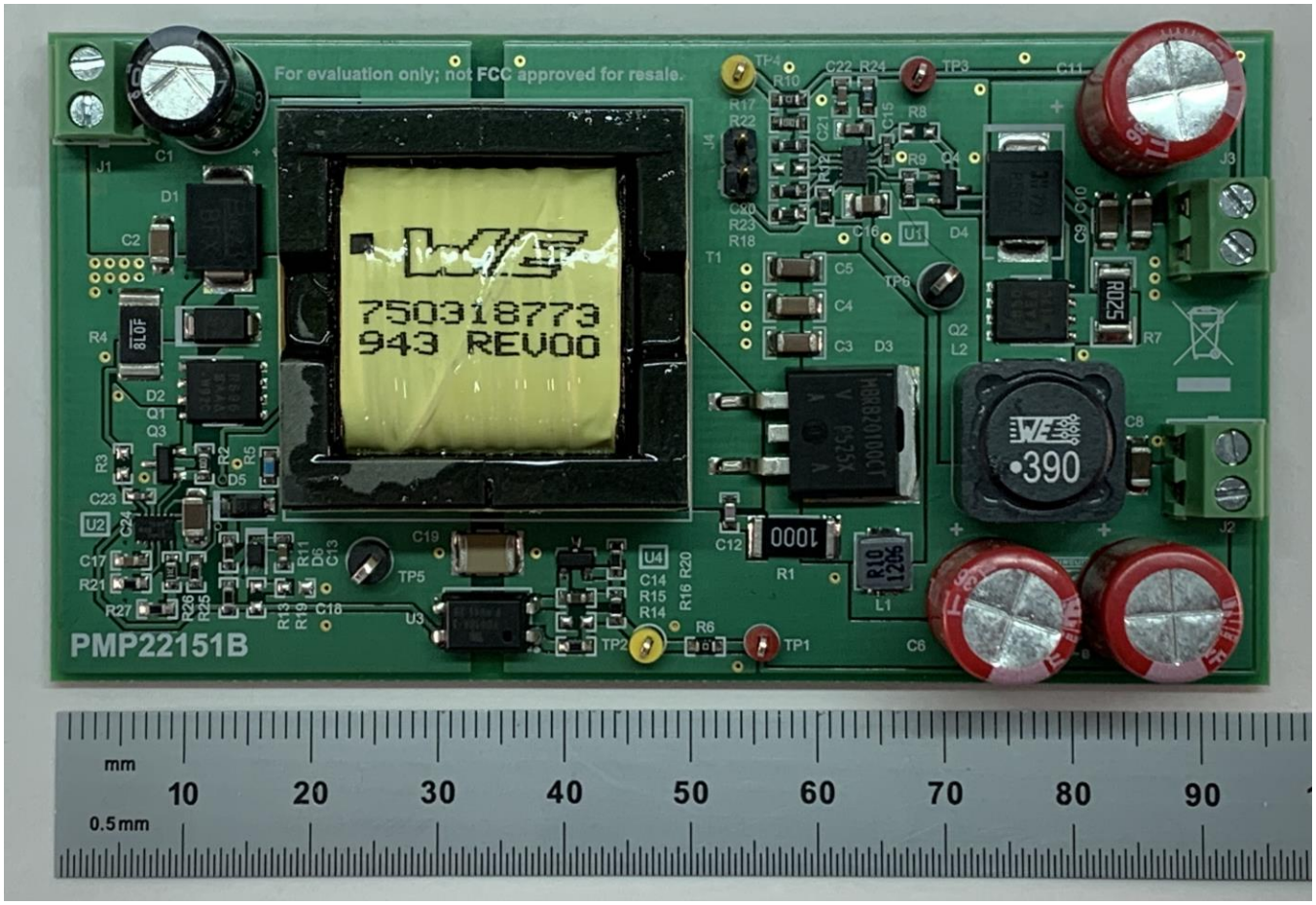

Figure 1. Board Top

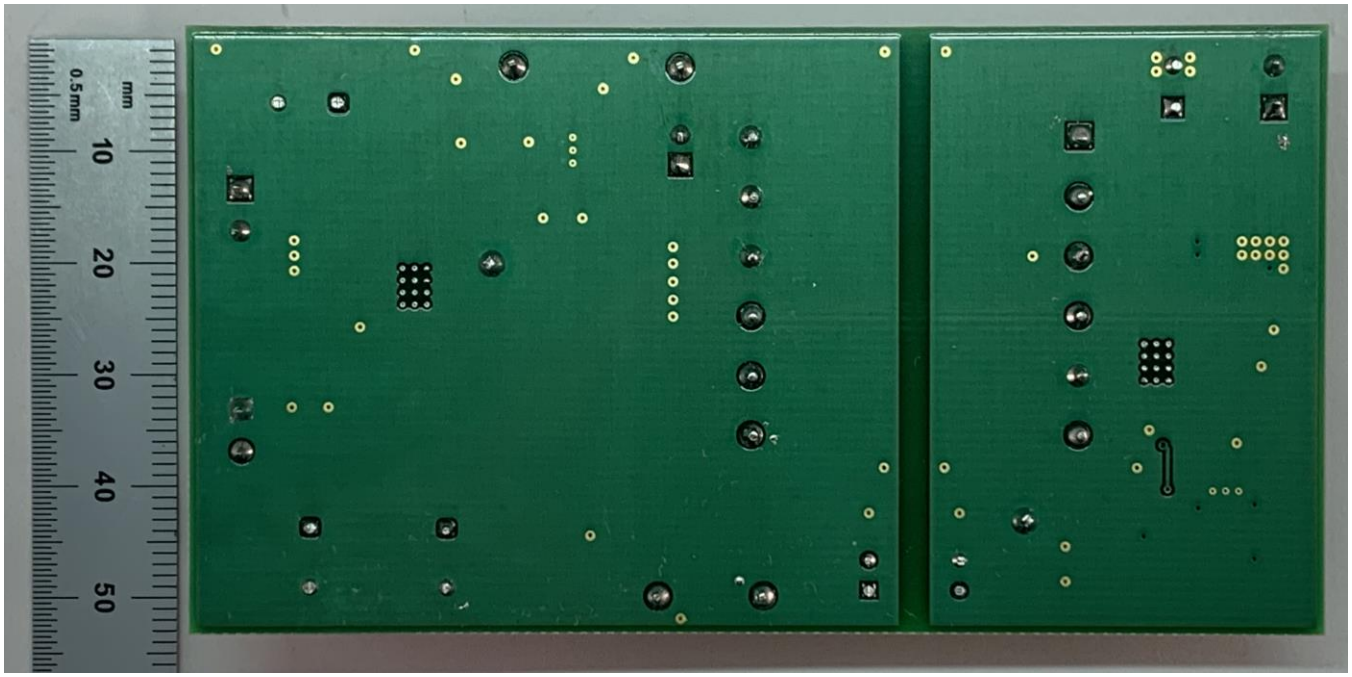

Figure 2. Board Bottom

1 Flyback Stage

1.1 Test Prerequisites

1.1.1 Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	19 Vdc – 28 Vdc, 24 Vdc nominal
Output Voltage	28 V +/- 1%
Output Current	2.5 A max, 1 A max when boost is loaded
Switching Frequency	100 kHz

1.1.2 Considerations

Unless otherwise indicated the input voltage was set to 24 Vdc. For all tests an electronic load was used. A jumper was added to J4 to disable the boost controller.

1.2 Testing and Results

1.2.1 Efficiency Graphs

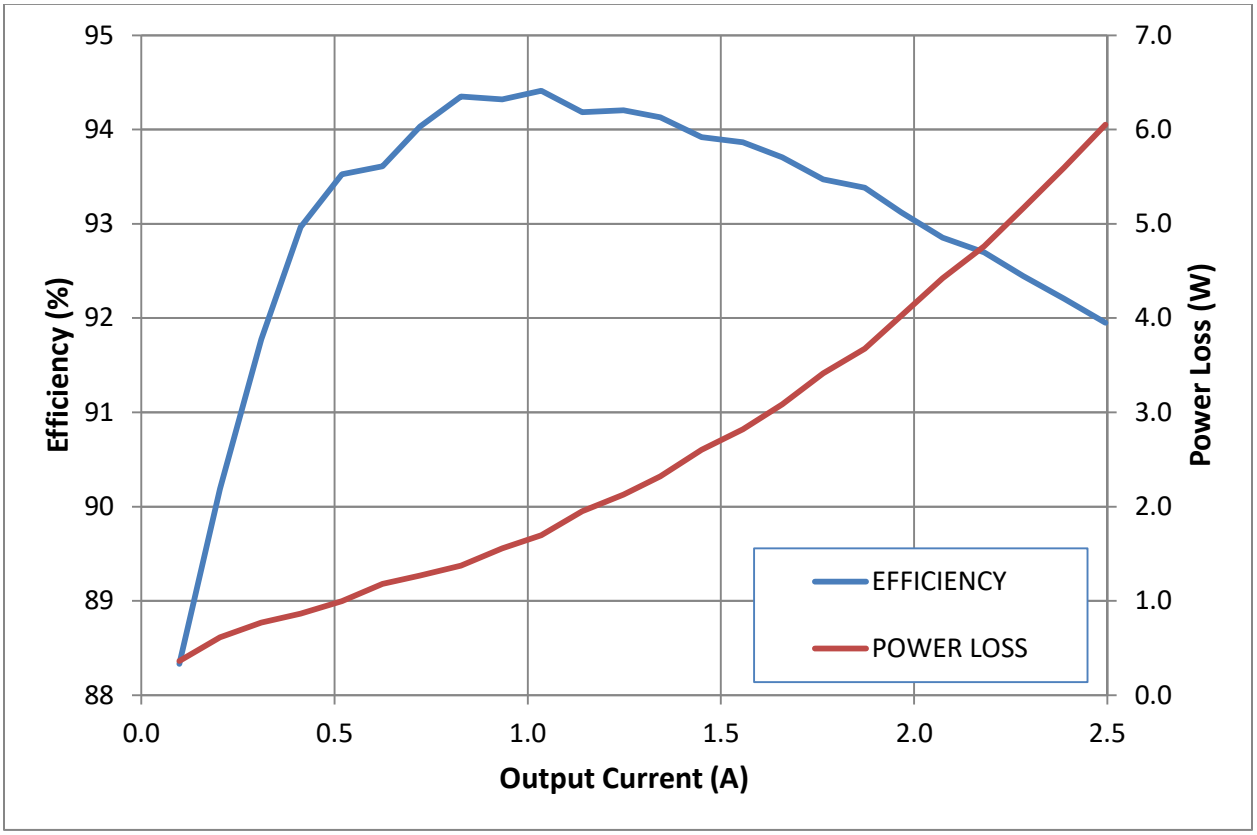

Figure 3. Efficiency with 24 Vdc Input

1.2.2 Efficiency Data

Input			Output			Total	
Voltage (V)	Current (A)	Power (W)	Voltage (V)	Current (A)	Power (W)	Power (W)	Efficiency (%)
24.0511	0.0067	0.1622	27.4582	0.0011	0.0295	0.1327	18.1616
24.0510	0.7682	18.4753	27.7120	0.6241	17.2945	1.1807	93.6091
24.0511	1.5266	36.7159	27.7102	1.2482	34.5884	2.1274	94.2057
24.0514	2.3098	55.5531	27.7076	1.8723	51.8771	3.6760	93.3830
24.0515	3.1255	75.1737	27.7034	2.4951	69.1235	6.0502	91.9518

Figure 4. Efficiency data from light load, one quarter load, half load, third quarter load, and full load

1.2.3 Thermal Images

Thermal images were taken after 15 minutes of running with the output at 2.5 A and no airflow.

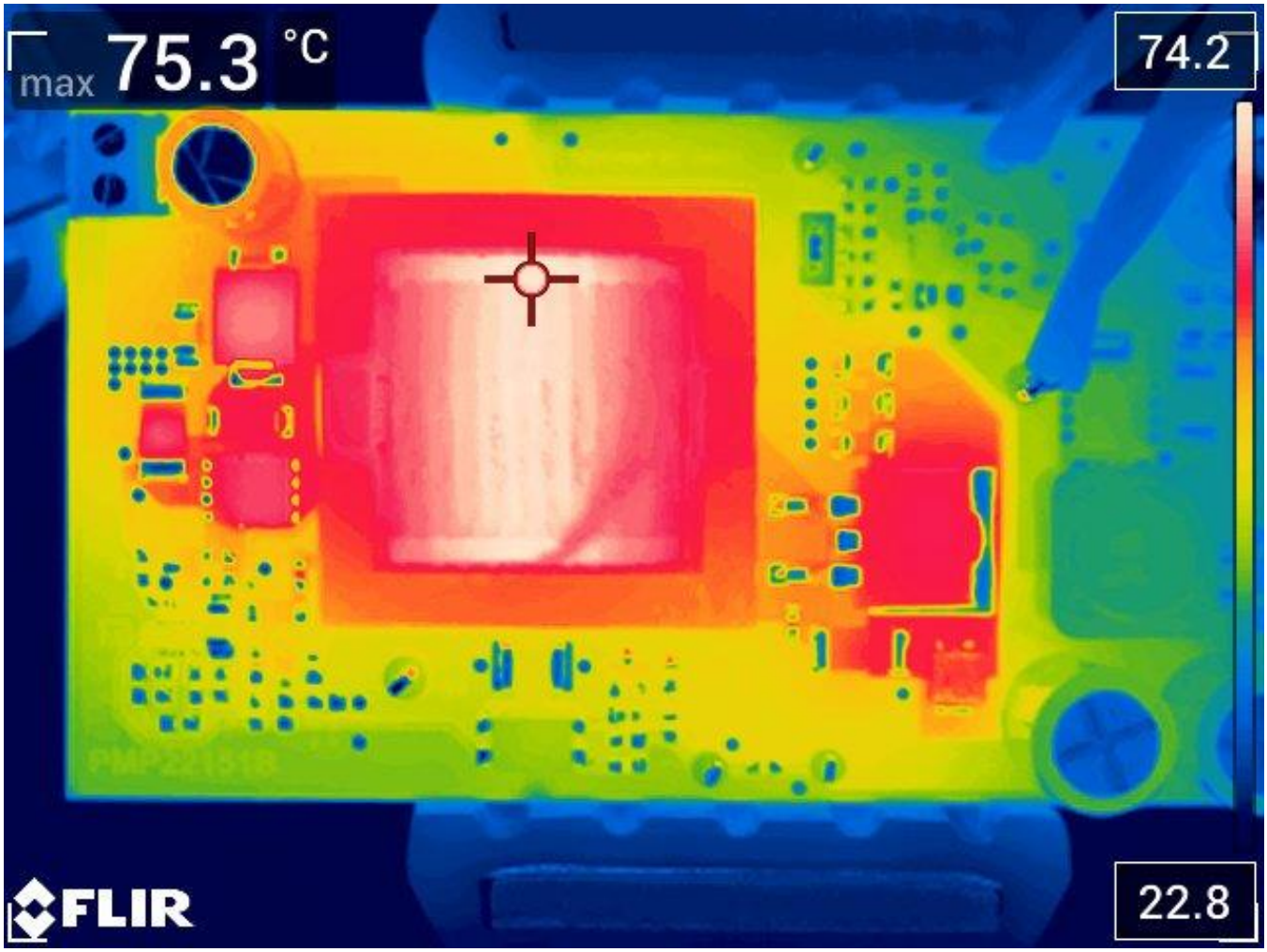

Figure 5. Board Top

1.3 Waveforms

1.3.1 Switching

The switch node was measured with the output at full load. The secondary side rectifier was measured using the math function on the oscilloscope and is shown in orange.

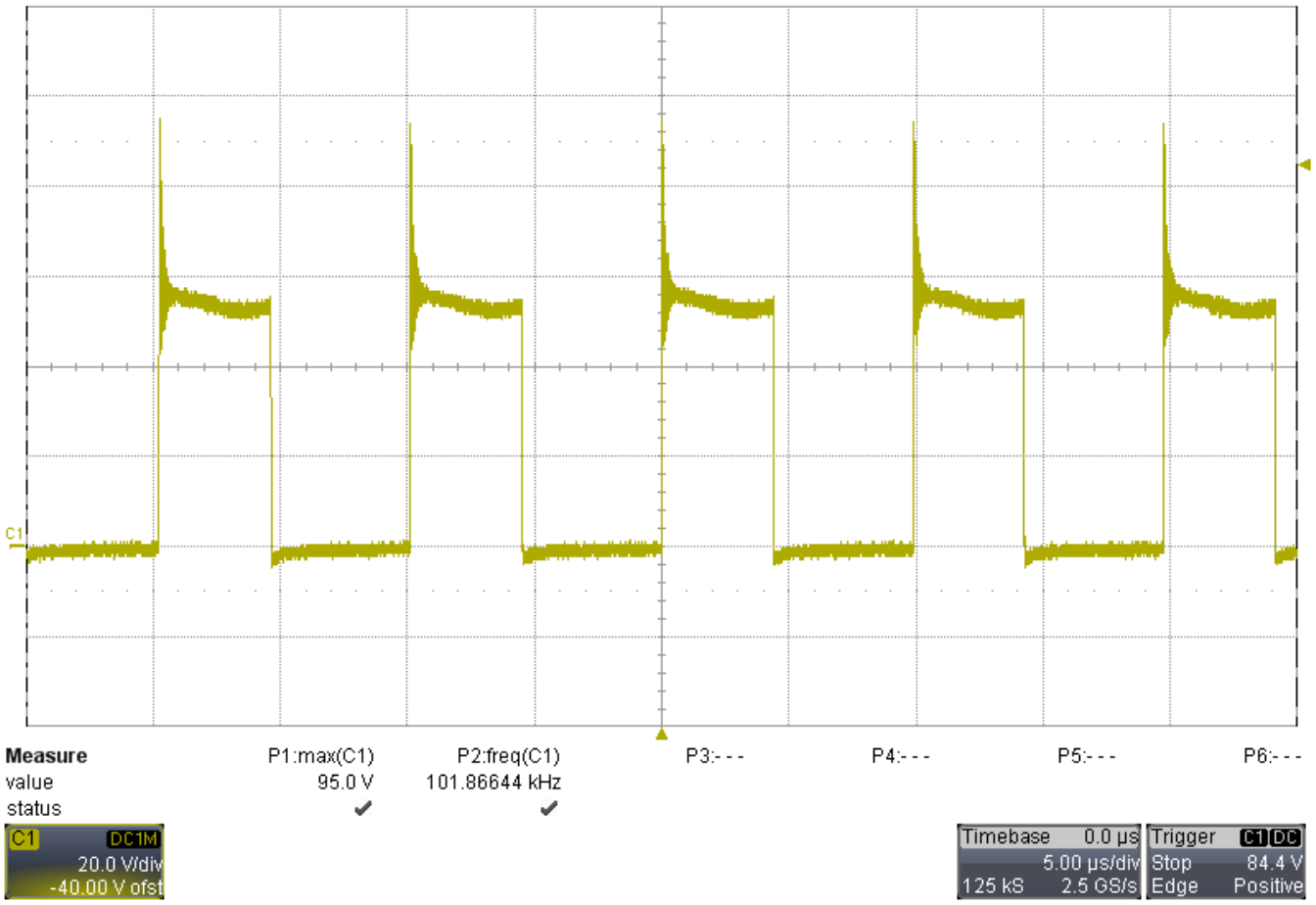

Figure 6. Primary Switching Node

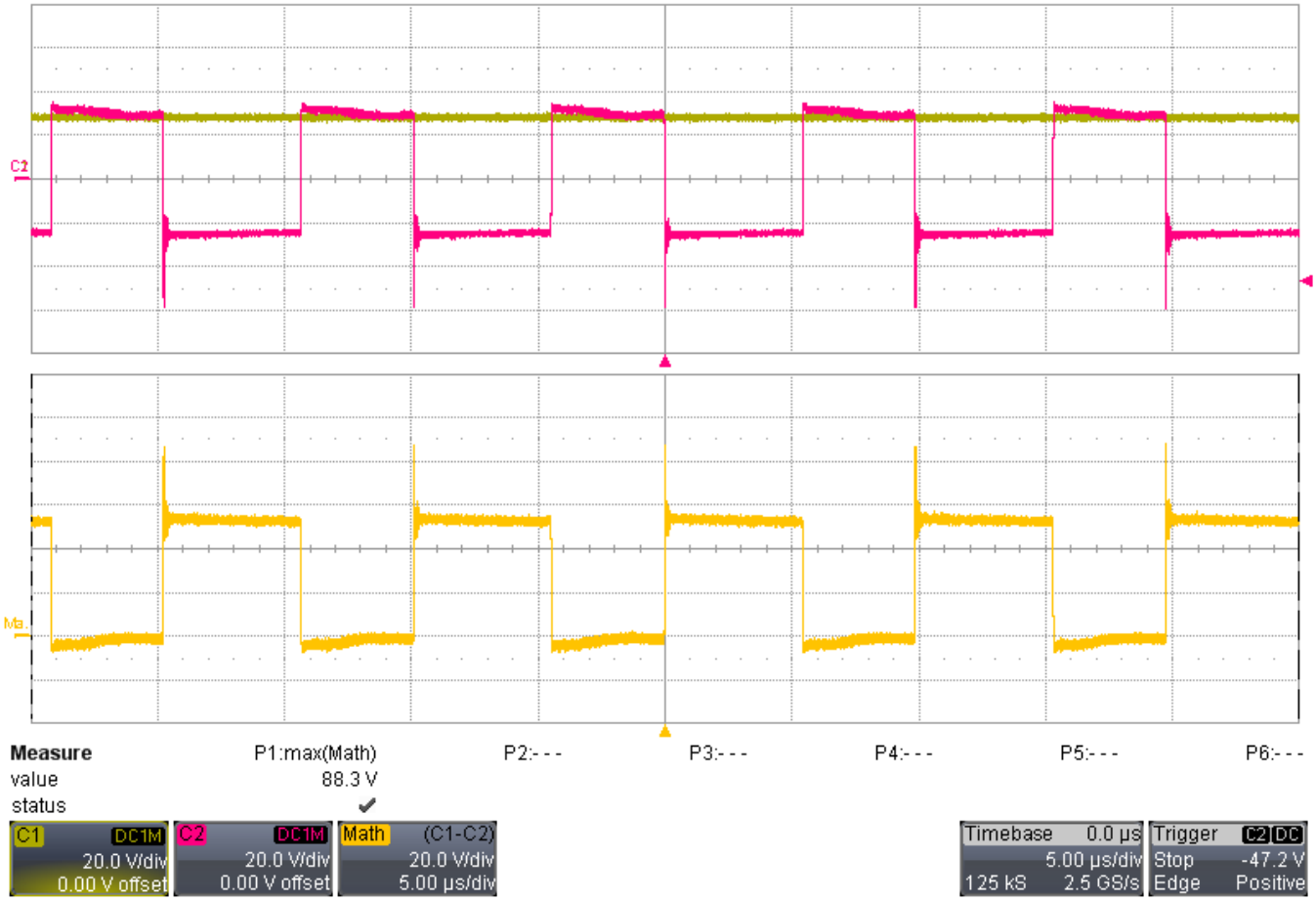

Figure 7. Secondary Switching Node

1.3.2 Output Voltage Ripple

Measurements were taken using the tip and barrel method across the output cap (C11) with the output at full load.

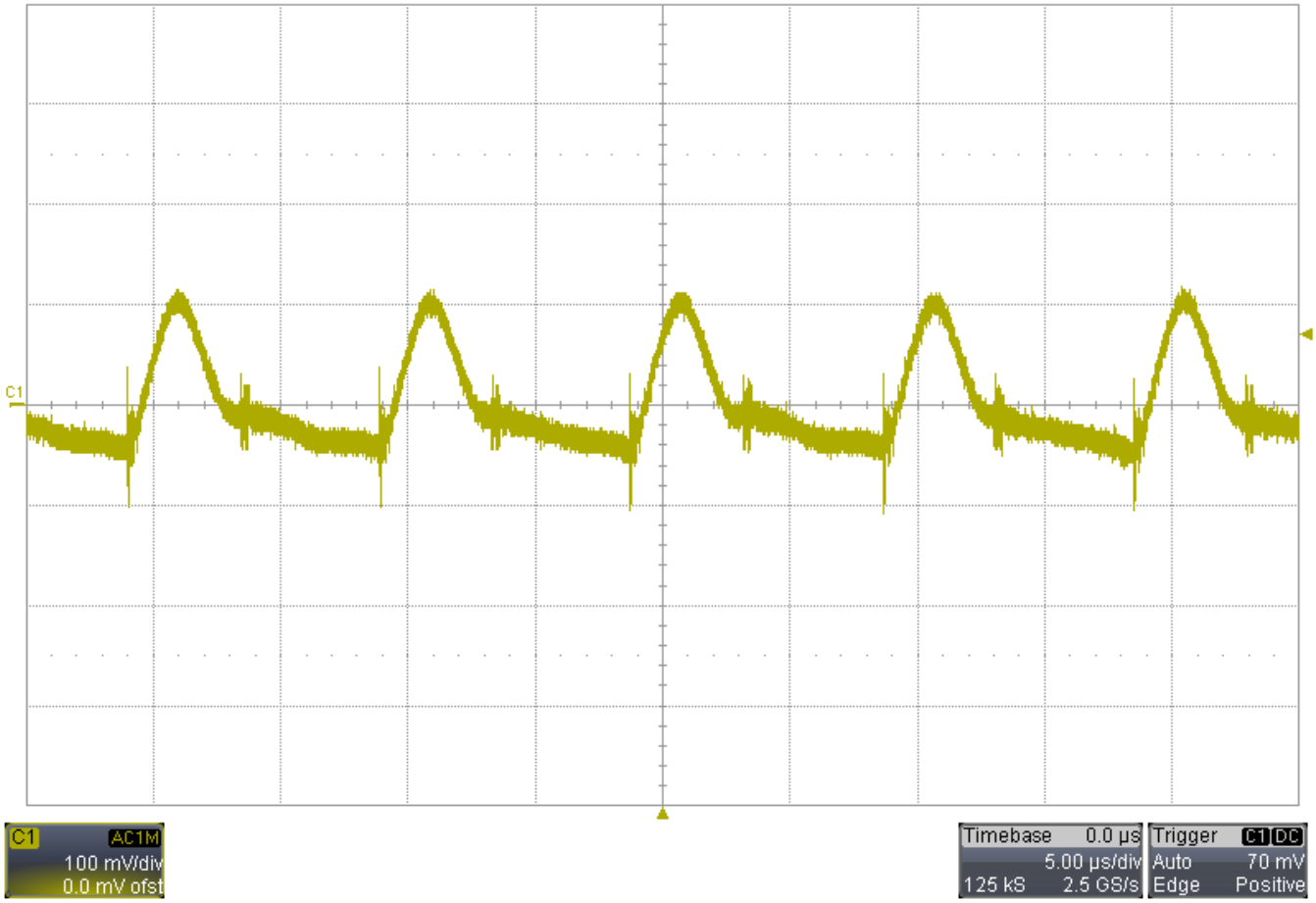

Figure 8.

1.3.3 Load Transients

The output voltage (AC coupled) was measured across the output capacitor (C11).

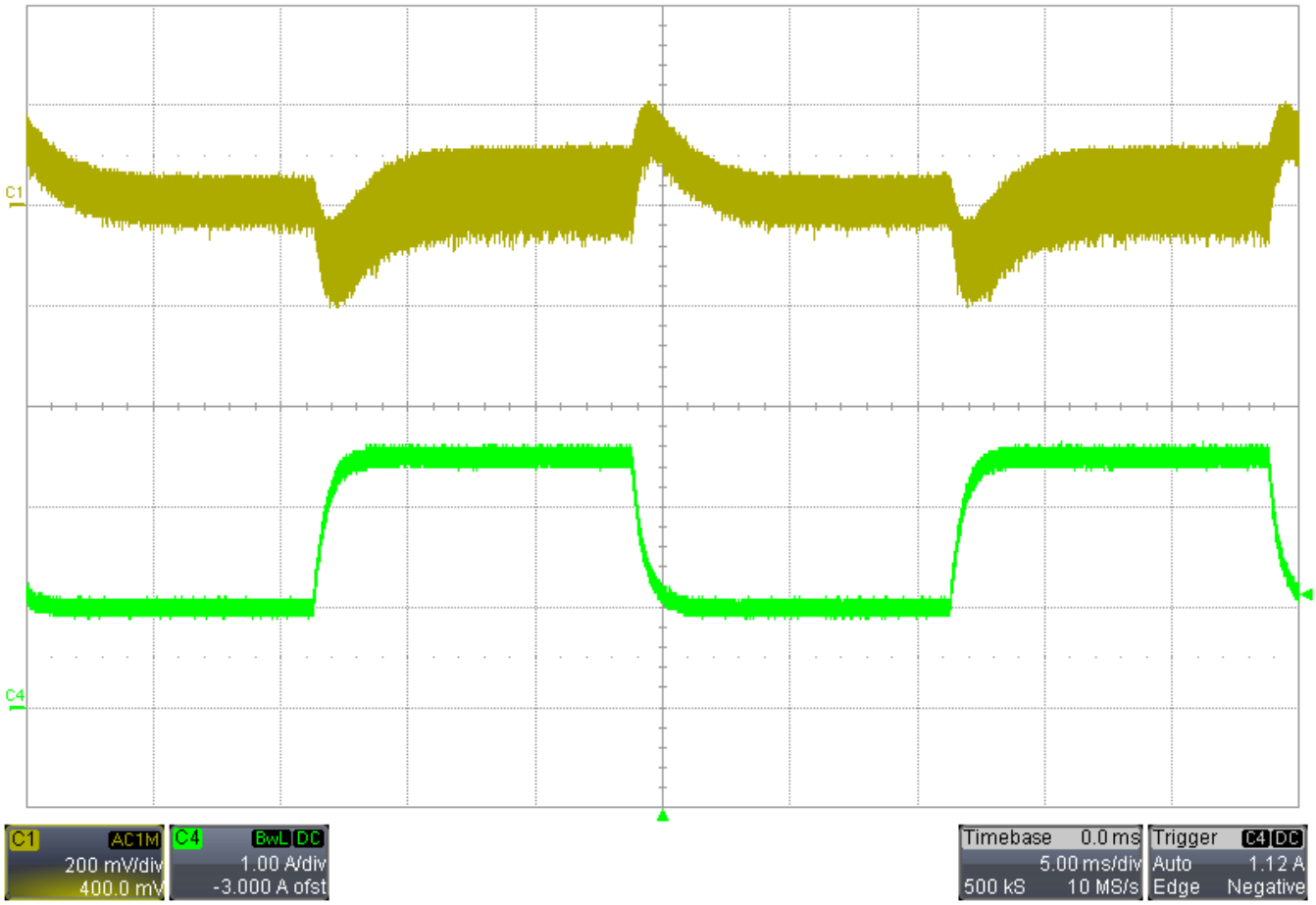

Figure 9. Load stepping between 1 A and 2.5 A

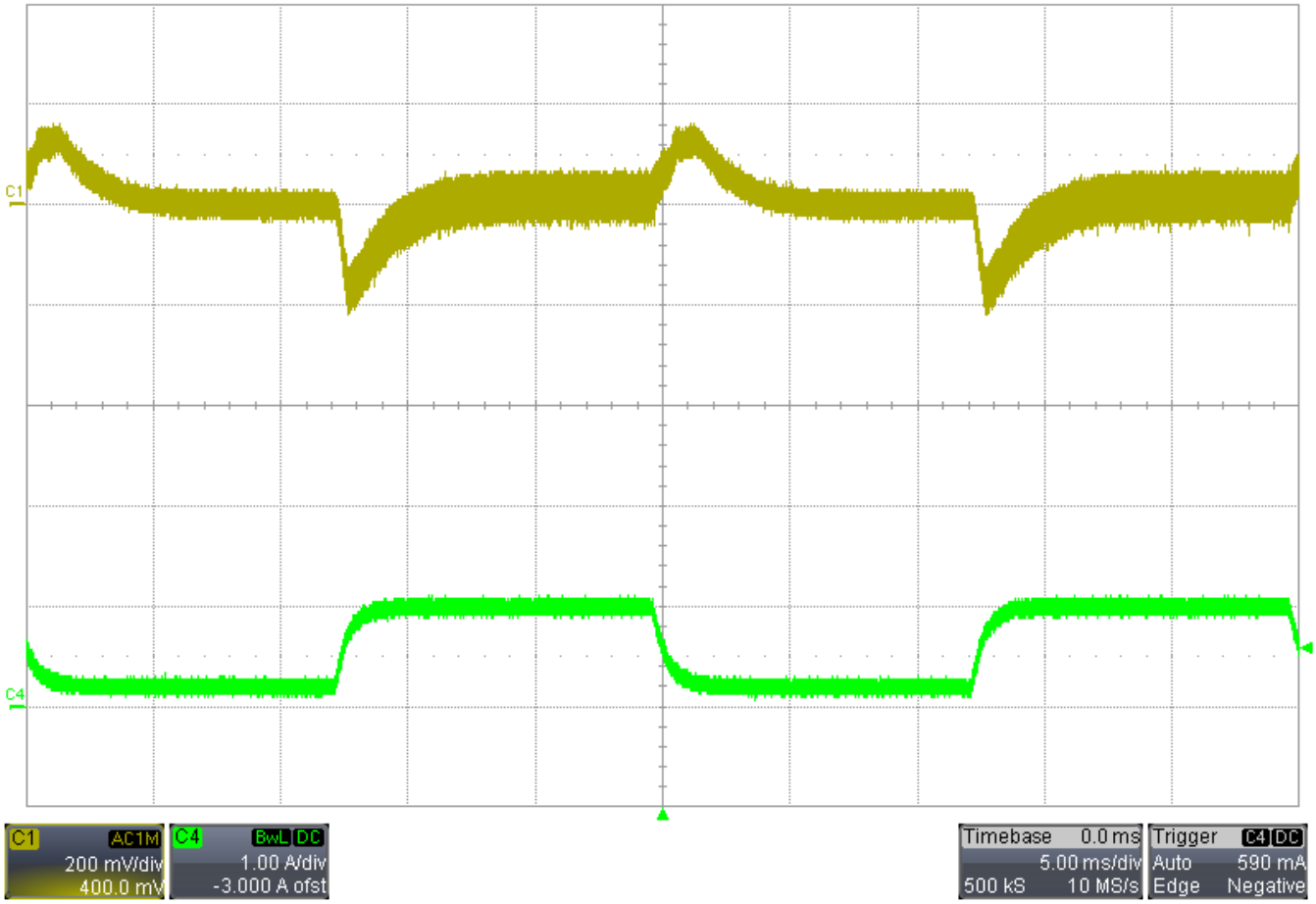

Figure 10. Load stepping between 0.2 A and 1 A

1.3.4 Control Loop/Stability

For this measurement the output was loaded to 2.5 A. The table below shows the bandwidth and phase margin measurements.

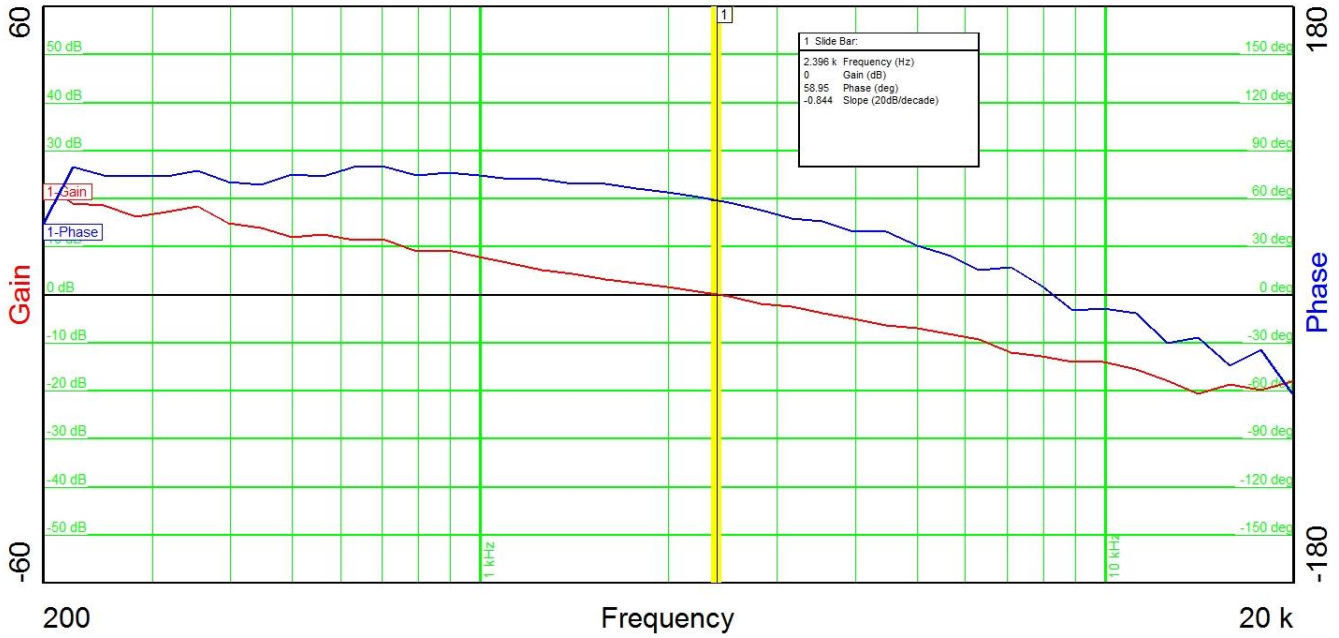

Figure 11.

Input Voltage (V)	Bandwidth (kHz)	Phase Margin (degrees)
24	2.396	58.95

2 Boost Stage

2.1 Test Prerequisites

2.1.1 Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	28 Vdc +/-1%
Output Voltage	37 V +/- 1%
Output Current	1 A max
Switching Frequency	300 kHz

2.1.2 Considerations

Unless otherwise indicated the input voltage was set to 28 Vdc. For all tests an electronic load was used.

2.2 Testing and Results

2.2.1 Efficiency Graphs

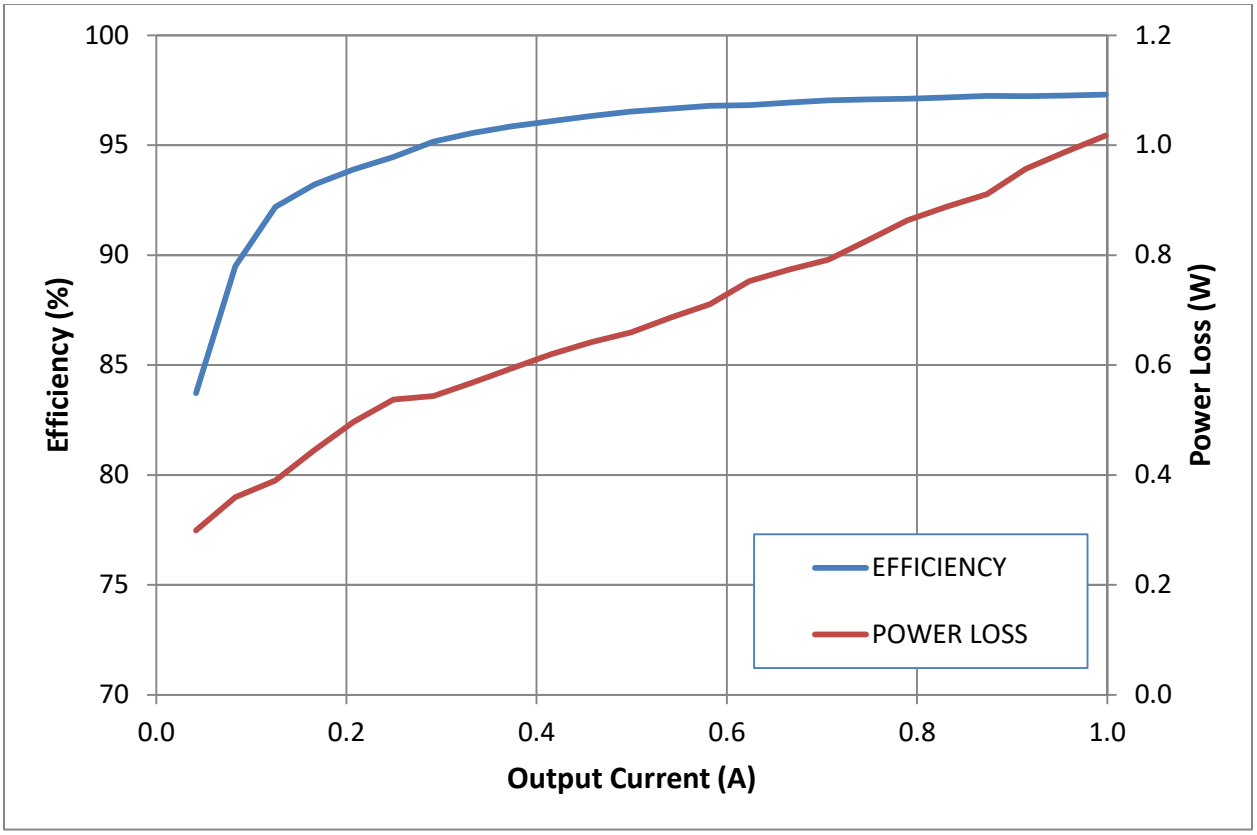

Figure 12. Efficiency with 28 Vdc Input

2.2.2 Efficiency Data

Input			Output			Total	
Voltage (V)	Current (A)	Power (W)	Voltage (V)	Current (A)	Power (W)	Power (W)	Efficiency (%)
28.0723	0.0038	0.1055	36.7424	0.0004	0.0153	0.0902	14.5391
28.0725	0.3454	9.6964	36.7412	0.2493	9.1595	0.5369	94.4628
28.0729	0.6772	19.0096	36.7404	0.4995	18.3504	0.6592	96.5323
28.0732	1.0091	28.3295	36.7399	0.7486	27.5024	0.8270	97.0806
28.0731	1.3430	37.7016	36.7397	0.9985	36.6842	1.0174	97.3014

Figure 13. Efficiency data from light load, one quarter load, half load, third quarter load, and full load

2.2.3 Thermal Images

Thermal images were taken after 15 minutes of running with the output at 1 A and no airflow.

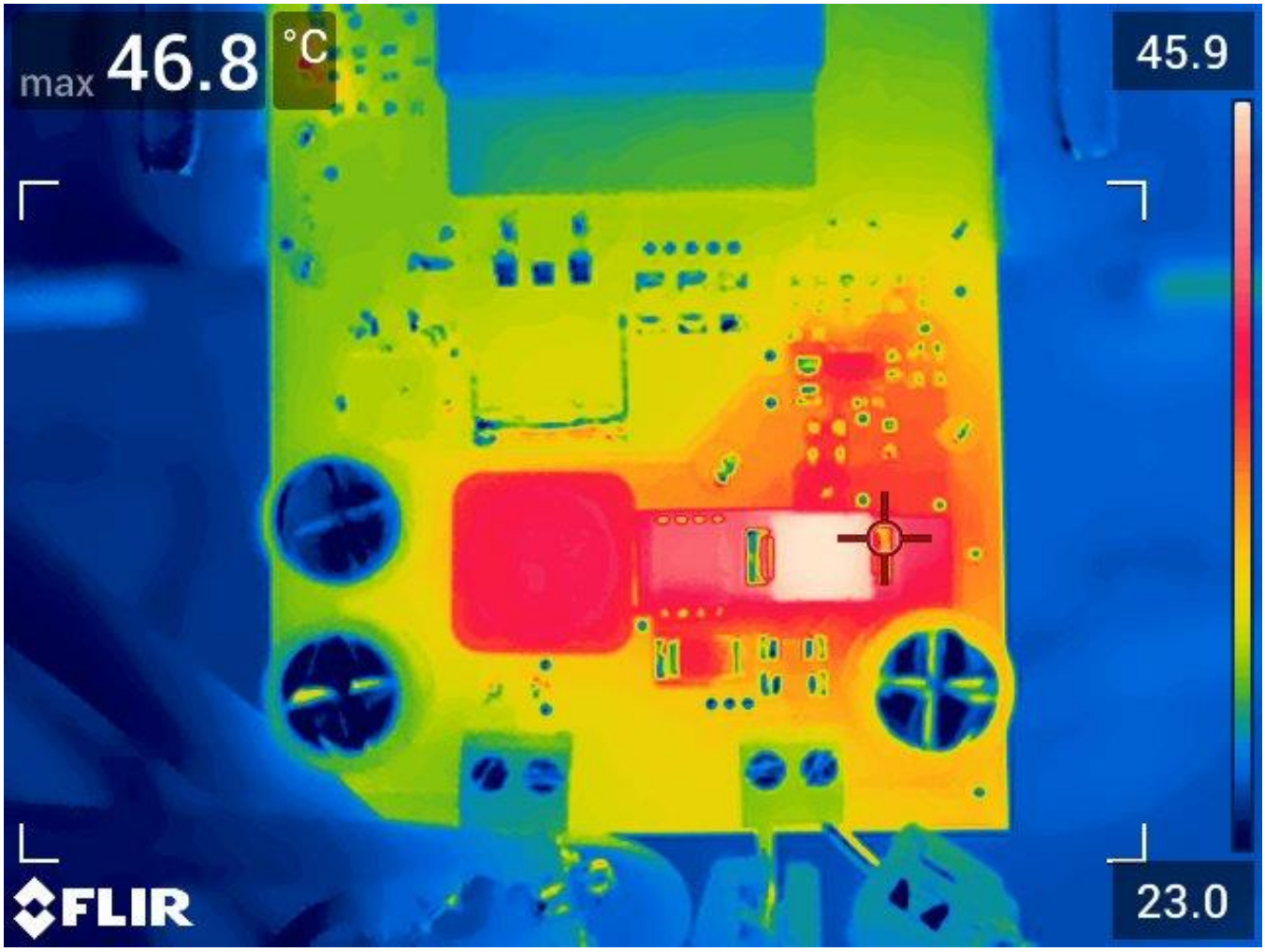

Figure 14. Board Top

2.3 Waveforms

2.3.1 Switching

The switch node was measured with the output at full load.

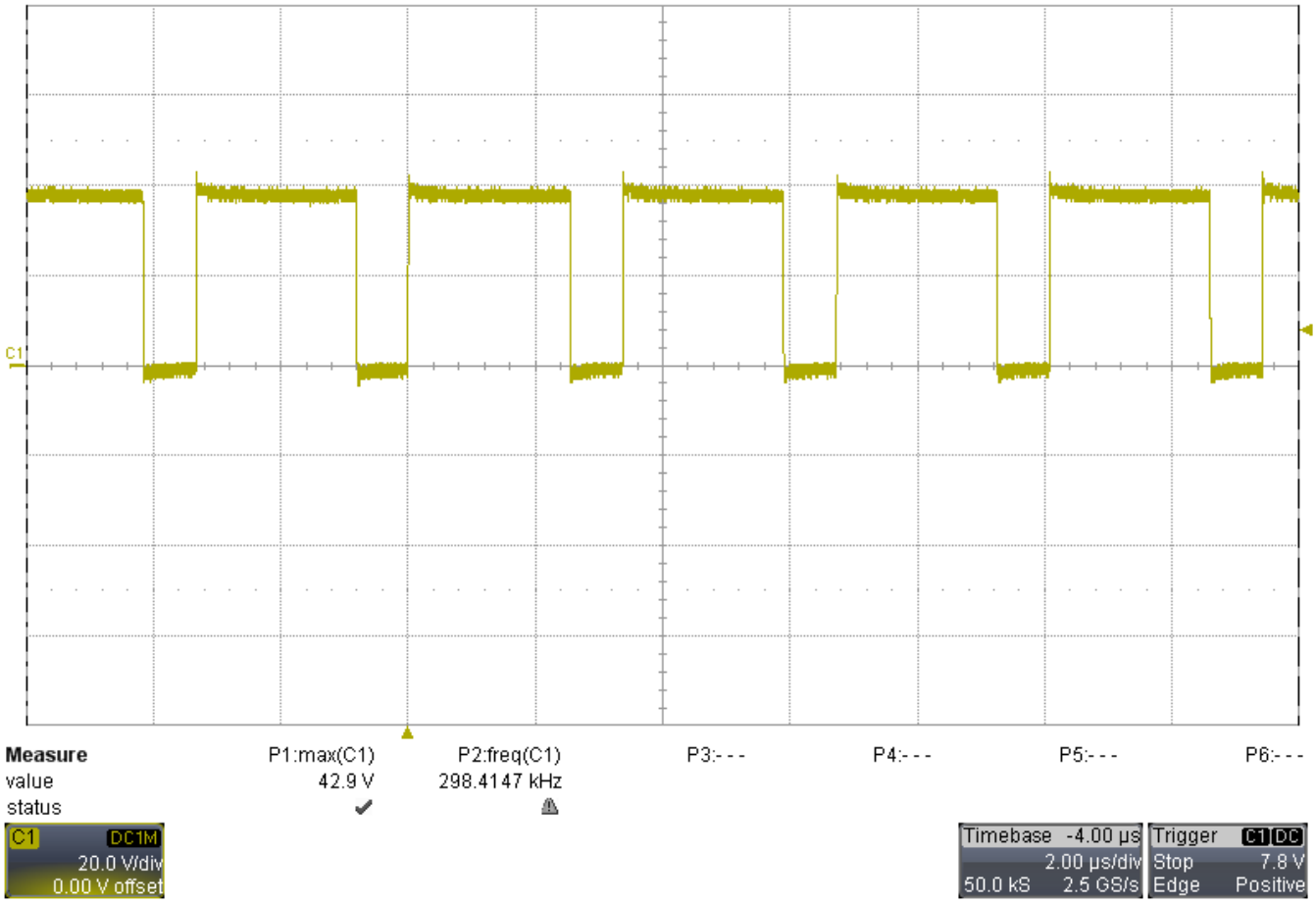

Figure 15. Primary Switching Node

2.3.2 Output Voltage Ripple

Measurements were taken using the tip and barrel method across the output cap (C5) with the output at full load.

Figure 16.

2.3.3 Load Transients

The output voltage (AC coupled) was measured across the output capacitor (C5).

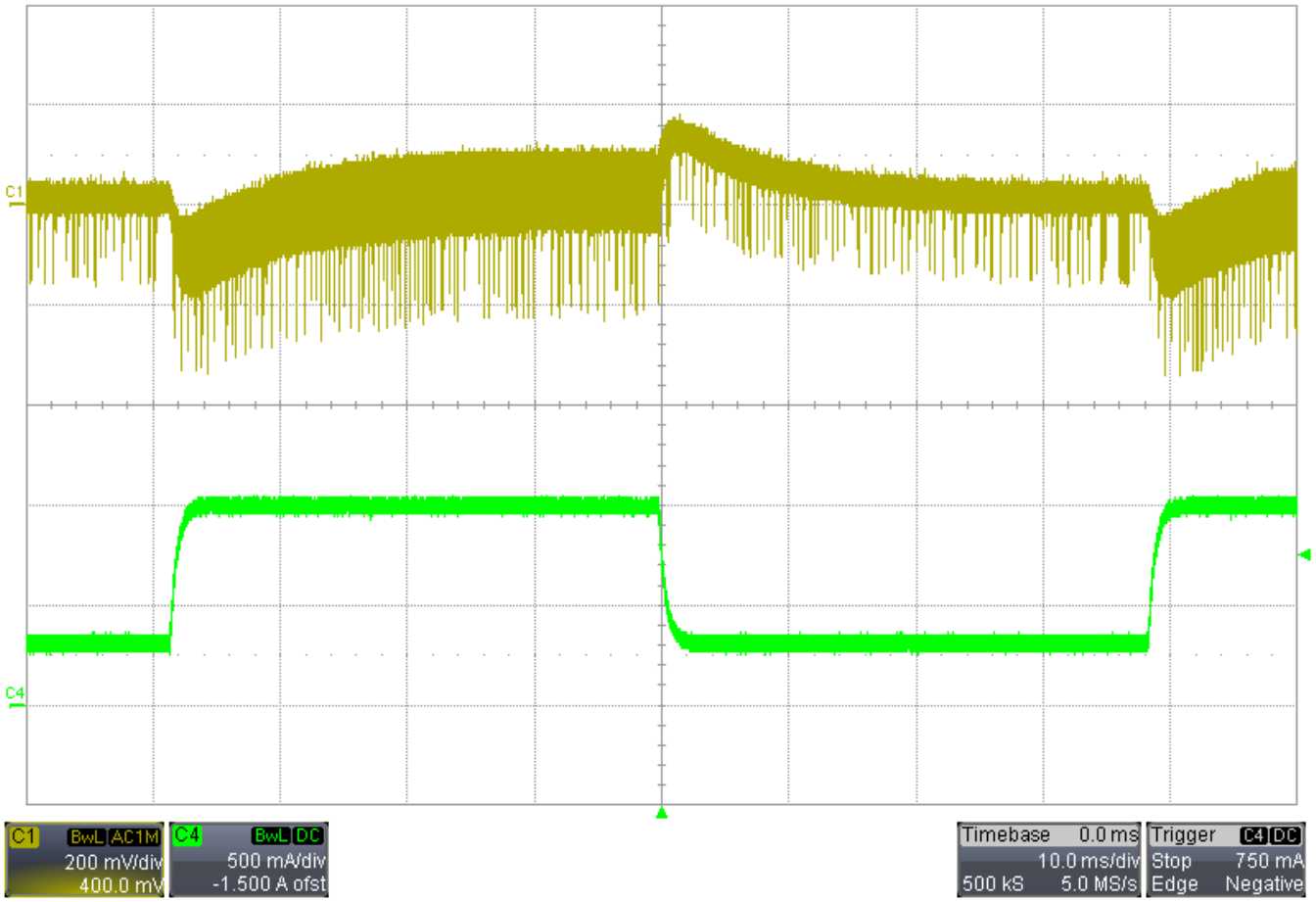

Figure 17. Load stepping between 0.3 A and 1 A

2.3.4 Control Loop/Stability

For this measurement the output was loaded to 1 A. The table below shows the bandwidth and phase margin measurements.

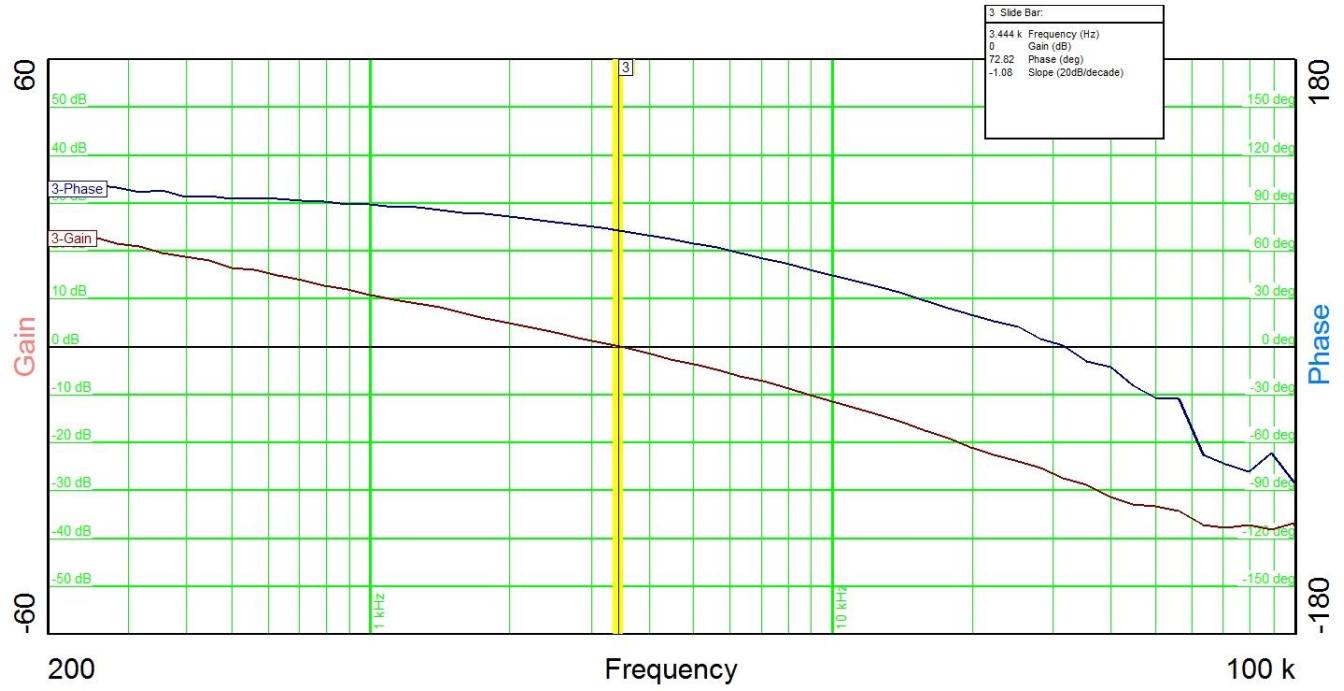

Figure 18.

Input Voltage (V)	Bandwidth (kHz)	Phase Margin (degrees)
28	3.444	72.82

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