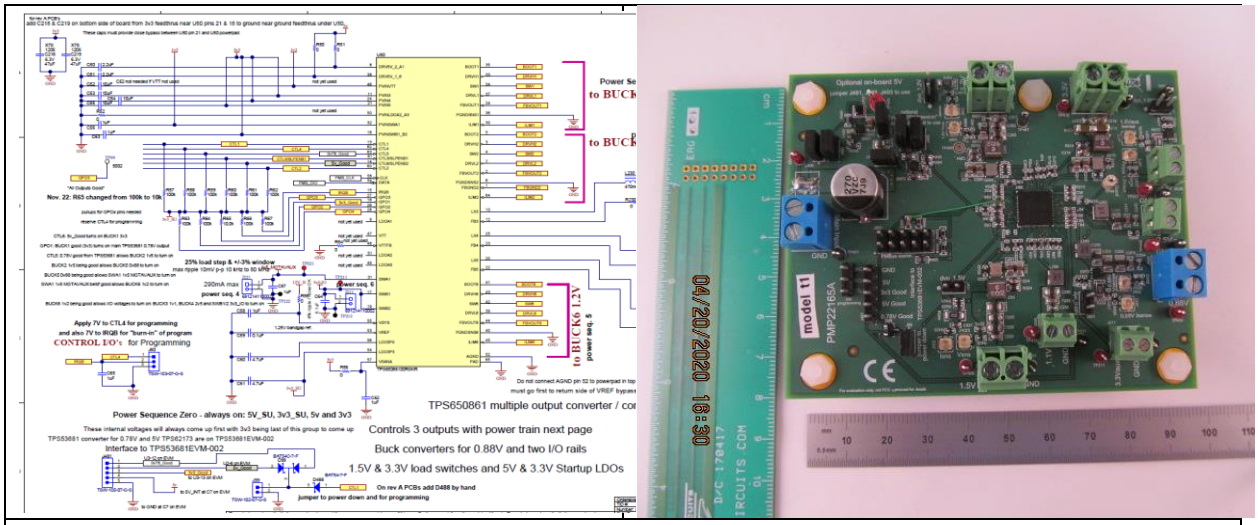
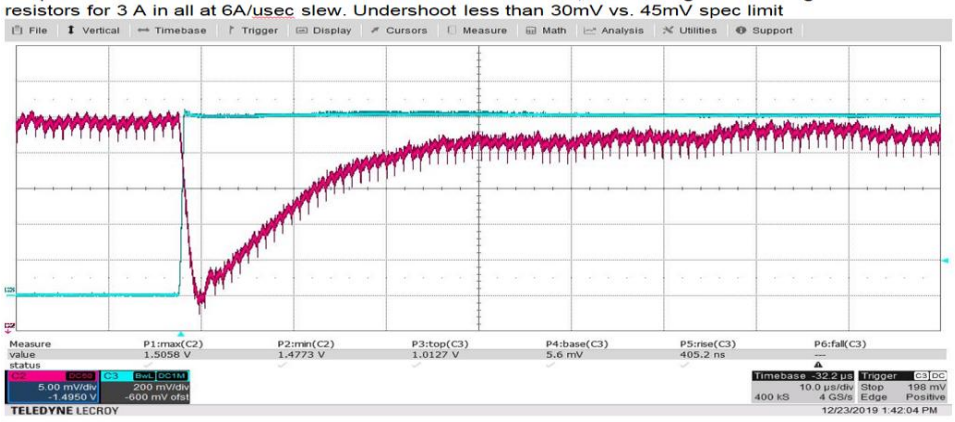
Test Report: PMP22165

Power for Xilinx Versal Adaptive Compute Acceleration Platform (ACAP) Reference Design

Description

PMP22165 reference design addresses Xilinx Versal Adaptive Compute Acceleration Platform (ACAP) platform requirements and consists of a Power Management Integrated Circuit (PMIC) for system-rails, plus a multiphase controller and power stages to support higher current processor loads. On board dynamic loads on the critical outputs allow testing to Xilinx's demanding power requirements. PMP22165 along with the TPS53681 EVM is a tested solution offering performance with cost-optimized components to meet processor requirements for Versal's most common use cases 1 & 3.





1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

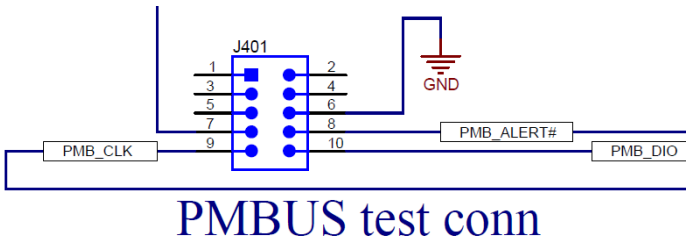
PARAMETER	SPECIFICATIONS
Input Voltage	7-14 VDC
Output Voltage Range	Various outputs 0.8V thru 3.3V
Max Load Current	165A on main, up to 4.8A on 1.2V
Max Output Power (electrical peak / for thermal purposes)	150W electrical peak

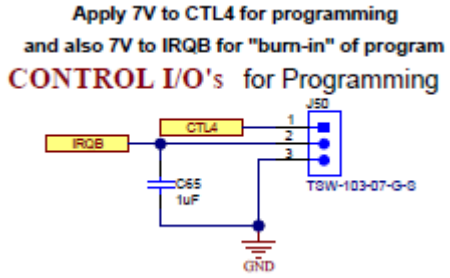
1.2 Required Equipment

- Lab 12 V 20 A source if testing with main 0.8V 165A, otherwise 12V 3A source OK
- Electronic loads rated to carry maximum static load
- Signal generator to drive on-board dynamic load. Example Tektronix AFG3102
- Thermal camera
- Oscilloscope and voltage / current meters or current shunts

1.3 Programming the TPS650861

The TPS650861 needs to be programmed for this application thru the PMB_CLK (J401-9) and PMB_DIO (J401-10) pins with J401-6 as ground. Also, during programming CTL4 (J50-1) needs to be pulled to 7V. Also, when “burning in” the program, IRQB (J50-2) also needs to be pulled to 7V.





See TPS65086100 Non-Volatile Memory Programming Guide for details. The following script was used on the PMP22165 boards.

```
var custom_program_199 = [
        {group: 'PART_NUMBER', value: 0x199},
        {register: 'DEVICEID2', value: 0x01},
        {register: 'BUCK1CTRL', value: 0xE8},
        {register: 'BUCK2CTRL', value: 0xDC},
        {register: 'BUCK3DECAY', value: 0x38},
        {register: 'BUCK3VID', value: 0x38},
        {register: 'BUCK3SLPCTRL', value: 0x38},
        {register: 'BUCK4CTRL', value: 0x0F},
        {register: 'BUCK5CTRL', value: 0x0F},
        {register: 'BUCK6CTRL', value: 0x0F},
        {register: 'LDOA2CTRL', value: 0x0C},
        {register: 'LDOA3CTRL', value: 0x0C},
        {register: 'DISCHCTRL1', value: 0x55},
        {register: 'DISCHCTRL2', value: 0x55},
        {register: 'DISCHCTRL3', value: 0x15},
```

{register: 'PG_DELAY1', value: 0x06},
{register: 'BUCK1SLPCTRL', value: 0xE8},
{register: 'BUCK2SLPCTRL', value: 0xDC},
{register: 'BUCK4VID', value: 0xA8},
{register: 'BUCK4SLPVID', value: 0xA8},
{register: 'BUCK5VID', value: 0x26},
{register: 'BUCK5SLPVID', value: 0x26},
{register: 'BUCK6VID', value: 0xA0},
{register: 'BUCK6SLPVID', value: 0xA0},
{register: 'LDOA2VID', value: 0xFF},
{register: 'LDOA3VID', value: 0xAA},
{register: 'BUCK123CTRL', value: 0x3F},
{register: 'PG_DELAY2', value: 0x00},
{register: 'SWVTT_DIS', value: 0x60},
{register: 'I2C_RAIL_EN1', value: 0x80},
{register: 'I2C_RAIL_EN2', value: 0x0D},
{register: 'PWR_FAULT_MASK1', value: 0x80},
{register: 'PWR_FAULT_MASK2', value: 0x31},
{register: 'GPO1PG_CTRL1', value: 0xFE},
{register: 'GPO1PG_CTRL2', value: 0xFF},
{register: 'GPO4PG_CTRL1', value: 0xFF},
{register: 'GPO4PG_CTRL2', value: 0xFF},
{register: 'GPO2PG_CTRL1', value: 0xFF},
{register: 'GPO2PG_CTRL2', value: 0xFF},
{register: 'GPO3PG_CTRL1', value: 0x80},
{register: 'GPO3PG_CTRL2', value: 0x7D},
{register: 'MISCSYSPG', value: 0x7F},
{register: 'VTT_DISCH_CTRL', value: 0x5F},
{register: 'LDOA1_SWB2_CTRL', value: 0x54},
{register: 'BUCK1_CTRL_EN1', value: 0xFF},
{register: 'BUCK1_CTRL_EN2', value: 0xFB},
{register: 'BUCK1_CTRL_EN3', value: 0x10},
{register: 'BUCK2_CTRL_EN1', value: 0xFE},
{register: 'BUCK2_CTRL_EN2', value: 0xCB},
{register: 'BUCK2_CTRL_EN3', value: 0x10},
{register: 'BUCK3_CTRL_EN1', value: 0xC4},
{register: 'BUCK3_CTRL_EN2', value: 0x6B},
{register: 'BUCK3_CTRL_EN3', value: 0x09},
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{register: 'BUCK4_CTRL_EN2', value: 0xEB},
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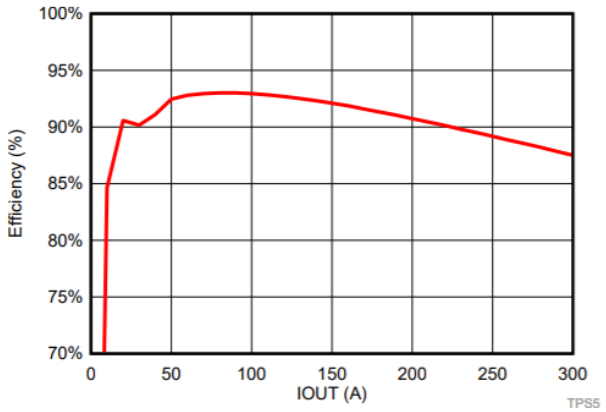
{register: 'BUCK6_CTRL_EN3', value: 0x01},
{register: 'SWA1_CTRL_EN1', value: 0xEC},
{register: 'SWA1_CTRL_EN2', value: 0x0B},
{register: 'SWA1_CTRL_EN3', value: 0x01},
{register: 'LDOA2_CTRL_EN1', value: 0xFF},
{register: 'LDOA2_CTRL_EN2', value: 0x5F},
{register: 'LDOA2_CTRL_EN3', value: 0x00},
{register: 'LDOA3_CTRL_EN1', value: 0xFF},
{register: 'LDOA3_CTRL_EN2', value: 0x1F},
{register: 'LDOA3_CTRL_EN3', value: 0x80},
{register: 'SWB1_CTRL_EN1', value: 0x8C},

```
{register: 'SWB1_CTRL_EN2', value: 0xEB},
{register: 'SWB1_CTRL_EN3', value: 0x08},
{register: 'SWB2_LDOA1_CTRL_EN1', value: 0xFF},
{register: 'SWB2_LDOA1_CTRL_EN2', value: 0x7F},
{register: 'SWB2_LDOA1_CTRL_EN3', value: 0x00},
{register: 'OTP_RSVD_38_28', value: 0x18},
{register: 'SLP_PIN', value: 0xFF},
{register: 'OUTPUT_MODE', value: 0x27},
{register: 'OTP_RSVD_38_2C', value: 0xA1},
{register: 'OTP_RSVD_38_2E', value: 0xAA},
{register: 'OTP_RSVD_38_32', value: 0x61},
{register: 'OTP_RSVD_38_34', value: 0xAA},
{register: 'OTP_RSVD_38_38', value: 0x61},
{register: 'OTP_RSVD_38_3A', value: 0xAA},
{register: 'OTP_RSVD_38_44', value: 0x05},
{register: 'OTP_RSVD_38_48', value: 0x25},
{register: 'OTP_RSVD_38_4C', value: 0x25},
{register: 'OTP_RSVD_38_53', value: 0xAE},
{register: 'I2CADDRESS', value: 0x00}];
```

1.4 Considerations

Tests here below focus on the meeting the demanding Xilinx Versal power requirements, especially in terms of output ripple and transient load response, and on the customized PMP22165 board designed specifically for the Xilinx Versal platform to provide all the outputs except for the main high current (165A max) VCCINT rail. For more details of operation of that rail, refer to the TPS53681 EVM user's guide. The main 6 phase rail was used with no hardware changes, only 2 GUI settings as described below for Vout and dynamic response were changed. Switching frequency remains the same at 500 kHz. Hence, the detailed efficiency data taken for 900mV can be extrapolated to 800mV by subtracting 1% from the values shown.

With the conservative assumption that losses at 800mV output are the same as losses at 900mV with switching frequency the same 500 kHz, the 93% peak efficiency at 900mV becomes 92% at 800mV.This is slightly conservative as transformer AC / core losses are slightly less at 800mV than 900mV due to lower peak to peak flux. From the EVM User's guide:



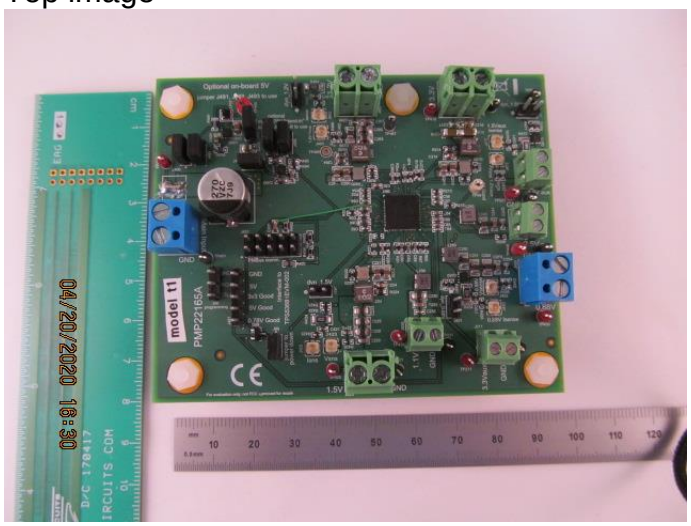
V_{OUT} = 0.9 V, V_{IN} =12 V

Figure 12. VOUT A Power Stage Efficiency

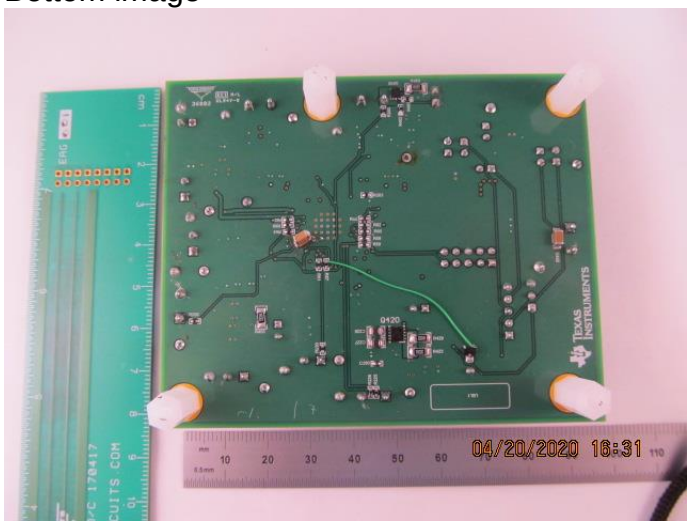
Section 1.5: PMP22165 Top & Bottom Images

3.75 inches by 3 inches

Top image



Bottom image



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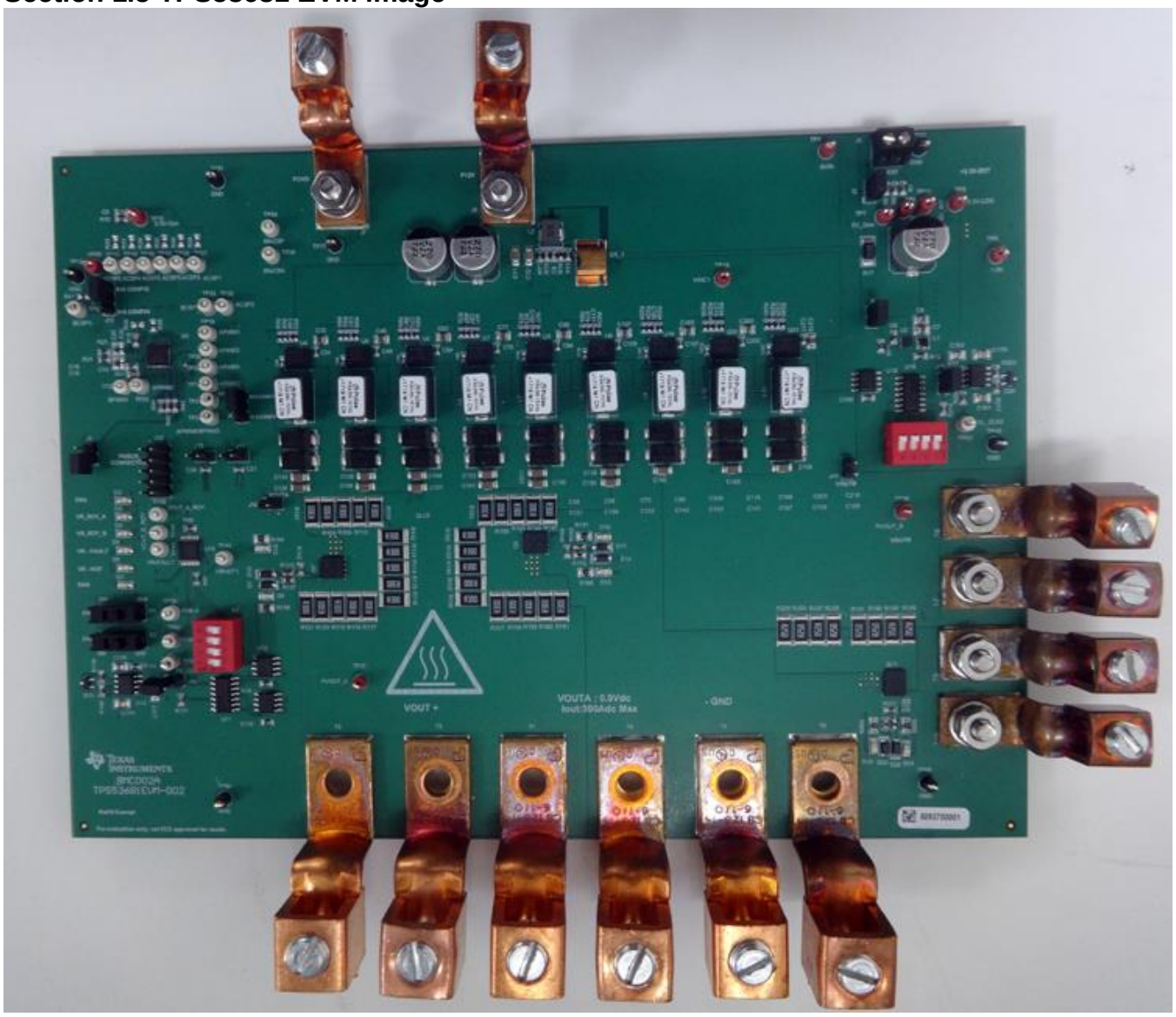
Section 1.5 TPS53681 EVM image

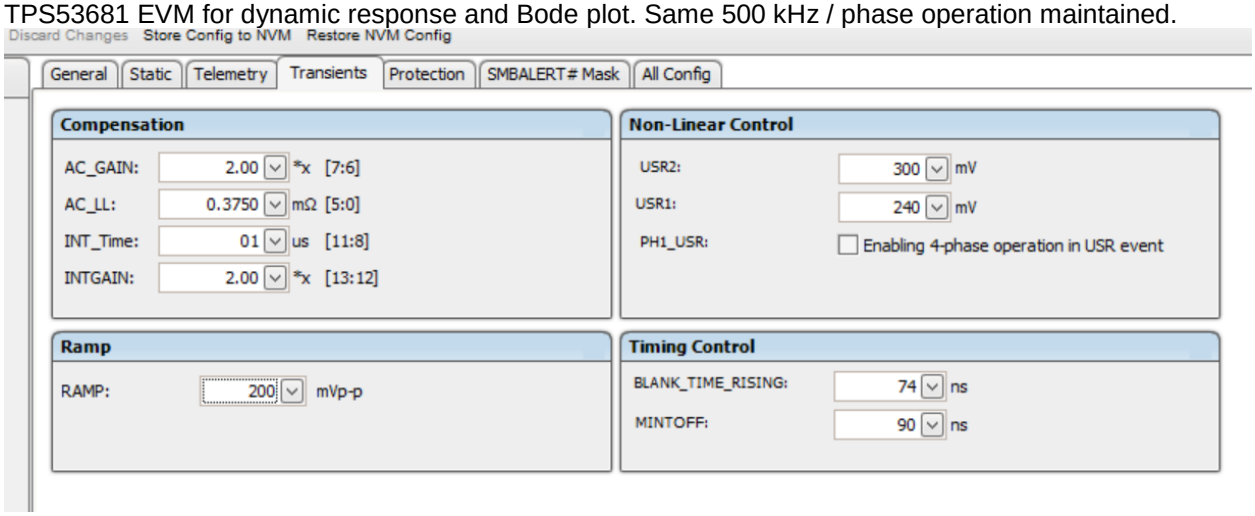


Testing and Results (Tests done by Josh Mandelcorn & Mitchell Spears)

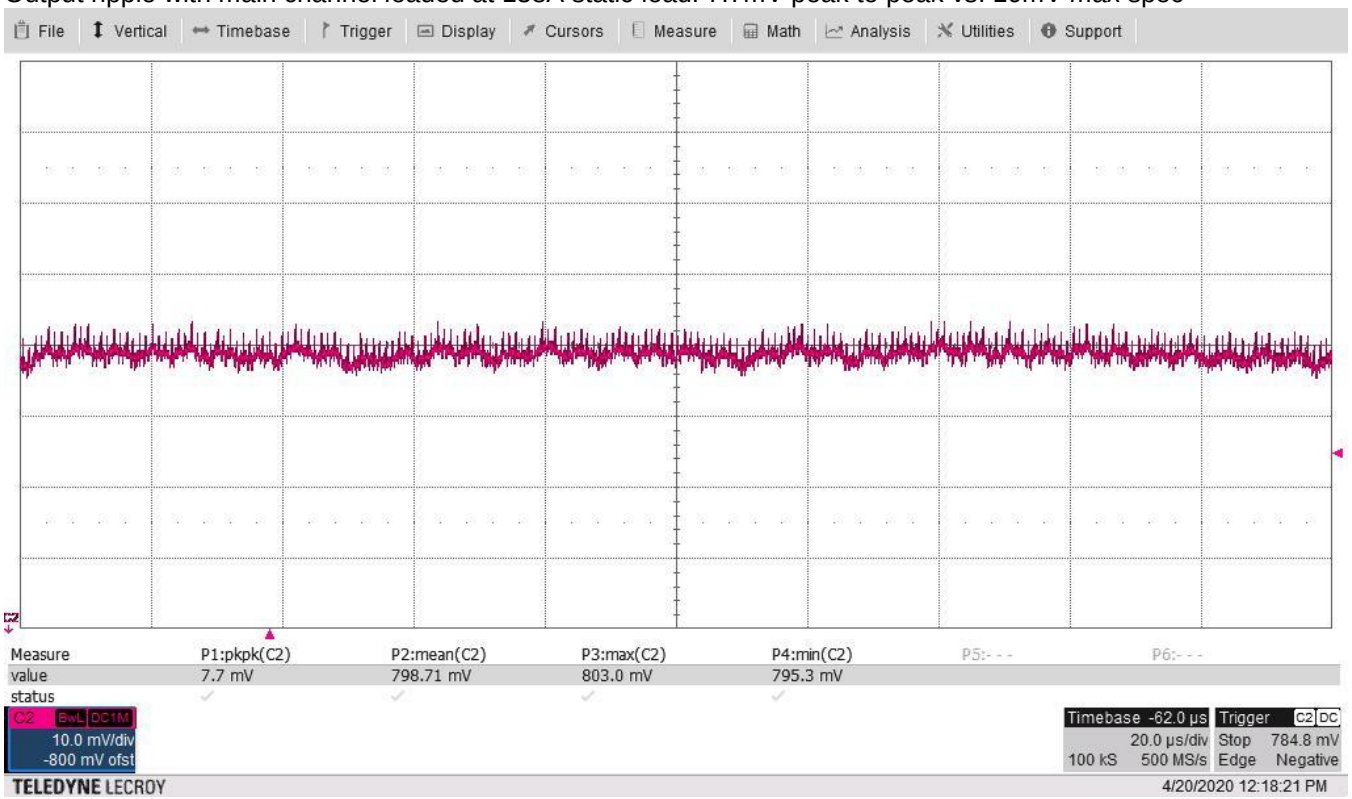
Section 2 overall will be output ripple and dynamics

Section 2.1 Main 800mV channel on the TPS53681 EVM: ripple & dynamics

Only changes from default GUI settings are Vout from 0.9V to 0.8V and AC_LL from 0.5mOhm to 0.375mOhm. This AC_LL setting of 0.375 is the midpoint between 0.5 conservative default setting and 0.25mOhms used in the TPS53681 EVM for dynamic response and Bode plot. Same 500 kHz / phase operation maintained.



Output ripple with main channel loaded at 138A static load: 7.7mV peak to peak vs. 10mV max spec



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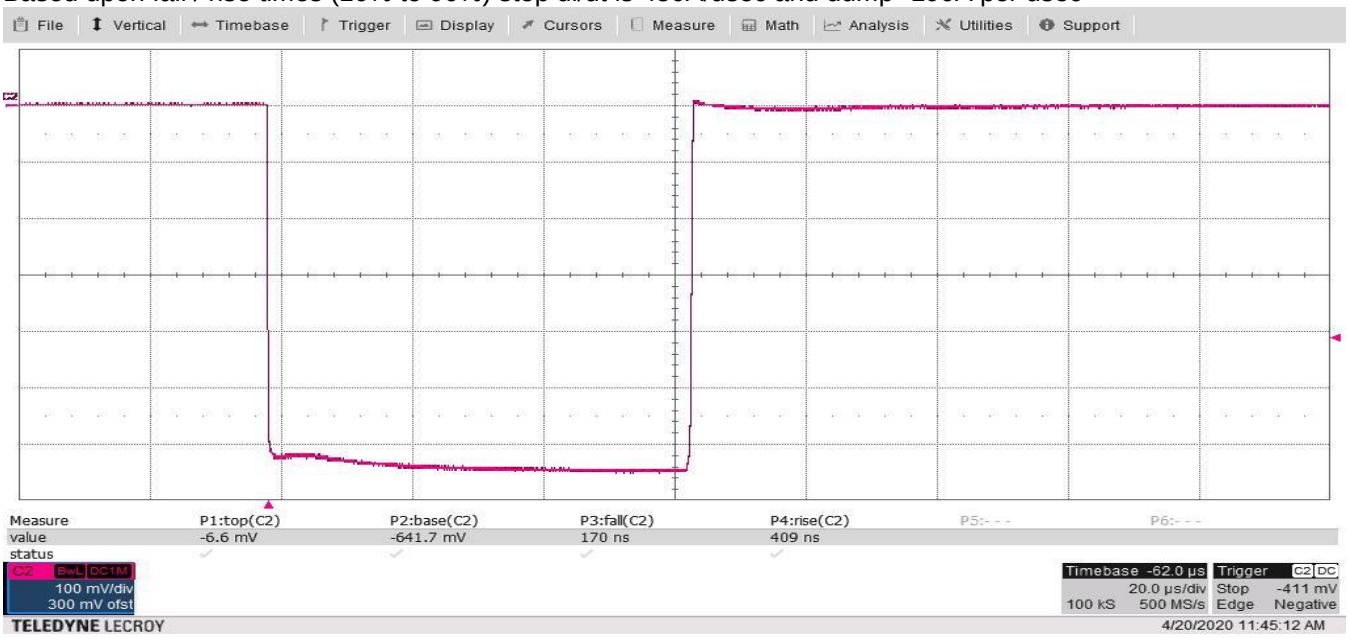
Section 2.1 Main 800mV channel on the TPS53681 EVM continued:

Dynamic load response:
First shown is test pulse across 1 of 45 300mOhm dynamic load resistors
640/300 is 2.13A times 45 is 96A or 60% of 160A
Based upon fall / rise times (10% to 90%) step di/dt is 450A/usec and dump -190A per usec



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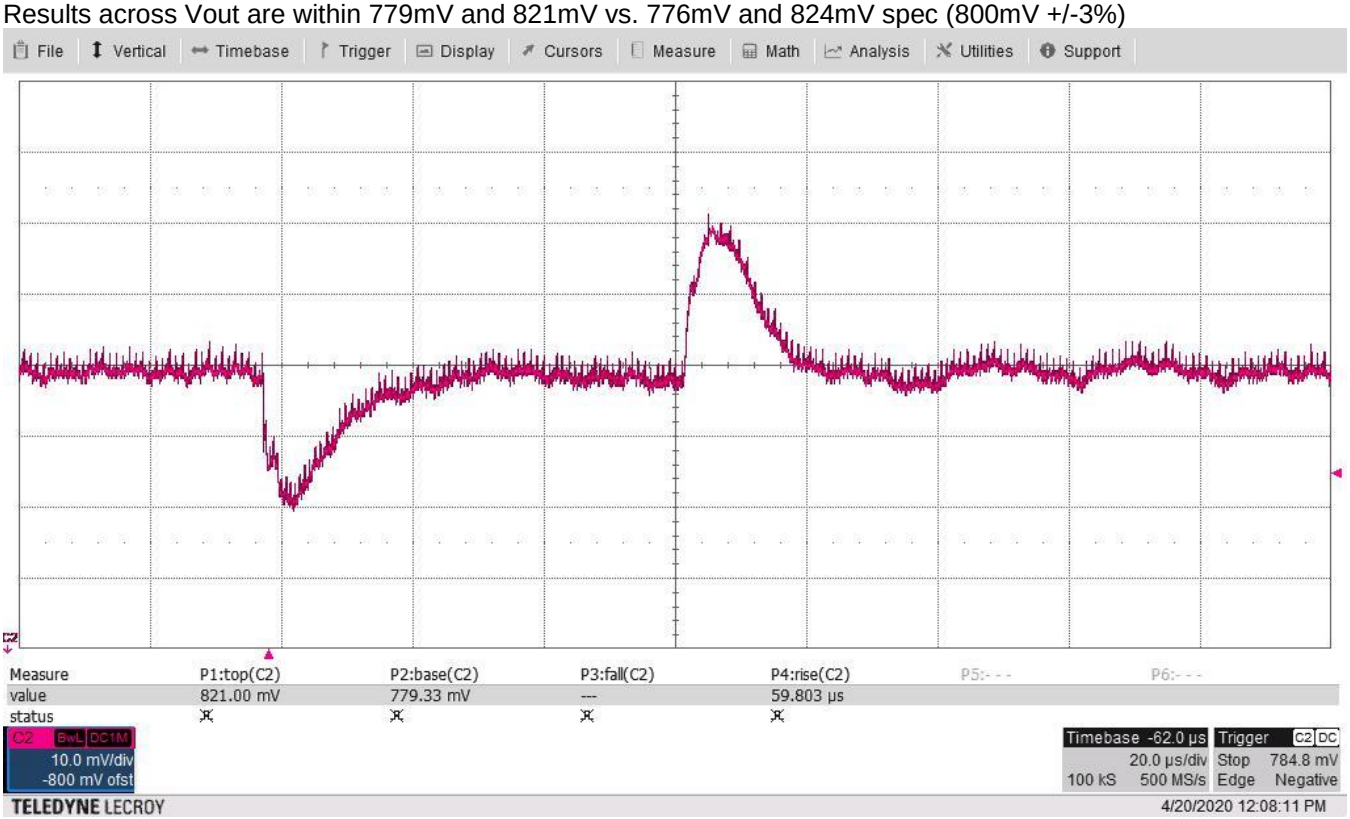
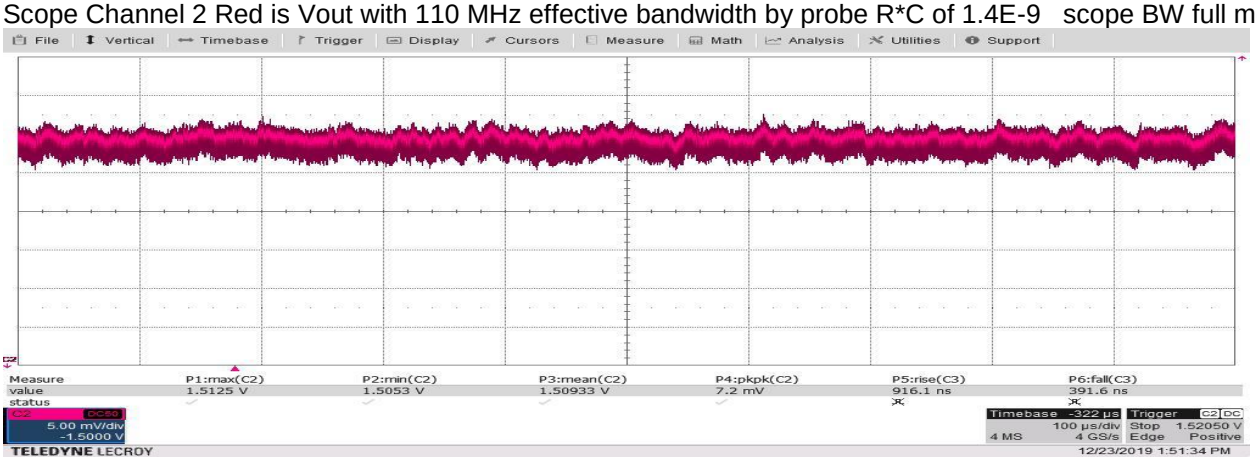
Results across Vout are within 779mV and 821mV vs. 776mV and 824mV spec (800mV +/-3%)



Now to the channels on the PMP22165 board itself

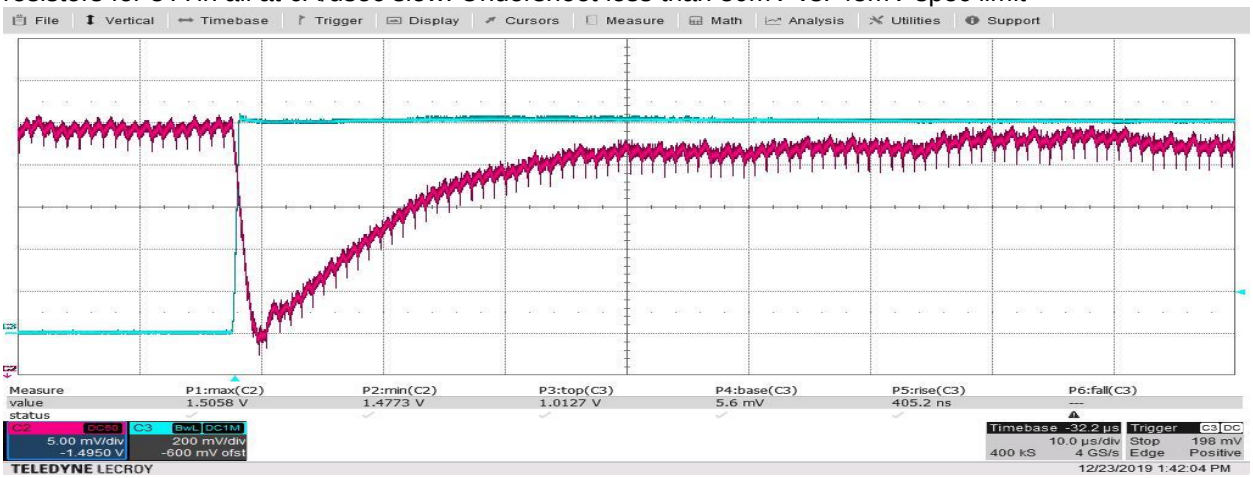
Section 2.2 1.5V 4.2A channel ripple & dynamics

1.5V 4.2A full load ripple: Xilinx requires at least 80 MHz bandwidth for this channel's measurements
Scope Channel 2 Red is Vout with 110 MHz effective bandwidth by probe R*C of 1.4E-9 scope BW full model t2

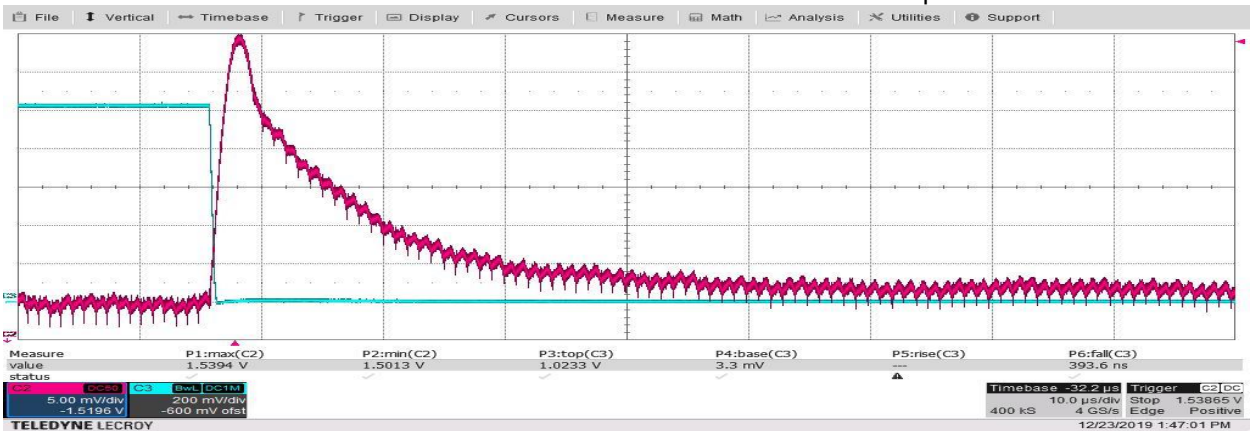


Spec is 10mV p-p max, measured 7.2mV p-p over 1000usec

1.5V output with 1 A static load and 3 A step load:
Scope Channel 2 Red is Vout with 110 MHz effective bandwidth, channel 3 green is voltage across 3x 1 ohm load resistors for 3 A in all at 6A/usec slew. Undershoot less than 30mV vs. 45mV spec limit



& dump.
Scope Channel 2 Red is Vout with 110 MHz effective bandwidth, channel 3 green is voltage across 3x 1 ohm load resistors for 3 A in all at -6A/usec slew. Overshoot less than 40mV vs. 45mV spec limit



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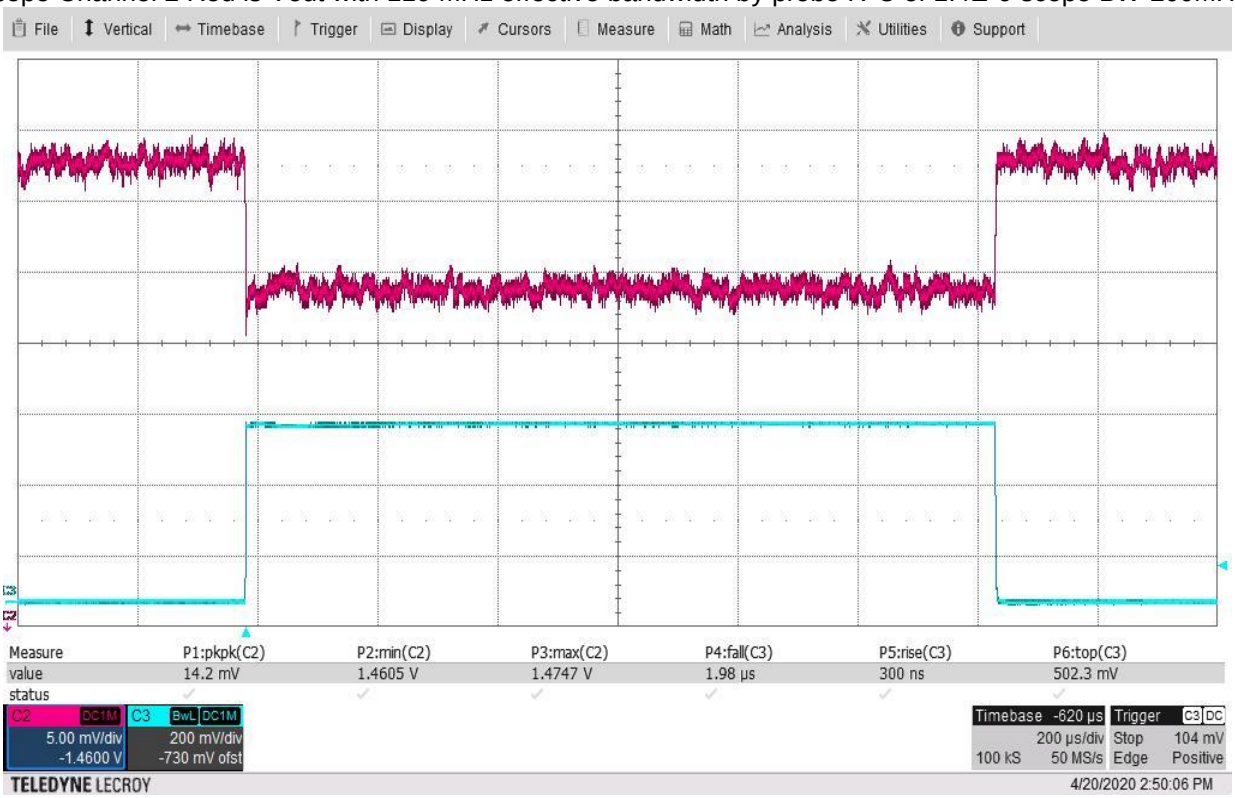
Section 2.3 1.5V 200mA channel ripple & dynamics

1.5V MGTAVAUX: 200mA max 10mV p-p max at 80MHz BW +/-3% @ 25% step / dump

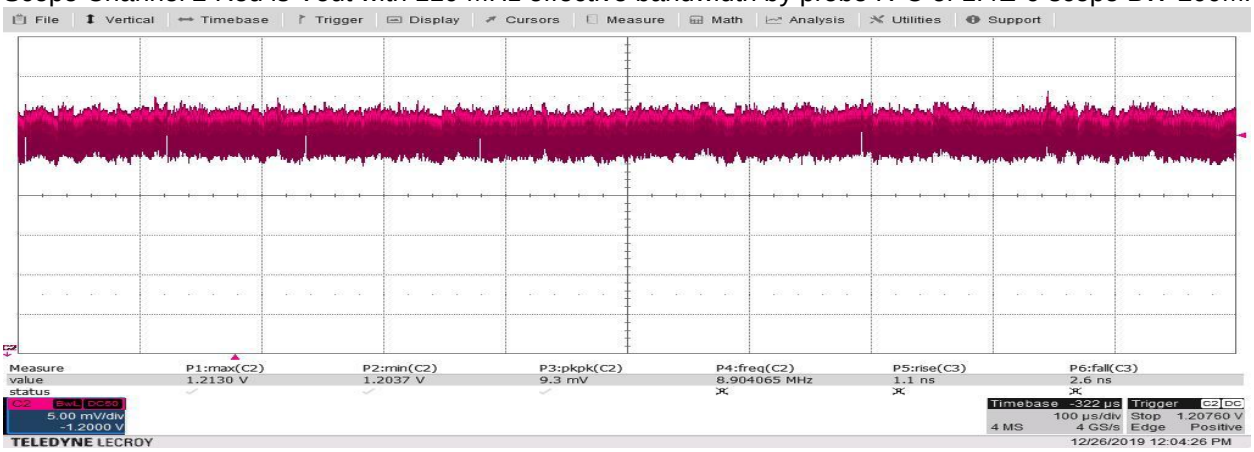
10	MGTAVAUX	1.5V	±3%	0.1 - 0.2A	25%	10mV pk-pk ripple at FPGA pins.

1V5 Transient at 150mA static and 50mA dynamic to 200mA min 1.460V vs. 1.455 spec min limit (1.5V -3%)
4.7uF size 0603 bypass cap near test point. (C472 on PCB) Full load ripple less than 5mV p-p
Scope Channel 2 Red is Vout with 110 MHz effective bandwidth by probe R*C of 1.4E-9 scope BW 200MHz

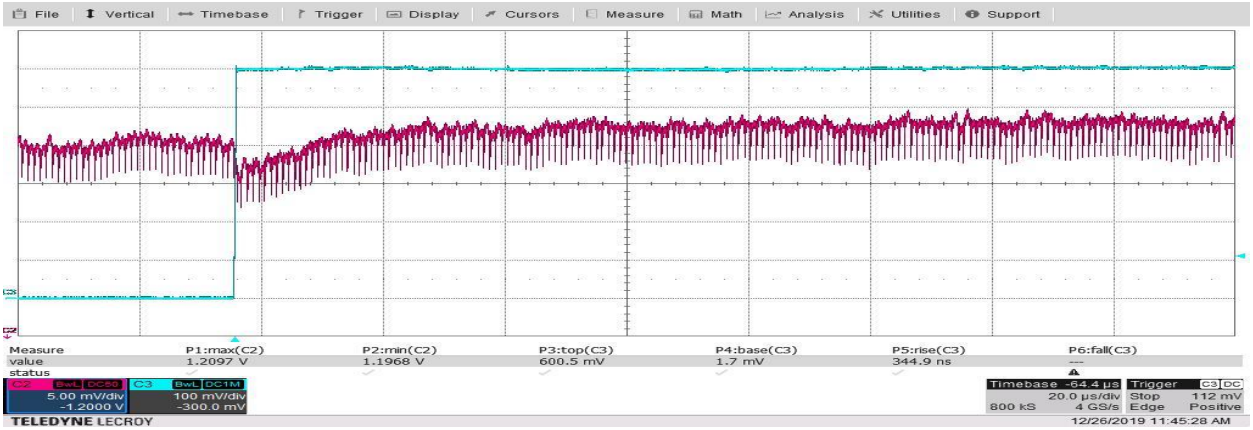


Section 2.4 1.2V 4.8A channel ripple & dynamics

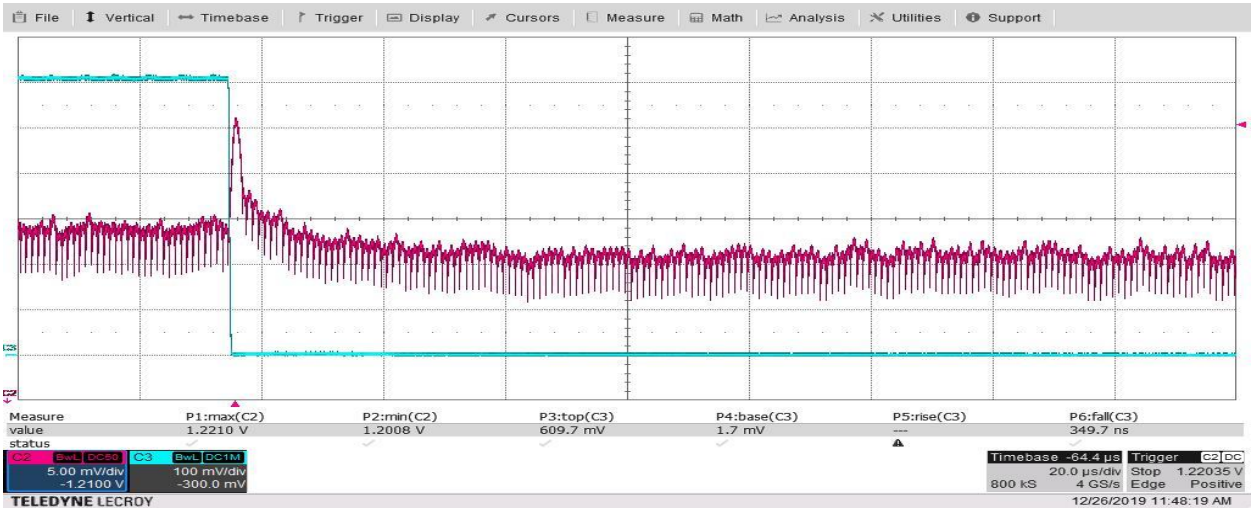
1.2V 4.8A full load ripple TP460 removed and trace to it cut model t1
Scope Channel 2 Red is Vout with 110 MHz effective bandwidth by probe R*C of 1.4E-9 scope BW 200MHz



Spec is 10mV p-p max, measured 9.3mV p-p over 1000usec
1.2V output with 3 A static load and 1.2 A step load:
Scope Channel 2 Red is Vout with 110 MHz effective bandwidth, channel 3 green is voltage across 2x 1 ohm load resistors for 1.2 A in all at >2.4A/usec slew. Undershoot max about 5mV



& dump.
Scope Channel 2 Red is Vout with 110 MHz effective bandwidth, channel 3 green is voltage across 2x 1 ohm load resistors for 1.2 A in all at -2.4A/usec slew.
Overshoot less than 15mV vs. +/-36mV allowed band



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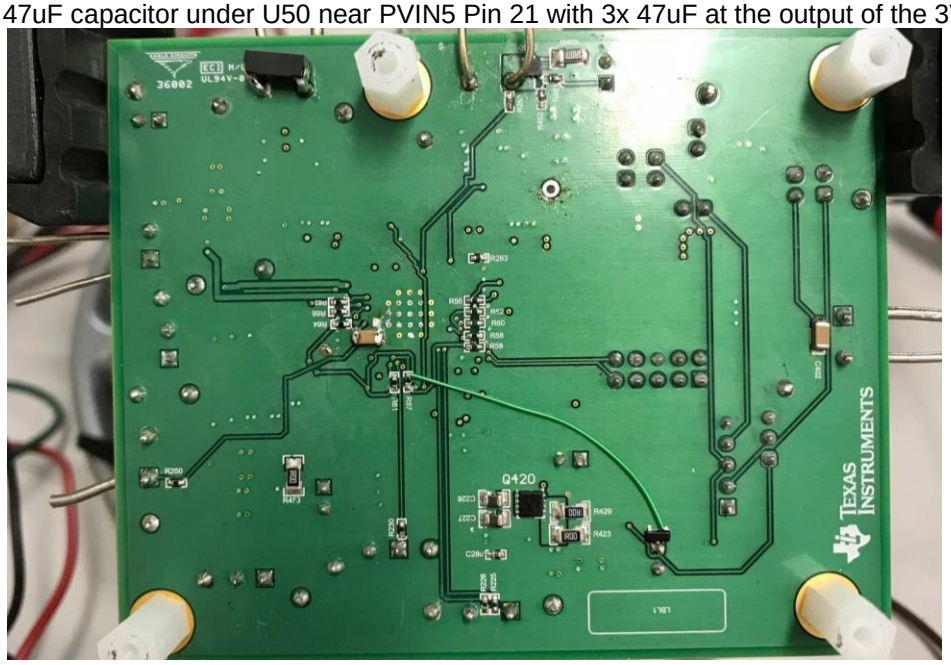
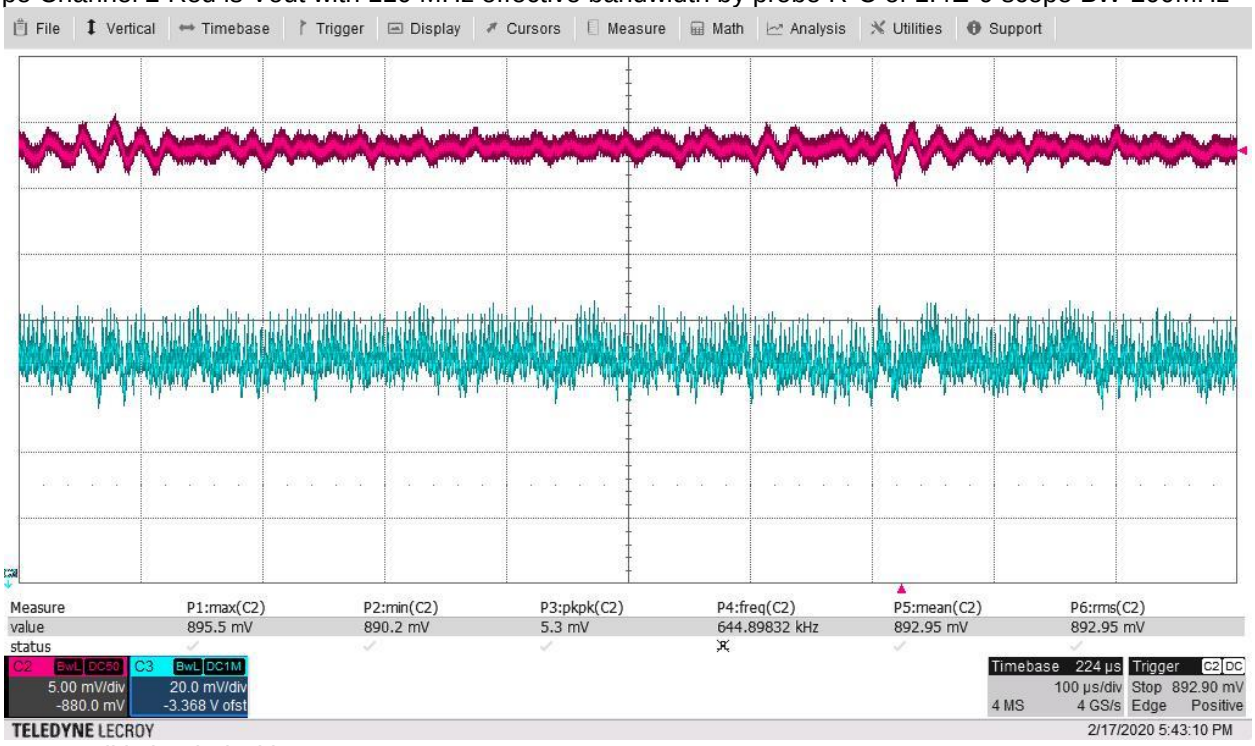
Section 2.5 0.88V 3.1A channel ripple & dynamics

0.88V testing for ripple / dynamics Model T3:
Made the following modifications to the board:
Added 47uF capacitor under U50 near PVIN5 Pin 21 with 3x 47uF at the output of the 3V3.



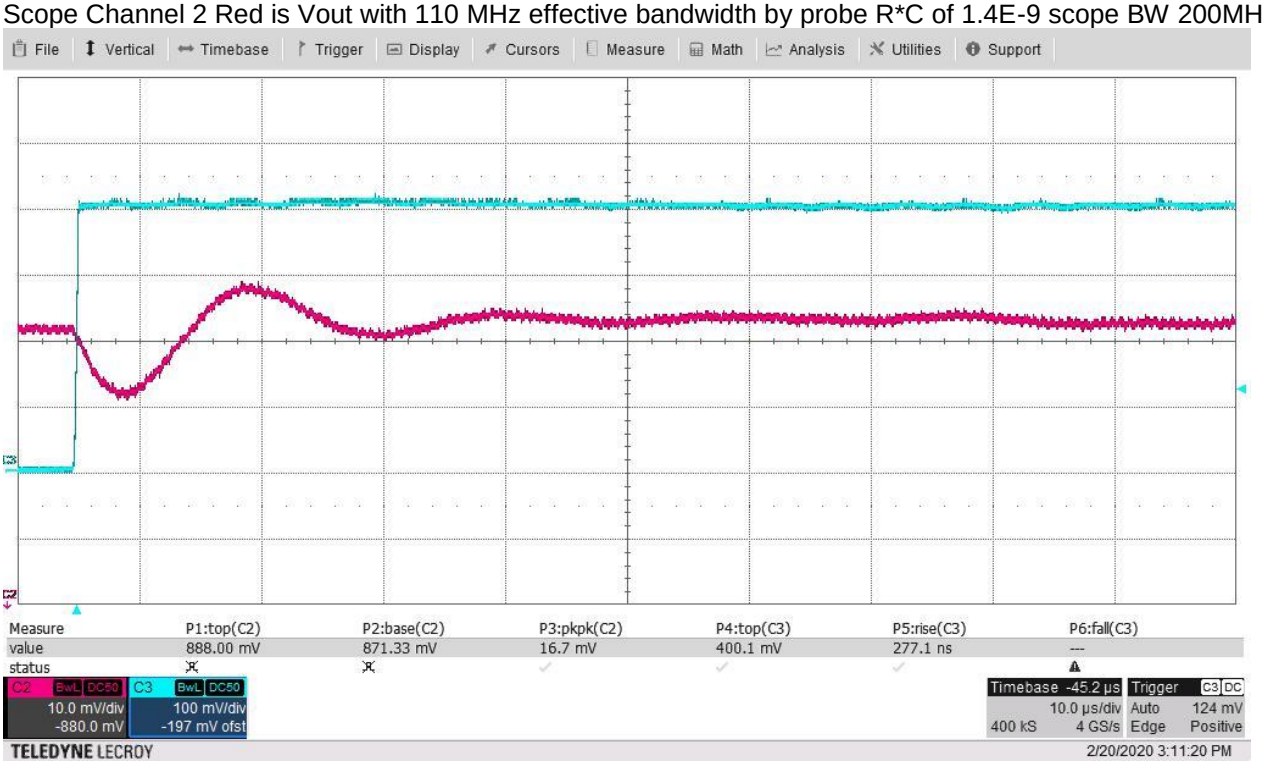
Output ripple on the 0.88V ~100MHz measurement spec 10mV p-p max @ 80 MHz BW
Scope Channel 2 Red is Vout with 110 MHz effective bandwidth by probe R*C of 1.4E-9 scope BW 200MHz



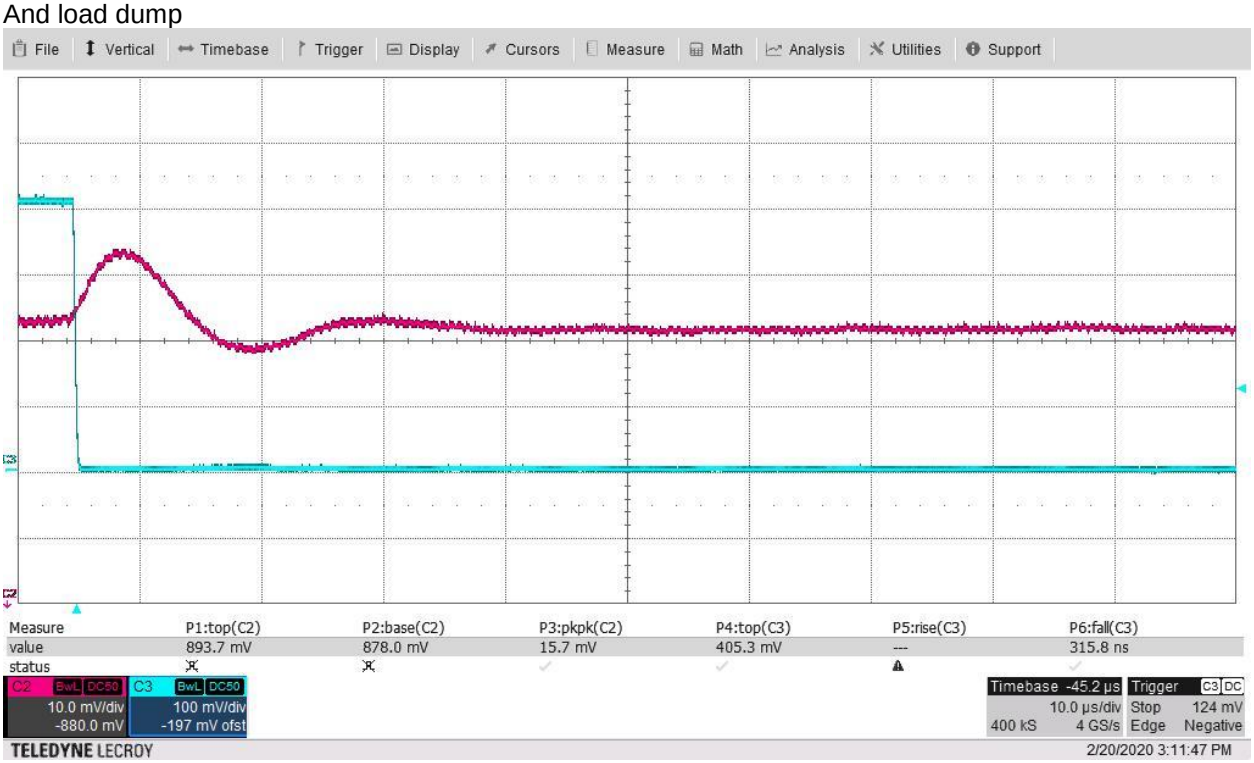
0.88V rail is loaded with 3A.

Section 2.5 0.88V 3.1A channel ripple & dynamics (continued)

0.88V transient response 1.5 static load 0.8A dynamic load (400mV across 2x 1.0 ohm for 800mA)
Step load response: +/-3% band allowed 856mV to 904mV range
Scope Channel 2 Red is Vout with 110 MHz effective bandwidth by probe R*C of 1.4E-9 scope BW 200MHz



And load dump



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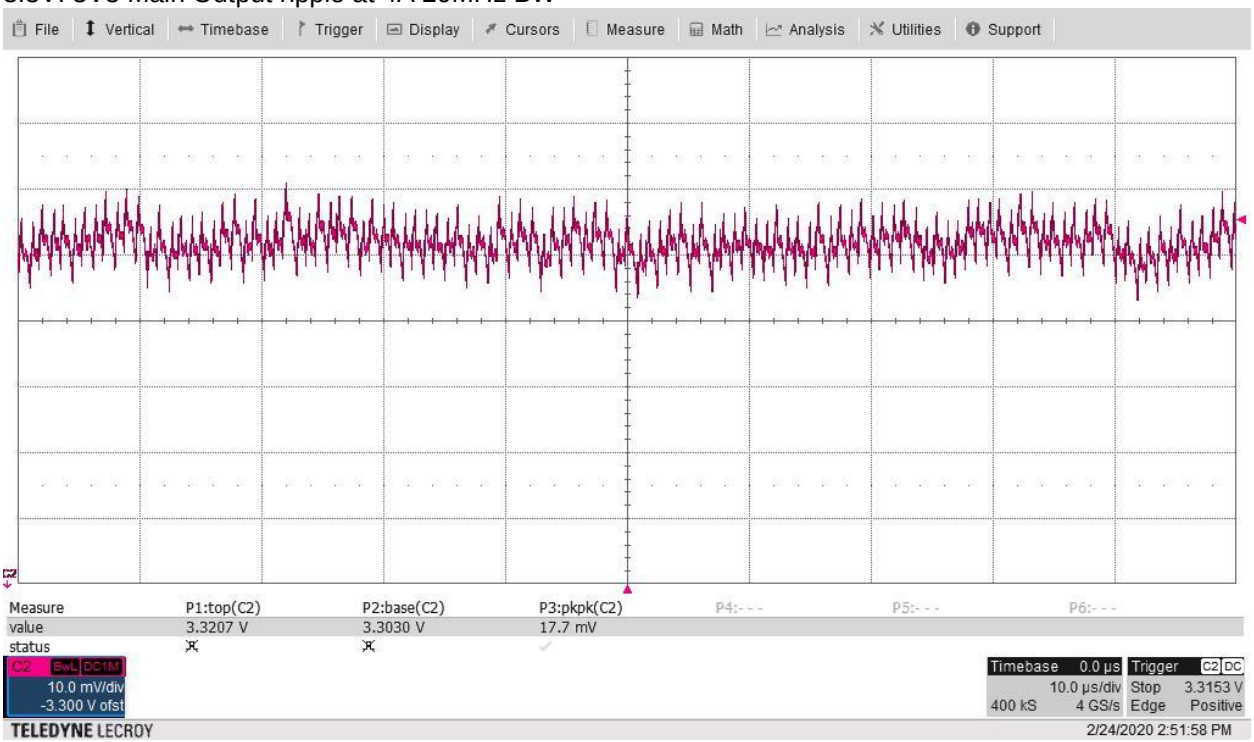
Section 2.6 3.3V main and 3.3V I/O ripple

3.3V: 3V3 Main Output ripple at 4A 20MHz BW



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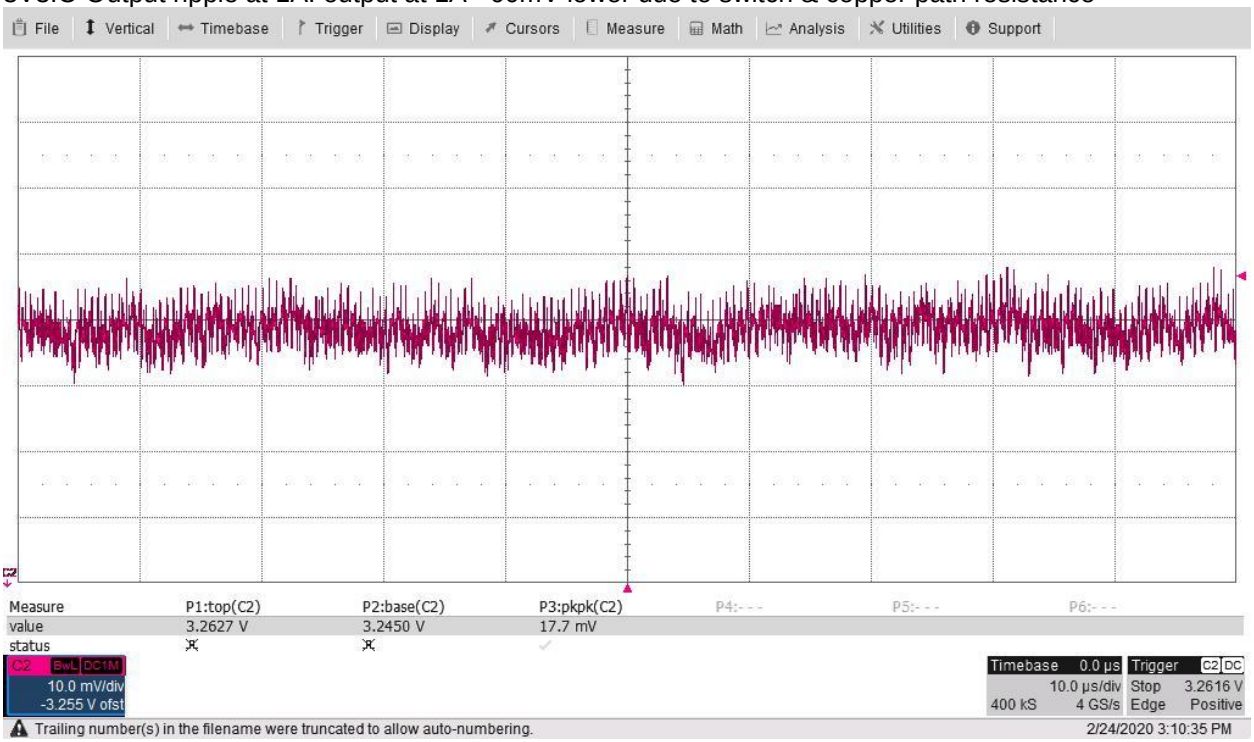
3V3IO Output ripple at 1A: output at 1A ~60mV lower due to switch & copper path resistance



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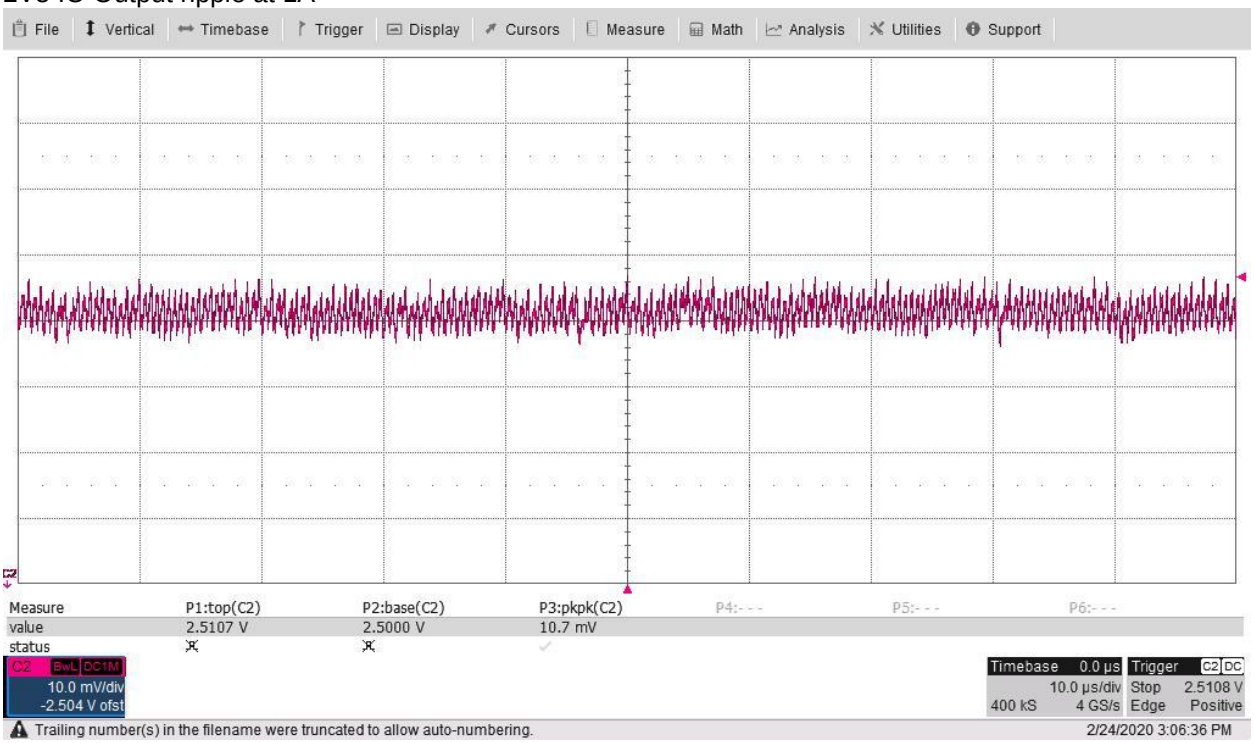
Section 2.7 2.5V I/O and 1.1V I/O ripple:

2V5 IO Output ripple at 1A



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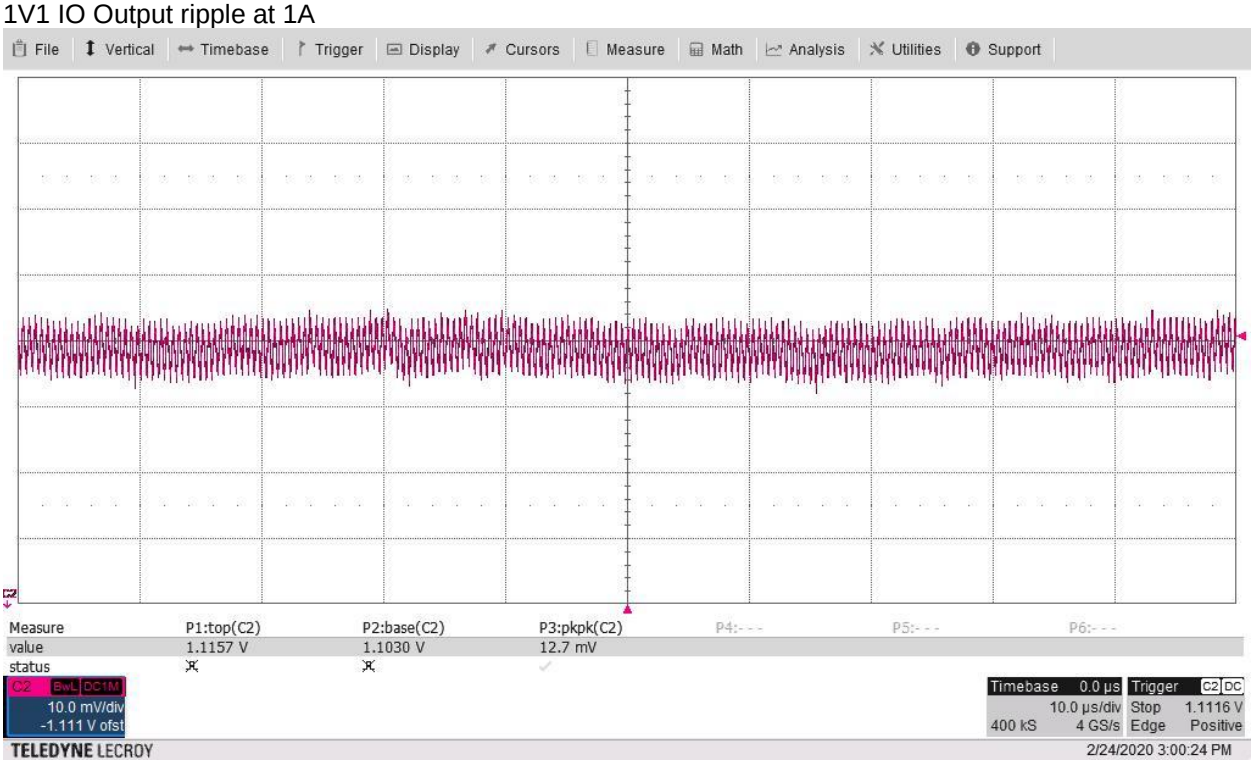
1V1 IO Output ripple at 1A



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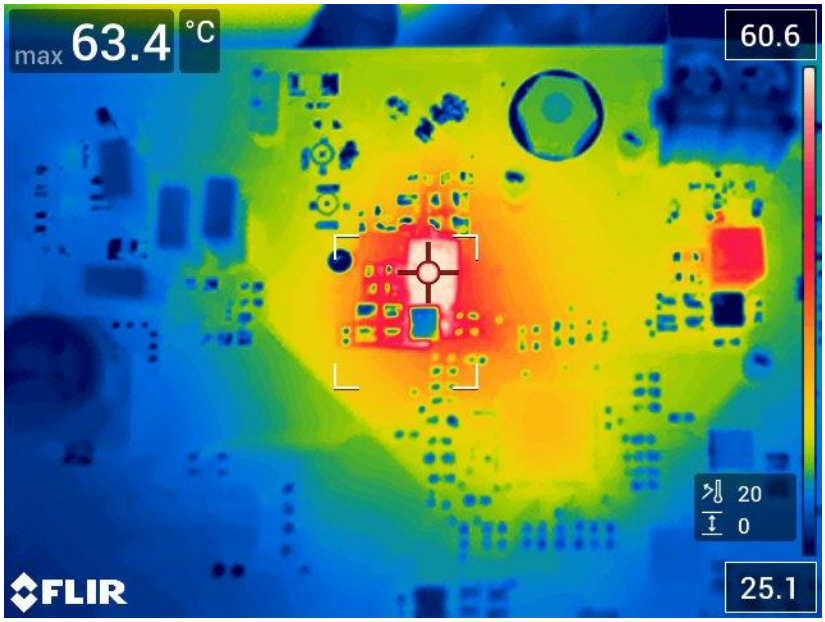
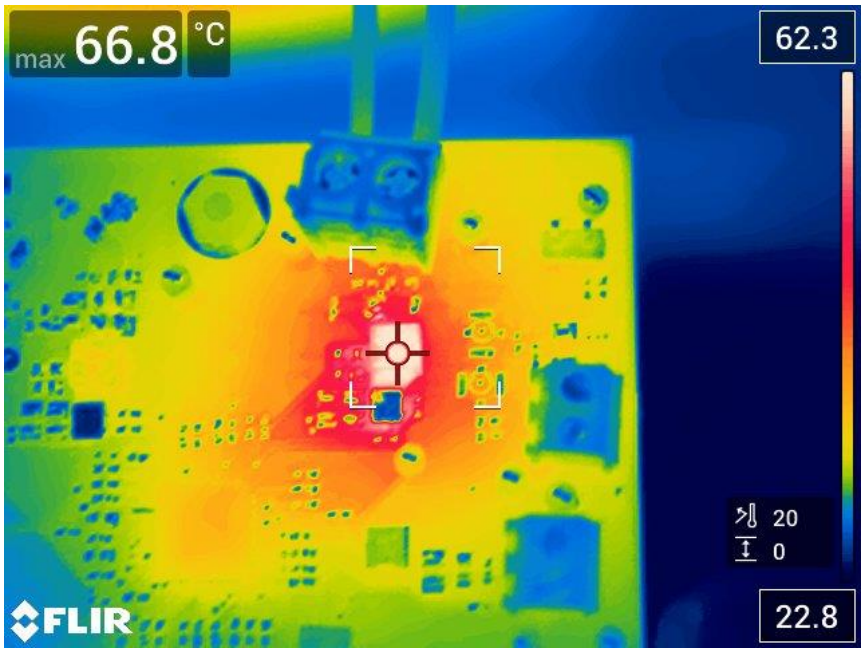
Section 3: thermal images page 1 of 3

1.2V at 4.8V converter off 12Vin: No fan



3.3V at 4A off 12Vin No fan



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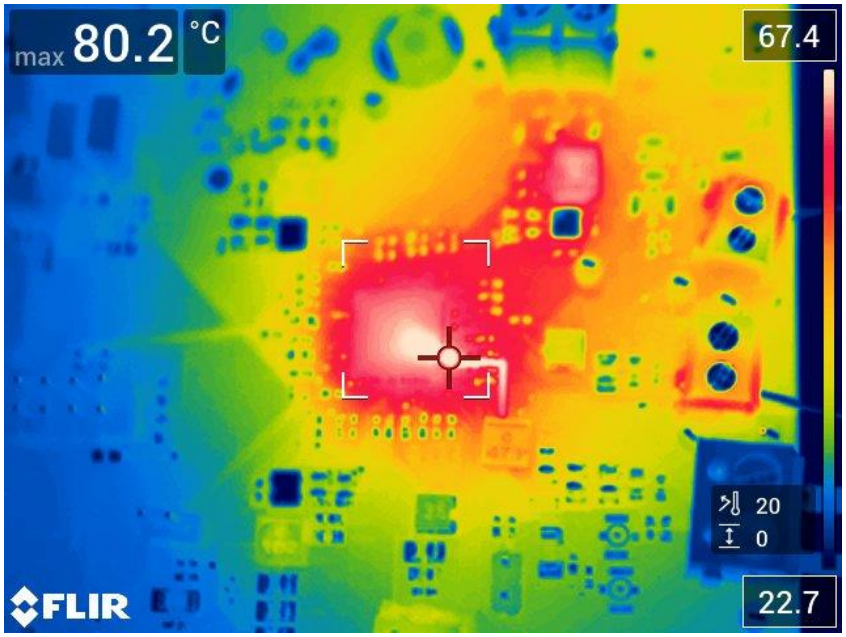
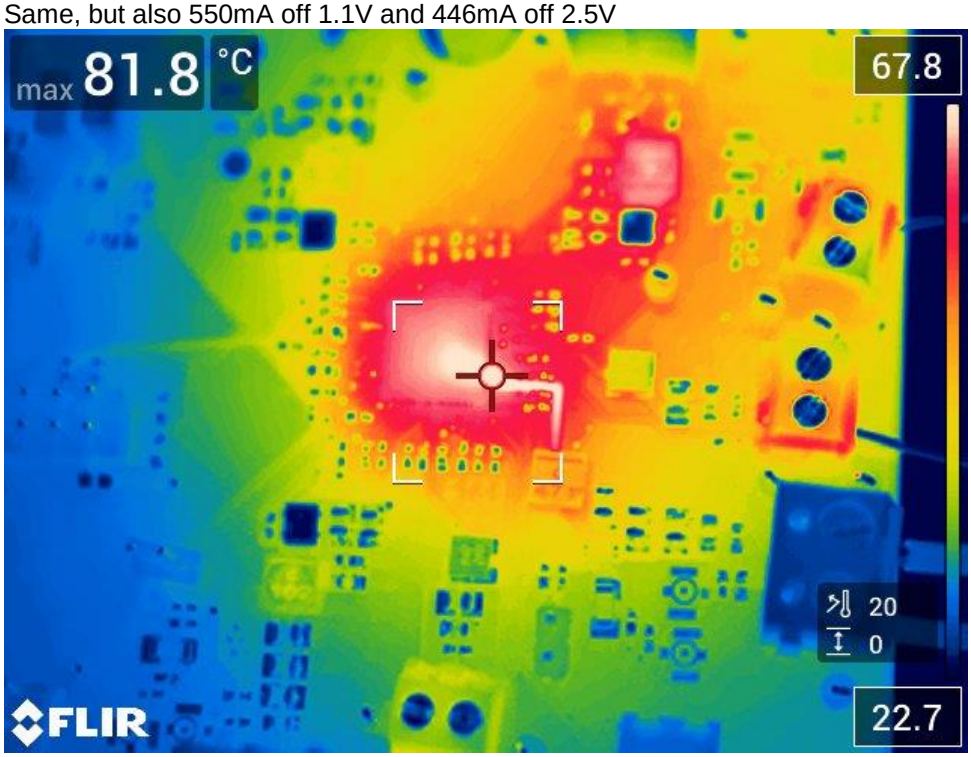
Section 3: thermal images continued page 2 of 3

0.88V off 3.3V TPS650861



Same, but also 550mA off 1.1V and 446mA off 2.5V



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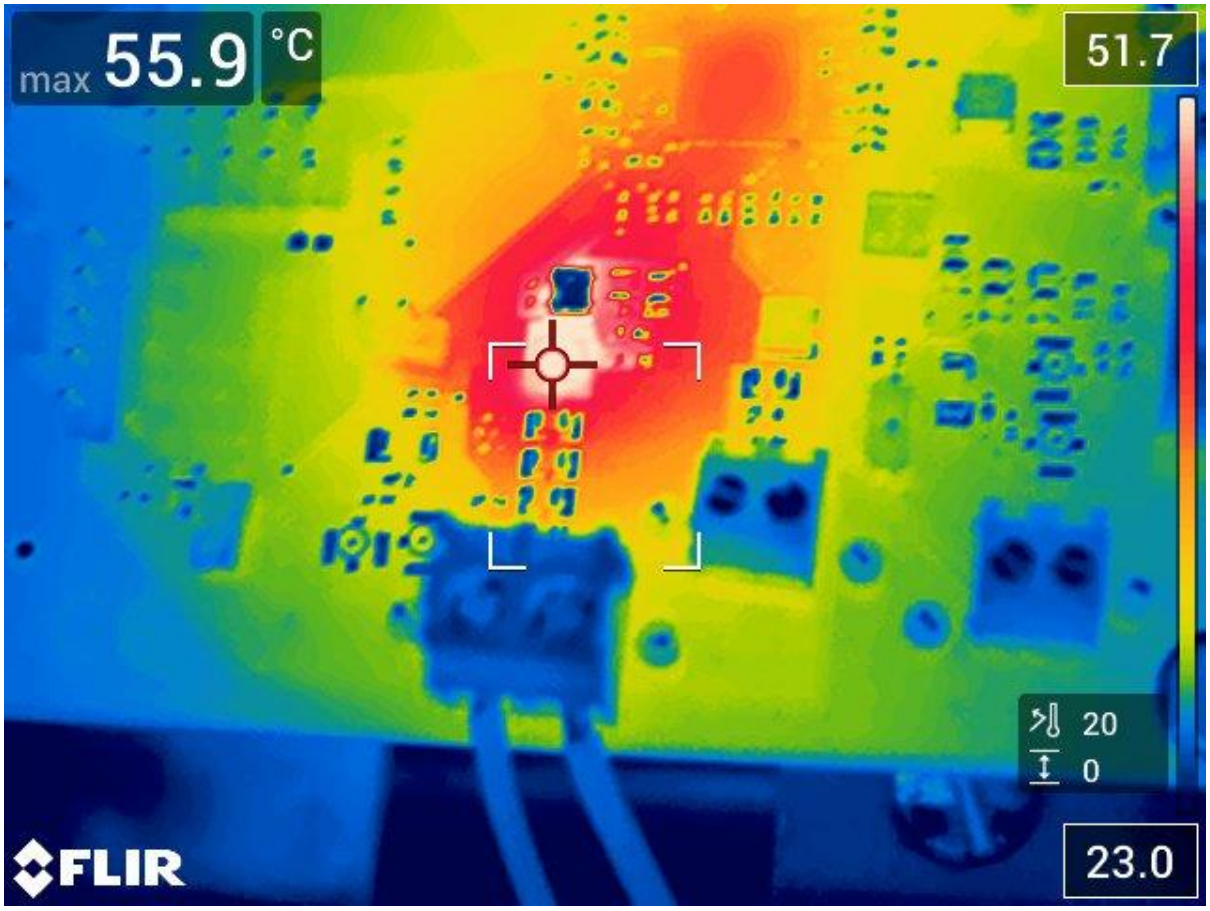
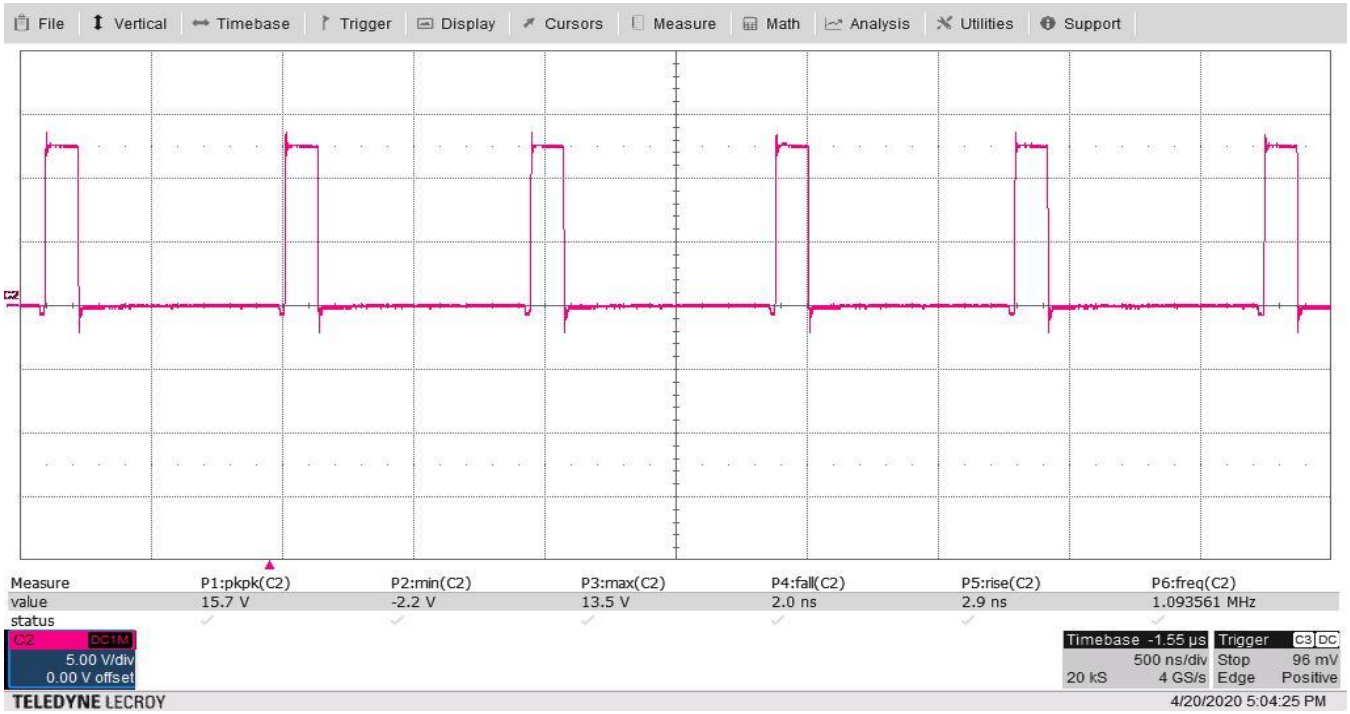
Section 3: thermal images continued page 3 of 3

1.5V 4.2A off 12Vin No fan

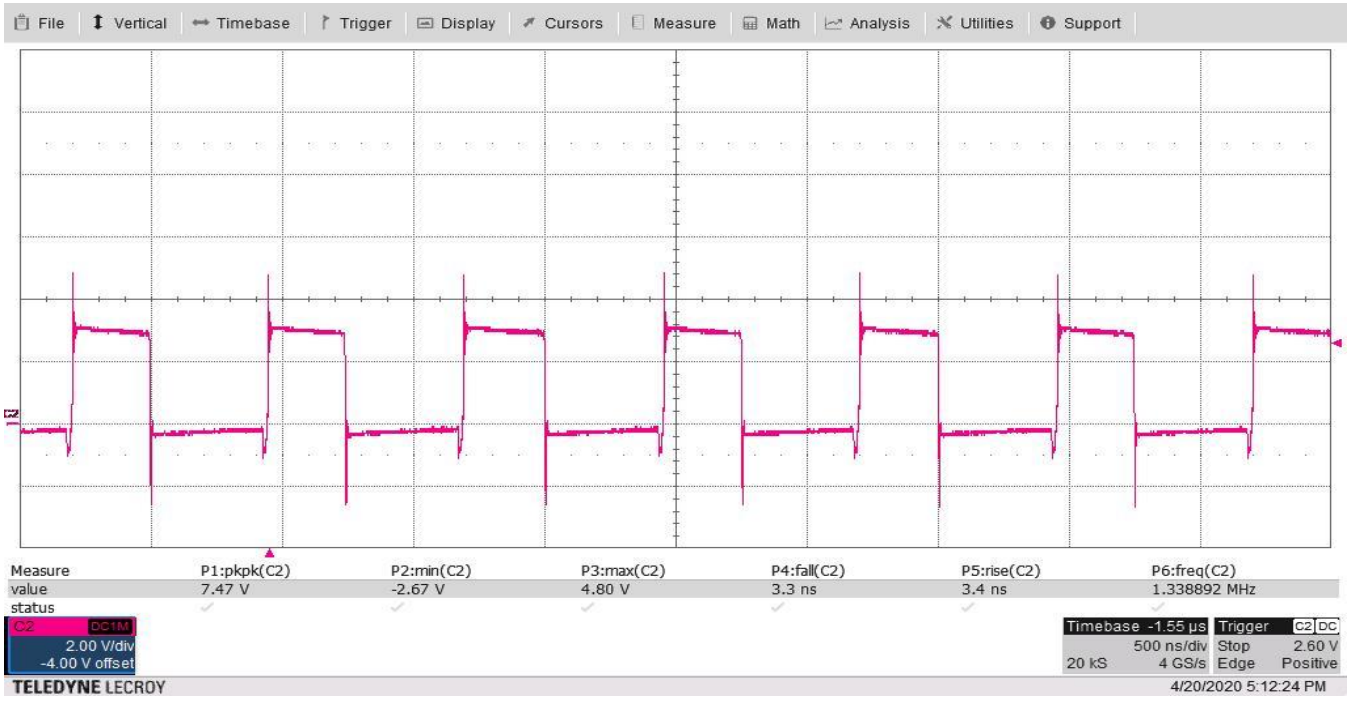


Section 4: major switching waveforms

Off 12V: 1.5V loaded to 4.8A

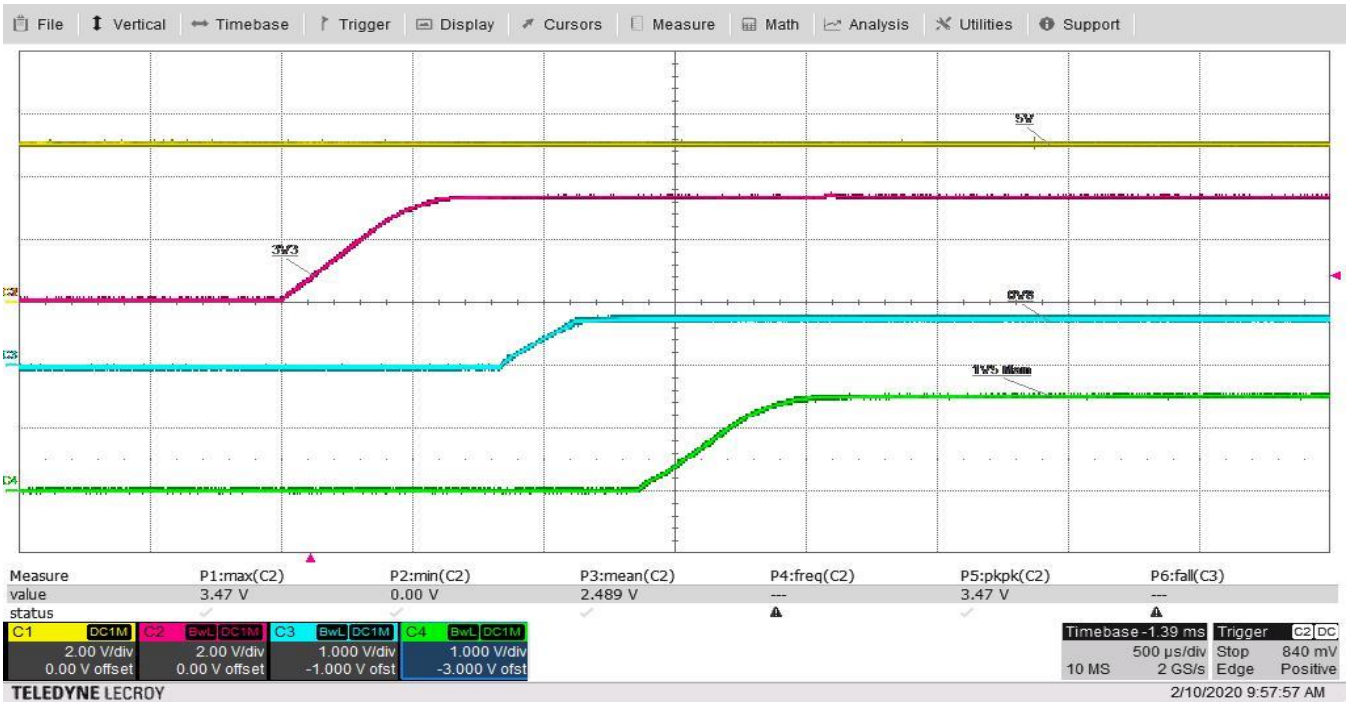


Off 3.3V 0.88V loaded to 3100mA

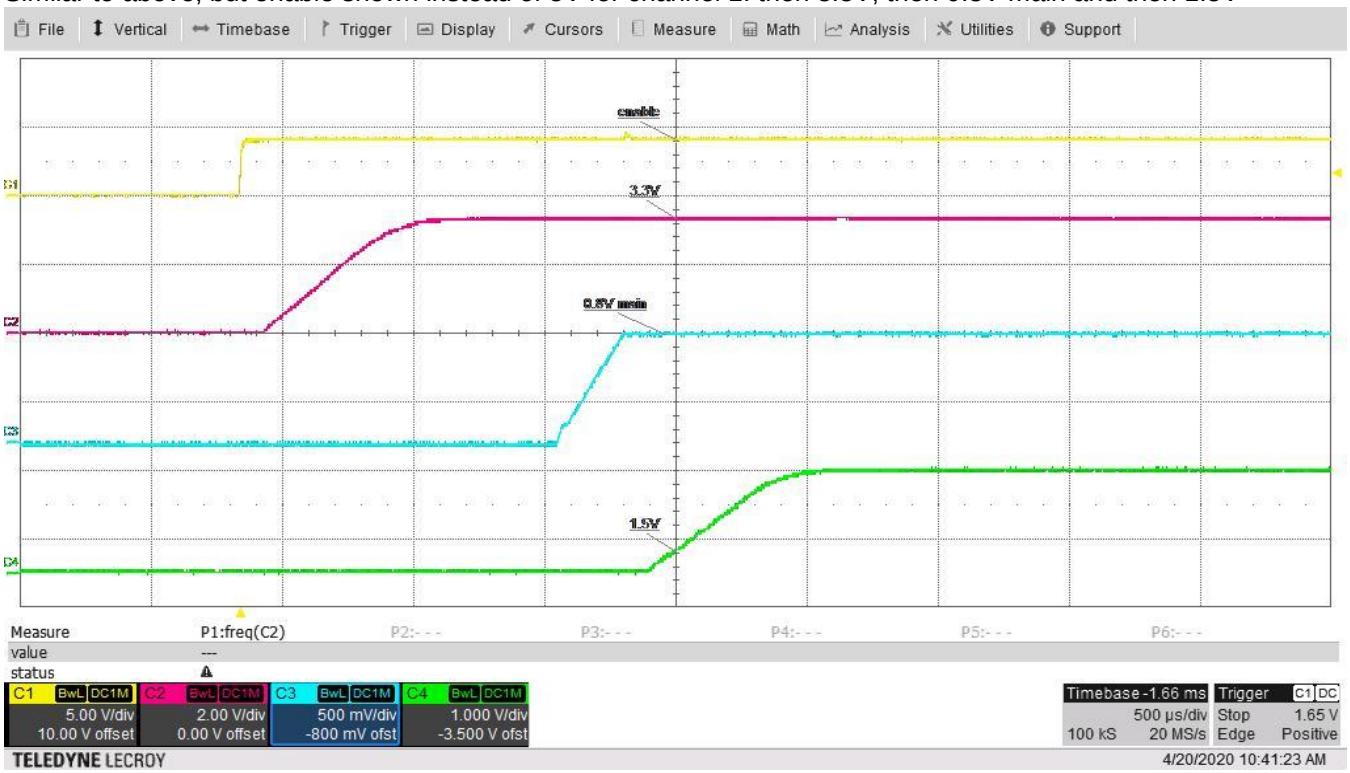


Section 5: Start up and sequencing page 1 of 2

Power up sequencing: This uses the on board 5V bias supply and fake main 0.8V.
5V for bias first and then main 3.3V and then “main 0.8V” and then main 1.5V

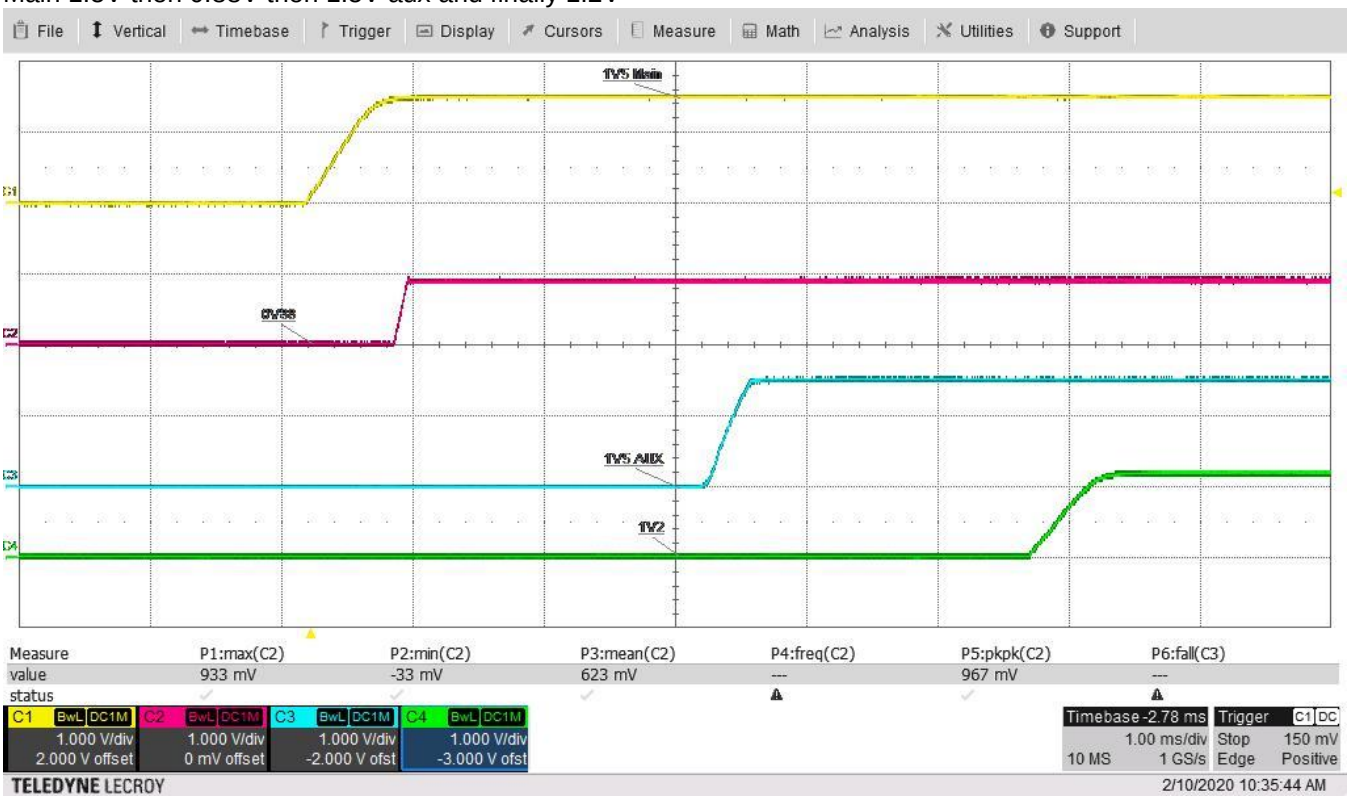


Power up sequencing with PMP22165 mated with TPS53681EVM:
Similar to above, but enable shown instead of 5V for channel 1: then 3.3V, then 0.8V main and then 1.5V



Section 5: Start up and sequencing continued: page 2 of 2

Main 1.5V then 0.88V then 1.5V aux and finally 1.2V



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I/O voltages coming up after 1.2V is up (2.5V, 3.3V_IO & 1.1V)

Q

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