Test Report: PMP31194

Automotive SEPIC Reference Design Using an Integrated FET

Description

This reference design is a small SEPIC auxiliary power supply using the LM5157-Q1 device with integrated FET. A highlight of this design is the small board space by achieving a reasonable efficiency, so switching frequency has been set to a tradeoff of 440 kHz. Output voltage can be set from 5 V to 7 V, depending on the load requirements.

Though the design has been tested up to 2-A peak current the continuous current is around 1 A, resulting in a reasonable temperature rise +30 K at the SMA rectifier (hottest spot). The maximum output current depends on the minimum input voltage due to peak current limitation.

Optional ORing diodes at the BIAS pin to supply the controller with output voltage are allowing cold cranking as low as 2 V after start up V_{IN} > 3 V. The undervoltage lockout UVLO allows a flexible set up.

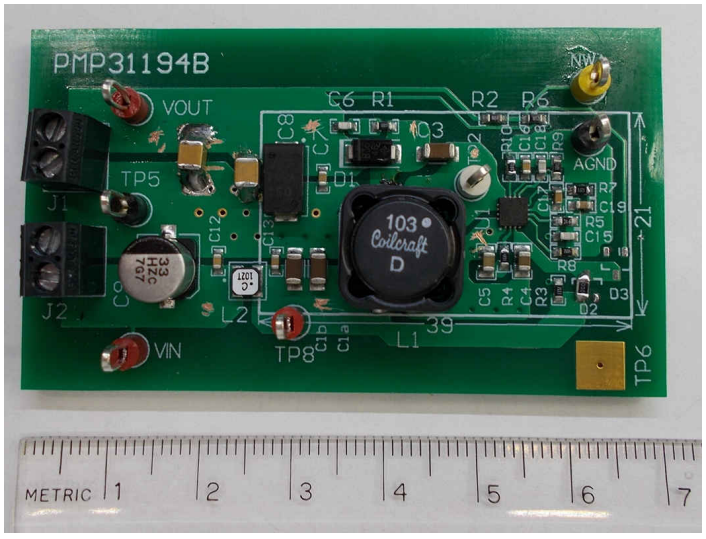
An optional tiny LC input filter attenuates reflected ripple. The inductor was selected for high self-resonance frequency to act beyond the FM band.

Features

- 6-V bias supply for automotive applications and general purposes, steps up and steps down
- Cost-effective with a single driver, single FET, and single rectifier
- High integration due to powerful internal FET
- Provides input filter to prevent FM band noise
- Supports ultra-low cold-cranking as low as 1.5-V input voltage by ORing diodes
- This reference design is completely built and has completed testing in a lab

Applications

- Steering wheel control



Top Board Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	8 V to 18 V
Output Voltage	6 V
Output Current	1 A_{CONT}, up to 2 A_{PK}
Estimated Switching Frequency	440 kHz
Topology	SEPIC
IC	LM5157-Q1

1.2 Considerations

Unless otherwise indicated, all measurements were done with 2-A output current. Resistors were used as load.

For all measurements dithering is disabled, R10 = 0 Ω.

The prototype on the bench showed a switching frequency of 437 kHz.

The ON threshold is 6 V and the OFF threshold is 4.7 V.

For lower output currents, LM5157**1**-Q1 with the same package and the same pin out is more cost-effective.

1.3 Dimensions

The size of the board is 68.6 mm × 39.4 mm. The board itself has two layers, using *single* side assembly. The copper thickness is 70 µm on each layer.

The bottom layer is a solid ground plane to achieve low noise at the radio frequency (RF) range. Images in this document do not reflect actual size.

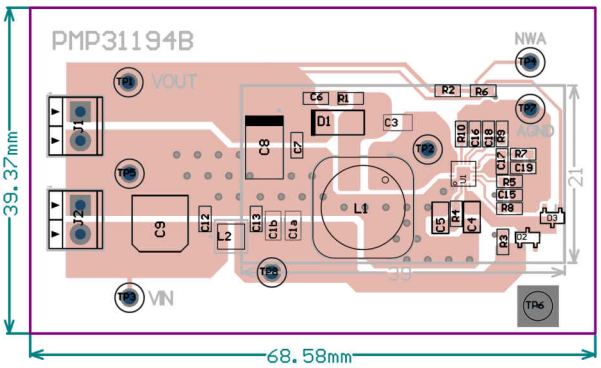


Figure 1-1. Layout Top Side

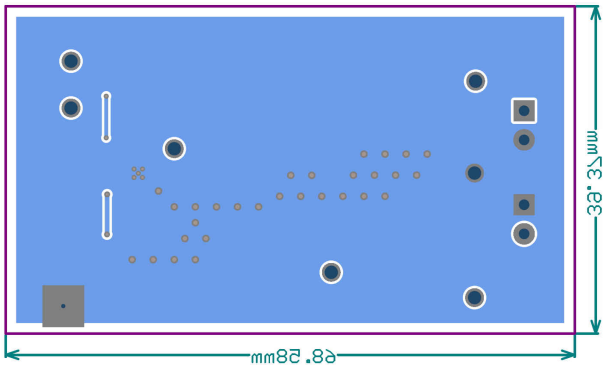


Figure 1-2. Layout Bottom Side

2 Testing and Results

2.1 Efficiency Graph

The input voltage of the power stage (TP8) was used for calculation of the efficiency and loss.

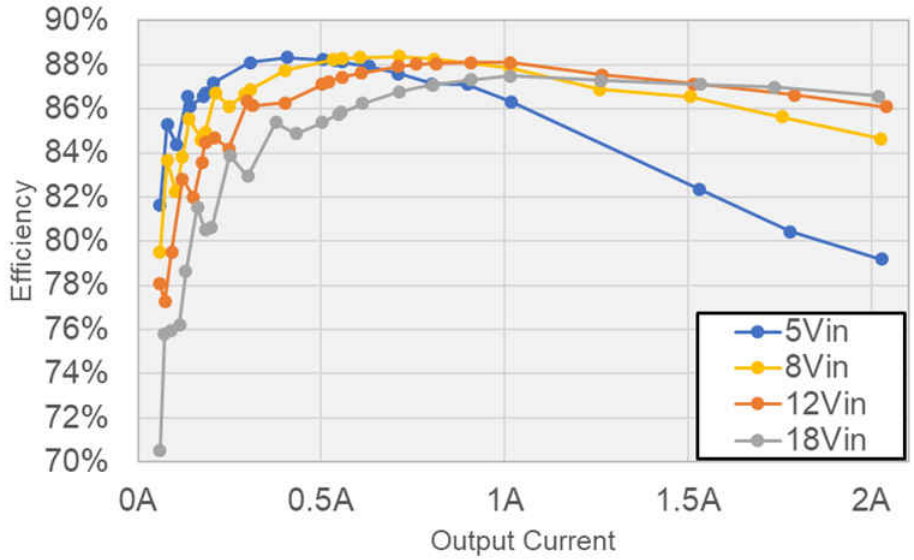


Figure 2-1. Efficiency Graph

The irregularity in the curve for 5-V input voltage at 0.8-A and 0.9-A output current is related to the measurement range change from the input current.

At nominal input voltage, 12 V and efficiency of 88% can be achieved at nominal output current 1 A.

2.2 Loss Graph

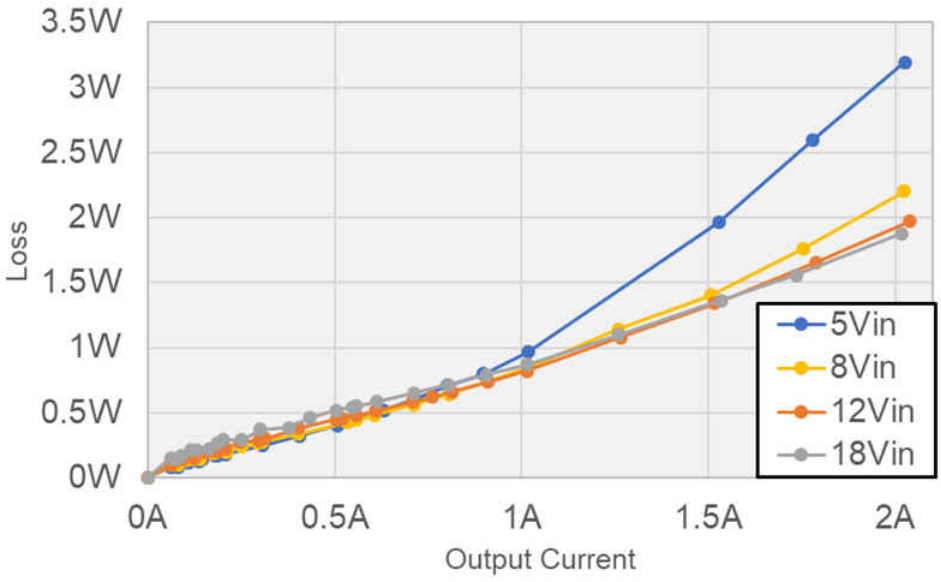


Figure 2-2. Loss Graph

2.3 Load Regulation

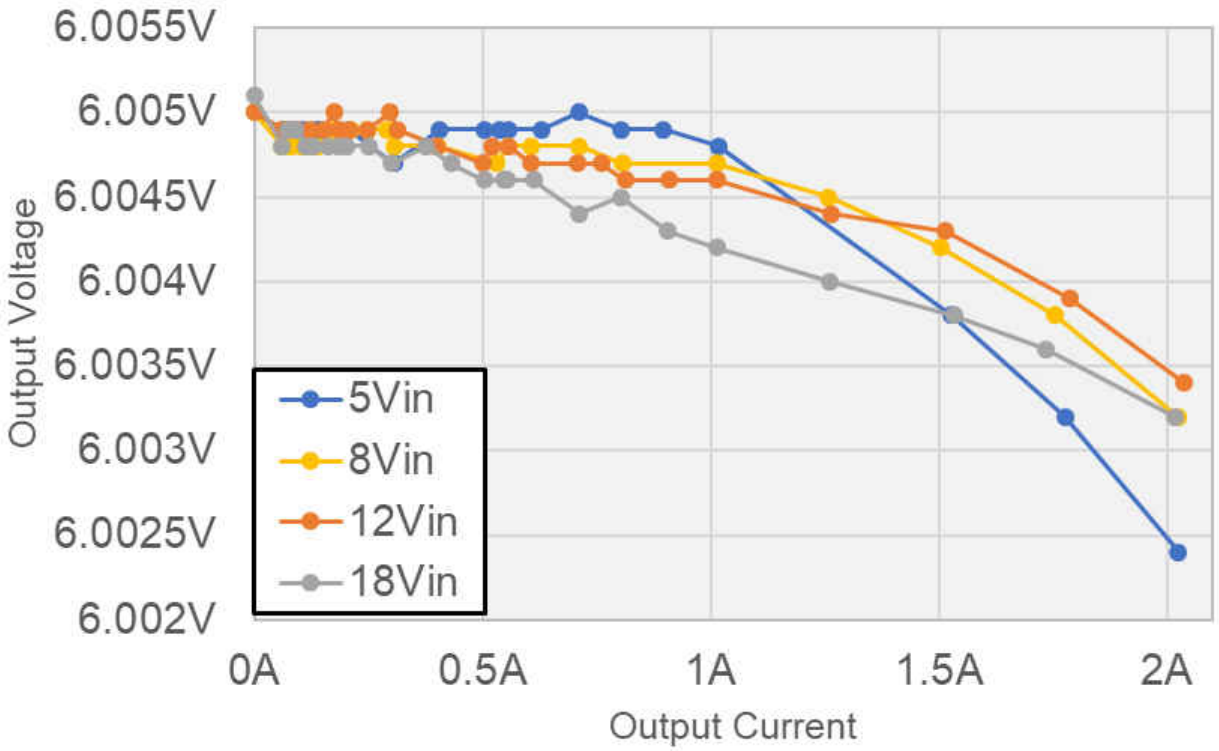


Figure 2-3. Output Voltage vs Output Current

2.4 Line Regulation

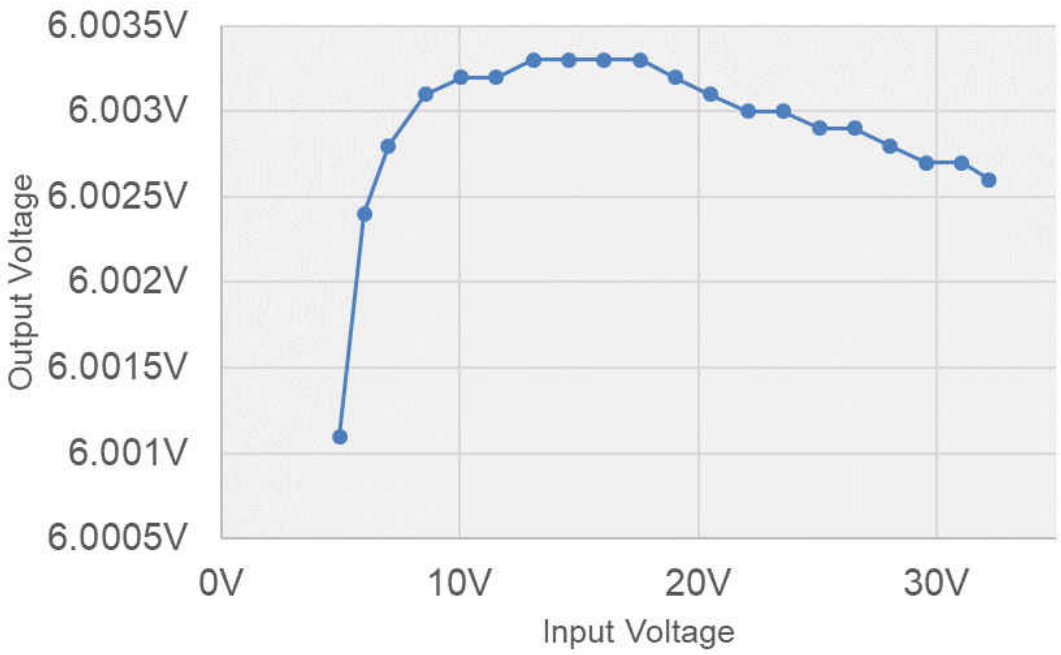


Figure 2-4. Output Voltage vs Input Voltage of Power-Stage

The measurement for line regulation data was gathered for efficiency and loss.

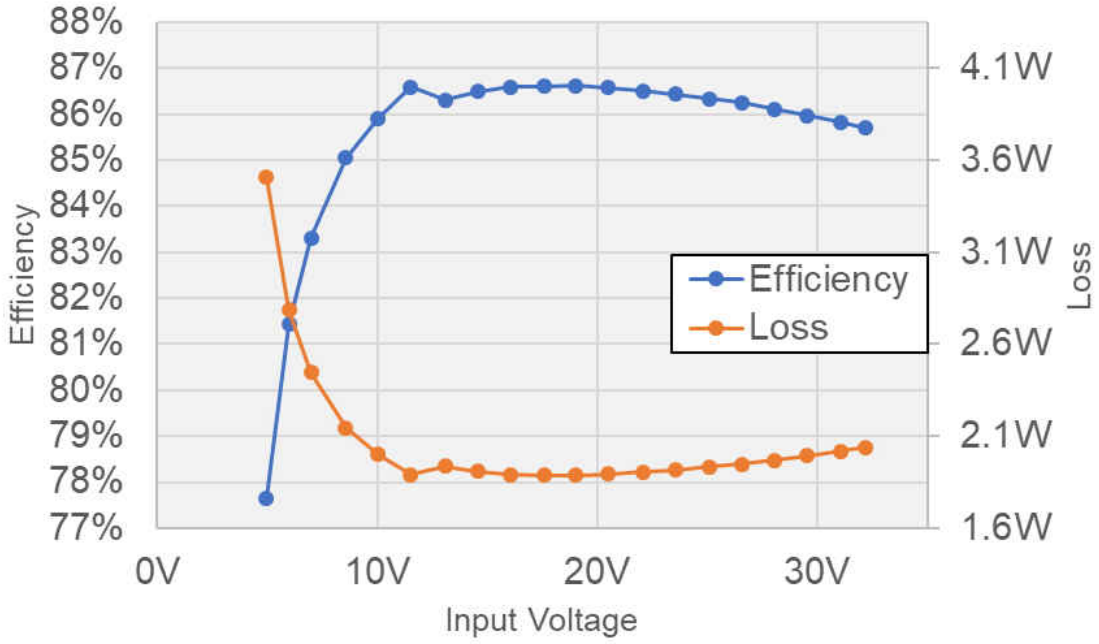


Figure 2-5. Efficiency and Loss vs Input Voltage of Power-Stage

The irregularity in the curves at 11.5-V to 13-V input voltage is related to the measurement range change from the input current.

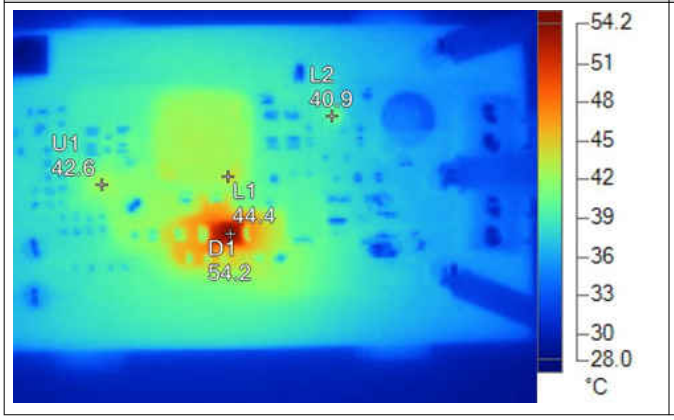
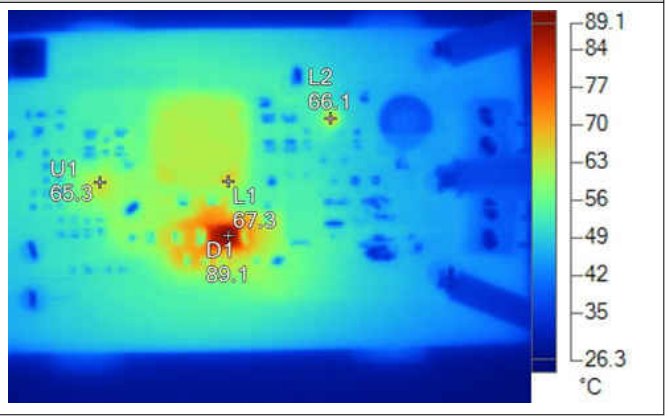
2.5 Thermal Images

2.5.1 8-V Input Voltage

Table 2-1. Temperature Values for 8 V_{IN}

Name	1 A_{OUT}	2 A_{OUT}
D1	54.2°C	89.1°C
L1	44.4°C	67.3°C
L2	40.9°C	66.1°C
U1	42.6°C	65.3°C

Table 2-2. Thermal Images for 8 V_{IN}

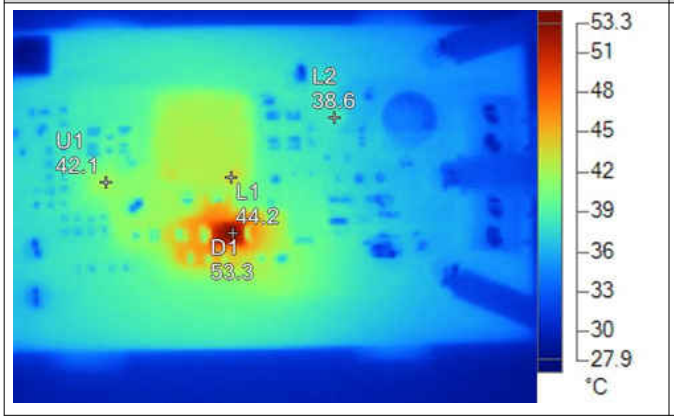
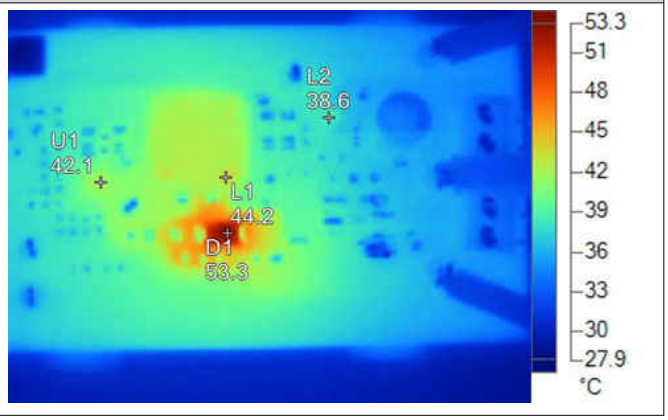
1 A_{OUT}	2 A_{OUT}
	

2.5.2 12-V Input Voltage

Table 2-3. Temperature Values for 12 V_{IN}

Name	1 A_{OUT}	2 A_{OUT}
D1	53.3°C	84.7°C
L1	44.2°C	63.3°C
L2	38.6°C	53.6°C
U1	42.1°C	59.3°C

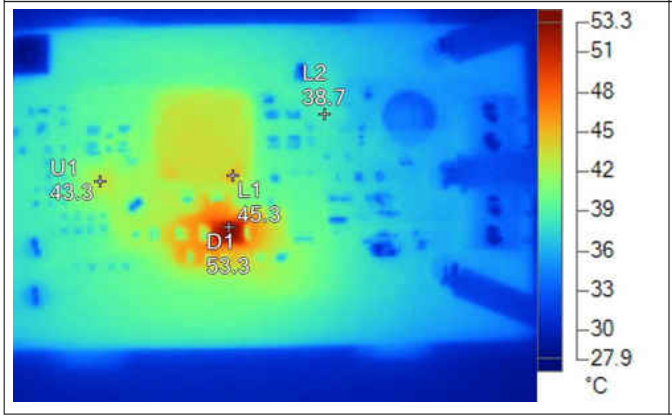
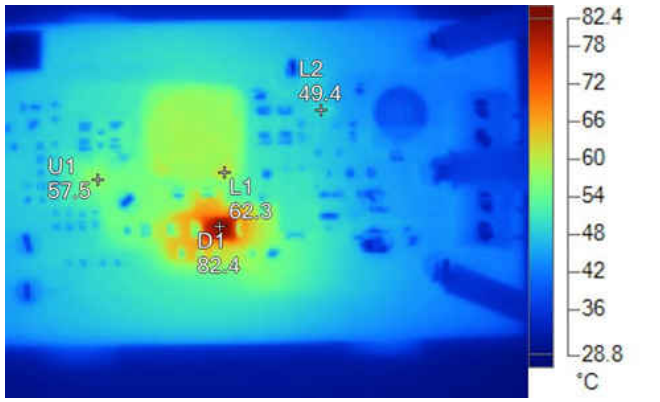
Table 2-4. Thermal Images for 12 V_{IN}

1 A_{OUT}	2 A_{OUT}
	

2.5.3 18-V Input Voltage

Name	1 A_{OUT}	2 A_{OUT}
D1	53.3°C	82.4°C
L1	43.3°C	62.3°C
L2	45.3°C	49.4°C
U1	38.7°C	57.5°C

Table 2-5. Thermal Image for 18 V_{IN}

1 A_{OUT}	2 A_{OUT}
	

2.5.4 Conclusion

For continuous output currents > 1 A, the Schottky rectifier can be diodes PDS360-13 in PowerDI-5 package. By adding some copper to the pads the thermal resistance $R_{\theta JA}$ can be as low as 50 K/W.

Especially at low cold cranking, a filter inductor with lower windings resistance R_{DC} is recommended.

2.6 Bode Plots

Table 2-6. Summery of Bode Plot Values

	5.2 V_{IN}	12 V_{IN}	18 V_{IN}
Bandwidth (kHz)	2.26	5.32	6.13
Phase margin	71.7°	72.2°	72.7°
Slope (20 dB/decade)	–0.97	–1.05	–1.06
Gain margin (dB)	–13.2	–19.2	–21.34
Slope (20 dB/decade)	–0.77	–1.48	–0.88
Frequency (kHz)	12.8	31.9	40.2

2.6.1 5.2-V Input Voltage (Board Input, 5.0 V at Power Stage)

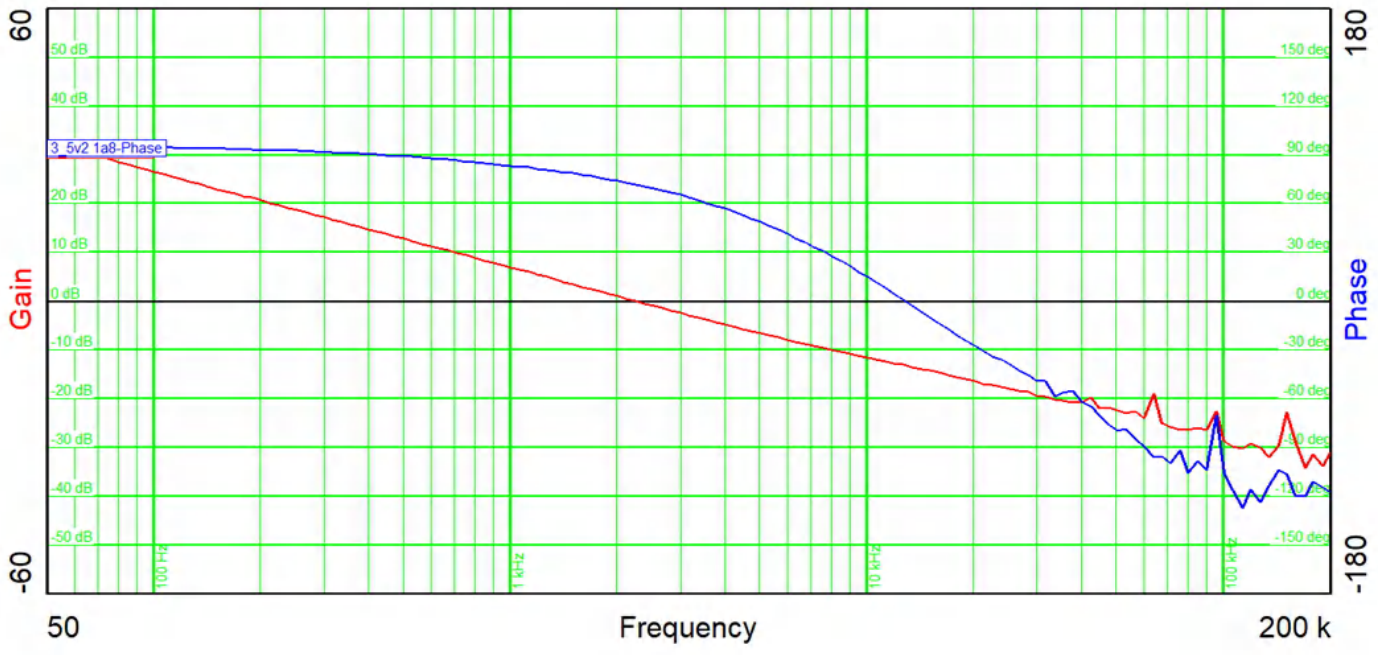


Figure 2-6. Bode Plot for 5.2-V Input Voltage and 1.8-A Output Current

2.6.2 12-V Input Voltage

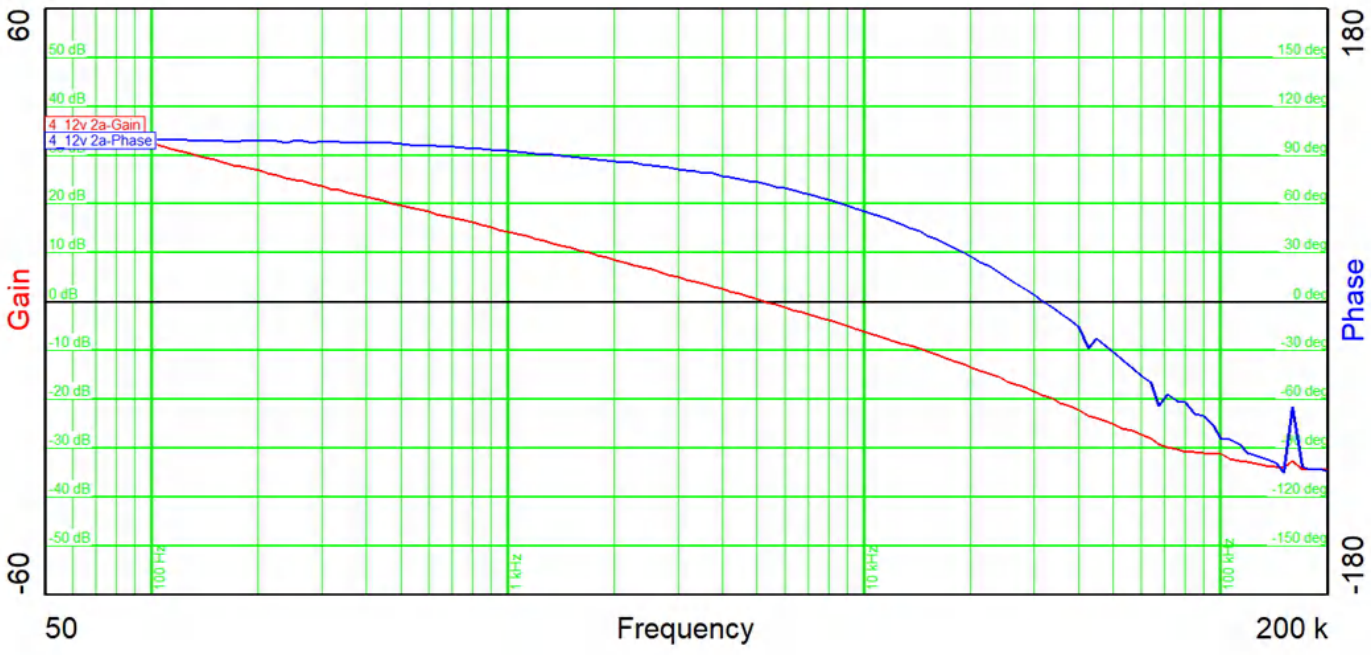


Figure 2-7. Bode Plot for 12-V Input Voltage and 2-A Output Current

2.6.3 18-V Input Voltage

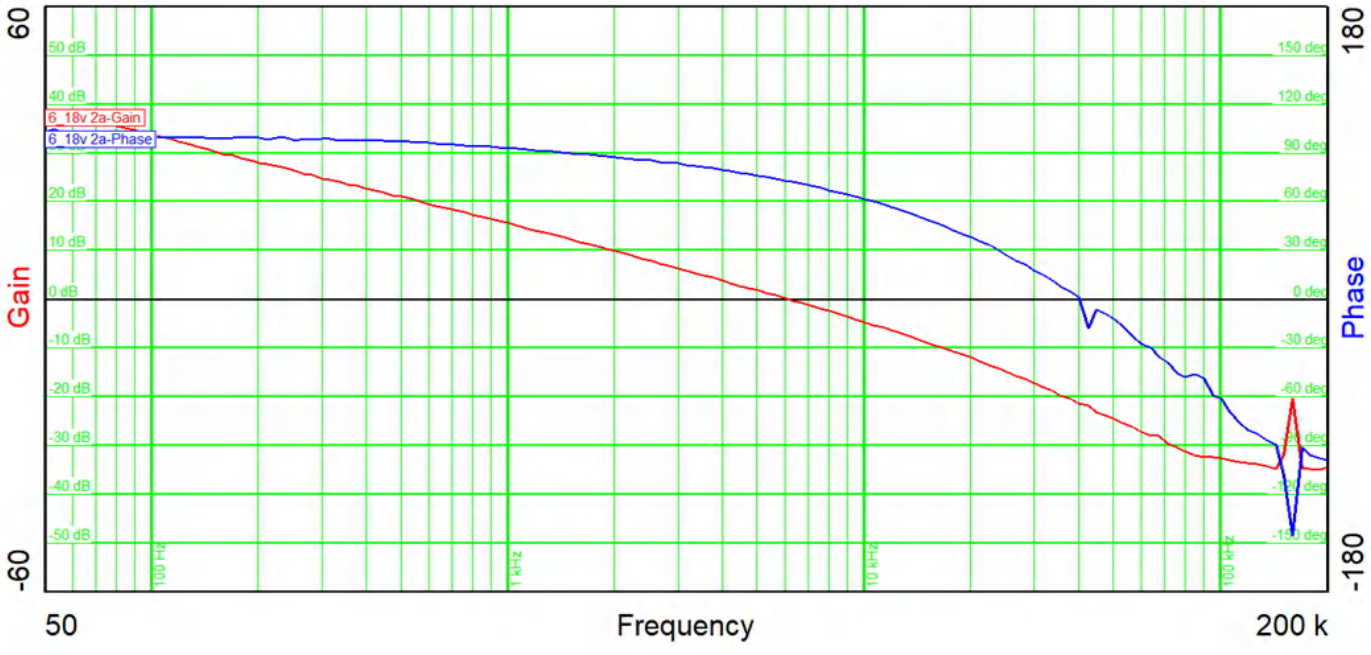


Figure 2-8. Bode Plot for 18-V Input Voltage and 2-A Output Current

3 Waveforms

3.1 Switching

3.1.1 Switchnode (SW) to GND

3.1.1.1 8-V Input Voltage

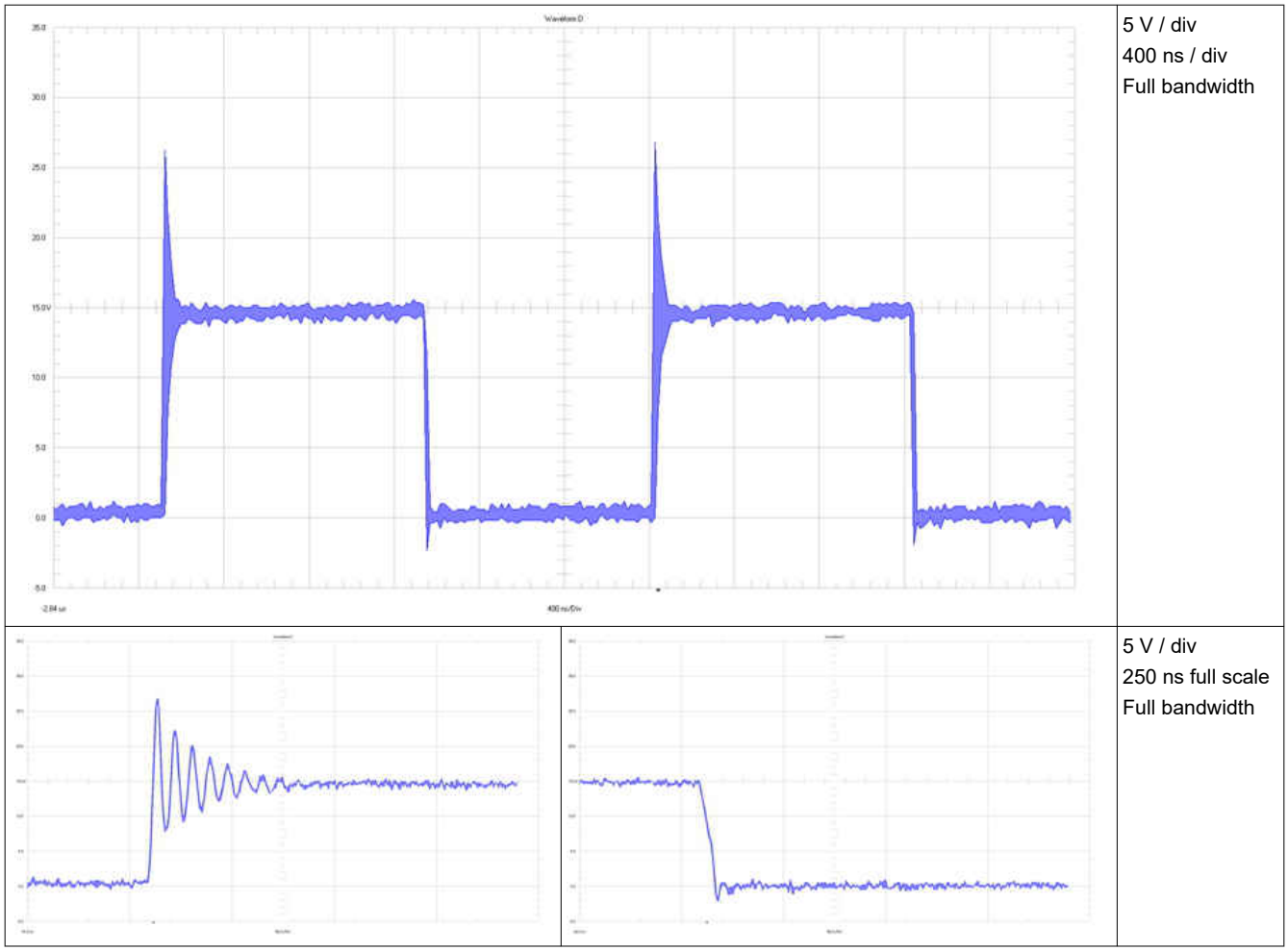


Figure 3-1. Switch Node (TP2 to GND), 8-V Input Voltage

3.1.1.2 12-V Input Voltage

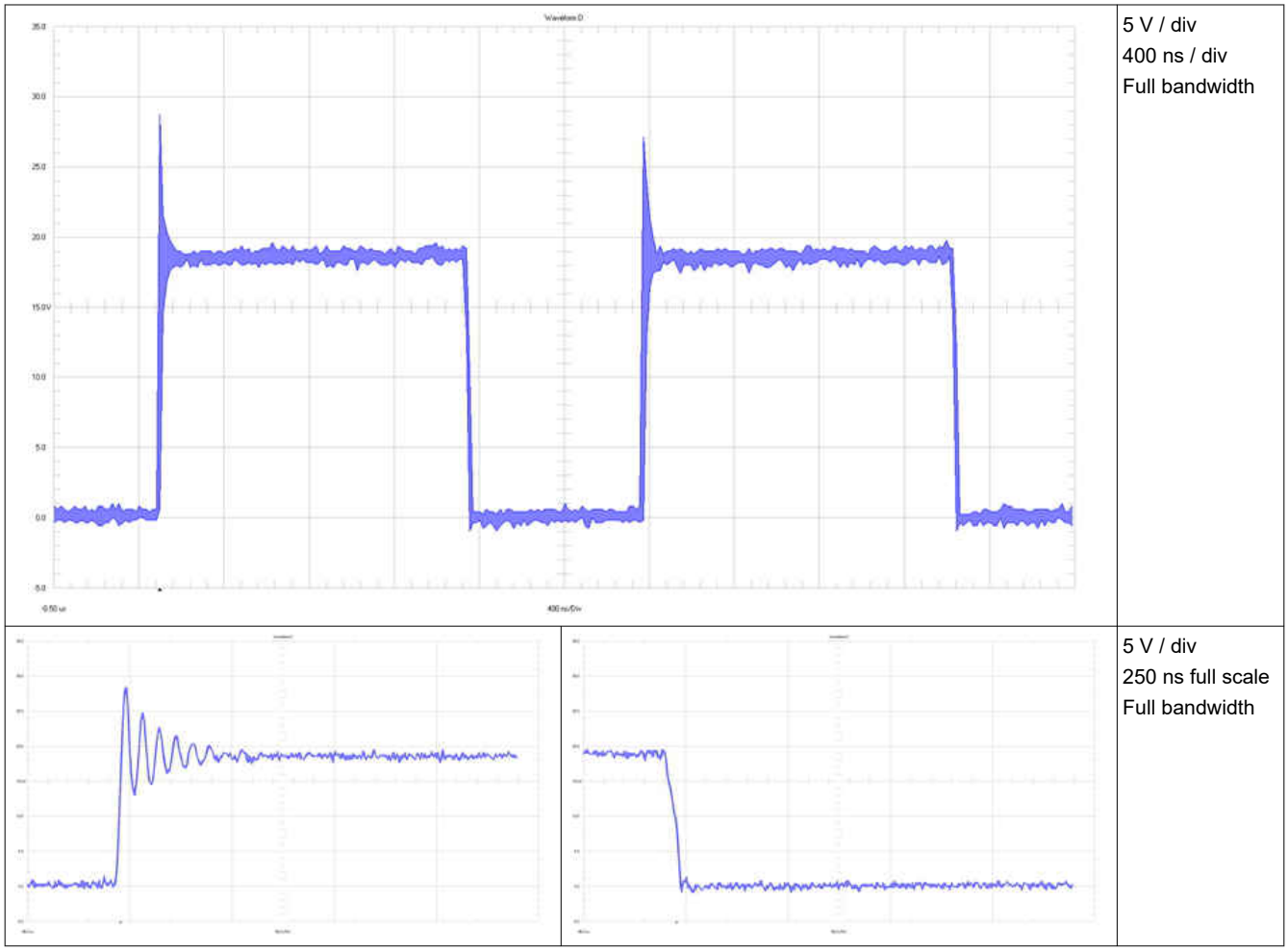


Figure 3-2. Switch Node (TP2 to GND), 12-V Input Voltage

3.1.1.3 18-V Input Voltage

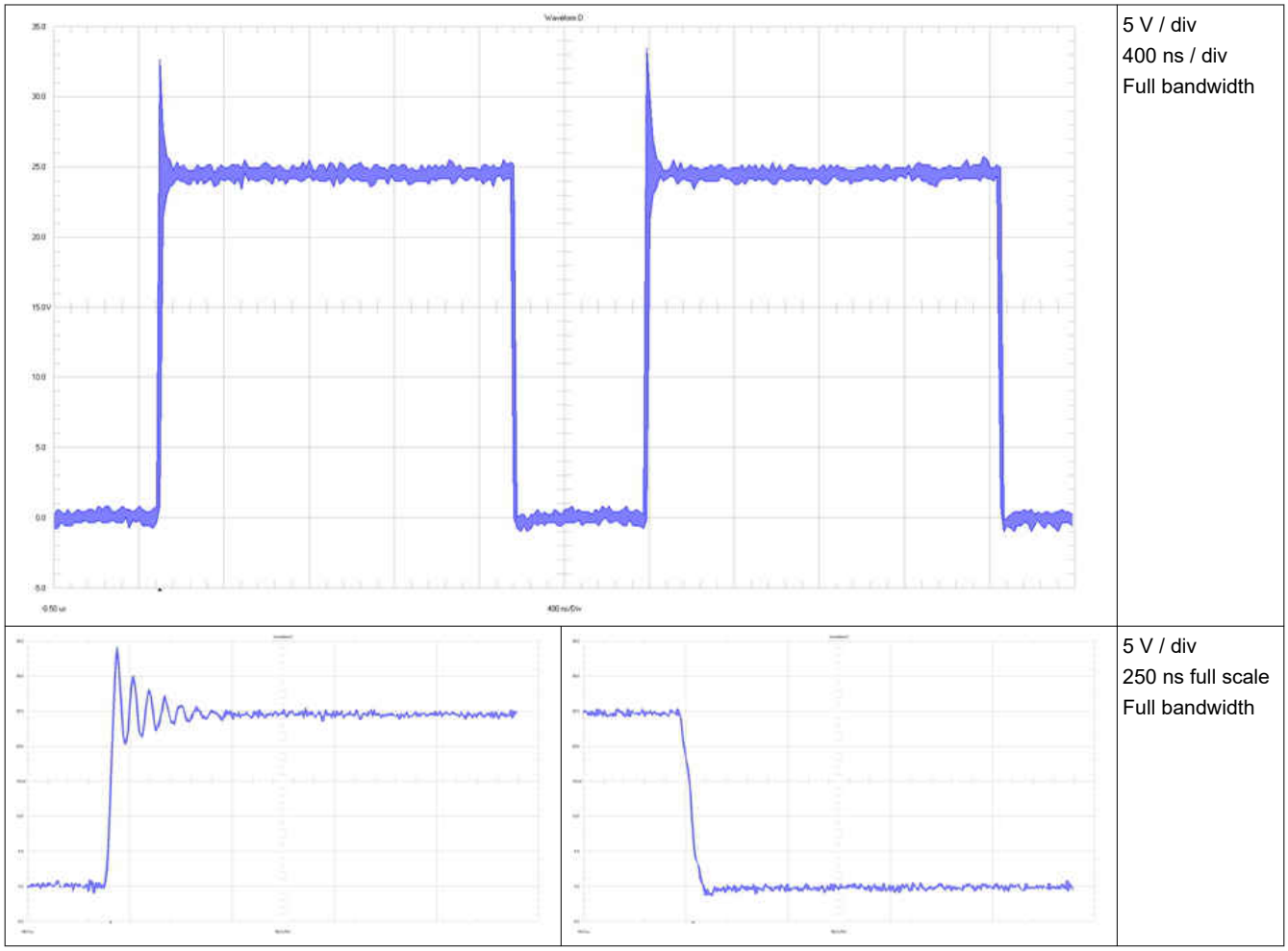


Figure 3-3. Switch Node (TP2 to GND), 18-V Input Voltage

3.1.2 Diode D1 (Referenced to V_{OUT})

3.1.2.1 8-V Input Voltage

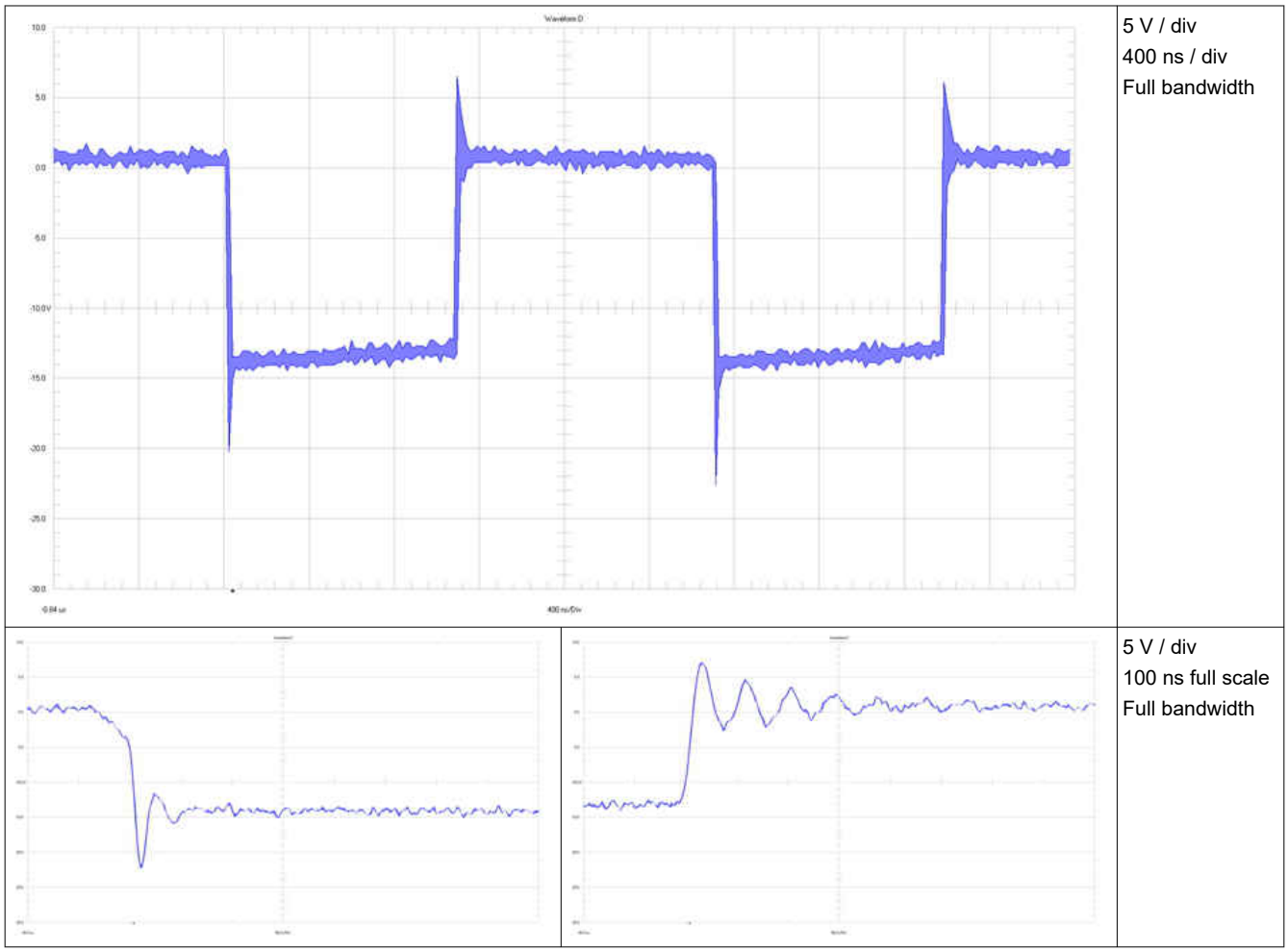


Figure 3-4. Diode D1, 8-V Input Voltage

3.1.2.2 12-V Input Voltage

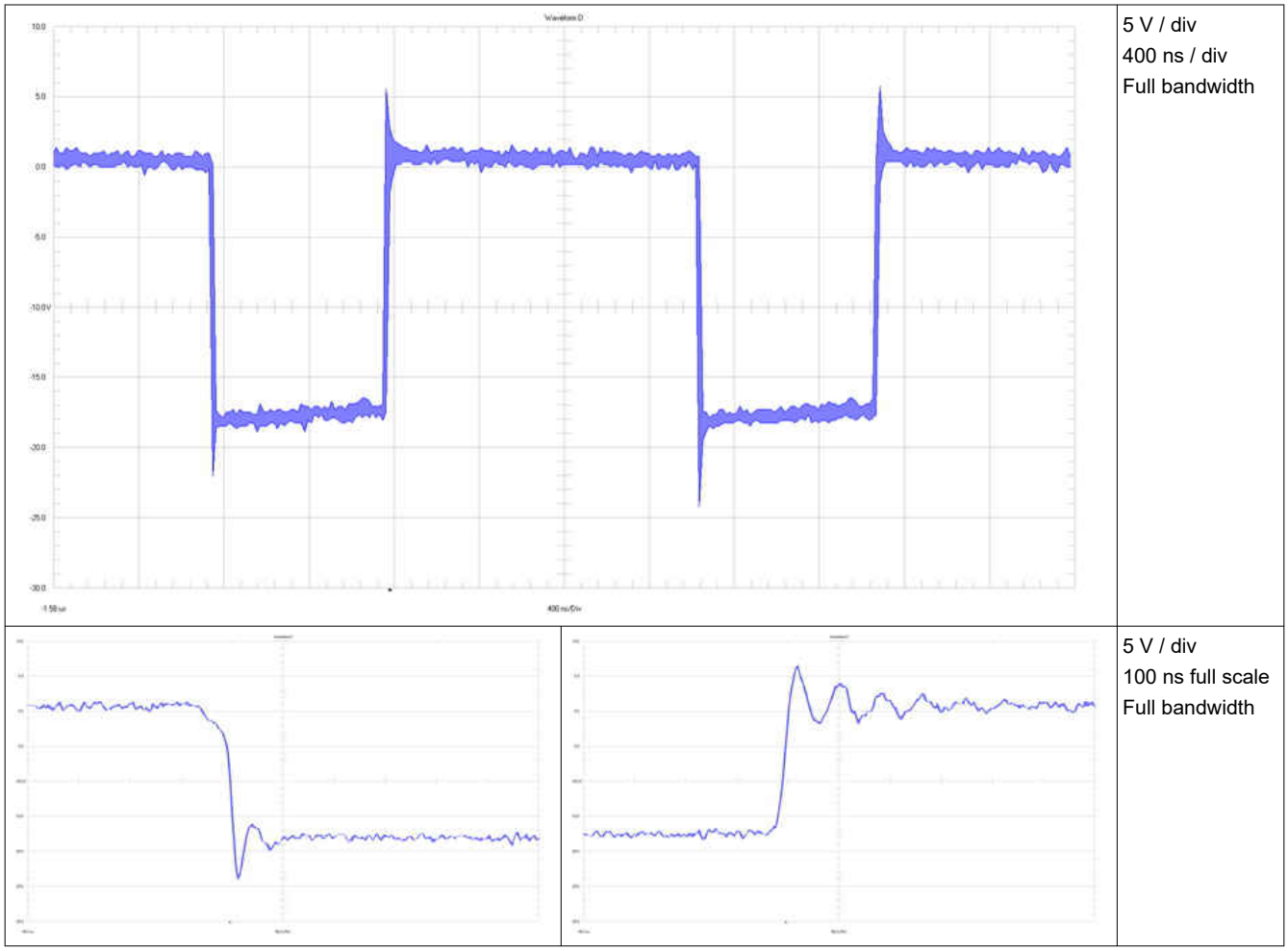


Figure 3-5. Diode D1, 12-V Input Voltage

3.1.2.3 18-V Input Voltage

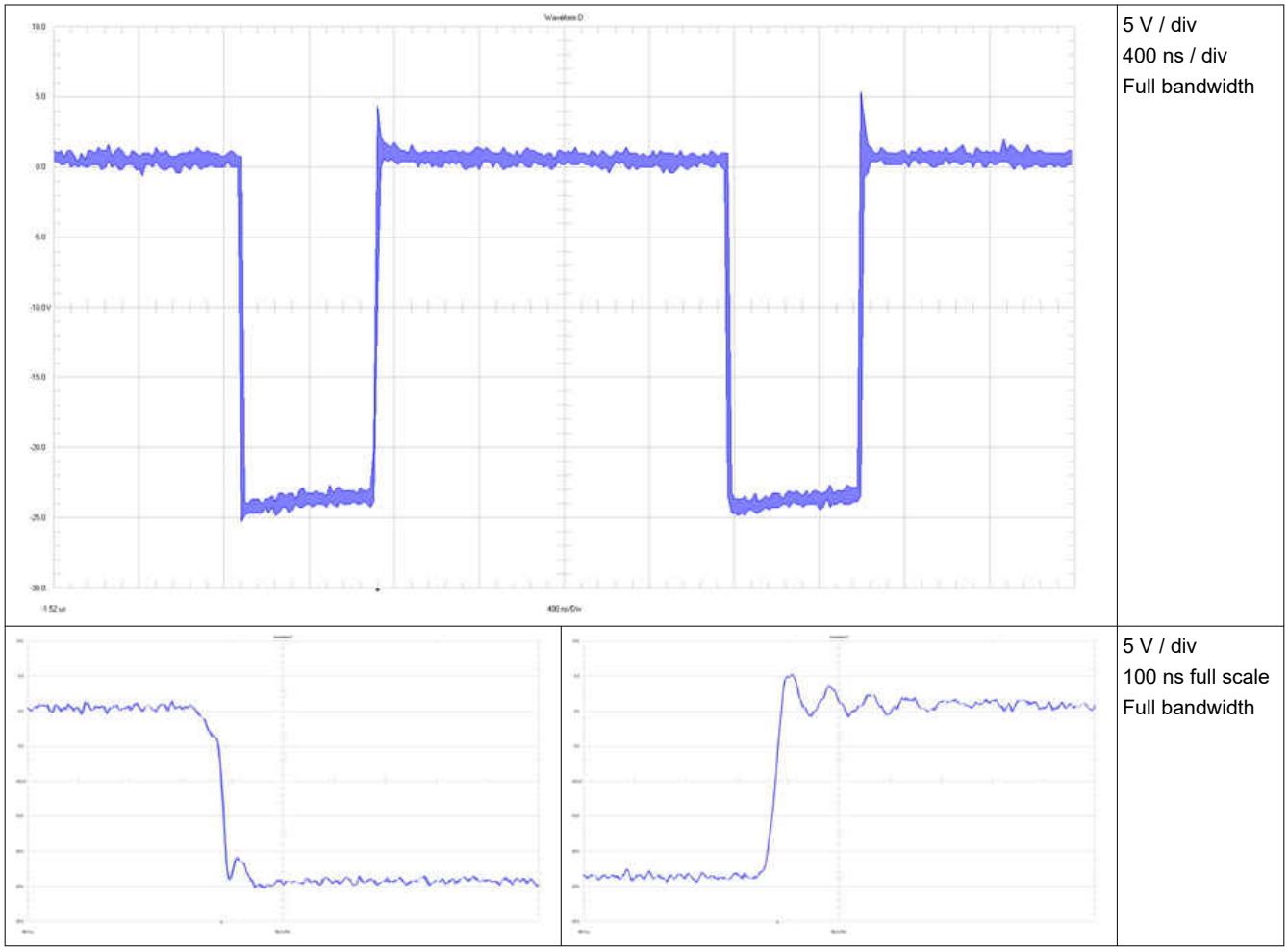


Figure 3-6. Diode D1, 18-V Input Voltage

3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figure.

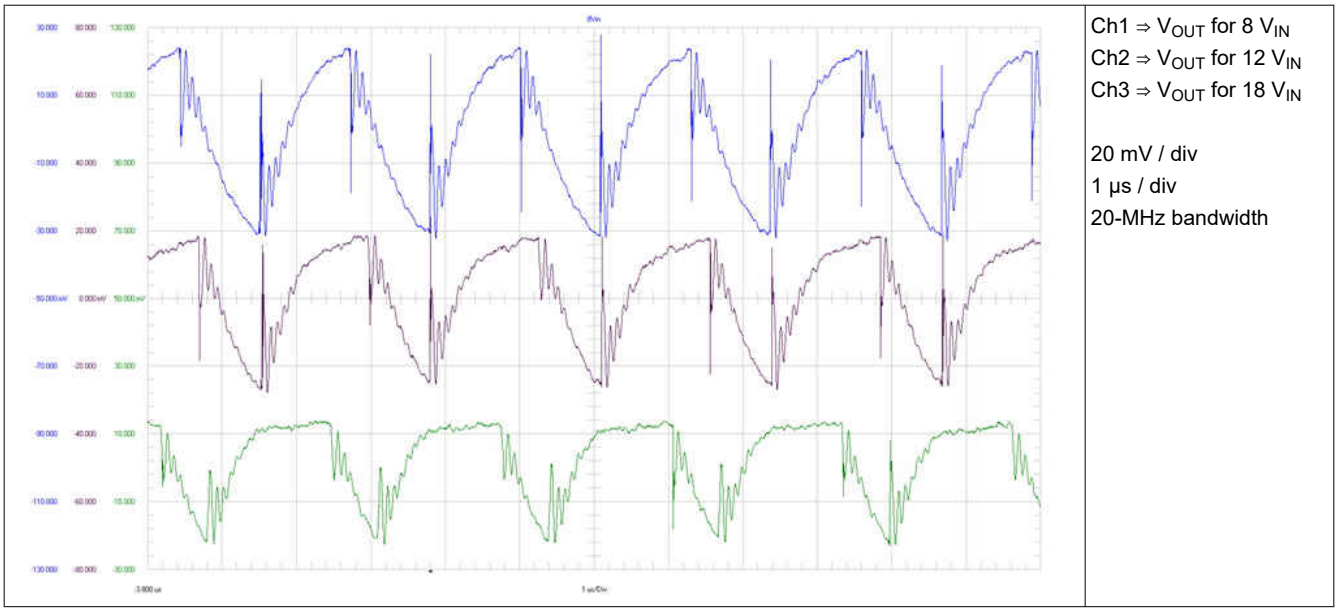


Figure 3-7. Output Voltage Ripple

3.3 Input Voltage Ripple (AC-Coupled)

3.3.1 Board Input

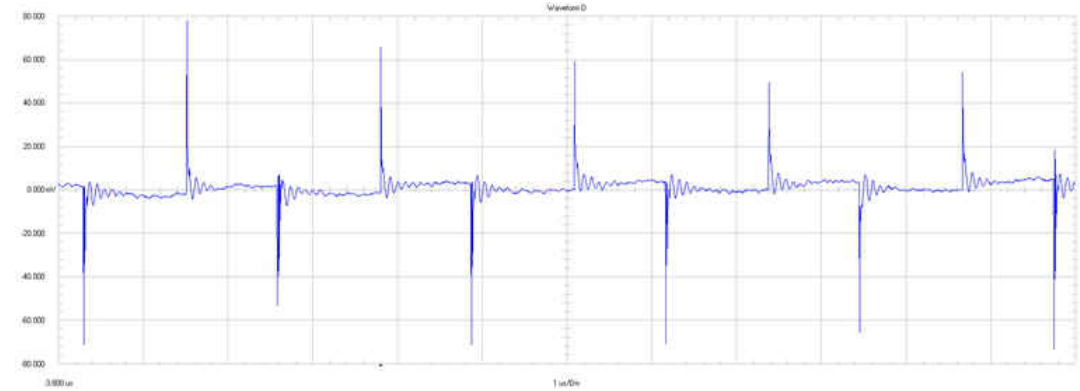
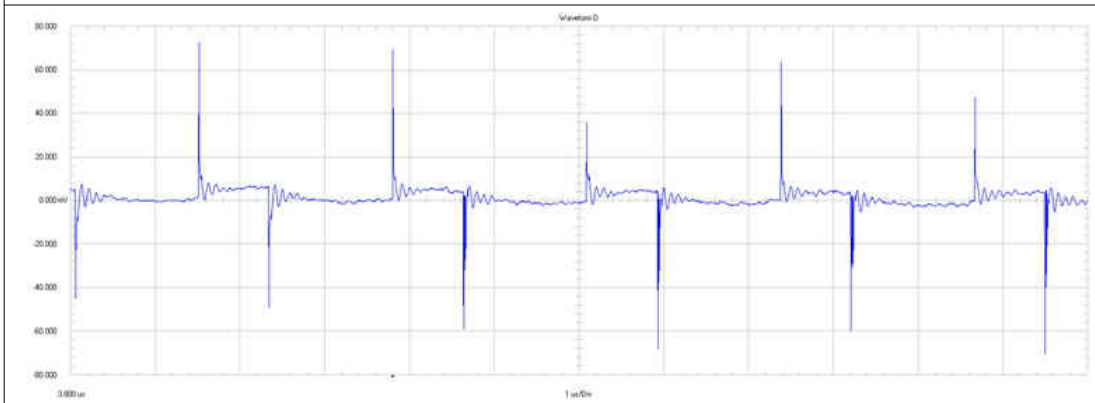
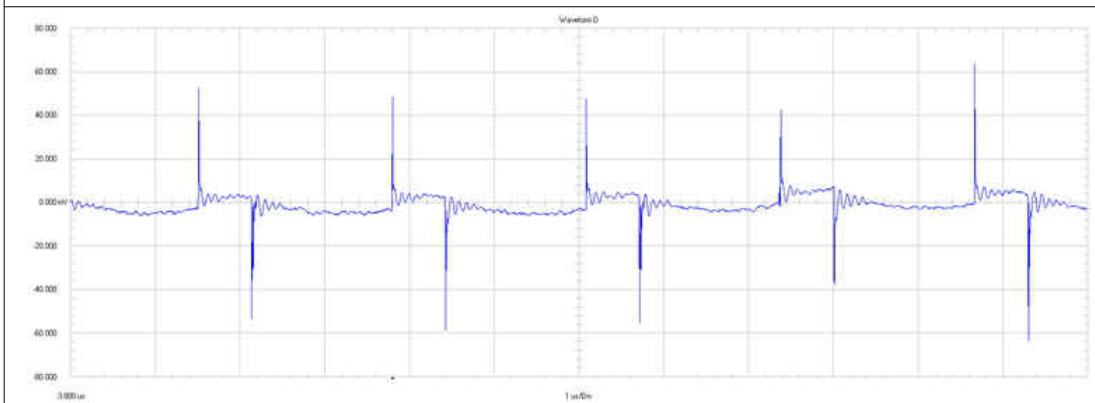
	V_{IN} 8 V 20 mV / div 1 µs / div 20-MHz bandwidth
	V_{IN} 12 V 20 mV / div 1 µs / div 20-MHz bandwidth
	V_{IN} 18 V 20 mV / div 1 µs / div 20-MHz bandwidth

Figure 3-8. Input Voltage Ripple (Board Input)

3.3.2 Power Stage Input

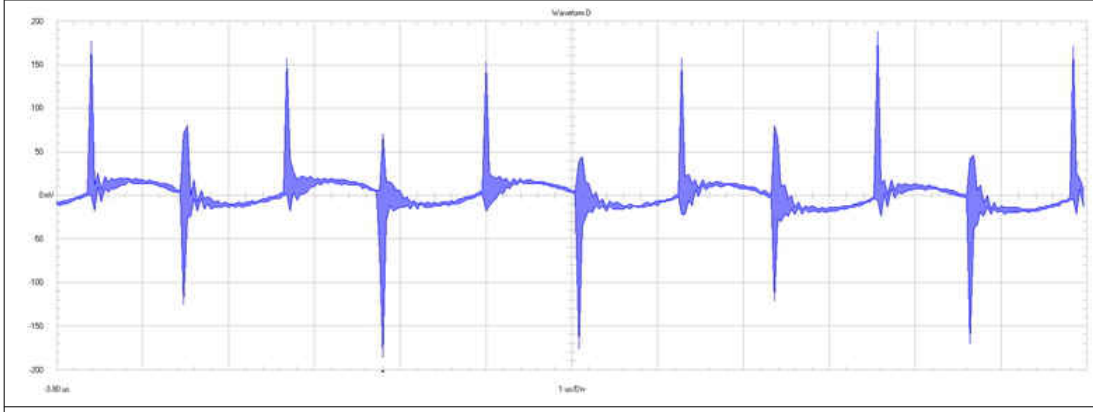
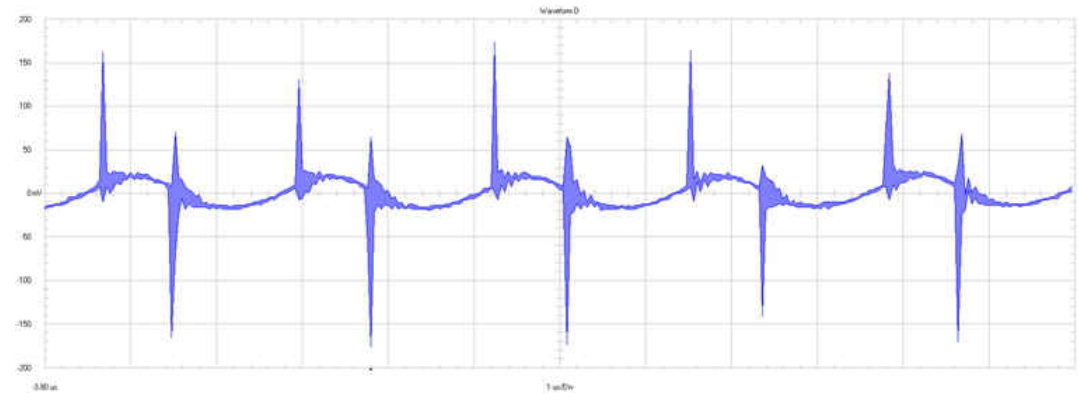
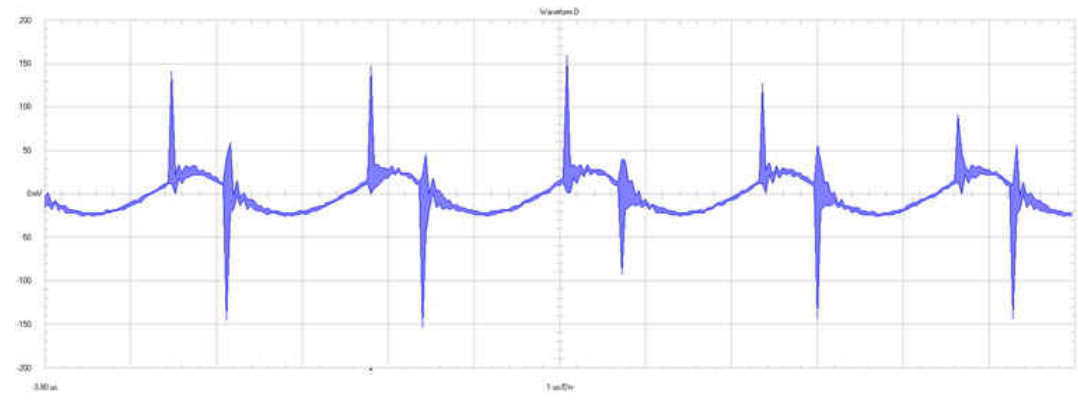
	V_{IN} 8 V 50 mV / div 1 µs / div 20-MHz bandwidth
	V_{IN} 12 V 50 mV / div 1 µs / div 20- MHz bandwidth
	V_{IN} 18 V 50 mV / div 1 µs / div 20-MHz bandwidth

Figure 3-9. Input Voltage Ripple (Power-Stage Input)

3.4 Load Transients

The electronic load toggles between 1 A and 2 A with a frequency of 100 Hz.

3.4.1 8-V Input Voltage

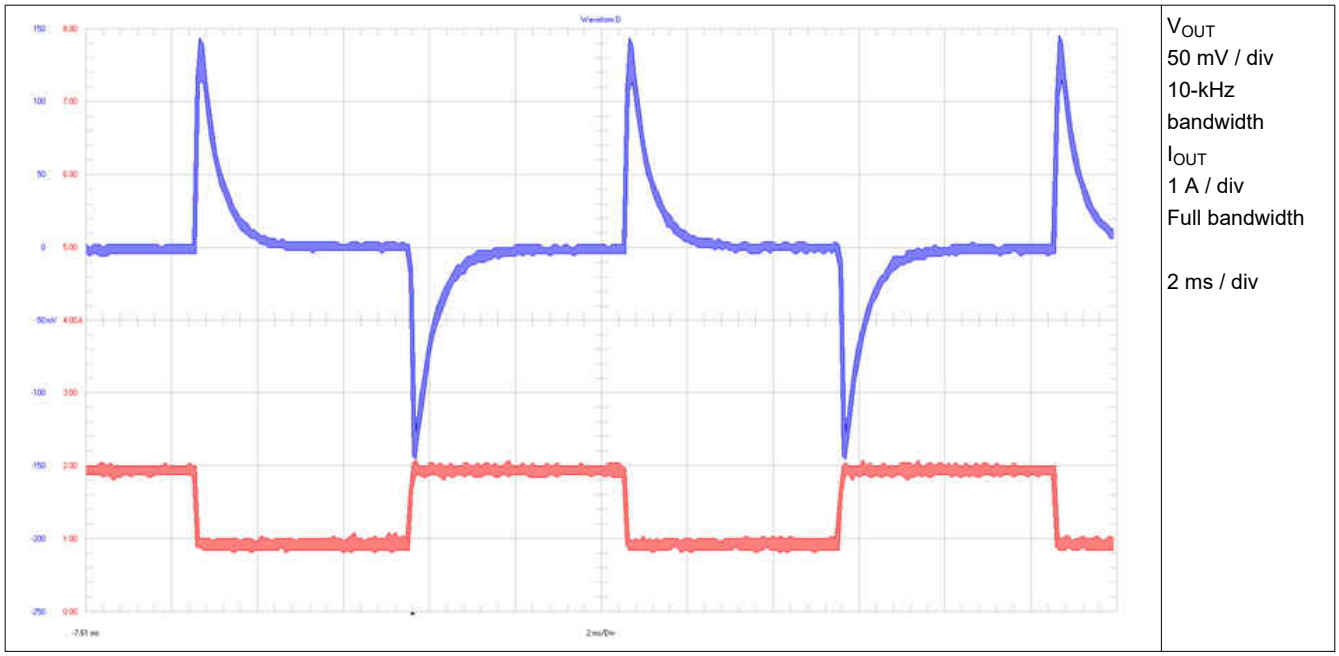


Figure 3-10. Load Transient for 8-V Input Voltage

3.4.2 12-V Input Voltage

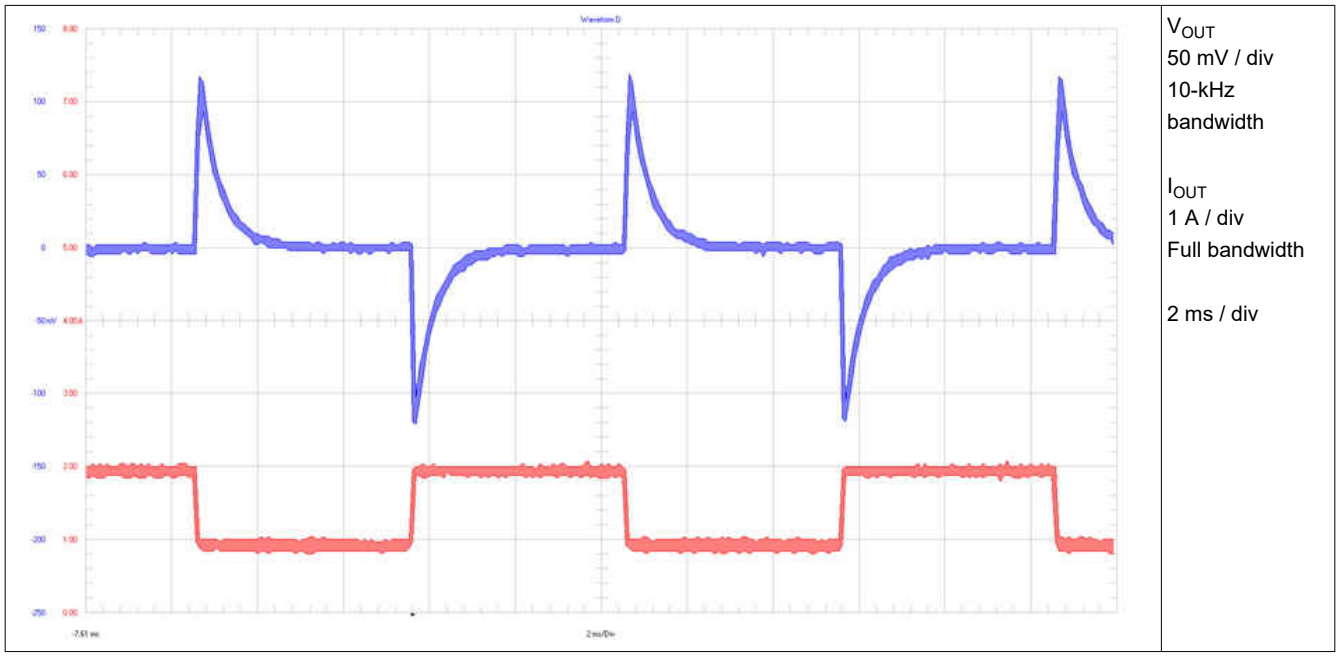


Figure 3-11. Load Transient for 12-V Input Voltage, Deviation 120 mV_{PK} = 2%

3.4.3 18-V Input Voltage

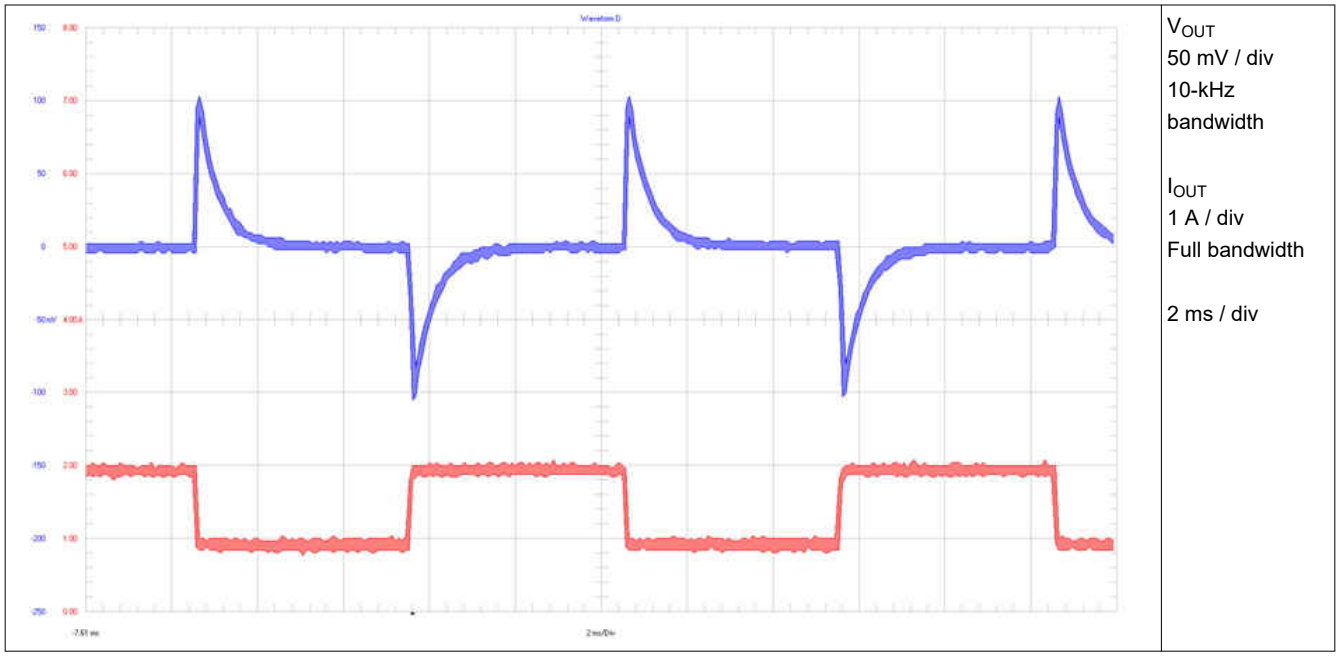


Figure 3-12. Load Transient for 18-V Input Voltage

3.5 Start-Up Sequence

3.5.1 8-V Input Voltage

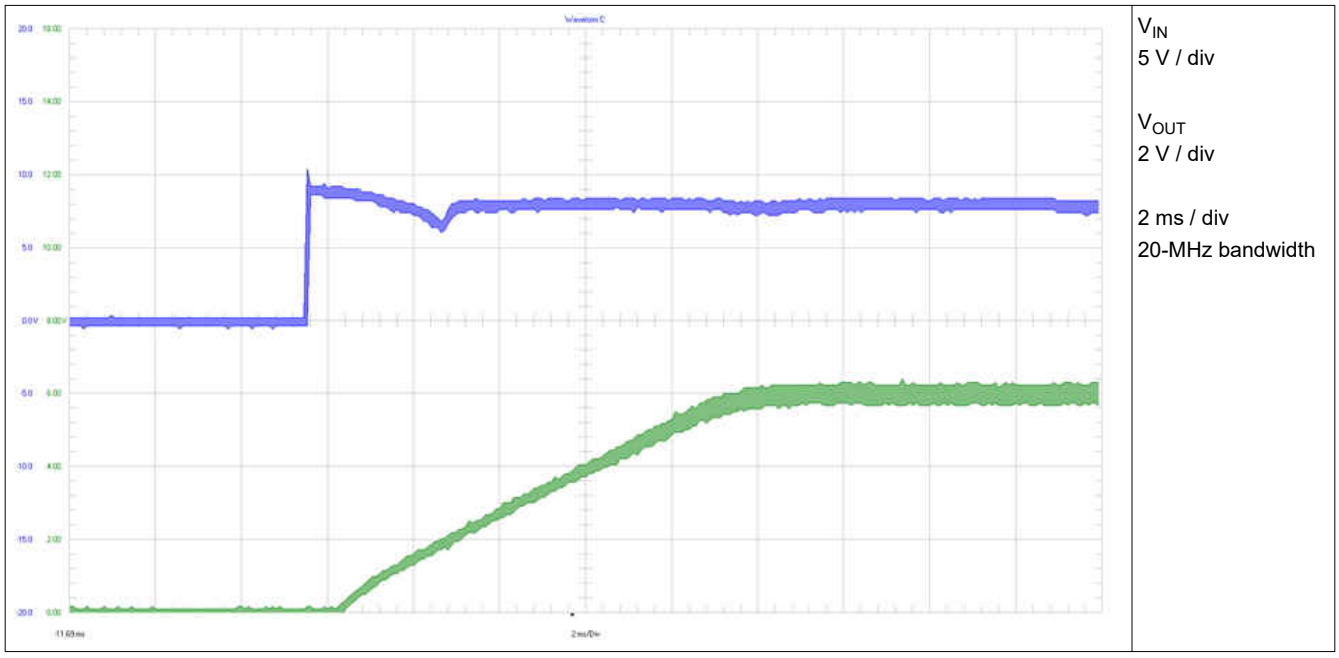


Figure 3-13. Start-Up 8-V Input Voltage

3.5.2 12-V Input Voltage

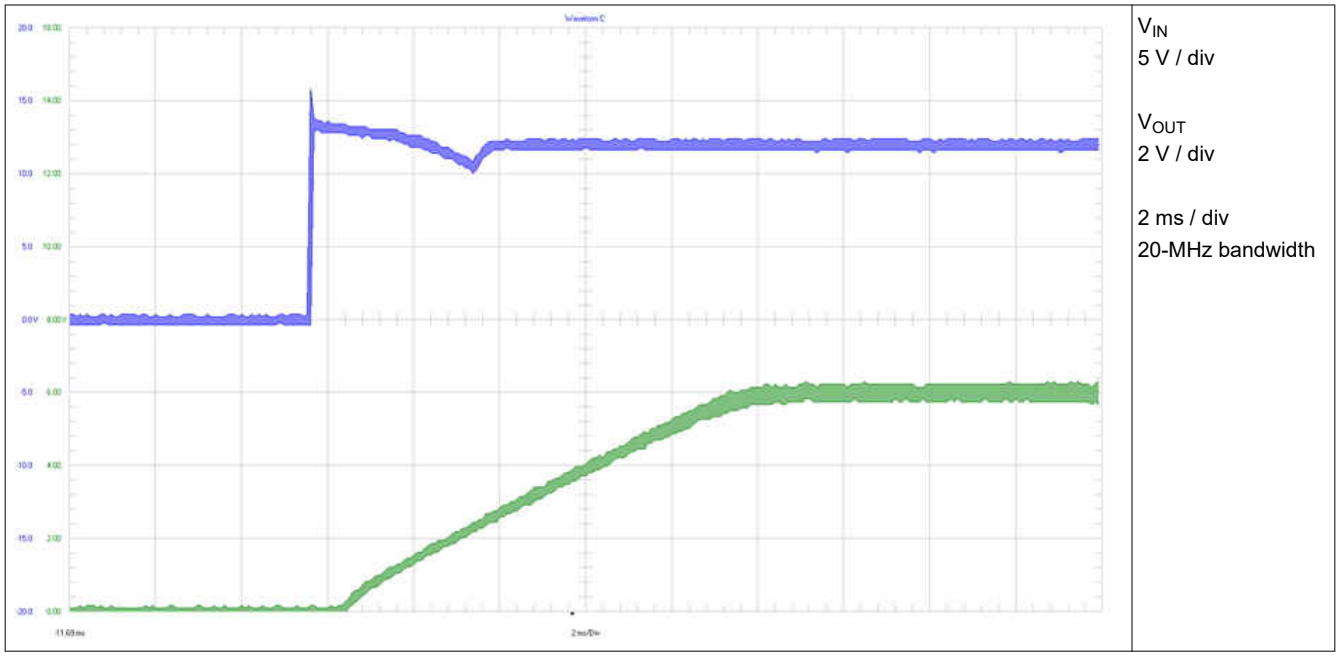


Figure 3-14. Start-Up 12-V Input Voltage

3.5.3 18-V Input Voltage

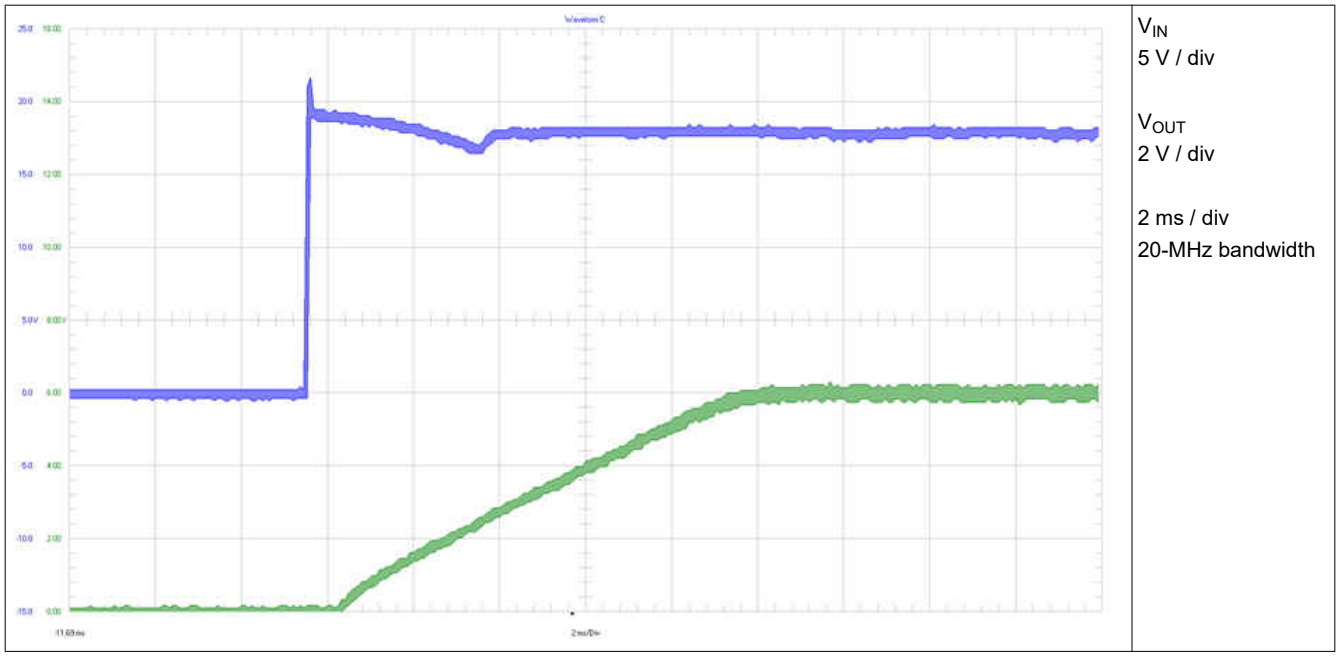


Figure 3-15. Start-Up 18-V Input Voltage

3.6 Shutdown Sequence

3.6.1 8-V Input Voltage

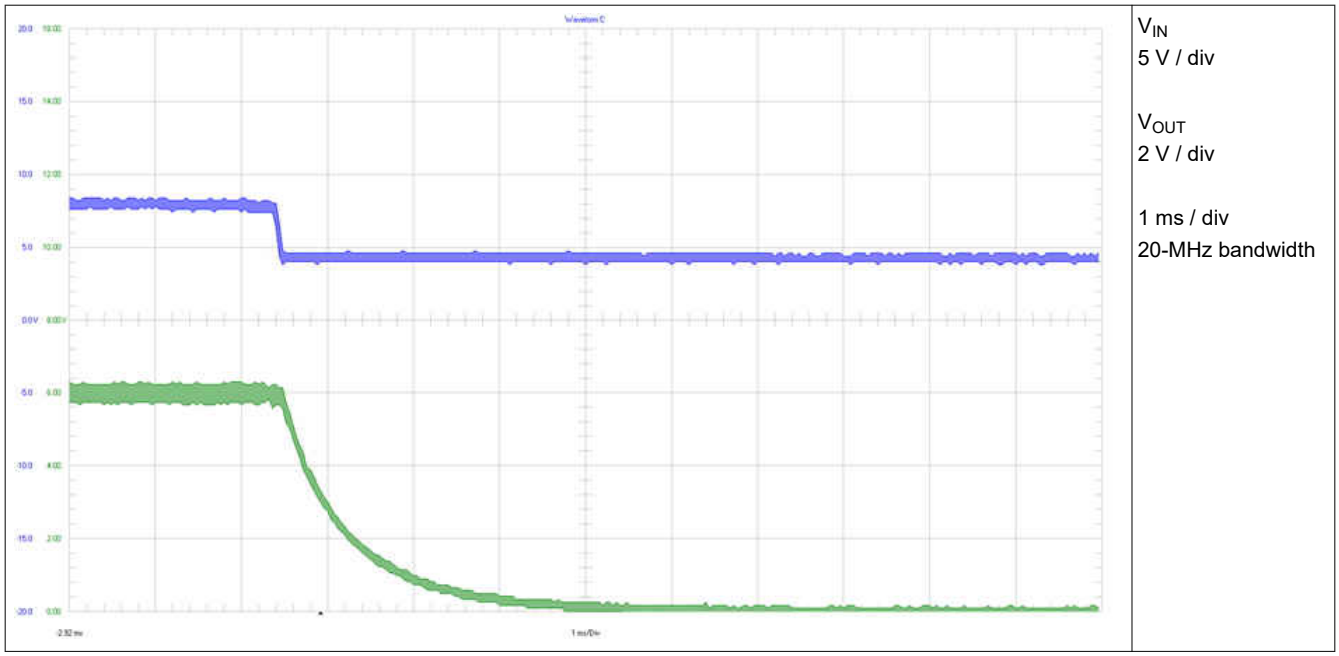


Figure 3-16. Shutdown 8-V Input Voltage

3.6.2 12-V Input Voltage

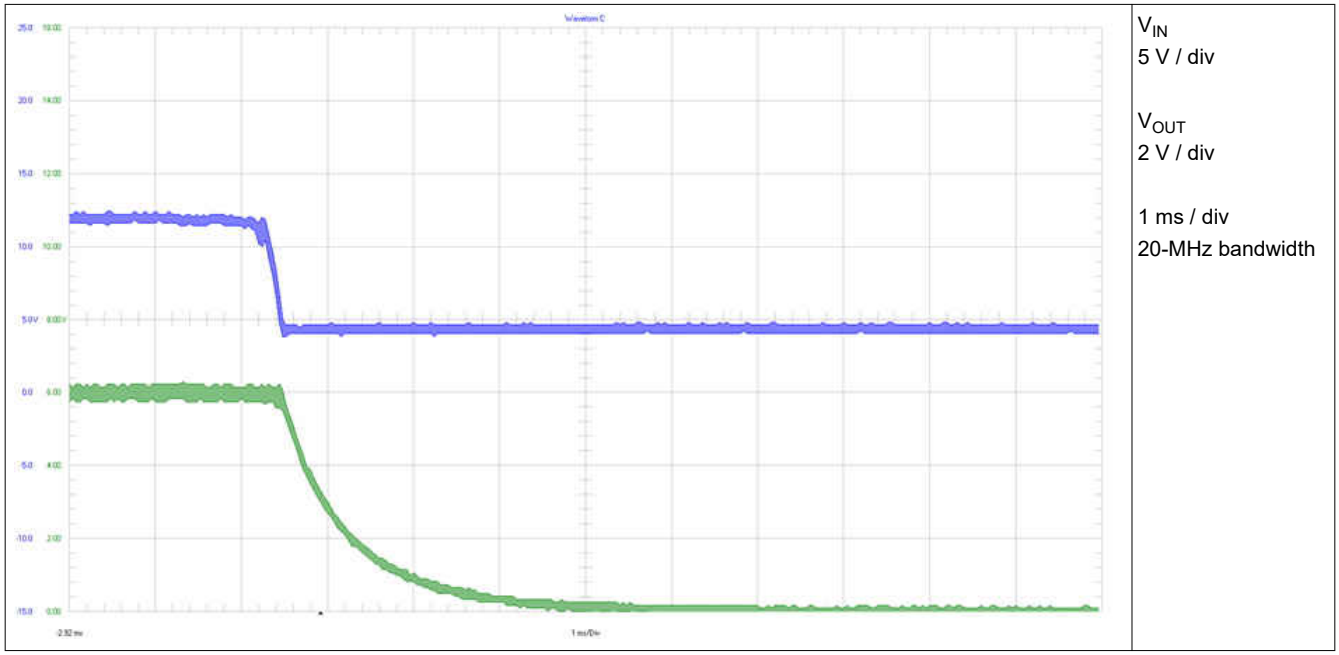


Figure 3-17. Shutdown 12-V Input Voltage

3.6.3 18-V Input Voltage

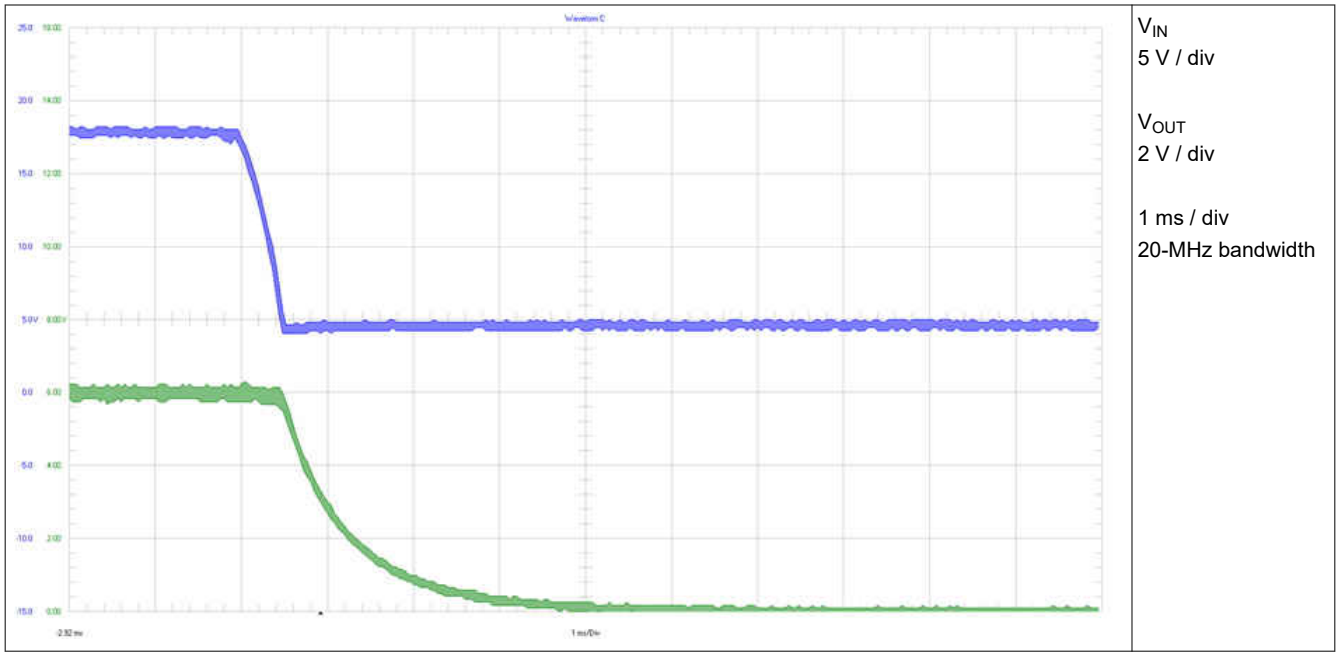


Figure 3-18. Shutdown 18-V Input Voltage

A Output Ripple Reduction, Output Current Capability, and Dithering Option

A.1 Output Ripple Reduction by Adding Ceramic Output Capacitors (MLCCs)

A.1.1 Initial Design

The initial design comes with 1 × 220-µF tantalum polymer capacitor and 1 × 100 nF X7R ceramic capacitor.

Figure A-1 displays the output ripple voltage waveform.

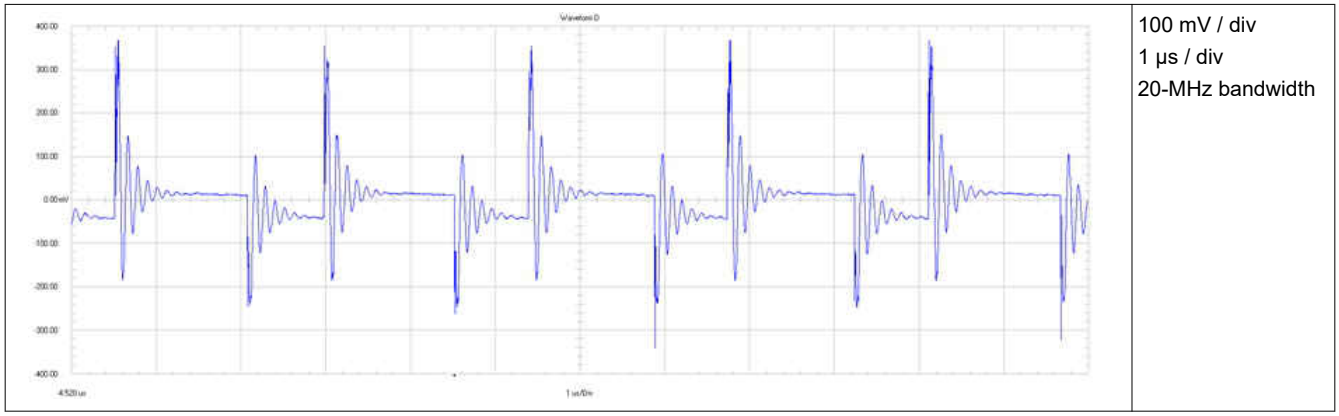
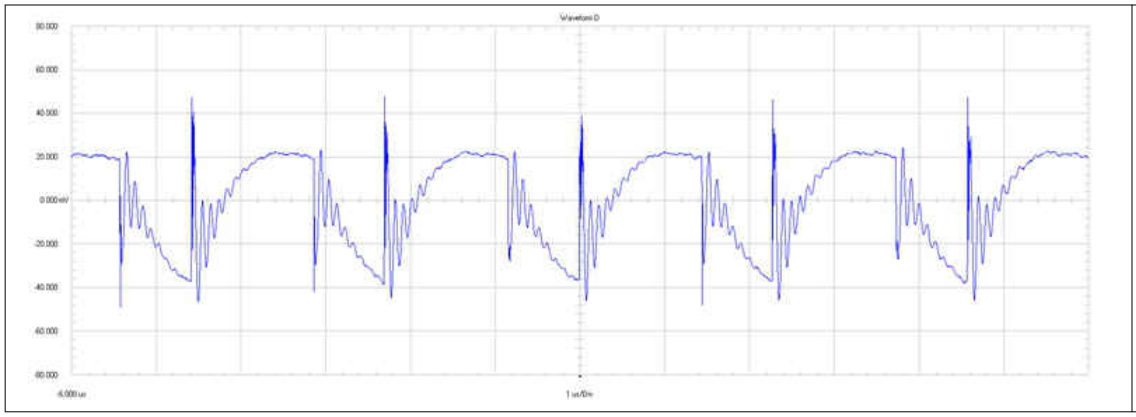


Figure A-1. Output Ripple Voltage of Initial Design at 12 V_{IN}

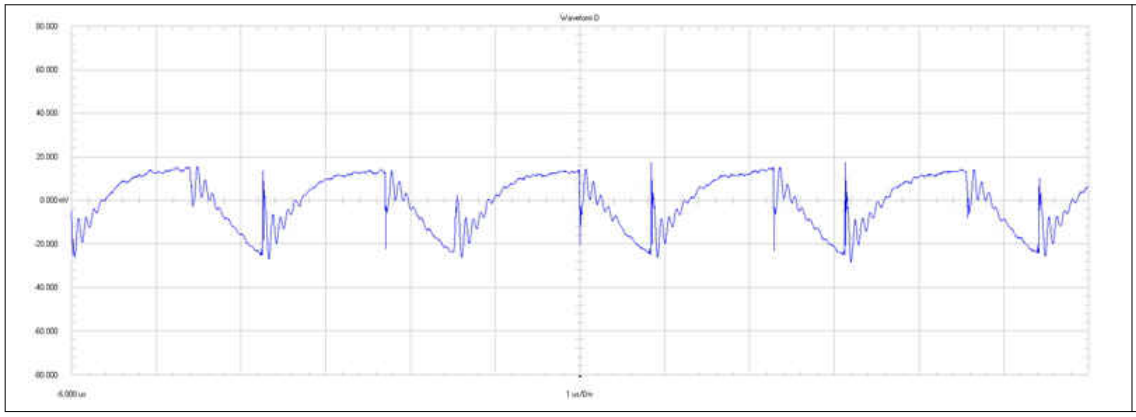
A.1.2 Adding one 47-µF X7R Ceramic Capacitor, MLCC, 10 V, X7R, 1210



20 mV / div
1 µs / div
20-MHz bandwidth

Figure A-2. Output Ripple Voltage of Initial Design and 1 × 47 µF at 12 V_{IN}

A.1.3 Adding a Second 47-µF Capacitor (Final Design)



20 mV / div
1 µs / div
20-MHz bandwidth

Figure A-3. Output Ripple Voltage of Initial Design and 2 × 47 µF at 12 V_{IN}

A.2 Maximum Output Current Capability at Ultra-Low Cold Cranking Using LM5157

With assembled ORing diodes (D2, D3) at bias input and disabled UVLO (R5 = OPEN), the circuit starts to switch at input voltage higher than 3 V.

Table A-1 shows the achievable output current at low-input voltages. Figure A-4 represents the result from the table graphically for the input voltage at the power stage.

Table A-1. Maximum Output Current at Low Input Voltages

Input Voltage at Power Stage	Board Input Voltage	Maximum Output Current
1.5 V	1.6 V	500 mA
2.0 V	2.1 V	700 mA
2.5 V	2.7 V	900 mA
3.0 V	3.2 V	1.3 A
3.5 V	3.7 V	1.6 A
4.0 V	4.2 V	1.9 A
4.5 V	4.6 V	2.1 A
5.0 V	5.1 V	2.3 A

A peak load capability of 2 A is achieved at input voltages higher than 4.5 V.

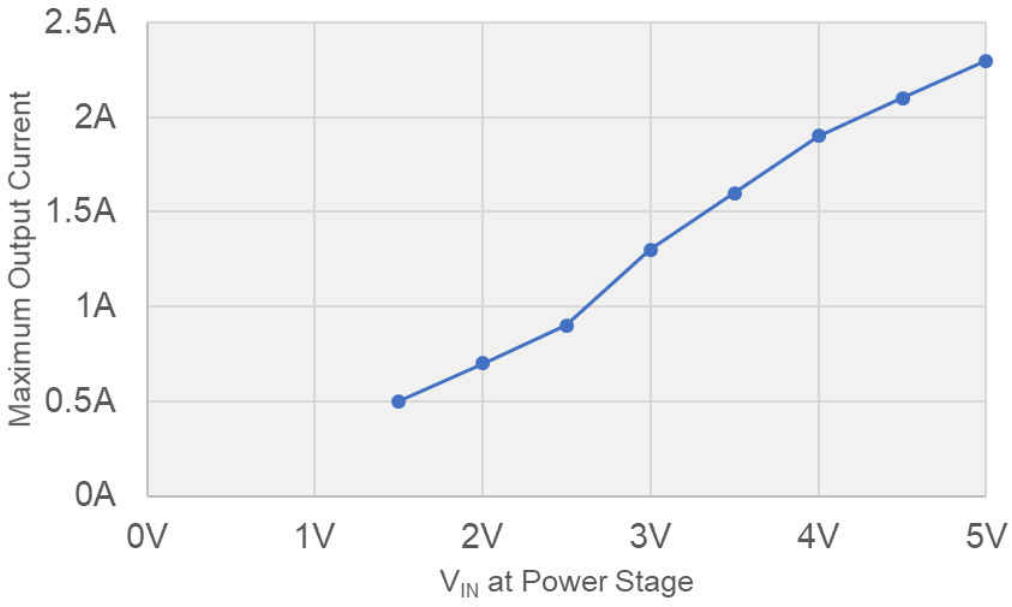


Figure A-4. Maximum Output Current vs Power Stage Input Voltage

A.3 Dithering Option via Resistor R10

A.3.1 Enabled

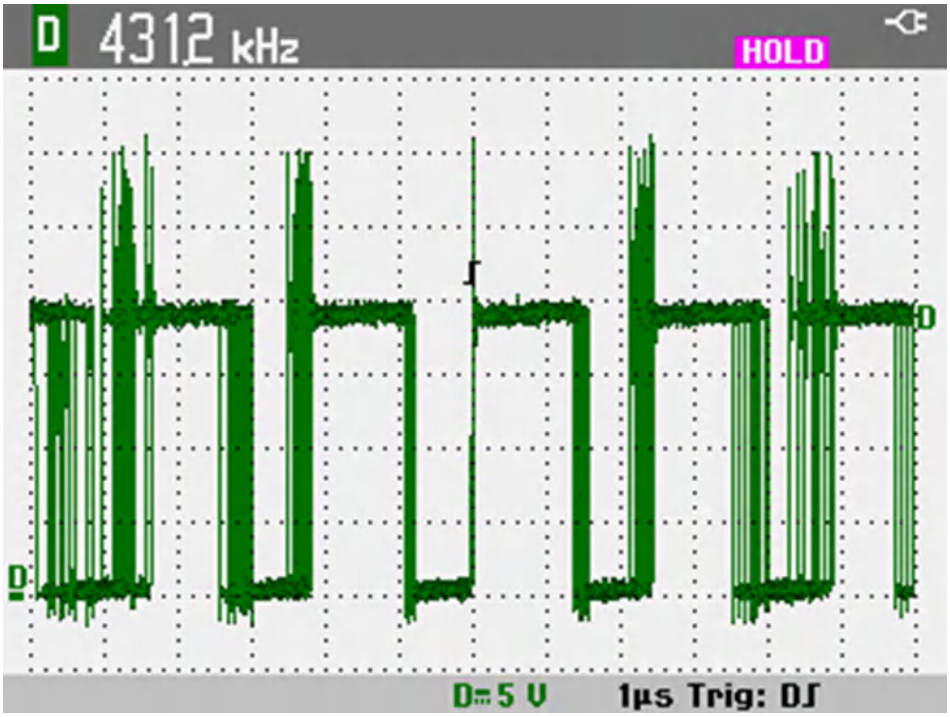


Figure A-5. Screenshot Dithering Enabled (R10 = 37.4 kΩ)

A.3.2 Disabled

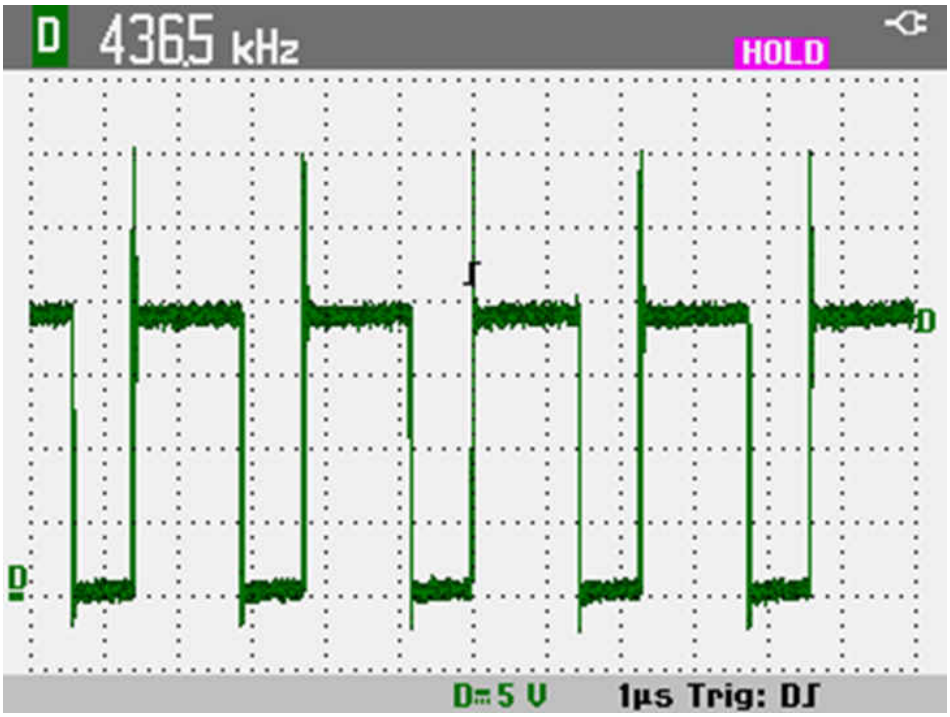


Figure A-6. Screenshot Dithering Disabled (R10 = SHORTED)

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