*Art Kay*

## *TI Precision Designs: Reference Design*

# *Level Translation: Dual to Single Supply Amp, ±15V to 5V*

TEXAS INSTRUMENTS

### TI Precision Designs

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### Circuit Description

Translating a +/-15V signal to a single supply 5V signal for use with an ADC is a common circuit requirement. This Dual Supply to Single Supply Amplifier translates a ±15V signal to a 0V to 5V signal. The output of this design will not be outside of 0-5V regardless of power supply sequencing or other transient conditions.

### Design Resources

| | |
|---|---|
| Design Archive | All Design files |
| TINA-TI™ | SPICE Simulator |
| OPA140 | Product Folder |
| OPA188 | Product Folder |
| OPA827 | Product Folder |
| OPA211 | Product Folder |
| OPA376 | Product Folder |
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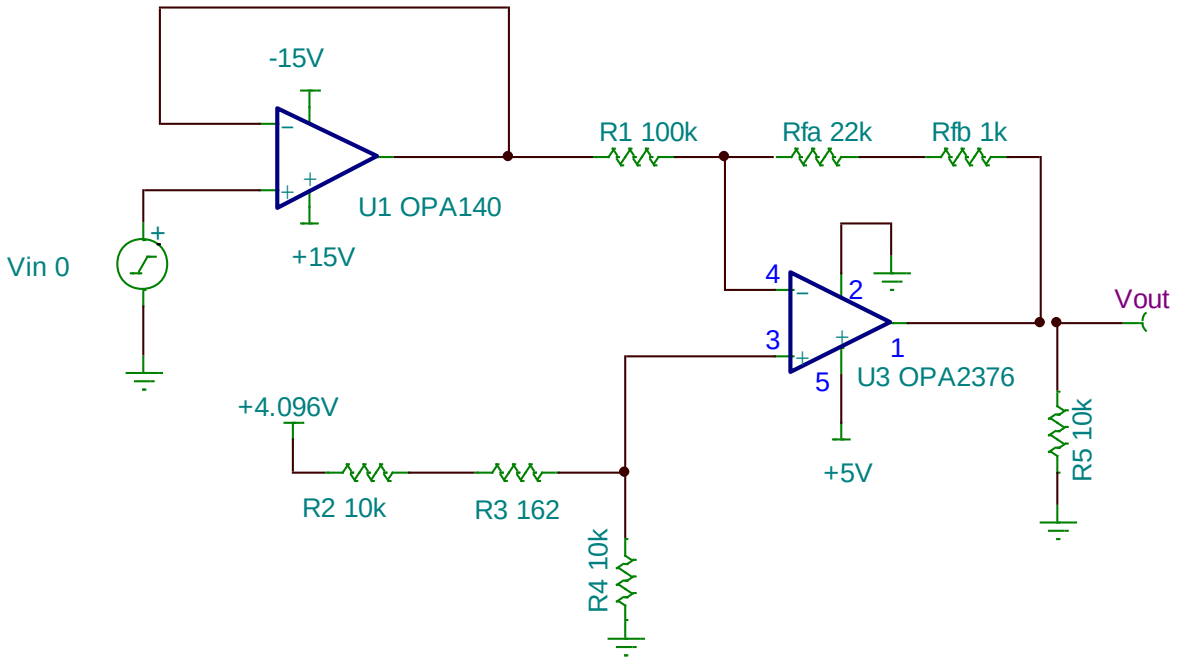


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## 1 Design Summary

The design requirements are as follows:

- Supply Voltage: ±15 V, and +5V
- Input: ±10 V (linear range), ±15 V safe range
- Output: 0.2V to 4.8V

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

**Table 1. Comparison of Design Goals, Simulation, and Measured Performance**

| | Goal | Simulated |
|---|---|---|
| **Zero Scale Error** | 0.5% | 0.196% |
| **Full-Scale Error** | 0.5% | 0.32% |

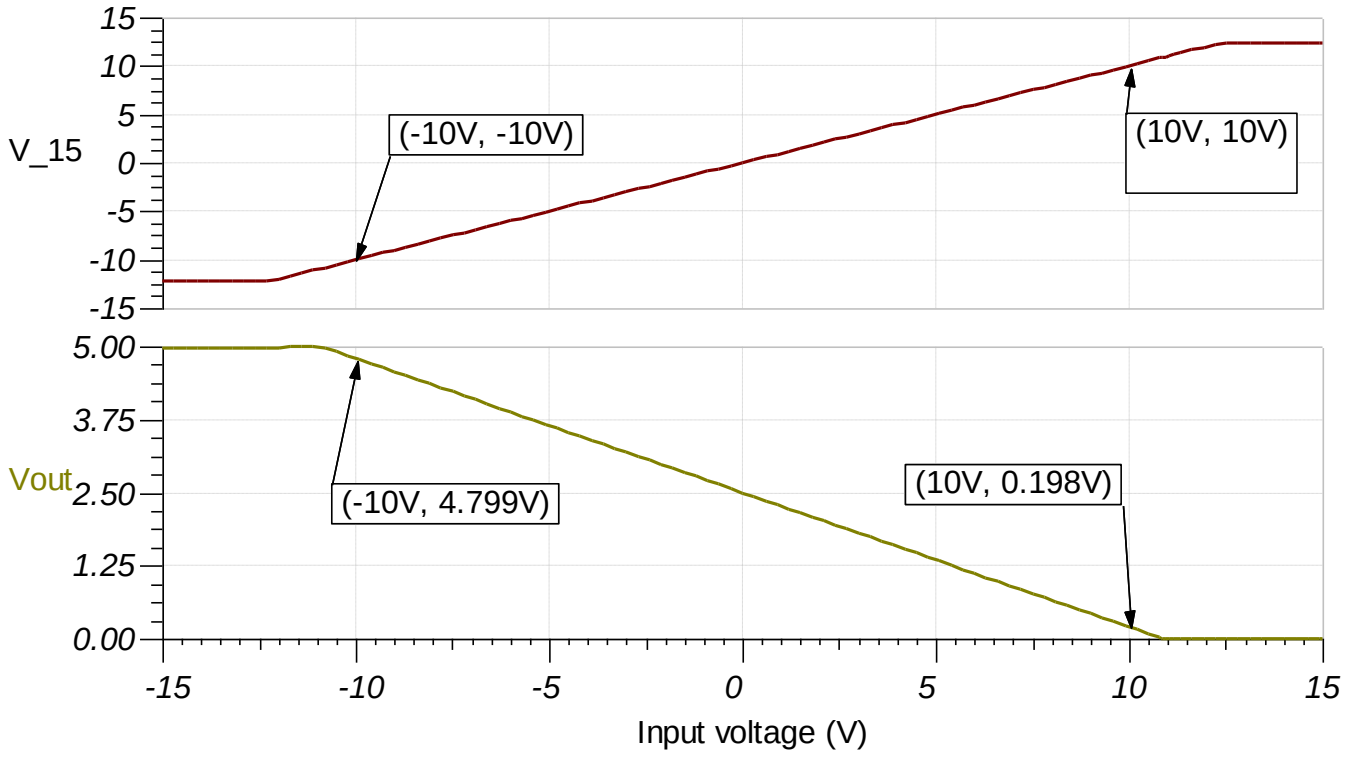


**Figure 1: Measured Transfer Function**

## 2 Theory of Operation

Figure 2 shows the full schematic for the design. The first stage (U1) is a ±15V amplifier with a ±10V linear output swing. In this example the first stage is shown as a buffer but other ±15V configurations can be used. For example an instrumentation amplifier with ±15V supplies could be used. The second stage translates the output of the first stage from ±15V to single supply 5V to be compatible with ADC inputs. The resistors in the second stage are scaled to attenuate the output from the first stage. A dc voltage (Vshift) is applied to the non-inverting input to shift the polarity of the signal to single supply. Table 2. Input to Output ScalingTable 2 shows the input to output scaling for the design in Figure 1.

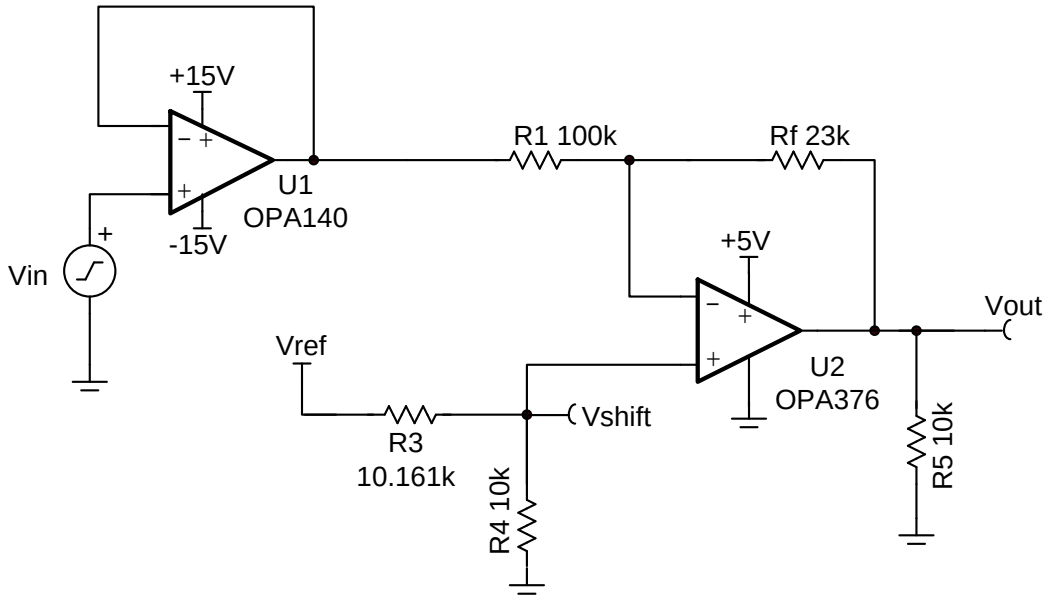


**Figure 2: Complete Circuit Schematic**

**Table 2. Input to Output Scaling**

| | Goal | Simulated |
|---|---|---|
| **Zero-Scale Input** | -10V | 0.2V |
| **Midscale Input** | 0 | 2.5V |
| **Full-Scale Input** | +10V | 4.8V |

## 2.1 Design of Level Translation Amplifier

The transfer function for the circuit in Figure 2 is given in Equation (1). The equation can be derived using superposition. The first term (-Rf/R1) is derived by grounding the non-inverting input and considering the amplifier as an inverting amplifier. It controls the attenuation of the level translation amplifier. The second term (Rf/R1 + 1) is derived by grounding the inverting path, and considering the amplifier as a non-inverting amplifier. This term adds an offset to shift the signal from dual supply to single supply.

$$V_{out} = -\left(\frac{R_f}{R_1}\right)V_{in} + \left(\frac{R_f}{R_1} + 1\right)V_{shift} \quad (1)$$

The first step in the design procedure is to choose resistors that set the gain of the amplifier. The gain of the amplifier is the change in output divided by the change in input signal (Equation (2)). The gain is also given by Equation (3). Using Equation (2) and Equation (3) and selecting an arbitrary value for R1 it is possible to solve for Rf. Note that 100kΩ was selected for R1 to minimize loading of the amplifiers. A smaller value could be used to minimize noise. Equation (6) gives the solution for Rf and Equation (7) shows how the resistor can be created using two standard value resistors. Table 3 lists standard resistor values for your reference.

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{(V_{out\_full} - V_{out\_zero})}{(V_{in\_full} - V_{in\_zero})} = \frac{(4.8V - 0.2V)}{(10V - (-10V))} = 0.23 \quad (2)$$

Where

$V_{out\_full}$ = Maximum linear output voltage.

$V_{out\_zero}$ = Minimum linear output voltage.

$V_{in\_full}$ = Maximum linear input. This input will produce $V_{out\_zero}$. Remember the amp is inverting.

$V_{in\_zero}$ = Maximum linear input. This input will produce $V_{out\_full}$. Remember the amp is inverting.

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{R_f}{R_1} \quad (3)$$

$$R_f = 0.23R_1 \quad (4)$$

$$\text{Let } R_1 = 100k\Omega \quad (5)$$

$$R_f = 0.23R_1 = 23k\Omega \quad (6)$$

$$R_f = 22k\Omega + 1k\Omega \text{ (for standard resistor values, Rfa \& Rfb)} \quad (7)$$

The second step of the design procedure is to determine the voltage applied to the non-inverting input (Vshift) that will offset the signal from ±10V to single supply 5V. An easy way to do this is to consider the midscale signal (Vin = 0V). When Vin is 0V the transfer function from Equation (1) reduces to Equation (8).

$$V_{out} = \left(\frac{R_f}{R_1} + 1\right) V_{shift} \text{ for } V_{in} = 0V \tag{8}$$

$$V_{shift} = \frac{V_{out}}{\left(\frac{R_f}{R_1} + 1\right)} = \frac{2.5V}{1.23} = 2.033V \tag{9}$$

The final step of the design procedure is to select values for the voltage divider to achieve the appropriate shift voltage. Equation (10) shows the relationship between Vref and Vshift. Vref is a reference output voltage. In this example, 4.096V is used as the reference voltage but any reference will work as long as Vref is greater than Vshift. The resistors (R2, R3, and R4) form a voltage divider. Two resistors were used (R2 and R3) to facilitate a more accurate resistor ratio using standard values. Equations (12), (13), and (14) show the math behind selecting the voltage divider resistors. Table 3 gives the standard resistor values.

$$V_{shift} = V_{ref} \frac{R_4}{(R_2 + R_3) + R_4} \tag{10}$$

$$\frac{V_{shift}}{V_{ref}} = \frac{2.033V}{4.096V} = \frac{R_4}{(R_2 + R_3) + R_4} \tag{11}$$

$$(R_2 + R_3) = 1.0161 R_4 \tag{12}$$

$$\text{Let } R_4 = 10k\Omega, (R_2 + R_3) = 10.161k\Omega \tag{13}$$

$$R_2 = 10.0k\Omega \text{ and } R_3 = 161\Omega \text{ (choose closest values from Table)} \tag{14}$$

**Table 3: Standard Resistor Table**

| Standard 1% Resistor Table | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | 10.2 | 10.5 | 10.7 | 11 | 11.3 | 11.5 | 11.8 | 12.1 | 12.4 | 12.7 | 13 |
| 13.3 | 13.7 | 14 | 14.3 | 14.7 | 15 | 15.4 | 15.8 | 16.2 | 16.5 | 16.9 | 17.4 |
| 17.8 | 18.2 | 18.7 | 19.1 | 19.6 | 20 | 20.5 | 21 | 21.5 | 22.1 | 22.6 | 23.2 |
| 23.7 | 24.3 | 24.9 | 25.5 | 26.1 | 26.7 | 27.4 | 28 | 28.7 | 29.4 | 30.1 | 30.9 |
| 31.6 | 32.4 | 33.2 | 34 | 34.8 | 35.7 | 36.5 | 37.4 | 38.3 | 39.2 | 40.2 | 41.2 |
| 42.2 | 43.2 | 44.2 | 45.3 | 46.4 | 47.5 | 48.7 | 49.9 | 51.1 | 52.3 | 53.6 | 54.9 |
| 56.2 | 57.6 | 59 | 60.4 | 61.9 | 63.4 | 64.9 | 66.5 | 68.1 | 69.8 | 71.5 | 73.2 |
| 75 | 76.8 | 78.7 | 80.6 | 82.5 | 84.5 | 86.6 | 88.7 | 90.9 | 93.1 | 95.3 | 97.6 |

## 2.2 Power Sequencing

This circuit is typically used to translate a ±15V signal to a single supply voltage that can be accepted by an ADC. A key goal of this type of circuit is to prevent the output from exceeding the input range of a single-supply ADC (0V to 5V in this example). Driving a 5V ADC or a 5V amplifier with a 15V signal will normally damage the ADC. Problems with this type circuit normally happen during power supply sequencing. The load resistance and the transient voltage suppressors prevent this design from outputting a transient signal outside of the ADC safe range.

Figure 3 illustrates what can happen if you do not take any precautions to protect against power supply sequencing issues. In this example the ±15V supplies turn on first and the 5V supply is floating. Assuming the output of U1 is at 15V, current will flow through R1 and the input ESD diode on U2 which will raise the power supply of U2 to 14.3V. The absolute maximum voltage on U2 is 7V, so the device is damaged.

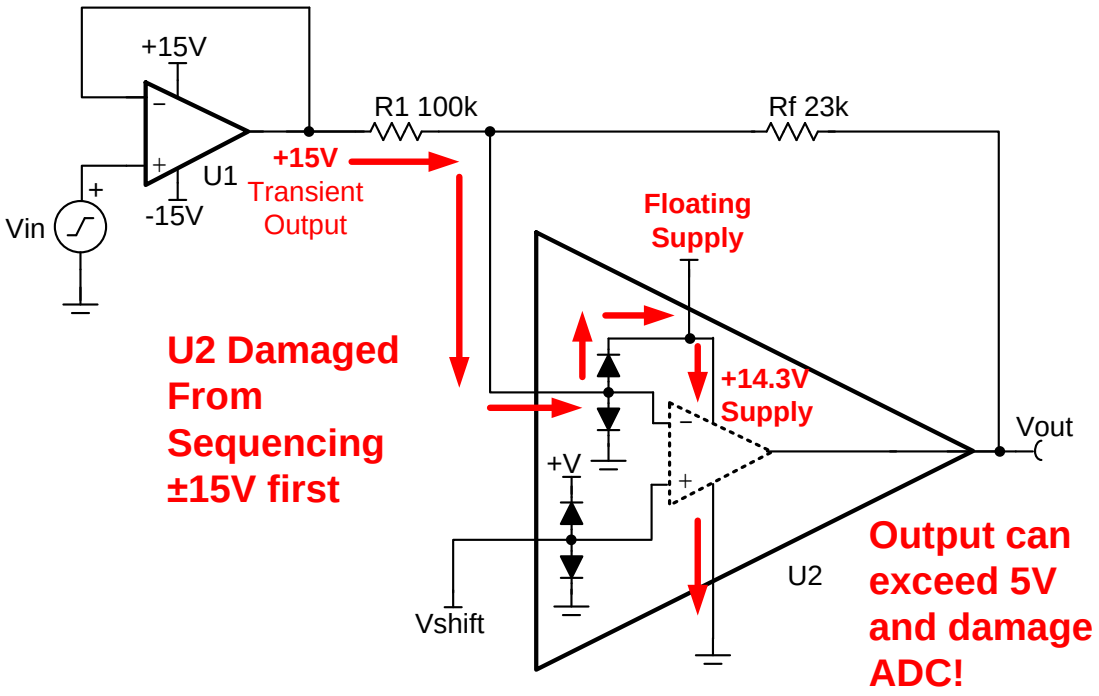


**Figure 3: Damage: No Protection for Supply Sequencing**

Figure 4 illustrates a circuit that uses a transient voltage suppressor (transorb) to prevent damage caused by power supply sequencing issues. A transorb operates like a zener diode but is optimized for fast response and capable of dissipating large energy transients for short times. In this example the ±15V supplies turn on first and the 5V supply is floating. Assuming the output of U1 is at 15V, current will flow through R1 and the input ESD diode on U2 which will raise the power supply of U2 until the transorb turns on. The transorb will limit the supply voltage to 7V which is within the absolute maximum voltage rating for U2, so the device is not damaged.

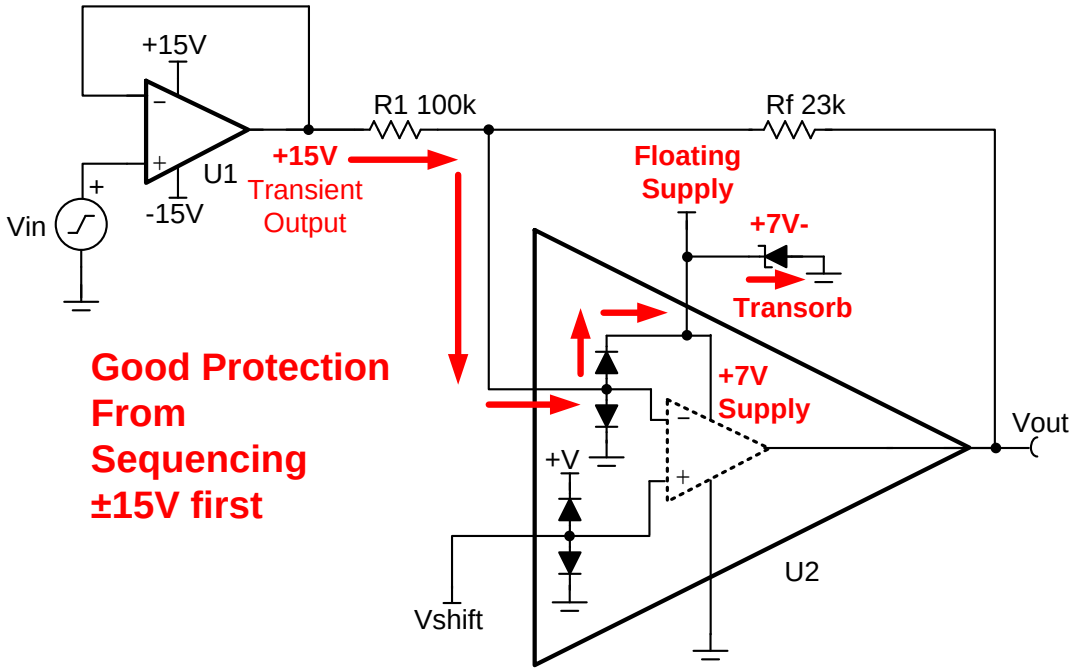


**Figure 4: Good protection from Power Supply Sequencing Issues**

Figure 5 illustrates a circuit that uses an output load as well as a transorb to prevent damage caused by power supply sequencing issues. The transorb acts as a secondary protection in this example. The primary protection is provided by the load resistor. In this example the ±15V supplies turn on first and the 5V supply is floating. The load resistor provides a path to ground for the output of U1. By considering the resistors R1, Rf, and R5 as a voltage divider you can calculate the voltage on U2's inverting input to be 3.7V. The 3.7V on the inverting input of U2 will cause current flow through the input ESD structure causing the power supply of U2 to rise to 3V. The 3V supply is well within the absolute maximum operating rating of U2. The 3V supply with not turn on the transorb. In this example, the transorb acts as a secondary protection for large transients. Thus, this circuit configuration offers two forms of protection from sequencing and general transients.

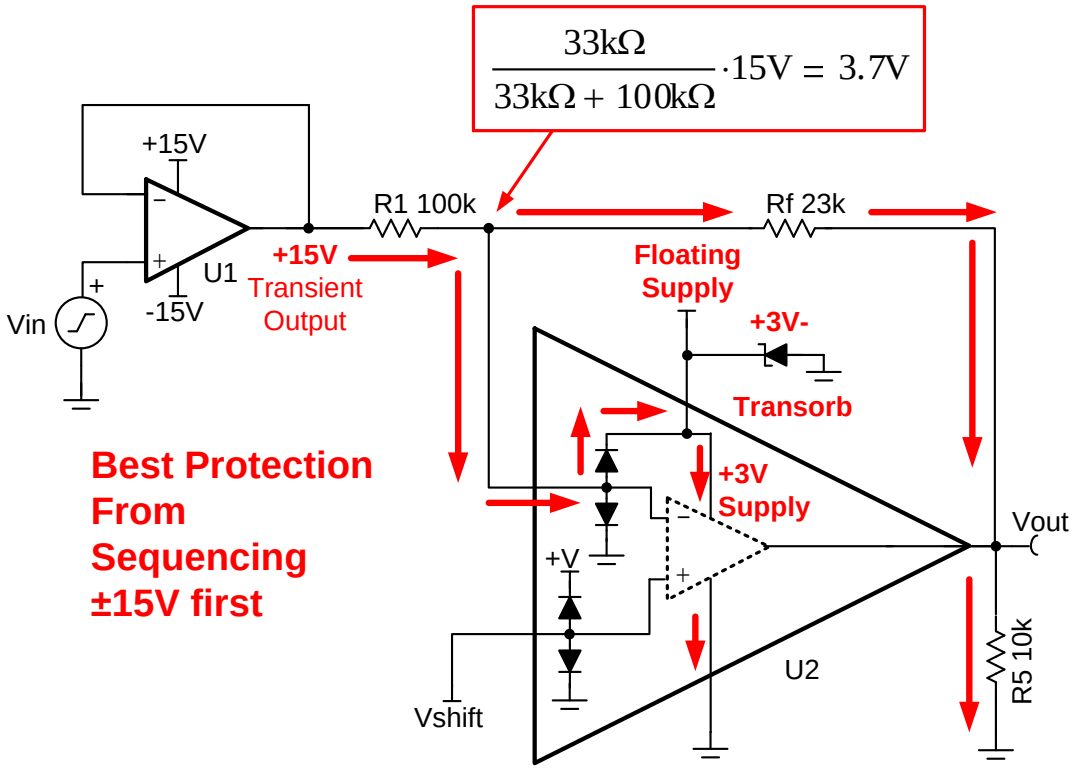


**Figure 5: Best Protection from Power Supply Sequencing Issues**

# 3 Component Selection

## 3.1 Op Amp Buffer Selection

The buffer could be any ±15V amplifier in need of level translation. In this example the OPA140 was selected for excellent dc precision, and good ac performance at an excellent price point. Other options are given in the modifications section (Section 5).

## 3.2 Op Amp Level Translation Selection

The level translation amplifier (U2) was selected for excellent dc precision, and good ac performance at an excellent price point. In this example the OPA376 was selected for excellent dc precision, and good ac performance at an excellent price point. Other options are given in the modifications section (Section 5).

## 3.3 Transient Voltage Suppressor Selection

The goal of the Transient Voltage Suppressor (TVS) is to keep the supply voltage lower than the op amps absolute maximum voltage rating (7V). Table 4 shows an example of a typical TVS specification. It is important to keep the "working peak voltage" equal to or greater than the supply voltage (5V in this example). The breakdown voltage should be less than the absolute maximum voltage. In this case the minimum breakdown voltage is 6V and the absolute maximum is 7V. Finally, pay attention to the leakage current. In some cases these diodes can have high leakage. In this example the leakage is 5µA which is small compared to the normal quiescent currents of the circuit.

**Table 4: Selecting the Transient Voltage Suppressor**

| Parameter | Symbol | CDSOD323- | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Uni-T03 | Bi-T03C | Uni-T05 | Bi-T05C | Uni-T08 | Bi-T08C | Uni-T12 | Bi-T12C | |
| Minimum Breakdown Voltage @ 1 mA | $V_{BR}$ | 4.0 | | 6.0 | | 8.5 | | 13.3 | | V |
| Working Peak Voltage | $V_{WM}$ | 3.3 | | 5.0 | | 8.0 | | 12.0 | | V |
| Maximum Clamping Voltage @ $I_P$ = 1 A | $V_C$ | 7.0 | | 9.8 | | 13.4 | | 19.0 | | V |
| Typical Clamping Voltage @ 8/20 µs @ $I_{PP}$ | $V_C$ | 19.0 V @ 20 A | | 18.3 V @ 17 A | | 18.5 V @ 17 A | | 28.3 V @ 11 A | | V |
| Maximum Leakage Current @ $V_{WM}$ | $I_D$ | 5 | | 5 | | 2 | | 1 | | µA |
| Typical Capacitance @ 0 V, 1 MHz | $C_J$ | 3 | | | | | | | | pF |

## 3.4 Passive Component Selection

The resistor tolerance and drift are the primary cause of full-scale and zero-scale error in this design. In this example, 0.1% 20ppm/C resistors are used to achieve highest accuracy for a reasonable cost target. Typical 0.1% 20ppm/C resistors cost $0.05 USD. Thus, the total cost of resistors is about $0.35 where as the cost of the active components is $2.2 USD. Choosing resistors that are more accurate than 0.1% generally costs significantly more and reduces availability. In some cases this design uses two resistors in series to achieve an accurate transfer function where standard values are not available.

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## 4 Simulation

The TINA-TI™ schematic shown in Figure 6 includes the circuit values obtained in the design process.

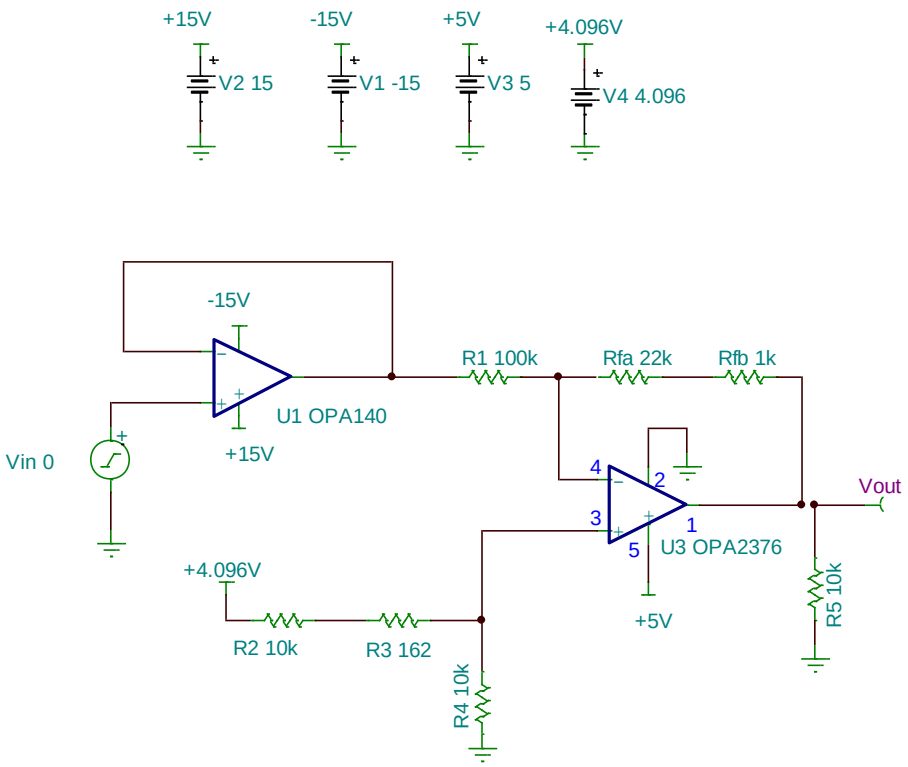


**Figure 6: TINA-TI™ Schematic**

### 4.1 Transfer Function

The result of the dc transfer function is shown in Figure 6.

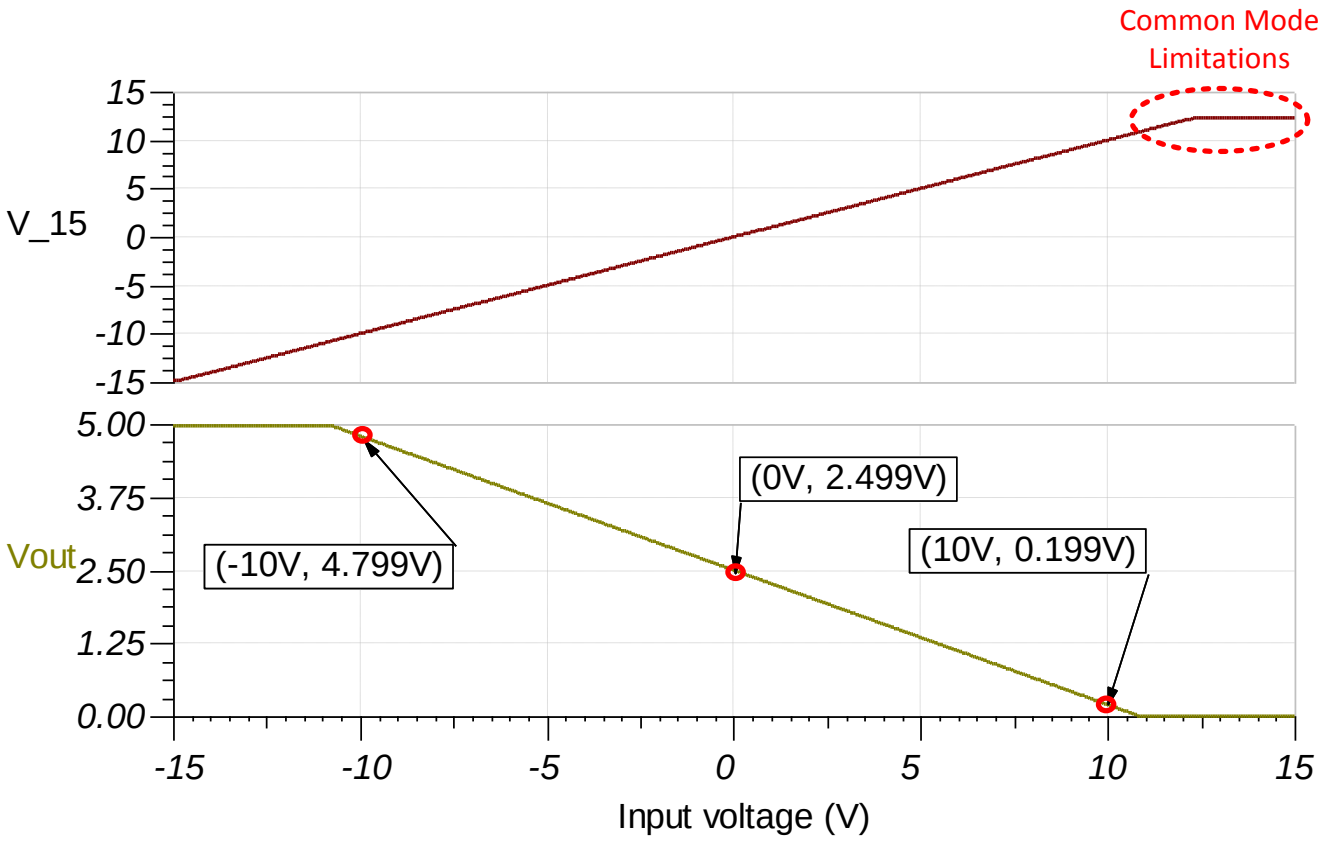


**Figure 7: Simulated Transfer Function**

### 4.2 Monte Carlo Analysis Full-Scale & and Zero-Scale Error

Figure 8 and Figure 9 show the results of a Monte Carlo analysis for the Zero-Scale Output and the Full-Scale Output. This error is dominated by resistor tolerance. In this example the tolerance was set to 0.1%.

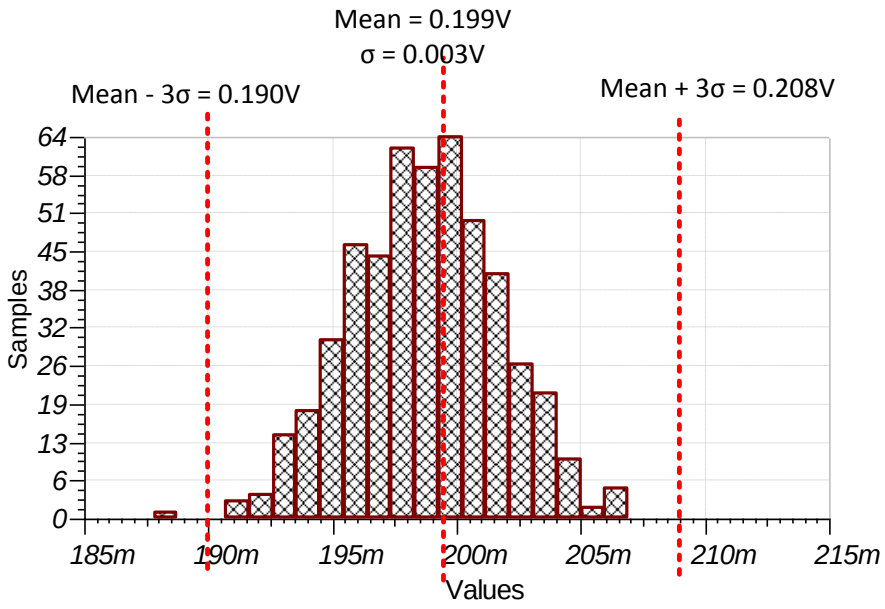


**Figure 8: Zero-Scale Output (Monte Carlo Distribution)**

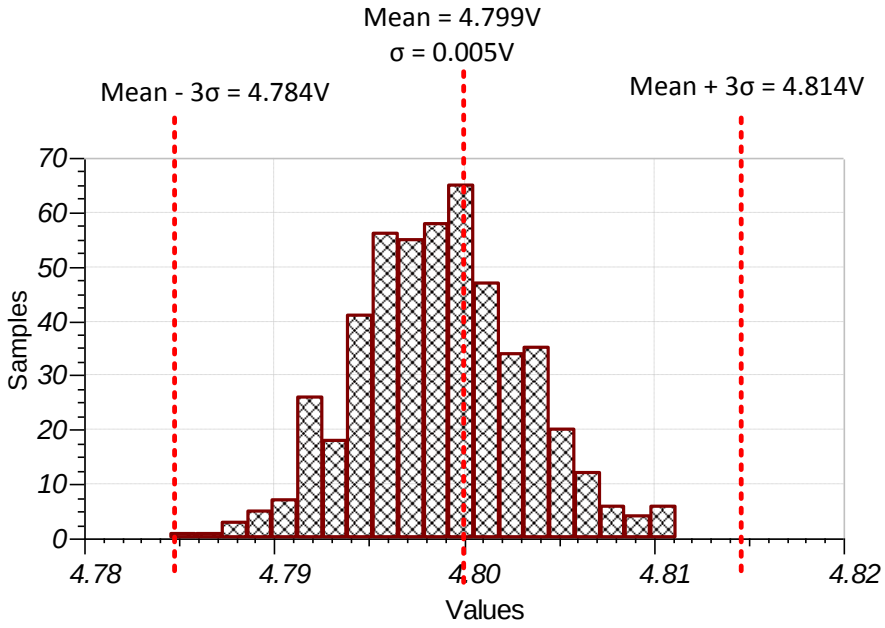


**Figure 9: Full-Scale Output (Monte Carlo Distribution)**

Equations (16) and (15) illustrate the calculation for zero-scale error and full-scale error using the statistical results from the simulation. Since the mean value in the distribution was approximately equal to the targeted performance the error is taken as plus or minus three standard deviations (±3σ). Based on probability theory, 99.7% of all devices should be within these error bands. This analysis only looks at resistor variation, because in this case resistor variation will be the dominant error source.

$$\text{Zero Scale Error (\%)} = \frac{\pm 3\sigma}{\left(V_{out\_full} - V_{out\_zero}\right)} = \frac{\pm 0.009V}{(4.8V - 0.2V)} * 100\% = 0.196\% \text{ of full scale} \quad (15)$$

$$\text{Full Scale Error (\%)} = \frac{\pm 3\sigma}{\left(V_{out\_full} - V_{out\_zero}\right)} = \frac{\pm 0.015V}{(4.8V - 0.2V)} * 100\% = 0.32\% \text{ of full scale} \quad (16)$$

### *4.3 Simulated Results Summary*

Table 5 summarizes the simulated performance of the design.

**Table 5: Summary of Simulated Results**

| | Goal | Simulated |
|---|---|---|
| **Zero-Scale Error** | 0.5% | 0.196% |
| **Full-Scale Error** | 0.5% | 0.32% |

## 5 Modifications

The method described Section 2.1 can be used for different supply voltages and different reference voltages. For example, the same method could be used to translate a ±15V amplifier to a single supply 3V amplifier. Also, any reference voltage can be used. Different amplifiers can be selected based on your requirements. Table 6 and Table 7 provide examples of different amplifiers that can be used to achieve different design objectives.

**Table 6. Brief Comparison of ±15V Supply Amplifiers**

| Output Amplifier | Design Objective | Vos uV | Vos Drift uV/degC | Iq uA | Voltage Noise nV/√Hz | GBW MHz | SR V/uS | Approx. Price US$ / 1ku |
|---|---|---|---|---|---|---|---|---|
| OPA140 | Wide Band, Low Noise, DC Precision | 30 | 0.35 | 1800 | 8 | 11 | 20 | 1.55 |
| OPA188 | DC Precision, Low Noise, Low Iq | 6 | 0.03 | 450 | 8.8 | 2 | 0.8 | 0.8 |
| OPA827 | Wide Band, Low Noise, DC Precision | 75 | 0.1 | 4800 | 4 | 22 | 28 | 3.75 |
| OPA211 | Wide Band, Low Noise, DC Precision | 30 | 0.35 | 3600 | 1.1 | 80 | 27 | 3.45 |

**Table 7. Brief Comparison of 5V Supply Amplifiers**

| Output Amplifier | Design Objective | Vos uV | Vos Drift uV/degC | Iq uA | Voltage Noise nV/√Hz | BW MHz | SR V/uS | Approx. Price US$ / 1ku |
|---|---|---|---|---|---|---|---|---|
| OPA376 | Wide Band, Low Noise, DC Precision | 5 | 0.26 | 760 | 7.5 | 5.5 | 2 | 0.65 |
| OPA313 | Low Noise, Low Iq | 500 | 2 | 50 | 25 | 1 | 0.5 | 0.3 |
| OPA333 | DC Precision, Low Iq | 2 | 0.02 | 17 | 50 | 350 | 0.16 | 0.95 |
| OPA350 | Wide Band, Low Noise, DC Precision | 150 | 4 | 5200 | 7 | 38 | 22 | 1.15 |

## 6 About the Author

Arthur Kay is an applications engineering manager at TI where he specializes in the support of amplifiers, references, and mixed signal devices. Arthur focuses a good deal on industrial applications such as bridge sensor signal conditioning. Arthur has published a book and an article series on amplifier noise. Arthur received his MSEE from Georgia Institute of Technology, and BSEE from Cleveland State University.

## 7 Acknowledgements & References

### *7.1 Acknowledgements*

The author wishes to acknowledge Collin Wells, Tim Green, and Marek Lis for technical contributions to this design.

### *7.2 References*

1. *Rfcafe.com, Standard Resistor Table: http://www.rfcafe.com/references/electrical/resistor-values.htm*

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