

TIDA-00255-bq76940, TI Design

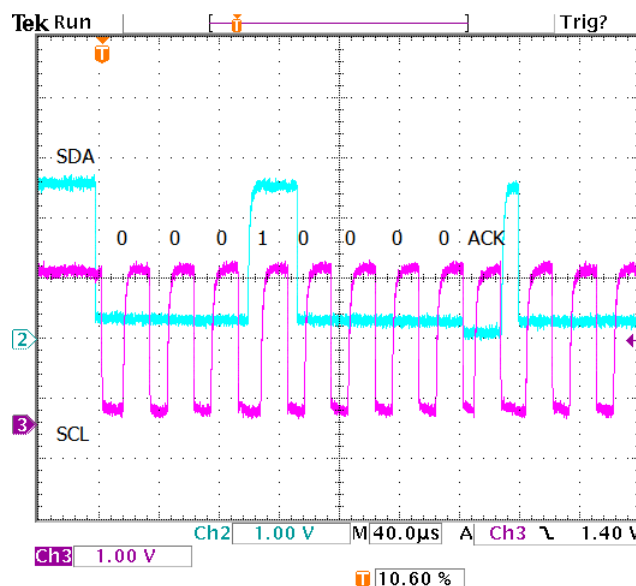
This test report describes results for TI Design using the bq76940EVM with 15-series lithium-ion cells. The bq76940EVM board schematic and layout are designed to allow easy access to signals for evaluation. Adjustments to the circuit and layout will be needed when using the design for other purposes. The gauge IC on the board is reserved for future use, it is disconnected for these tests and is not covered in this test report. Additional circuitry will be needed when implementing this circuit subsystem in to a complete product.

For this testing the board is operated with the gauge IC connection removed at J14 and communication is provided to the AFE using an EV2300 interface module connected at J8. Pull-up resistors jumpers for the I2C lines are installed at J6 and J7. Control comes from the operator of a PC using the bq76940/bq76930/bq76920 Evaluation Software. The board includes a resistive cell simulator selected with S3 and S4. The cell simulator is used where appropriate with external test equipment to provide clear demonstration of the operation. The cell simulator is a test convenience on the evaluation board and should not be considered part of a system design. It would normally be provided in a test fixture when desired. Inclusion of a cell simulator on a system board will cause discharge of the system cells.

Different boards and test setups have been used for the various tests in this report.

Communication

The AFE on the board communicates through an I2C compatible interface. The part will ACK its address as shown in the following figure. The 7 bit address 0x08 of the datasheet shows as 0x10 on the bus with the write command.



Measurement

A substantial function of the circuit is to collect cell voltage and system temperature and current data. The associated spreadsheet appended at the end of this report shows a log of this data with an overcurrent event and change of the board temperature. Measurement accuracy for the part is shown in the bq76940 datasheet.

Example measurement accuracy

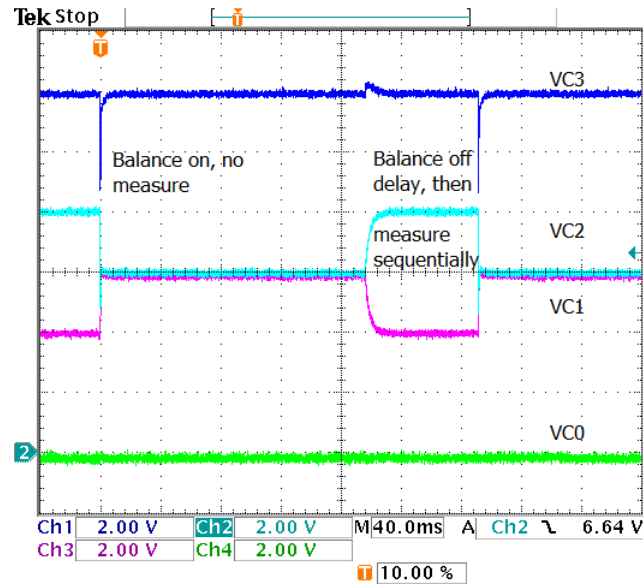
The following tables show a comparison of the reported cell voltage vs the applied cell voltage. See the datasheet for allowed variation of the ICs.

	Voltage Cell 1	Voltage Cell 2	Voltage Cell 3	Voltage Cell 4	Voltage Cell 5	Voltage Cell 6	Voltage Cell 7	Voltage Cell 8
reported	3.203	3.195	3.211	3.207	3.201	3.191	3.197	3.2
meter	3.202	3.194	3.211	3.207	3.201	3.192	3.197	3.2
mV difference	1	1	0	0	0	-1	0	0

	Voltage Cell 9	Voltage Cell 10	Voltage Cell 11	Voltage Cell 12	Voltage Cell 13	Voltage Cell 14	Voltage Cell 15
reported	3.209	3.197	3.197	3.21	3.204	3.201	3.191
meter	3.209	3.197	3.2	3.21	3.206	3.203	3.193
mV difference	0	0	-3	0	-2	-2	-2

Cell balancing

Cell balancing operates by pulling the VCn pins which monitor a cell voltage together as shown in the following figure. Balancing operates for a time and then releases to allow measurement of the cells. The input filter will take some time to respond to the application and release of this voltage.



The EVM uses large input filter capacitors C_c . These allow observation of a voltage effect due to settling of the voltage during the measurement with cell balancing operating. The induced error decreases with the number of the cell in the group. Where this is objectionable, the designer should modify the design to use smaller C_c filter capacitors.

	Voltage Cell 1	Voltage Cell 2	Voltage Cell 3	Voltage Cell 4	Voltage Cell 5	Cell Balance 1	Cell Balance 2	Cell Balance 3
bal on	4.077	3.993	4.009	4.01	3.995	0x02	0x02	0x02
bal off	4.068	3.994	4.008	4.01	3.994	0x00	0x00	0x00
mV difference	9	-1	1	0	1			

	Voltage Cell 6	Voltage Cell 7	Voltage Cell 8	Voltage Cell 9	Voltage Cell 10	Cell Balance 1	Cell Balance 2	Cell Balance 3
bal on	4.05	3.979	4.053	4.001	4.069	0x02	0x02	0x02
bal off	4.041	3.983	4.052	4.001	4.069	0x00	0x00	0x00
mV difference	9	-4	1	0	0			

	Voltage Cell 11	Voltage Cell 12	Voltage Cell 13	Voltage Cell 14	Voltage Cell 15	Cell Balance 1	Cell Balance 2	Cell Balance 3
bal on	4.076	4.037	3.984	4.085	3.989	0x02	0x02	0x02
bal off	4.067	4.036	3.983	4.085	3.988	0x00	0x00	0x00
mV difference	9	1	1	0	1			

The 3 cell groups in the bq76940 operate independently for cell balancing. This design uses the same connection to the cells for both monitoring and cell balance current. Common resistance in the path to the shared cell connection will show a voltage error on adjacent cell groups as the non-balancing group measures the addition or subtraction of the balance current \times the path resistance to the cell value. This table shows this effect on cell 11 when cell 10 is balanced. Return the cell balance current as close as possible to the cells to avoid this condition.

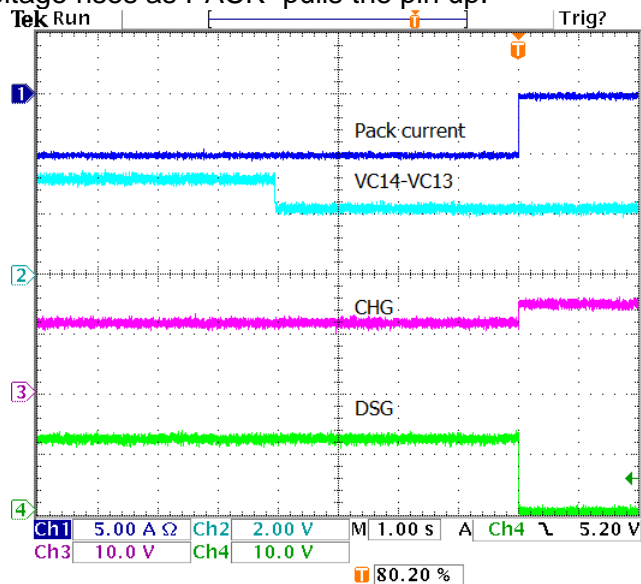
	Voltage Cell 10	Voltage Cell 11	Voltage Cell 12	Voltage Cell 13	Voltage Cell 14	Voltage Cell 15	Cell Balance 2	Cell Balance 3
bal on	4.069	4.071	4.034	3.983	4.084	3.988	0x10	0x00
Bal off	4.069	4.066	4.034	3.983	4.084	3.988	0x00	0x00
mV difference	0	5	0	0	0	0		

Protection

The board supports the protection functions of the bq76940.

Undervoltage

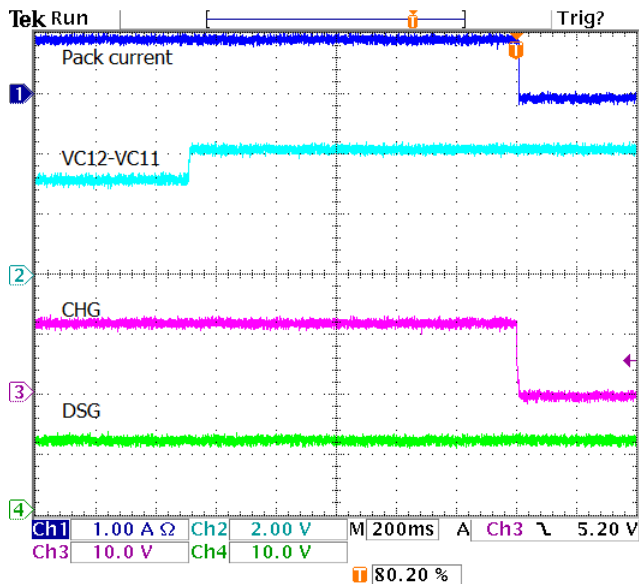
Undervoltage protection results in the turn off of the DSG signal which stops discharge current flow. An UV_TRIP register value of 0x97 results in a UV threshold of 0x1970. The devices used in this test has an offset of 45 mV and a gain of 0.377 mV/bit. The threshold for UV is $45\text{mV} + (0\text{x}1970 \times .377\text{mV}) = \sim 2500\text{mV}$. Cell 14 is stepped from 3 to 2V across that threshold. The following figure and table shows that following the under voltage delay (set at 4 s for this test) DSG goes low and current stops. CHG remains on and its voltage rises as PACK- pulls the pin up.



250 ms samples	Coulomb Counter	Battery Voltage	Voltage Cell 13	Voltage Cell 14	Voltage Cell 15	System Status	System Control2	Protection 3	UV_TRIP
-1	-0.00496	47.859	3.192	3	3.219	0x80	0x43	0x40	0x97
0	-0.00496	48.384	3.263	3	3.219	0x80	0x43	0x40	0x97
1	-0.00497	47.871	3.263	2.016	3.29	0x80	0x43	0x40	0x97
2	-0.00495	47.871	3.263	2.016	3.29	0x80	0x43	0x40	0x97
3	-0.00496	47.869	3.263	2.016	3.29	0x80	0x43	0x40	0x97
4	-0.00496	47.871	3.263	2.016	3.29	0x80	0x43	0x40	0x97
5	-0.00496	47.871	3.263	2.016	3.29	0x80	0x43	0x40	0x97
6	-0.00495	47.872	3.263	2.016	3.29	0x80	0x43	0x40	0x97
7	-0.00497	47.871	3.263	2.016	3.29	0x80	0x43	0x40	0x97
8	-0.00496	47.871	3.263	2.016	3.291	0x80	0x43	0x40	0x97
9	-0.00496	47.872	3.263	2.016	3.29	0x80	0x43	0x40	0x97
10	-0.00496	47.872	3.263	2.015	3.29	0x80	0x43	0x40	0x97
11	-0.00496	47.871	3.263	2.016	3.29	0x80	0x43	0x40	0x97
12	-0.00496	47.872	3.263	2.016	3.29	0x80	0x43	0x40	0x97
13	-0.00496	47.871	3.263	2.016	3.291	0x80	0x43	0x40	0x97
14	-0.00496	47.871	3.263	2.016	3.291	0x80	0x43	0x40	0x97
15	-0.00496	47.872	3.263	2.016	3.291	0x80	0x43	0x40	0x97
16	-0.00097	48.005	3.27	2.016	3.302	0x88	0x41	0x40	0x97
17	0.00001	48.028	3.274	2.016	3.302	0x88	0x41	0x40	0x97
18	0	48.028	3.274	2.016	3.302	0x88	0x41	0x40	0x97
19	0	48.026	3.274	2.016	3.302	0x88	0x41	0x40	0x97

Overvoltage

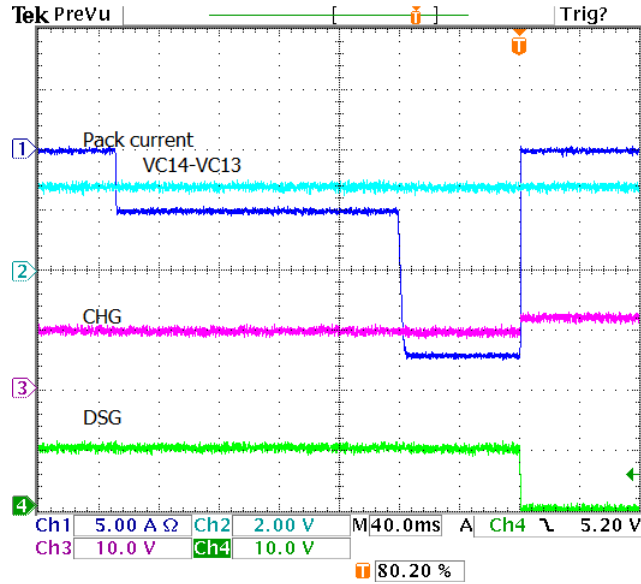
Overvoltage protection results in the turn off of the CHG signal which stops discharge current flow. A 3.8V protection threshold is desired for the test of this part having an offset of 45 mV and gain of 0.377 mV/bit. Calculating the threshold value: $(3800 \text{ mV} - 45 \text{ mV}) / 0.377 \text{ mV} = \sim 0x26E8$. The OV_TRIP register 0x09 is set to 0x6E. In this test example, cell 12 is stepped from 3V to 4V across the threshold. The following figure shows that following the over voltage delay (set at 1 s for this test) CHG goes low and current stops. DSG remains high.



250 ms samples	Coulomb Counter	Battery Voltage	Voltage Cell 11	Voltage Cell 12	Voltage Cell 13	System Status	System Control2	Protection 3	OV_TRIP
-1	0.001	48.056	3.203	3.002	3.244	0x80	0x43	0x00	0x6E
0	0.001	47.696	3.203	3.002	3.244	0x80	0x43	0x00	0x6E
1	0.001	48.26	3.133	3.99	3.244	0x80	0x43	0x00	0x6E
2	0.001	48.058	3.133	3.99	3.174	0x80	0x43	0x00	0x6E
3	0.001	48.058	3.133	3.99	3.174	0x80	0x43	0x00	0x6E
4	0.001	48.034	3.133	3.99	3.174	0x84	0x42	0x00	0x6E
5	0.00022	47.978	3.127	3.99	3.169	0x84	0x42	0x00	0x6E
6	0	47.978	3.127	3.99	3.169	0x84	0x42	0x00	0x6E

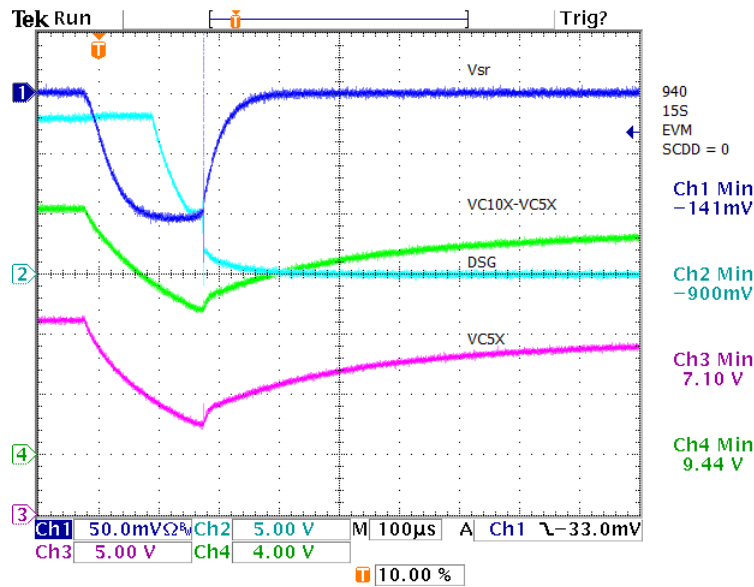
Overcurrent in discharge

Overcurrent in discharge protection response turns off the DSG output and discharge FET on the board. The following figure shows an example response with register 0x07 set to 0x32 (OCD_D = 80 ms, OCD_T = 14 mV or ~14A for the board).



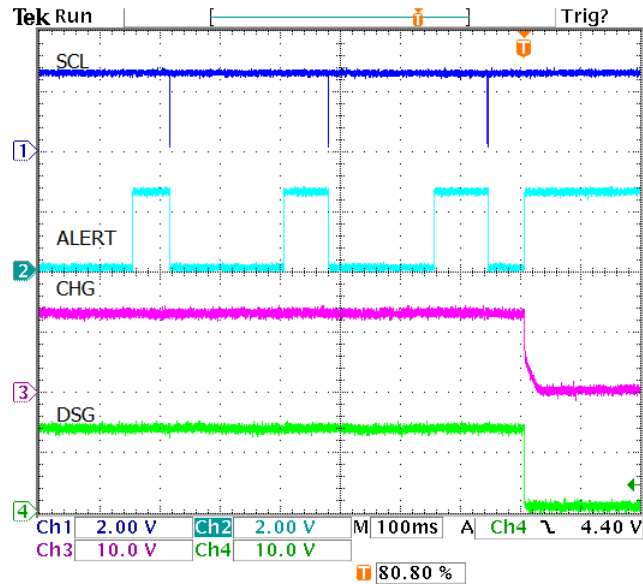
Short circuit in discharge

Short circuit in discharge protection can be a fast response to a current just over the threshold or a response to a short of the battery pack. A battery pack short is shown in the following figure. The system designer should be sure the circuit design and short circuit delay settings keep the bq76940 power supply voltages above the V_{SHUT} level in all conditions.



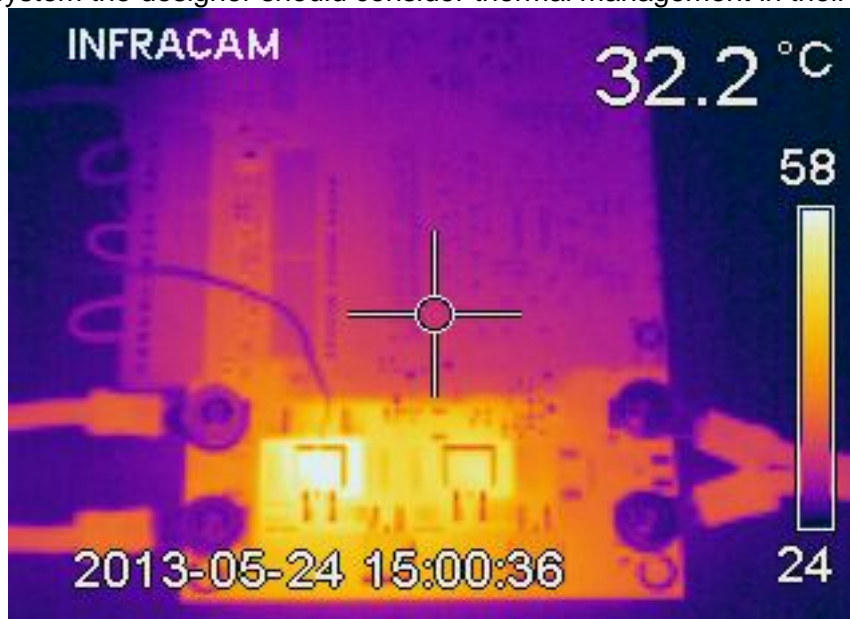
Secondary protector fault detection

The design does not include a secondary protector. The device ALERT pin is available on a test point for connection to an external circuit. ALERT is a bi-directional pin and is set by the coulomb counter completion. When ALERT is periodically cleared it provides an input for the application of an external signal through a diode to trigger the fault protection. Both DSG and CHG are turned off



Board temperature rise

The bq76940EVM board is intended for operation up to 15A at room temperature (~ 25°C). The board surface area is used to dissipate heat from the FETs, sense resistor and the high current traces. The user should provide adequate heat sinking and air flow for their evaluation. When using the design as a reference for a system the designer should consider thermal management in their design.



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