TIDA-00262 Design Considerations

Serializer Design Considerations

Serialized Output: The high speed FPDLink communication is output on the DOUT+/DOUT- pins of the DS90UB913A device. The lines are coupled with small capacitors to remove DC bias from the lines. Our application uses a single-ended output (DOUT+), and the other differential output is terminated with a 50Ω resistor. Using single-ended output rather than differential allows us to use a small coax cable, but results in a slightly less reliable signal.

During layout, minimize the distance between the coax connector and the serializer device. This line will also split off to the power-over-coax filter; this can create a stub on the transmission line, so this length after the split should also be minimized.

Reset Circuit: The PDB pin on the DS90UB913A is used to hold the device in a power-down mode until the voltages in the rest of the system can stabilize. It is important that the ID(X) and MODE pins, supply rails, and oscillator are stable when the devices comes out of reset.

Some reference designs will use an RC circuit with a large time constant to create a delay, but our design uses a Supply Voltage Supervisor (SVS). This device will hold the PDB pin low (low = powered down) once the 1.8V rail rises to about 1.1V, and will hold it low until it crosses a threshold voltage (1.71V in this case). Once reaching the threshold, there is a hard 2ms delay until the SVS will release the serializer from reset. In systems where more GPIOs are available, there is also a manual reset available on this device as well.

Parallel Image Data Interface: The DIN[0…11], HSYNC, VSYNC, and PCLK inputs to the serializer make up the interface to the Aptina Digital Image Sensor. These signals are relatively slow, especially compared to the serialized data output, but need to be length-matched on the board to a certain extent. There should not be a difference of greater than 0.25” between any of the traces.

Power Supply Decoupling and Filters: There are five supply rails on the device. All have some decoupling capacitors which supply the device with current during transient loads. These capacitors should be placed close to each supply pin, with the smaller values being placed the closest. Larger values can be further away.

In addition to decoupling, some of the supplies (VDDPLL and VDDCML) are very susceptible to noise from the switching power supplies, and can also produce high frequency noise which couples back into the system. Ferrite beads and larger capacitors are added to these lines to attenuate this high frequency noise. The behavior of these filters can be seen in the simulations section.

GPOs: The serializer has 3 GPO (General Purpose Output) pins which are also serialized and control via the FPDLink-III interface. However, in systems (like ours) where the Serializer is generating the clock for the imager, GPO3 is used as an oscillator input, and GPO2 supplies a clock for the imager. It is actually possible to instead generate the clock on the Imager and gain these GPOs back.

The two signals used on our remaining GPOs are Trigger and Reset. The Reset goes to an active-low reset pin on the Aptina imager and is used during the start-up sequence; this is a required connection. The Trigger pin is used as a "Frame Sync", which has the imager capture an image at a specified time. This is used in Surround View systems where multiple cameras are synchronized, and their images are later stitched together to create one image. If this feature is not needed, this GPO can be repurposed.

Power over Coax Design Considerations

Coax Connector: As discussed in the BOM Analysis, TI only recommends one family of automotive coax connectors be used with our FPDLink-III SerDes devices: the Rosenberger Fakra connectors. There are several variations of the housing for the same basic connector (straight/right angle, different footprints, etc.) which can be chosen depending on the form factor needed.

Power Supply Filter: One of the most critical portions of a design which uses Power over Coax is the filter circuitry. The goal is twofold: 1) deliver a clean DC supply to the input of the switching regulators, and 2) protect the FPDLink communication channels from noise coupled backwards from the rest of the system.

The DS90UB913/914 SerDes devices used in this system communicate over two carrier frequencies, 700MHz at full speed ("forward channel") and a lower frequency between 1.75 and 3.25MHz ("back channel") determined by the deserializer device. The filter should attenuate this rather large band spanning both carriers, hoping to pass only DC. Luckily, by filtering the back channel frequency, we will also be filtering the frequencies from the switching power supplies on the board.

An **ideal** series 100 µH inductor could work as a low pass filter, with impedance >1KΩ at frequencies starting at 1MHz. However, due to parasitic capacitances, a real 100 µH inductor would cease to have high impedance around 70MHz. To cover the higher frequency band, we need another series inductor. A 4.7 µH inductor will ensure we have high impedance up to frequencies well above the 700MHz forward channel.

For this design we want to minimize the physical size of the inductors used, which is determined by the saturation current of the inductor. As discussed in the Power Budget section in the Power Supply design considerations, ideally we would only be drawing 67.33 mA of current @9V to power our system. However, we need to take into consideration a few non-idealities. First, the efficiency of our power supply is designed to be 77%, not 100%. Second, any voltage droop (due to various causes) from the supply will cause the system to draw more current. Due to this, a conservative approach is to add saturation current headroom above what is needed (37% headroom used in this design).

The ferrite bead is added for filtering out coupled Electro-Magnetic Interference (EMI) in the coax cable. The capacitors are simply bulk capacitance to reduce current ripple to the input of the power supplies. Of course these components effect the frequency response of the filter as well. See the simulations section to see the frequency response with these components removed. Here is a summary:

Topology	-3dB Point (Hz)
As Designed	9.28k
No Ferrite Bead	9.47k
No FB or Caps	146.9k
Inductors Only	160k

Power Supply Design Considerations

General Comments: Due to the fact that our design is targeted at automotive applications, there are a few considerations that constrict our design choices. In addition, there are a few systems-level specifications as well which shaped our overall design:

-The total solution size needs to be minimized to meet our size requirements for the system (less than 20 x 20 mm). This means that we need to minimize the need for external components by choosing parts which integrate as much as possible, such as FETs, diodes, and compensation networks, or even choosing a fixed-voltage part to eliminate feedback resistor dividers.

-To avoid interference with the AM radio band, all switching frequencies need to either be greater than 1700 kHz or less than 540 kHz. Lower switching frequencies are less desirable in this case because they require larger inductors, and can still produce harmonics in the AM band. For this reason, we chose to look at higher frequency switchers.

-All devices chosen need to be AEC Q100 (-Q1) rated.

-Efficiency is important insofar as to keep the total power budget <1W. We can balance efficiency with size and cost, but wanted to keep this as a good number to stay below. Though the system will be quite low-power anyway, it is also an extremely small board in a hot environment.

Power Budget: Before choosing parts, one needs to know a few things: input voltage range, rails needed, and current required on each rail. The input voltage in our case is a pre-regulated 9V supply coming in over coax. We will discuss the possible range later, but this is our nominal value. Our system has only two main ICs which will consume the majority of the power. Here are the requirements for those devices:

	Voltage	Current (Typ) (A)	Current (Max) (A)	Power (Typ) (W)	Power (Max) (W)
DS90UB913Q					
VDDT	1.8	0.061	0.08	0.1098	0.144
VDDIO	1.8	0.0015	0.003	0.0027	0.0054
Aptina Imager					
VDD	1.8	0.12	0.14	0.216	0.252
VDDIO	1.8	0.018	0.025	0.0324	0.045

VAA	2.8	0.035	0.045	0.098	0.126
VAA_PIX	2.8	0.003	0.004	0.0084	0.0112
VDD_PLL	2.8	0.006	0.008	0.0168	0.0224
TOTALS		0.2445	0.305	0.4841	0.606

Summing these values up, we need **~248mA for the 1.8V rails**, and **57mA for the 2.8V rails**. If we later choose to cascade these power supplies, then the 2.8V regulator will actually need to source the current for the 1.8V rail as well. This neglects the consumption of passive components, oscillator, IC quiescents currents, etc., but is a good ballpark number. We now have our input and output voltages, and our output current requirements. Also, since we know the total wattage needed, we can calculate what our input currents will look like:

$$P_{out} = P_{in} = I_{in} * V_{in} \rightarrow 606mW = I_{in} * 9V \rightarrow I_{in} = \mathbf{67.33\ mA\ (Max)}$$

These numbers give us a good starting point for selecting the parts and topology for our regulators, as well as our inductor selections later on. However, this does not take into account the efficiencies of our power supplies.

Part Selection: There are several factors affecting our part selection for the power supplies. We can immediately filter out all parts that are not Q100 rated, as well as those with switching frequencies in the AM band. We also need them to satisfy the voltage and current in/out requirements listed above (though this depends a bit on which topology we choose, which is discussed in the next section). We also know that our input voltage will always be strictly greater than any of our power rail needs, so we choose from buck regulators and LDOs only. This still leaves us with a huge range of devices to choose from.

The key feature of our system design is small solution size, so the biggest factor in choosing parts is high integration. Integrating FETs, compensation networks, and sometimes feedback, can significantly reduce total solution size. Many of our buck regulators integrate everything but the input/output caps and the inductor into very small packages. With high integration, you also lose a lot of efficiency across different operating points. However, for our design we were willing to sacrifice some efficiency for size and simplicity reasons.

Ultimately we chose two device families that would be good candidates, the TPS621x0 (TPS62170 for the 2.9V rail), TPS621x1 (possibly the TPS62171 as an option for the 1.8V rail) and TPS6223x (TPS62231 is the fixed-1.8V option).

Topologies: Since we only have two rails, we have the option of either having a parallel topology (both rails being fed by the input voltage), or a cascaded topology (one rail is fed by the input voltage, and then feeds the second rail). We present here a few sample options, including buck regulator only (which is what our final design uses), buck + LDO, and LDO only solutions. There are of course many more ways to design this power supply, these being just a few.

Device (2.9V)	Device (1.8V)	Topology	Efficiency (theoretical)	Cost (1ku)

TPS62170	TPS62171	Parallel	80.70%	$1.30
TPS62170	TPS62231	Cascade	77.10%	$1.15
TPS62170	LM2941 (LDO)	Cascade	60.20%	$1.33
LM2941 (LDO)	TPS62171	Parallel	57.50%	$1.33
LM2941 (LDO)	LM2941 (LDO)	Cascade/Parallel	22.30%	$1.36

Clearly the largest trade-off with using LDOs is that the efficiency drops significantly, raising our total power draw to over 1W. We chose to go for a lower-power design; however, in some situations a designer may sacrifice the efficiency in order to avoid the inherent noise and EMI issues associated with switching power supplies.

Another decision to make is parallel vs. cascaded topologies. In this case, the parallel topology is actually the most efficient. However, it presents a few problems, especially in the case of the TPS62170+TPS62171 parallel combination. The first issue is that the TPS62170 would be running in discontinuous mode, which could potentially introduce noise into the system that is different from the typical switching frequency. The second issue is that we would now have two different regulators introducing noise backwards to the input. Since they have similar switching frequencies, this could cause low-frequency beat frequencies that are very difficult to filter out. We were willing to sacrifice the efficiency in order to avoid these possible issues.

Ultimately we chose to go with the TPS62170 & TPS62231 Cascaded topology. It is significantly more efficient than designs using LDOs, though not the most efficient design available. It is, however, lower cost than the more efficient options. Functionally, the cascaded topology means that the output current is sufficient such that neither device will operate in discontinuous mode, allowing us to better predict and control the switching noise produced by the devices, and operate with better efficiency.

Component Selection/Circuit Design: Finally, we'll discuss some specifics for the circuitry around each chosen part.

TPS62170: A lot of the component selection and design theory can be found in the Application Information section of the datasheet. There are very few external components to choose.

Since the device is internally compensated, it is only stable for certain component values in the LC output filter:

	4.7µF	10µF	22µF	47µF	100µF	200µF	400µF
1µH							
2.2µH		√	√(2)	√	√	√	
3.3µH		√	√	√	√		
4.7µH							

On the left are inductor values, across the top are output capacitor values, and the check-marked boxes are stable combinations. There are only two values to choose from for the inductor; lower inductances will give better transient response, while larger inductances reduce ripple current. We chose to use 2.2uH, the recommended value. We also chose to use a 22uF output capacitor, as larger values would

require prohibitively large package sizes for our application. Larger capacitance values would give better output current ripple filtering.

With our inductance value chosen, we now need an inductor with a proper saturation current. This is going to be the combination of the steady state supply current, as well as the inductor ripple current. We want the current rating to be sufficiently high, but minimize it as much as possible to reduce the physical size of the inductor. The following is the equation used to calculate the inductor ripple current (from the datasheet):

$$\Delta I_L = V_{out} * \left(\frac{\left(1 - \frac{V_{out}}{V_{in}}\right)}{L * f_{sw}} \right)$$

Here are the parameters for our design using the TPS62170:

$$V_{out} = 2.9V, V_{in} = 9V, L = 2.2\mu H, f_{sw} = 2.25MHz$$

Which yields an inductor current of ΔI_L = 397mA. The maximum current draw of the system through this regulator is 238mA. Finally, the following equation gives us our minimum saturation current (as discussed in the Power Section of the BOM Analysis):

$$L_{sat} \geq \left(I_{max} + \frac{I_{ripple}}{2} \right) * 1.2 = \left(238mA + \frac{397mA}{2} \right) * 1.2 = \mathbf{524mA}$$

We chose a MuRata LQM21PN2R2MC0D which has a saturation current of 600mA in a very small 0805 SMD package.

The input capacitor value was chosen to be 10uF. This can be increased for better decoupling, and to reduce input current ripple. However, in order to keep the package size small (0805 in this case), we chose not to go any higher.

The output voltage is determined by the resistor divider to the feedback pin. The following is the calculation for our output voltage. We aim for 2.9V out, but wanted to work with readily available resistor values:

$$R_1 = R_2 * \left(\frac{V_{out}}{V_{ref}} - 1 \right) \rightarrow V_{out} = \left(\frac{R1}{R2} \right) * V_{ref} + 1 = \left(\frac{261k\Omega}{100k\Omega} \right) * 0.8V + 1 = 2.888V$$

This gives us a close enough output voltage to the desired 2.9V.

TPS62231: This device is a bit easier than the TPS62170 because it is a simpler, fixed voltage device. However, the considerations are quite similar.

Following the same procedure as for the TPS62170, we select the output LC filter for this supply. This converter is stable with a 1uH or 2.2uH inductor and a 4.7uF capacitor. The larger inductance was chosen in this case in part to reduce ripple current (important for keeping the regulator in continuous

mode), but also because we are able to use the same inductor for both regulators, reducing unique BOM count. The above equations can be used to find a minimum L_{SAT} of 360mA which our inductor covers easily.

The only additional feature of this device not present on the TPS62170 is the Mode select pin. By pulling this pin up we are able to force PWM mode. With our typical load current, the PFM/PWM mode option would not provide additional efficiency benefits.

Layout: There are a few guidelines for placement and layout of the power supplies. There are not many components in this design due to the high integration of the devices.

- Generally, avoid long traces and keep the components as close to the regulators as possible
- The input capacitor should be located as close as possible to the VIN and GND pins of the devices
- The inductors should be kept close to the regulator, and the switch nodes (between the inductors and SW pins) kept short. Other traces should not be routed directly under the switch node or the inductor body on other layers. If possible, place a ground layer between the regulator and signals on other layers. This will help decouple radiated noise from the high energy switch nodes.
- Feedback resistors (where used) should be placed close to the device
- Ensure that the device is well grounded to a pour on the same layer and through vias to ground layers

Aptina Digital Image Sensor Design Considerations

Parallel Image Data Output: Please see the same section in the Serializer design considerations for comments on this data bus which is also connected to that device.

Power Supply Filters: Imaging devices are particularly susceptible to noise from the rest of a system. Disturbances to power supplies can actually visually affect the image data captured, which is very undesirable. The three analog supplies (VAA, VDD_PLL, and VGND_PIX) therefore need filtering to ensure noise is not coupled into the critical imaging parts of the IC. RC low-pass filters are used, and are designed to have corner frequencies well below the frequency of any other frequencies being produced on our board. The following is a table of the corner frequencies of each of the three filters:

Device Supply	-3dB Point (Hz) of filter
VAA	7.58k
VDD_PLL	86.79k
VGND_PIX	3.05k

This is well below the frequency range of anything being produced on our boards.

In addition to filtering, the RC circuits serve a second purpose: power supply sequencing. Due to the different RC time constants of the filters, each rail comes up about 100µS after the last one (VDD_PLL->VAA->VGND_PIX), which is a requirement set in the Aptina datasheet.

Optics and Mechanical Considerations: Optics is a very important part of a camera design. After selecting a Digital Image Sensor, the lens itself can be chosen. Be sure that the lens is chosen for the size of the sensor being used; in our case, the ¼" AR0140AT sensor is being used, so we chose the DSL945D lens from Sunex Optics which is designed for this size sensor in Automotive applications.

One of the determining factors in the physical shape of our design was the optics housing needed for the lens selected. Our board was actually shaped to exactly fit on the bottom of the lens housing we chose, the CMT821 from Sunex Optics. After choosing a housing, there are some very important considerations for layout to ensure the integrity of the housing and your board:

- If screws will be used to mount the housing to your board, ensure that when the screw is tightened, there is no risk that it will come into contact (physical or electrical) with any components on the board. For this reason, it is wise to choose the screw you will use before finishing the layout and creating a keep-out area on the PCB where the screw head will come down.
- The area where the housing will rest on the PCB, there needs to be a strict keep-out of components, pads, and through-hole components from the other side. Traces and tented vias which will not be soldered are ok. One needs to ensure that the housing will mount completely flush with the board, so that the lens will not be askew with respect to the image sensor
- The lens will screw down into the lens housing. It is possible for the lens (when focusing) to come down and nearly make contact with the image sensor. For this reason, it is best to keep component bodies outside of this area to avoid interference with focus or possibly crushing a component.

TIDA-00262 BOM Analysis

General Comments: There are a few general requirements for components in this design:

Automotive Qualification: Every IC and passive component must be automotive qualified. For all components this implies an extended automotive temperature range. For TI ICs this means they need to be AEC Q100 rated (denoted as Q or –Q1 on part numbers). For capacitors, this means that the dielectric must have an appropriate temperature coefficient (X7R should be used).

Voltage Rating: During selection of capacitors, consider the possible maximum voltage that could be seen by that component. This will affect the size of the capacitor. Parts that are directly exposed to an external source (such as those on the input filter) should be chosen with high voltage ratings to protect from unexpected spikes from other parts of the system not under the

designers control. Other capacitors which are driven only by on-board supplies can have their voltage rating requirements relaxed.

Resistor Precision: Unless otherwise noted, 5% tolerance resistors should be fine in most places (pull-ups/pull-downs, part of RC filters, etc.). There are certainly some places where it is appropriate, but cost can be saved by not choosing high precision resistors where it isn't necessary.

Coax Input: The only electrical input/output to the board is a single coax connection, which carries power to the board as well as data riding on two carrier frequencies, as discussed in the design considerations section. There are several key components in this section:

Coax Connector: This is an extremely critical component to signal integrity. The baseline requirements are that it should be an automotive graded SMB 50Ω connector. TI's FPDLink interface team has characterized several manufacturers' connectors with our SerDes devices, and has determined that the Rosenberger Fakra connector series is the only one which provides great signal integrity. It is heavily recommended that the one sticks with a connector within this family.

Inductors: The inductors are the most important part of the filter to the power supplies. The inductance values chosen for the inductors are discussed in the design considerations section. Besides the inductance, the most important factor is the saturation current of the two inductors. The designer must take into consideration both the normal maximum power draw, as well as the **peak** current, especially during startup when there could be a large inrush current. The inductor's physical size scales with its saturation current, so there is reason to minimize this value. Good practice would be to find the max current of your system, and add a safety factor (perhaps 20% of current overhead). Finding the maximum current is a topic discussed in the design considerations.

Other Components: Other components in the filter simply need to be rated for the voltage and power that they can be expected to be seen by them. Their necessity to the design of the filter is discussed in the design considerations section. The ferrite bead is used for EMI compliance; if the user doesn't need to pass EMI tests, it may be removed. The capacitors may also be unnecessary if the filter is already very close to the input capacitor of the power supply.

Power Section: The IC's for the power section were chosen to reduce the BOM count to save on space and complexity, as discussed in design considerations.

Output Filters: The inductor and capacitor values are important to the stability of the power supplies, but they are discussed in the design considerations. Once the inductance value is selected, the only important factor is the saturation current. In addition to the normal current draw of that rail, one must also consider the ripple current of the inductor, which is quite large. This ripple current can be calculated from the inductance, switching frequency, and input/output voltages (this calculation is done elsewhere). Choose a saturation current which satisfies the following:

$$L_{sat} \geq \left(I_{max} + \frac{I_{ripple}}{2} \right) * 1.2$$

Where L_{sat} is the saturation current of the inductor, I_{max} is the maximum current draw of that power rail, $I_{ripple}/2$ is half of the inductor ripple current (the part of the ripple above the maximum current draw), and 1.2 provides a 20% overhead.

Pull-ups and test resistors: The pull-ups on enable and mode lines, as well as the 0 Ω resistors in series with the outputs, are there simply for testing purposes. If needed, the 'Rtest' resistors can be removed, and the pull-ups can be replaced with shorts and pulled directly up to the rail.

Feedback resistors: These resistors need to be 1% tolerance. To reduce current, they can be large values, but should not be made any larger than 400kΩ at the very most.

Imager Section: The CMOS imager has some power supply filtering and other components associated with it, but not much needs to be noted.

Test Resistors: There are several resistors on the schematic which are only present for testing, and could be removed if needed; specifically, the 0Ω pull-downs on OE_BAR and STANDBY lines, as well as the R_{vddio} & R_{vdd}. Functionally, these serve no purpose.

Pull-up Resistors: The pull-ups on the I2C lines are currently set to 3.3kΩ, but this value can be changed. Be aware that using weak pull-ups can cause the rise-time of the I2C lines to be too slow, potentially leading to problems with communication. 10kΩ or stronger pull-ups should be used.

Serializer Section: The FPDLink-III serializer has mostly just power supply decoupling/filtering and some resistor dividers, but some are notably important.

Resistor Dividers: The resistor dividers on the ID(X) and MODE pins feed internal comparators/ADCs to determine settings for the device. Do not vary the values of these components, and use precision resistors if possible. Currently the bottom leg of the ID(X) divider is a 0Ω resistor; normally this would indicate that it could be replaced with a short if needed, but in this case it is best to leave it. It can be replaced with other values to change the I2C address of the device, which could be important in designs with multiple serializer devices.

Supply Voltage Supervisor: This device is selected to hold the device in a power-down mode while other voltages on the boards settle. Ensure that any SVS selected has an active-low, push-pull output. If a device with open-drain output is used, add a 10kΩ pull-up. This circuit could be replaced by an RC delay circuit to save on silicon costs, but is less of a robust design.

Power Supply Filters: The power supply decoupling and filter components are discussed in design considerations, but there are no special considerations for the components themselves.

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