Design Guide: TIDA-00236

Low-Side 0.5A, 8-Channel Digital Output Module for PLC

TEXAS INSTRUMENTS

Description

TI reference designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI reference designs help *you* accelerate your time to market.

Resources

TIDA-00236	Design Folder
TIDA-00123	Design Folder
DRV81646	Product Folder
ISO6441	Product Folder
ISO6421	Product Folder
TLC5927	Product Folder
LM5009	Product Folder
LM2936	Product Folder

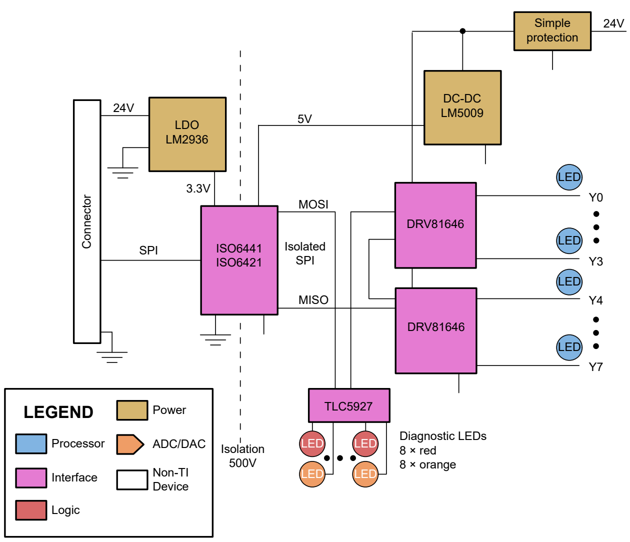
Ask our TI E2E™ support experts

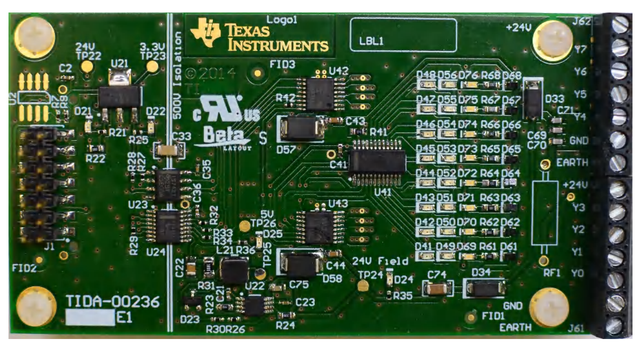
Features

- High-density 8-channel, 24V low-side digital output
- 500mA/channel unregulated (20%), 2A peak
- Data serializer to save isolation channels
- Capable of switching inductive loads
- LED to indicate output state and faults
- Standalone use or with TIDA-00123

Applications

- Programmable Logic Controller (PLC) I/O modules
- Distributed Control System (DCS) I/O modules
- Motor control I/O modules
- Sensor concentrators





1 Key System Specifications

Table 1-1. Key System Specifications

SYMBOL	PARAMETER	CONDITIONS	SPECIFICATION			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage	Normal operation	10	24	33	V
I_{IN}	Input current	Normal operation	-	15	50	mA
V_{LOAD}	Load supply voltage	Normal operation	0	24	44	V
I_{LOAD}	Load current	Per channel T_A = 60°C	-	500	600	mA
		Per channel T_A = 25°C	-	700	1000	mA
P_{LOSS}	Power loss per channel	R_L = 48Ω, V_{LOAD} = 24V, T_A = 25°C	-	200	-	mW
f_{SW}	Switching frequency	Resistive load		1000		Hz
		Inductive load, 0.1H all channels		10		Hz
t_{RISE}	Load voltage rise time 10% .. 90%	R_L = 48Ω, V_{LOAD} = 24V, T_A = 25°C	-	600	-	ns
t_{FALL}	Load voltage fall time 90% .. 10%	R_L = 48Ω, V_{LOAD} = 24V, T_A = 25°C	-	120	-	ns
t_{PD}	Propagation delay (latch to output change)	R_L = 48Ω, V_{LOAD} = 24V, T_A = 25°C	-	150	-	ns
I_{PEAK}	Peak current (1ms)		2.3		3.8	A
P_{IND}	Inductive power for each group of channels[(1)]				0.5	J/s

(1) Outputs Y0 to Y3 are one group and outputs Y4 to Y7 are one group.

2 System Description

A digital output (DO) module is a standard module in a PLC or DCS system. The DO module is used to permanently turn on and off resistive, capacitive, or inductive loads or control them with pulse width modulation (PWM).

A digital output with a MOSFET can be realized as a high-side or low-side switch. This design uses the low-side switch principal, which means that the load connected to the output between the 24V supply and the output of the module. Therefore, the switch is below the load seen from the 24V DC supply.

The advantage with this principal is the lower cost of the switching MOSFETs as the MOSFETs can be of NMOS type, which are smaller compared to a PMOS FET with the same $R_{DS(on)}$ and does not need a voltage above the supply voltage to operate the FET in the saturated region. Conversely, low-side configuration is more sensitive to corrosion as the load is permanently connected to a 24V supply even when switched off. This configuration also means that a short to ground turns on the load unintentionally.

In most cases, the digital outputs are galvanic isolated from the control of the outputs. This design uses low power digital isolators to separate the 24V field supply from the SPI control signals. The use of SPI as a control interface reduces the number of isolated channels from eight channels to four. The field side also has a high efficiency power supply from 24V DC to power the digital isolators, the LED driver, and status LEDs.

The form factor of the board and the connector enables the TIDA-00236 to be used with TIDA-00123 and use the onboard microcontroller (MCU) to control the outputs. The board can also be used alone and use the standard connector on the top side for connection to any MCU or microprocessor (MPU) capable of handling SPI communication.

3 Block Diagram

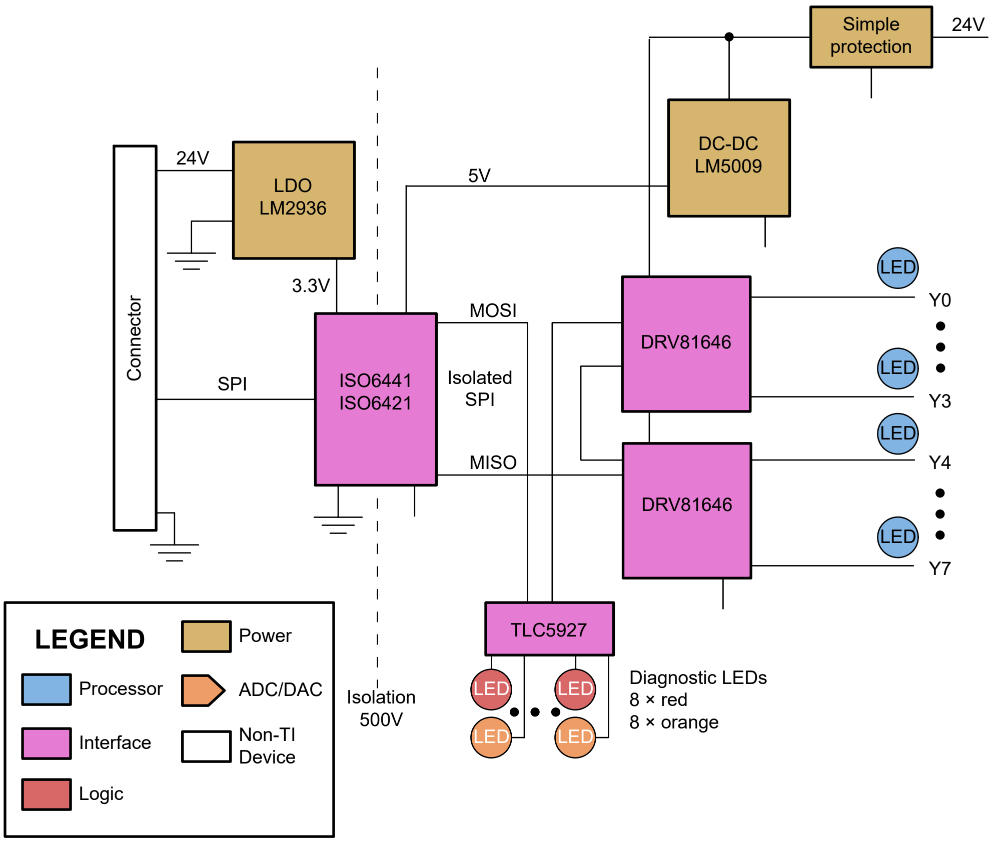


Figure 3-1. Simplified Block Diagram

3.1 Highlighted Products

The TIDA-00236 has eight digital outputs configured as low-side drivers. The design uses two DRV81646 with four protected low-side drivers integrated in each device. The on-chip shift register control logic makes it possible to control the output through SPI and also daisy chain multiple devices (in this case, two). Compared to a paralleled control approach, this saves isolation channels as one SPI channel (four lines) can control eight output channels or more. The ISO6441 provides galvanic isolation for the SPI channel. Each DRV81646 also has a global fault pin, which indicates fault on any of the four output channels. Those signals are connected to the ISO6421, which galvanic isolates the signal. LM5009 is used in a low-cost buck configuration to provide 5V to power the secondary side of the ISO6441 and ISO6421. The 5V is also used for the TLC5927 including LEDs. The LED lighting driver TLC5927 drives to two programmable status LEDs per output, 16 in total. An additional eight status LEDs are connected to the outputs of the DRV81646 and indicates the physical status of the output. The LM2936 is a low-cost low dropout (LDO) to supply the primary side of the ISO6441 and ISO6421 with 3.3V.

3.1.1 DRV81646

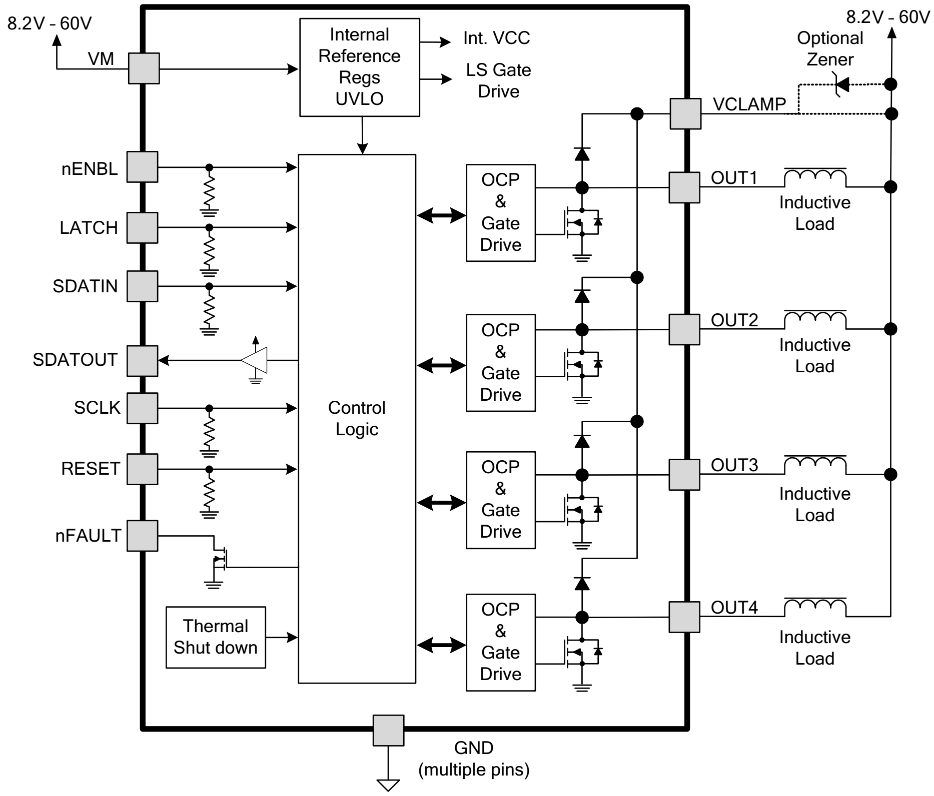


Figure 3-2. DRV81646 Functional Block Diagram

The DRV81646 is a four-channel low-side driver with overcurrent protection in combination with built-in clamping diodes makes the device an excellent choice for driving resistive, capacitive, or inductive loads. The control logic provides an SPI, which can daisy chain multiple devices. DRV81646 also supports parallel (GPIO) interface control. The DRV8803 has similar functionality but with a parallel interface instead of SPI, so this design can be used for evaluating thermal and driving performance of that device as well.

Internal shutdown functions are provided for overcurrent protection, short circuit protection, undervoltage lockout, and overtemperature and are all connected to the nFAULT pin.

3.1.2 ISO6441 and ISO6421

The ISO6441 and ISO6421 provide galvanic isolation at 5000V_{RMS} for one minute per UL or 10400V_{PK} per VDE. The ISO6441 offers three channels in the forward direction and one back channel, which makes the device an excellent choice for SPI communication isolation. The ISO6421 has one forward and one backward channel and is used to isolate the /XFAULT signal. The ISO6441 can work up to 150Mbps, which is well above the SPI communication speed used in this design. The ISO6421 is also fast enough to support the slower speed signals /XFAULT and RST.

3.1.3 LM5009

The LM5009 is a wide-input, step down non-synchronous converter with integrated FET. This design has a 5V regulated output from the 24V field connector to supply the ISO6441, ISO6421, and the LED driver including LEDs.

3.1.4 TLC5927

The TLC5927 is designed for LED lighting applications with open-load, shorted-load, over-temperature detection, and constant-current control. The TLC5927 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC5927 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs.

4 System Design Theory

The ISO6441 isolates the host from the field side for the SPI signals. The ISO6441 is a very fast isolator, and data speeds up to 1Mbps can easily be supported. Therefore, a large number of outputs can controlled over this interface. At 1Mbps, it is theoretically possible to control up to 250 output signals at a refresh rate of 4kHz. This small form factor design demonstrates eight outputs and an additional 16 diagnostic LEDs, requiring in total 24 output signals. Given those requirements up to 64 outputs with the same control technique are feasible. The design is fully static and for diagnostic purposes the serial shift clock can go as low as DC.

4.1 Low-Side Driver Selection

To demonstrate the small form factor, this design uses two DRV81646 devices. These devices integrate four power outputs in a PWP package at 5 × 7mm board space and are capable of simultaneously driving 0.5A at each output with only PCB cooling. An area of about $15cm^2$ is sufficient for operation at ambient temperatures of 85°C. The DRV81646 devices provide internal diodes to a common clamping pin, which allows setting a clamping voltage different from the operating voltage for fast inductive discharge. The discharge then happens in an external Zener diode (D57 and D58). The power capability of the Zener diodes defines the quantity of inductive discharge the module can handle and can be set application specific. The TIDA-00236 uses a clamp of 48V and the Zener diodes can dissipate 3W each. Therefore, an inductive discharge of 750mJ can occur once each second for each output.

4.2 Thermal Management

The thermal management budget is calculated based on the following design considerations:

- The junction temperature remains below 150°C
- The thermal resistance of the package is 2.3 K/W junction to bottom plate
- The thermal vias have an inner diameter of 8 mil and capable of 170 K/W
- Board space provides thermal resistance to air of around 900 K/W per cm^2 (see formula 23 in *Reference 2*)

The $R_{DS(on)}$ of the DRV8804 is a maximum of 140mΩ and with four outputs turned on at 0.5A the total power dissipation is 0.28W per device (4 × 0.5 × 0.140). For an ambient temperature of 60°C, the junction temperature increases 8.5°C (from 0.28W × 30.6°C/W = 8.5°C). The TIDA-00236 has 15 thermal vias per device, which provides sufficient cooling for each FET. The TIDA-00236 has approximately 10 cm^2 available per DRV81646.

Use a four-layer board if an ambient temperature beyond 85°C is desired. DRV81646 can provide 2.0A per channel at 85°C in the PWP package with proper PCB layout and thermal vias.

4.3 Switch Off an Inductive Load

The TIDA-00236 can be used to switch off inductive loads like motors, valves, and so on. An inductive load stores energy. This energy releases when the switch wants to turn the inductive load off. The inductor tries to keep the current flowing, which can result in a high voltage spike at the output of the switch. Typical methods to prevent the occurrence of spikes are freewheeling diodes. These diodes limit the voltage at the inductor so that the voltage does not exceed the diode forward voltage of typical 0.7V. The resulting voltage at the output of the switch is 24.7V assuming a power supply of 24V. The method is simple but the method has the disadvantage that the current keeps flowing for some period of time. The time is reverse proportional to the freewheeling voltage. For high-speed actuators like injection valves in process control systems, this is not desired. The preferred method is to use a Zener diode so that the freewheeling voltage can be higher. In this reference design, the freewheeling voltage is clamped to 48V. At a 24V supply, this clamping results in a freewheeling voltage of 24V and a much faster decay of the inductor current. Therefore, this reference design is best suited for direct control of stepper motors or injection valves.

The DRV81646 has protected the low-side switches with one integrated clamping diode per each output. All clamping diodes are fed to one pin for an external Zener diode. This diode clamps the voltage to 65V.

The external Zener diodes (D57 and D58) in the TIDA-0023 is a 3W TVS diode with cooling calculated for 500mW, meaning all outputs of one DRV81646 can absorb 0.5J/s of energy. An inductive load of 100mH can store around 12.5mJ ($E = ½ \times L \times I^2$) at a current of 0.5A. The load can therefore switch at a rate of 40Hz for one output or 10Hz if all four outputs are loaded and switched. DRV81646 supports up to 500kHz switching frequency, so a larger Zener diode can be selected for higher frequencies.

4.4 Switching Light Bulbs

The TIDA-00236 can be used to switch conventional light bulbs. Such a load has a very low cold resistance, so the initial current can be as much as 10 times higher than the continuous current. A 24V, 5W light bulb has an in-rush current of 2A, which falls within the operating range of the DRV81646. Larger light bulbs trigger the overcurrent protection or the ILIM analog current limit feature in DRV81646. Such a light bulb does not harm the device, but the light bulb can fail to turn on as expected.

5 Getting Started Hardware

The TIDA-00236 can be used either as a plug-in card in the TIDA-00123 PLC evaluation platform or as a standalone card with any processor capable of handling SPI communication. For the connection to the TIDA-00123 platform, the connector J2 handles the communication.

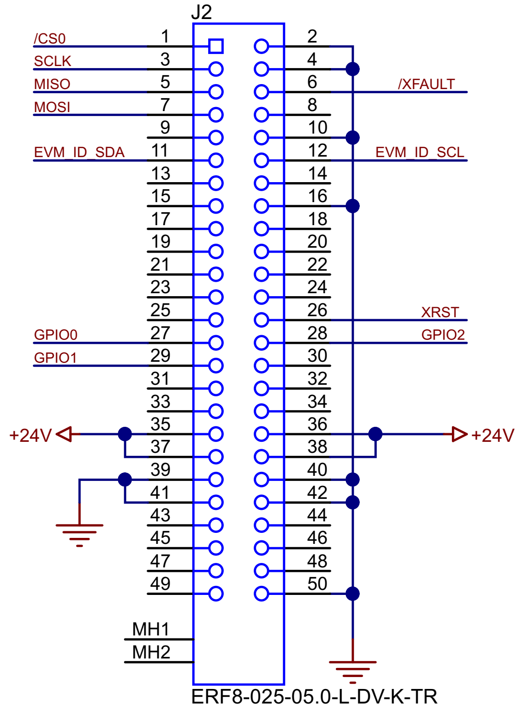


Figure 5-1. Connector J2 (Bottom Side)

The connector, J1, on the top side of the board, is a 14-pol connector that can connect the board to any processor platform with a standard flat cable.

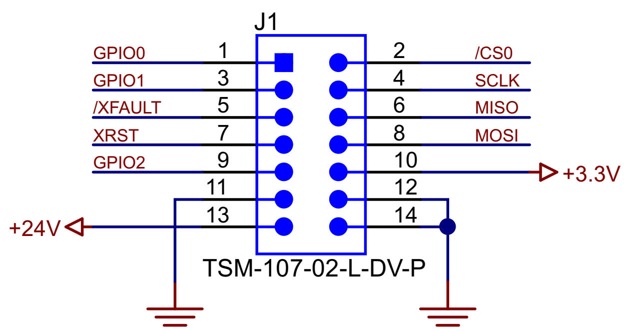


Figure 5-2. Connector J1 (Top Side)

The pins described in Table 5-1 have to be connected to the connector J1 of the TIDA-00236 to communicate with the card.

Table 5-1. Pin Description J1

J1	SIGNALS	DESCRIPTION
2	/CS0	Chip select / latch: rising edge to transfer data to outputs Y0 to Y7
4	SCLK	Serial clock
7	XRST	Reset: high to reset the outputs
8	MOSI	Master Out Slave In: Data to be sent to the digital output card
13	24V	5 to 24V host-side power
14	GND	Ground signal

5.1 Serial Peripheral Interface (SPI)

The implemented serial is a standard SPI with all four channels implemented. The processor connected to the board must act as SPI host and provide the clock on the SCLK pin.

Table 5-2. SPI Signal Connections

PIN	DESCRIPTION	POSITION ON J1	POSITION ON J2
SCLK	Serial Clock (output from host)	4	3
PICO	Controller Output, Peripheral Input	8	7
POCI	Controller Input, Peripheral Output	6	5
/CS0	Chip Select and Latch (active low, data transferred to outputs Y0 to Y7 with rising edge).	2	1

5.2 Fault Signal

The /XFAULT (pin 5 on J1 and pin 6 on J2) is a global fault signal for any of the eight outputs. The pin is driven low in the case of an overcurrent event in any of the DRV81646 channels. At the same time, the output with an overcurrent event is turned off. The output remains turned off for 15.5ms to 62ms depending on the COD pin resistor value before it retries to start and clear the fault signal. /XFAULT also is cleared if the 24V field supply is removed (J61 or J62).

If the overall die temperature in the DRV81646 exceeds safe limits, all output is switched off and the /XFAULT is driven low. Operation resumes when the temperature falls under the limit.

5.3 Power Supply

For the board to operate a 24V power supply needs to be supplied to the pin 35, 36, 37, or 38 on the connector J2 or pin 13 on connector J1. The ground needs to be connected according to Figure 5-1 or Figure 5-2 depending on which connector is in use. This power supplies the primary side of the ISO6441 and ISO6421 over the LM2936.

5.4 Output and Field Power Connector

In the connector J61 and J62, connect 24V and the ground to the labeled screw terminals. The eight loads can be connected between 24V and the eight outputs labeled as Y7 to Y0 on the connectors J61 and J62. Earth on J61 and J62 is connected to machine earth.

6 Getting Started Firmware

The TIDA-00236_demo_code.c is a SPI driver in c-code that, with small modifications, can be compiled on most MCU and MPU platforms. The most important sectors of the code are described in the following sections.

6.1 Data Bits

DB23:DB0 is sent to the digital output card through software controlled SPI. DB23:DB16 corresponds to output **Y7-Y0**. DB15:DB0 corresponds to the eight red LEDs (D49 to D56) and the eight orange LEDs (D41 to D48) interleaved as shown in Table 6-1.

Table 6-1. Data Bits (DB23:DB0) with Corresponding Function

Data Bits (DB23:DB0)																							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	R7	O7	R6	O6	R5	O5	R4	O4	R3	O3	R2	O2	R1	O1	R0	O0

The sequence for sending DB23:DB0 is as follows:

1. Assert XRST (pin 7 on J1 or pin 26 on J2) to reset the card and de-assert the pin.
2. Assert /CS0 (pin 2 on J1 or pin 1 on J2) to enable the card.
3. Set SCLK (pin 4 on J1 or pin 3 on J2) to LOW Put DB23:DB0 on MOSI (pin 8 on J1 or pin 7 on J2) starting with MSB (DB23) and make SCLK HIGH. Repeat this for DB23:DB0 in total 24 times to shift out all data bits.

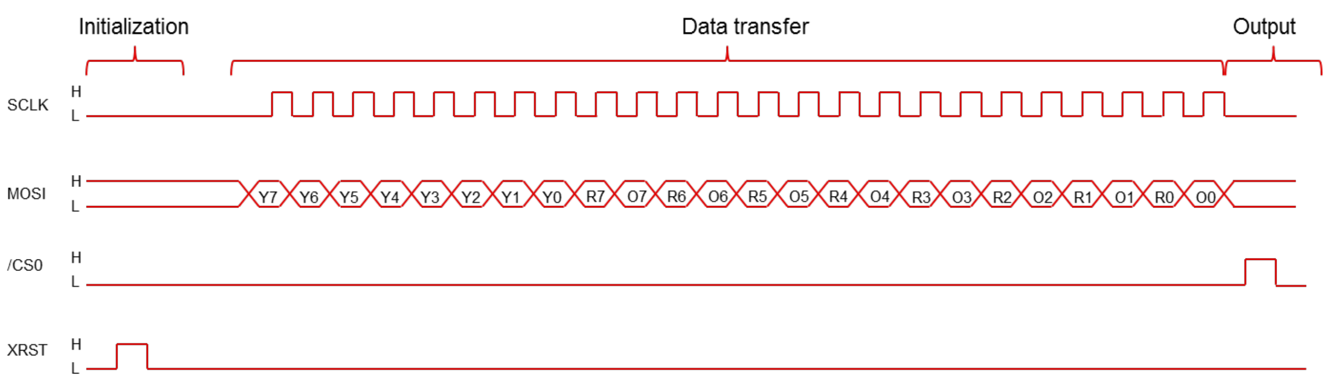


Figure 6-1. Data Bits Transfer Pattern

6.2 GPIO for SPI

The code assumes a port on address 0x100 (variable IOPort). For the SPI communication, the GPIOs are listed in Table 6-2.

Table 6-2. GPIOs used for SPI

SPI SIGNAL	SCLK	MOSI	MISO	/CS	XRST	/XFAULT
PORT PIN	0	1	2	3	4	5

If another port and pins are used the addresses in the variable *IOPort* and *Pin_Masks* should be changed accordingly. In the code, set the output (Y7 to Y0) one by one and check the /XFAULT pin. If /XFAULT is high, then switch on the red LEDs (D49 to D56).

The MOSI is not used in this code example. In other words, there is no SPI data transfer from the card to the controller side.

7 Test Setup

7.1 Output Current Capability

The GW inSTEK GPS-4303 quad-output DC power supplies are:

- Two 0 to 30V at up to 3A
- One 8 to 15V at 1A
- One 2.2 to 5.5V at 1A

All four outputs of one group (Y0 to Y3 or Y4 to Y7) are connected with individual 48Ω, 12W resistors to 24V of the power supply. GND and Earth are connected to 0V of the power supply. Then all outputs are programmed to turn on. The current from the power supply into the resistors should read 2A. The temperature of the driving switch is observed and settle around 50°C at a room temperature of 25°C. The drop voltage over the switch is around 250mV.

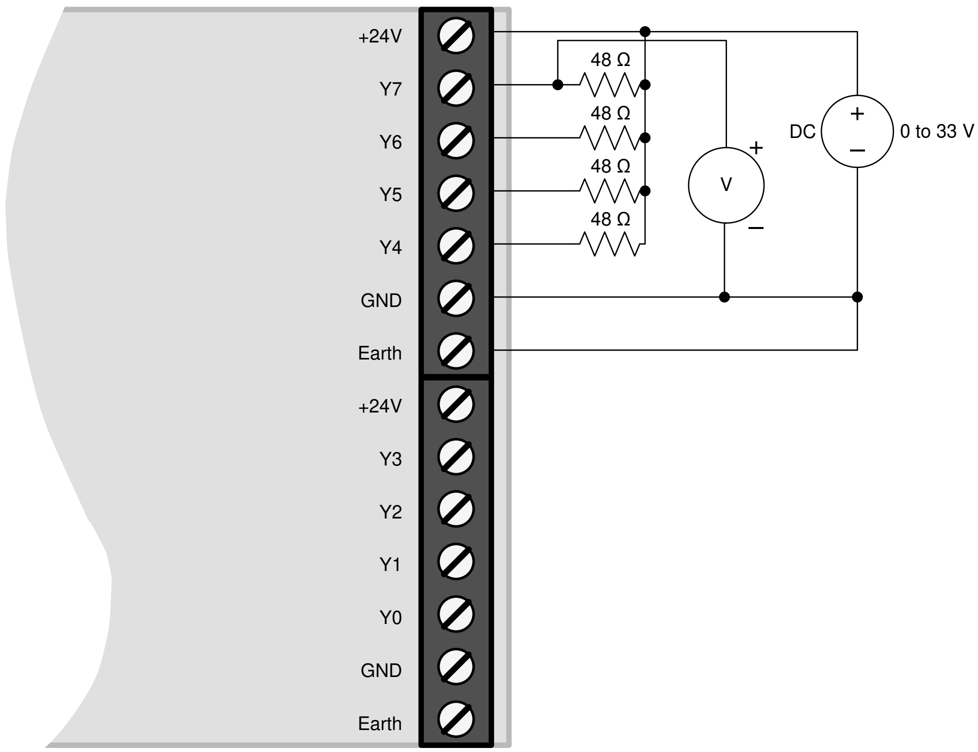


Figure 7-1. Measurement Setup for Overvoltage and Undervoltage Lockout

7.2 Rise and Fall Times, Propagation Delay

The GW inSTEK GPS-4303 quad-output DC power supplies are:

- Two 0 to 30V at up to 3A
- One 8 to 15V at 1A
- One 2.2 to 5.5V at 1A
- Oscilloscope: Tektronix TDS 3034

All four outputs of one group (Y4 to Y7) are connected with individual 48Ω, 12W resistors to 24V of the power supply. GND and Earth are connected to 0V of the power supply. Connect the oscilloscope to the latch input on the host side with channel one and to output Y7 with channel two. Set the oscilloscope to normal trigger rising edge with the trigger coming from channel one. The trigger level is 1V. Then all outputs are programmed to turn on. The oscilloscope captures a falling edge on Y7. Afterwards, all outputs are programmed to turn off, and the oscilloscope captures a rising edge on Y7. The measurement is repeated with the other three outputs of the same group. Then the resistors are connected to the second group of outputs (Y0 to Y3) and the measurement continues on these.

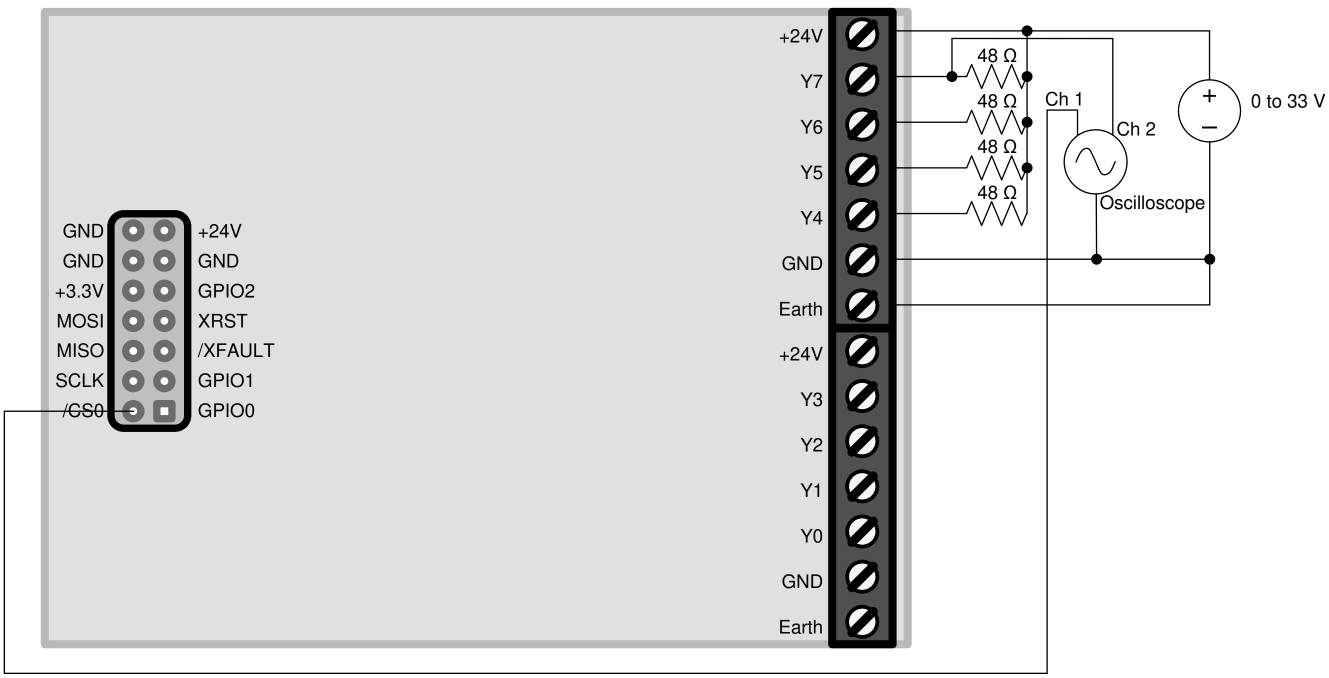


Figure 7-2. Measurement Setup for Rise and Fall Times and Propagation Delay

8 Test Data

Table 8-1. Test Results

SYMBOL	PARAMETER	CONDITIONS	SPECIFICATION			MEAS.	UNIT
			MIN	TYP	MAX		
V_{IN}	Input voltage	Normal operation	10	24	33	24.5	V
I_{IN}	Input current	Normal operation	-	15	50(1)	14	mA
V_{LOAD}	Load supply voltage	Normal operation	0	24	44	24.5	V
I_{LOAD}	Load current	Per channel T_A = 60°C	-	500	600	-(2)	mA
		Per channel T_A = 25°C	-	700	1000	-(2)	mA
P_{LOSS}	Power loss per channel	R_L = 48Ω, V_{LOAD} = 24V, T_A = 25°C	-	200	-	-(2)	mW
f_{SW}	Switching frequency	Resistive load		1000		1000	Hz
		Inductive load, 0.1H all channels		10		-(2)	Hz
t_{RISE}	Load voltage rise time 10% .. 90%	R_L = 48Ω, V_{LOAD} = 24V, T_A = 25°C	-	600	-	550	ns
t_{FALL}	Load voltage fall time 90% .. 10%	R_L = 48Ω, V_{LOAD} = 24V, T_A = 25°C	-	120	-	125	ns
t_{PD}	Propagation Delay (latch to output change)	R_L = 48Ω, V_{LOAD} = 24V, T_A = 25°C	60	150	200	165	ns
I_{PEAK}	Peak current (1ms)		2.3		3.8	-(2)	A
P_{IND}	Inductive power for each group of channels(3)				0.5	-(2)	J/s

(1) Depends on number of LEDs on and communication activity
(2) Based on calculations derived from DRV8804 datasheet. DRV81646 provides improved performance and lower temperatures.
(3) Outputs Y0 to Y3 are one group and outputs Y4 to Y7 are one group

In Figure 8-1 and Figure 8-2, channel 3 (purple) is connected to the /CS0 signal of the host connector and triggers on the rising edge. This edge causes the data to transfer to the outputs Y0 to Y7 and is therefore best suited to capture the output transitions (channel 4, green) and the timings for the propagation delay measurement. The fall time is dominated by the switching speed of the output transistor in the driver. Due to the open drain configuration, the rise time results from the RC combination formed by the 10nF capacitor connected to the switch output in the reference design, the driver output capacitance and the 48Ω load resistor at the output.

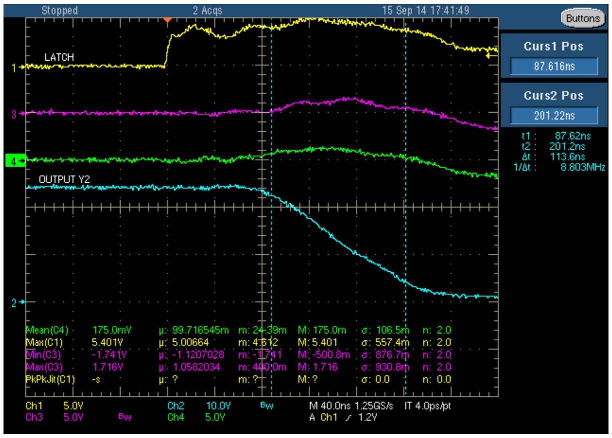


Figure 8-1. Fall Time

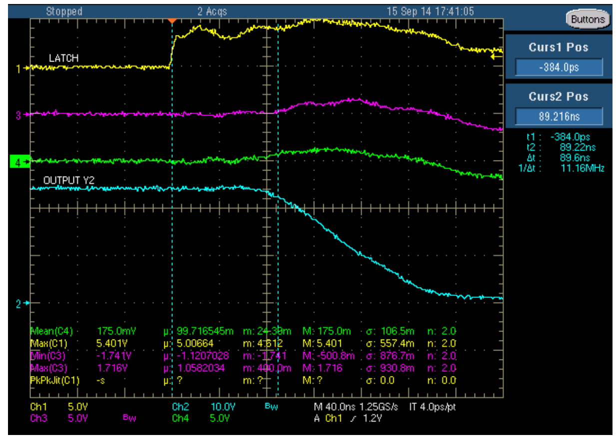


Figure 8-2. t_{PD} Falling Edge

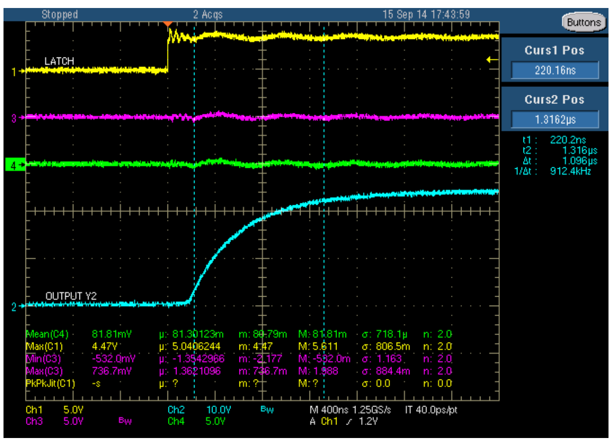


Figure 8-3. Rise Time

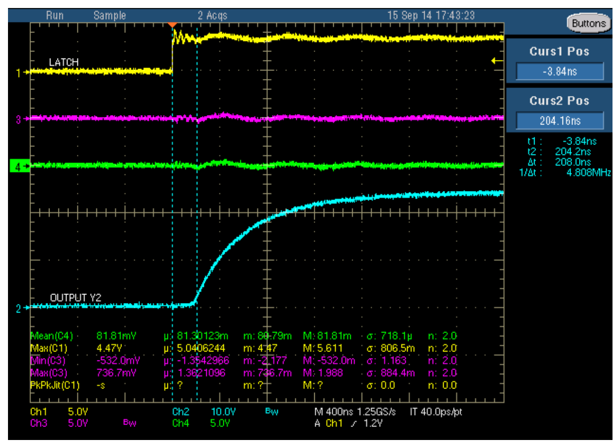


Figure 8-4. t_{PD} Rising Edge

9 Design Files

9.1 Schematics

To download the schematics, see the design files at TIDA-00236.

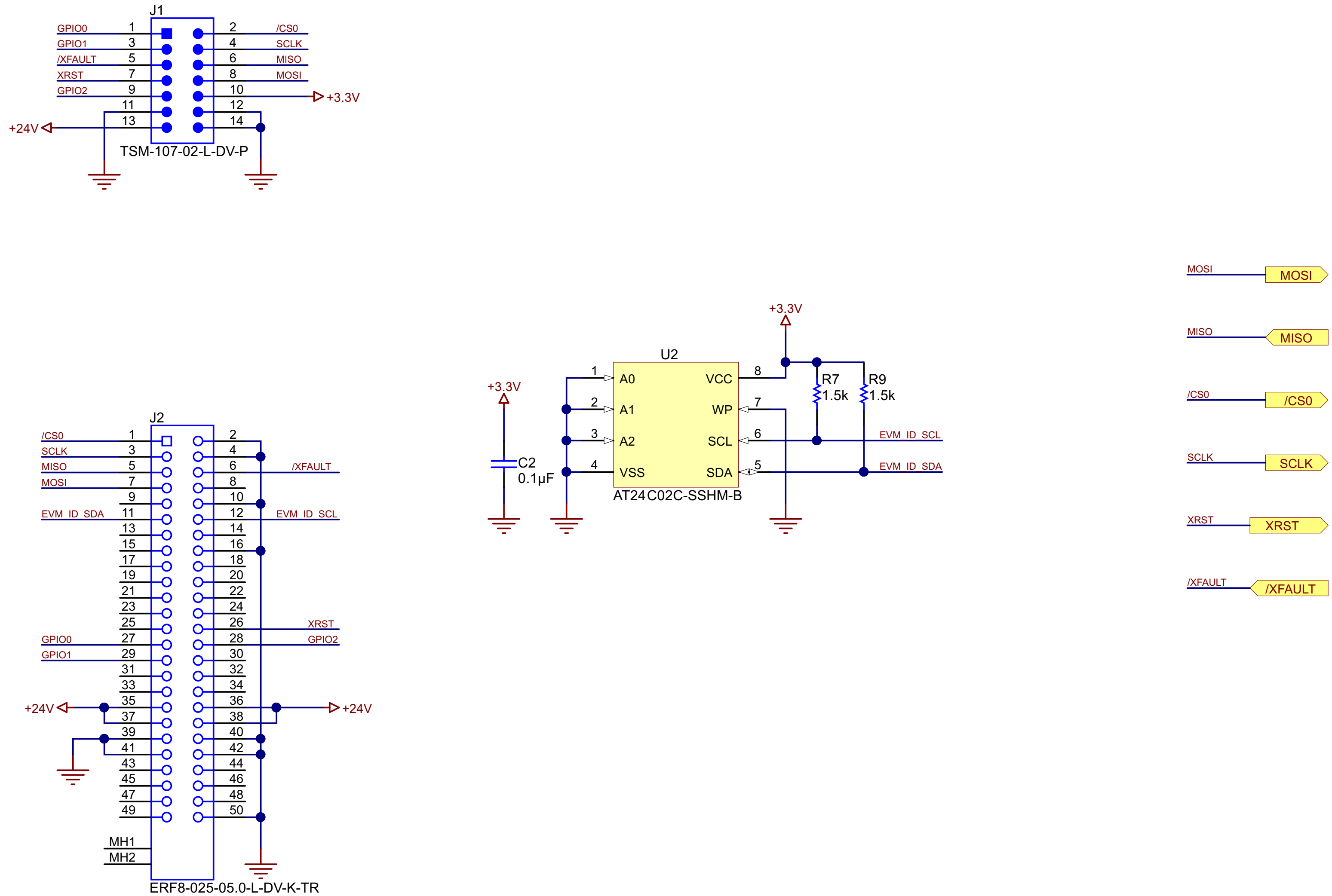


Figure 9-1. Connectors Schematic

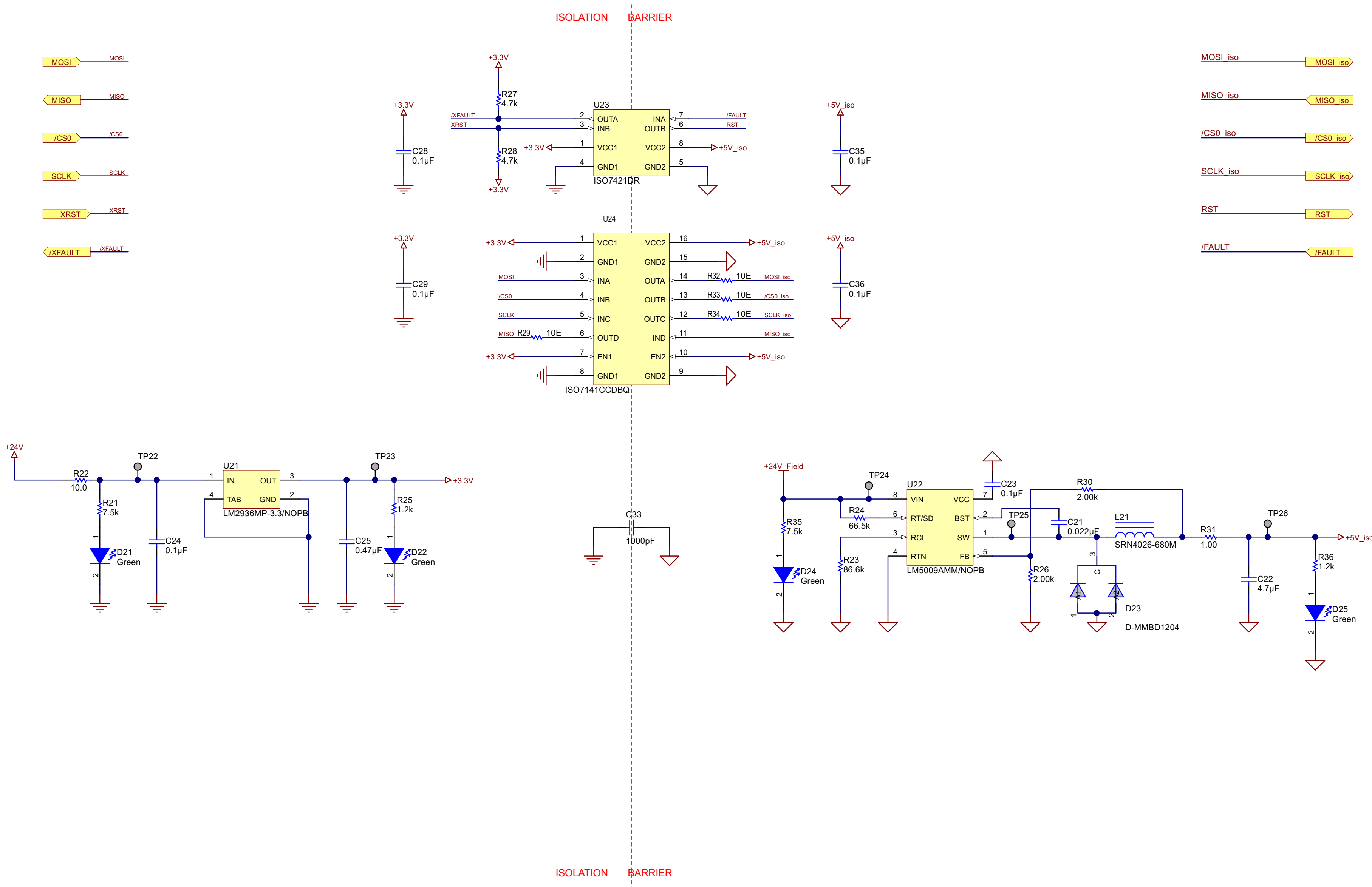


Figure 9-2. PSU Schematic

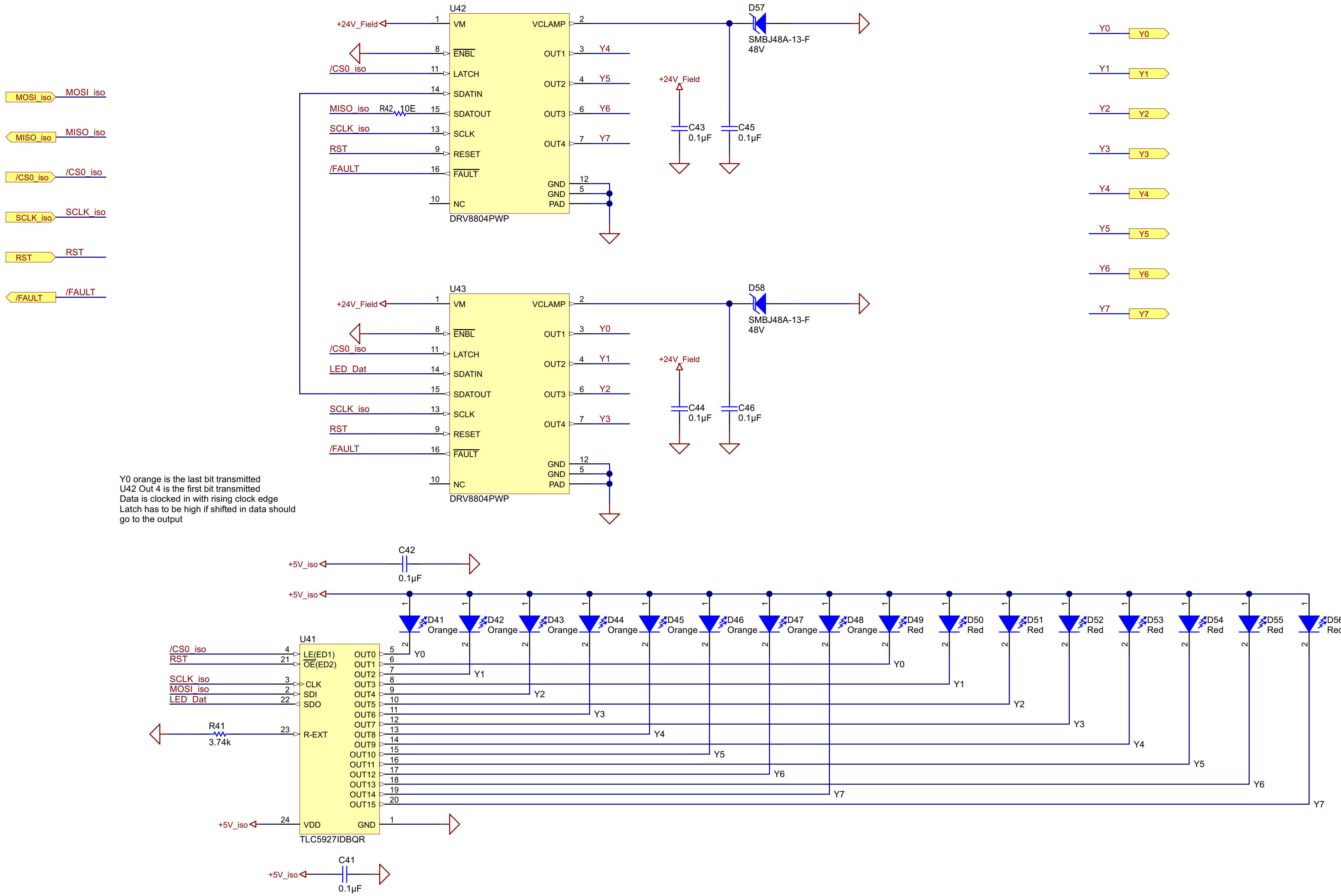


Figure 9-3. LED Drivers and Power Stages Schematic

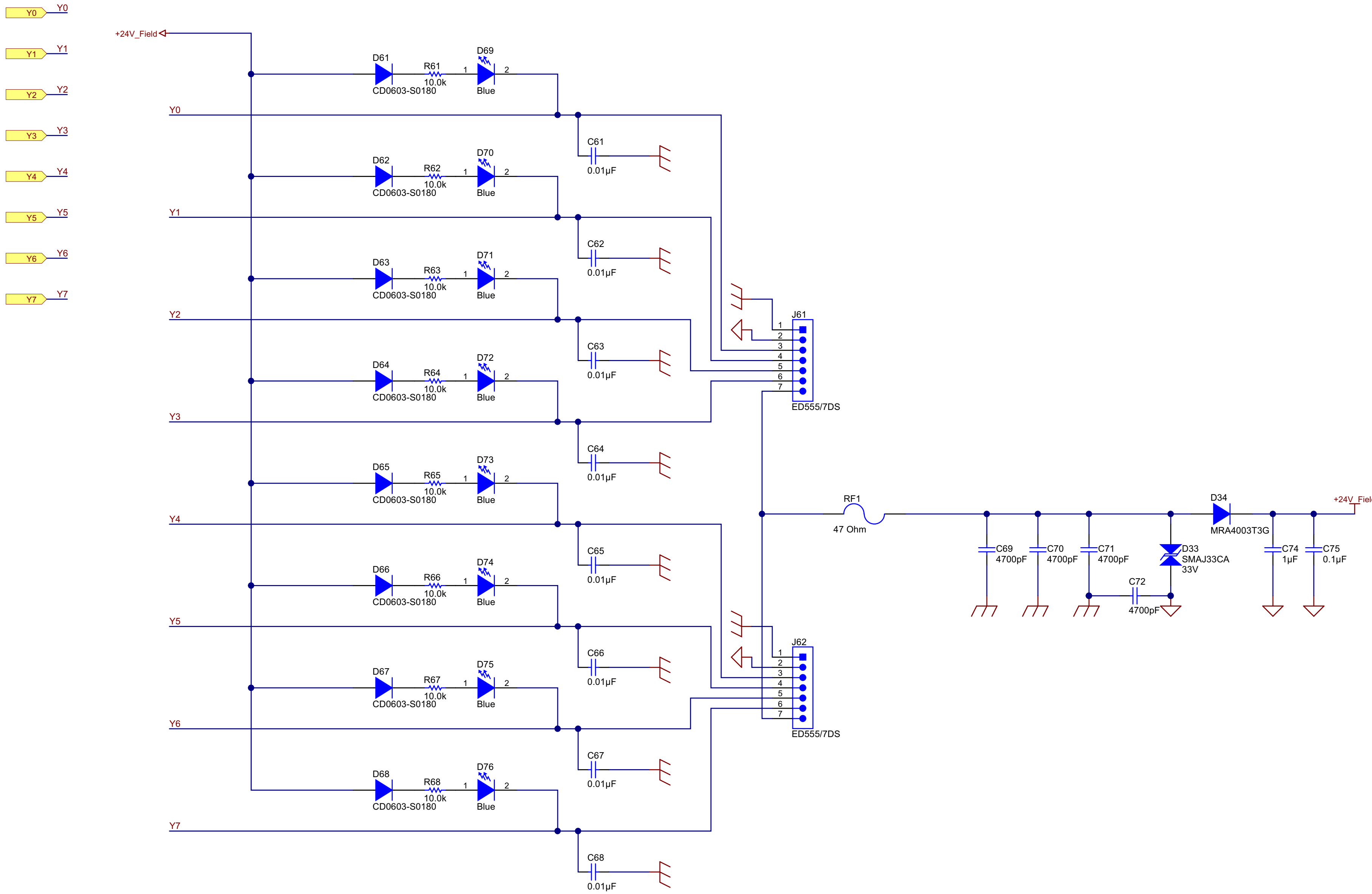


Figure 9-4. Output Connectors and Protection Schematic

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00236.

Table 9-1. BOM

ITEM	QTY	REFERENCE	VALUE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	1	!PCB1		Printed Circuit Board	Any	PCB		Printed Circuit Board
2	7	C2, C23, C28, C29, C35, C36, C41	0.1 µF	CAP, CERM, 0.1 µF, 25 V, ±10%, X5R, 0402	MuRata	GRM155R61E104KA87D	0402	GRM155R61E104KA87D
3	1	C21	0.022 µF	CAP, CERM, 0.022 µF, 50 V, ±10%, C0G/NP0, 0402	MuRata	GCM155R71H223KA55D	0402	GCM155R71H223KA55D
4	1	C22	4.7 µF	CAP, CERM, 4.7 µF, 16 V, ±10%, X7R, 0805	MuRata	GRM21BR71C475KA73L	0805_HV	GRM21BR71C475KA73L
5	1	C24	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	MuRata	GCM188R71H104KA57D	0603	GCM188R71H104KA57D
6	1	C25	0.47 µF	CAP, CERM, 0.47 µF, 6.3 V, ±10%, X5R, 0402	MuRata	GRM155R60J474KE19D	0402S	GRM155R60J474KE19D
7	1	C33	1000 pF	CAP, CERM, 1000 pF, 2 KV, 10% X7R 1206	Johanson Dielectrics Inc	202R18W102KV4E	1206	202R18W102KV4E
8	3	C42, C43, C44	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	AVX	06035C104KAT2A	0603	06035C104KAT2A
9	2	C45, C46	0.1 µF	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, 0805	Samsung	CL21B104KCFSFNE	0805_HV	CL21B104KCFSFNE
10	8	C61, C62, C63, C64, C65, C66, C67, C68	0.01 µF	CAP, CERM, 0.01 µF, 50 V, ±10%, X8R, 0603	TDK	C1608X8R1H103K	0603	C1608X8R1H103K
11	4	C69, C70, C71, C72	4700 pF	CAP, CERM, 4700 pF, 50 V, ±10%, X5R, 0603	MuRata	GRM188R61H472KA01D	0603	GRM188R61H472KA01D
12	1	C74	1 µF	CAP, CERM, 1 µF, 50 V, ±10%, X7R, 1206	TDK	C3216X7R1H105K	1206	C3216X7R1H105K
13	1	C75	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	Kemet	C0603C104K5RACTU	0603	C0603C104K5RACTU
14	4	D21, D22, D24, D25	Green	LED, Green, SMD	Lite-On	LTST-C190KGKT	LED_LTST-C190_G	LTST-C190KGKT
15	1	D23	MMBD1204	Diode, Small Signal, 100 V, 200 mA	Fairchild	D-MMBD1204	SOT-23	D-MMBD1204
16	1	D33	33 V	Diode, TVS, Bi, 33 V, 400 W, SMA	Littelfuse	SMAJ33CA	SMA	SMAJ33CA
17	1	D34	300 V	Diode, Standard Recovery Rectifier, 300 V, 1 A, SMA	ON Semiconductor	MRA4003T3G	SMA	MRA4003T3G
18	8	D41, D42, D43, D44, D45, D46, D47, D48	Orange	LED, Orange, SMD	Lite-On	LTST-C190KFKT	LED_LTST-C190	LTST-C190KFKT
19	8	D49, D50, D51, D52, D53, D54, D55, D56	Red	LED, Red, SMD	Lite-On	LTST-C190CKT	LED_LTST-C190_Red	LTST-C190CKT
20	2	D57, D58	48 V	Diode, TVS, Uni, 48 V, 600 W, SMB	Diodes Inc.	SMBJ48A-13-F	SMB	SMBJ48A-13-F
21	8	D61, D62, D63, D64, D65, D66, D67, D68	90 V	Diode, Switching, 90 V, 0.1 A, 0603 Diode	Bourns	CD0603-S0180	Diode_0603	CD0603-S0180
22	8	D69, D70, D71, D72, D73, D74, D75, D76	Blue	LED, Blue, SMD	OSRAM	LB Q39G-L2N2-35-1	LB Q39G_BLUE	LB Q39G-L2N2-35-1
23	1	J1		Header, 100mil, 7×2, Vertical, Gold, SMT	Samtec	TSM-107-02-L-DV-P	SAMTEC_TSM-107-02-L-DV-P	TSM-107-02-L-DV-P
24	1	J2		Receptacle, 0.8 mm, 25×2, SMT	Samtec	ERF8-025-05.0-L-DV-K-TR	CONN_ERF8-025-05_0-L-DV-L-TR	ERF8-025-05.0-L-DV-K-TR
25	2	J61, J62		Terminal Block, 6 A, 3.5-mm Pitch, 7-Pos, TH	On-Shore Technology	ED555/7DS	On-Shore_ED555-7DS	ED555/7DS
26	1	L21	68 µH	Inductor, Wirewound, Ferrite, 68 µH, 0.35 A, 0.852 Ω, SMD	Bourns	SRN4026-680M	SRN4026	SRN4026-680M
27	1	LBL1		Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	Brady	THT-14-423-10	Label_650x200	Size: 0.65" × 0.20 "
28	2	R7, R9	1.5 k	RES, 1.5 kΩ, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K50JNED	0402	CRCW04021K50JNED
29	2	R21, R35	7.5 k	RES, 7.5 kΩ, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04027K50JNED	0402S	CRCW04027K50JNED
30	1	R22	10.0	RES, 10.0 Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310R0FKEA	0603	CRCW060310R0FKEA
31	1	R23	86.6 k	RES, 86.6 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060386K6FKEA	0603	CRCW060386K6FKEA

Table 9-1. BOM (continued)

ITEM	QTY	REFERENCE	VALUE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
32	1	R24	66.5 k	RES, 66.5 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060366K5FKEA	0603	CRCW060366K5FKEA
33	2	R25, R36	1.2 k	RES, 1.2 kΩ, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K20JNED	0402S	CRCW04021K20JNED
34	2	R26, R30	2.00 k	RES, 2.00 kΩ, 1%, 0.063 W, 0402	Vishay-Dale	CRCW04022K00FKED	0402	CRCW04022K00FKED
35	2	R27, R28	4.7 k	RES, 4.7 kΩ, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04024K70JNED	0402S	CRCW04024K70JNED
36	5	R29, R32, R33, R34, R42	10 E	RES, 10 Ω, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040210R0JNED	0402S	CRCW040210R0JNED
37	1	R31	1.00	RES, 1.00 Ω, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08051R00FKEA	0805_HV	CRCW08051R00FKEA
38	1	R41	3.74 k	RES, 3.74 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06033K74FKEA	0603	CRCW06033K74FKEA
39	8	R61, R62, R63, R64, R65, R66, R67, R68	10.0 k	RES, 10.0 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA	0603	CRCW060310K0FKEA
40	1	RF1	47	RES, 47 Ω, 10%, 2 W, Fusible, TH	TT Electronics/IRC	EMC2-47RKI	EMC2	47 Ohm
41	1	U2		IC, EEPROM, 2KB, 1 MHZ, SOIC-8	Atmel	AT24C02C-SSHM-B	SOIC-8M	AT24C02C-SSHM-B
42	1	U21		Ultra-Low Quiescent Current LDO Voltage Regulator, 4-pin SOT-223, Pb-Free	National Semiconductor	LM2936MP-3.3/NOPB	MP04A_N	LM2936MP-3.3/NOPB
43	1	U22		100-V, 150-mA Constant On-Time Buck Switching Regulator, 8-pin MSOP, Pb-Free	Texas Instruments	LM5009AMM/NOPB	MUA08A_N	LM5009AMM/NOPB
44	1	U23		150 Mbps Dual Channels, 1 / 1, Digital Isolator, 2.25 V / 5 V, –40°C to 125°C, 8-pin SOIC (D), Green (RoHS and no Sb/Br)	Texas Instruments	ISO6421DR	D0008A_N	ISO6421DR
45	1	U24		10400-VPK Small-Footprint and Low-Power Quad Channels Digital Isolators, DBQ0016A	Texas Instruments	ISO6441DBQR	DBQ0016A_N	ISO6441DBQR
46	1	U41		16-Bit Constant-Current LED Sink Driver, 3 to 5.5 V, –40°C to 85°C, 24-pin SOP (DBQ24), Green (RoHS and no Sb/Br)	Texas Instruments	TLC5927IDBQR	DBQ0024A_N	TLC5927IDBQR
47	2	U42, U43		Quad Serial Interface Low-Side Driver IC, PWP0016D	Texas Instruments	DRV8804PWPR	PWP0016D_N	DRV8804PWPR
48	2	U42, U43 alternate		Four-Channel Low-side Driver with Hardware, SPI, and Configurable Slew Rate and Cut-off Duration, PWP-20	Texas Instruments	DRV81646PWPR	PWP0020AC	DRV81646PWPR

9.3 PCB Layout

9.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00236.

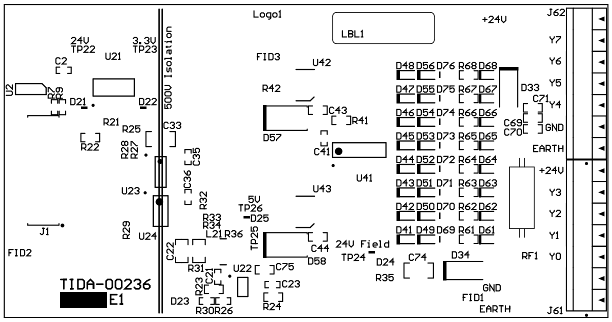


Figure 9-5. Top Silkscreen

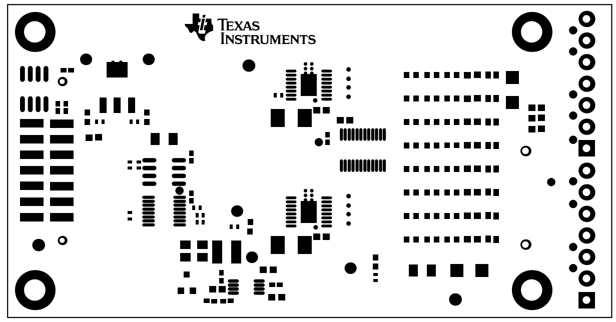


Figure 9-6. Top Solder Mask

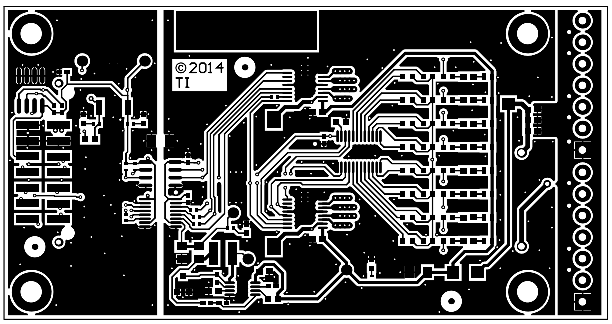


Figure 9-7. Top Layer

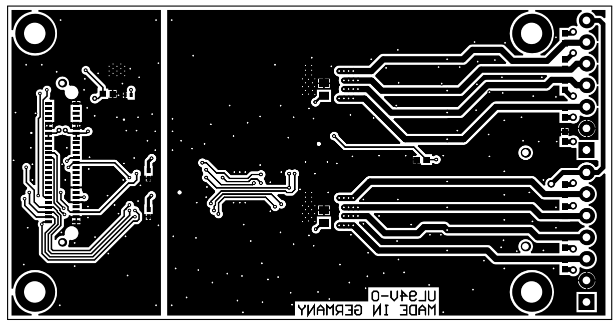


Figure 9-8. Bottom Layer

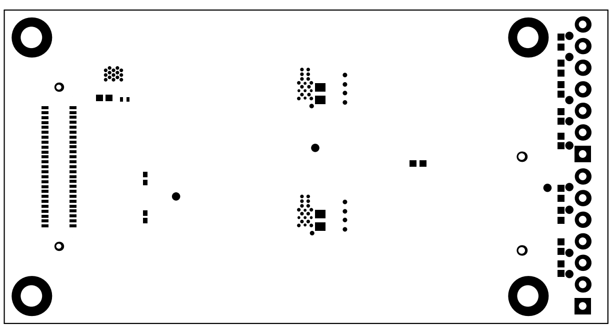


Figure 9-9. Bottom Solder Mask

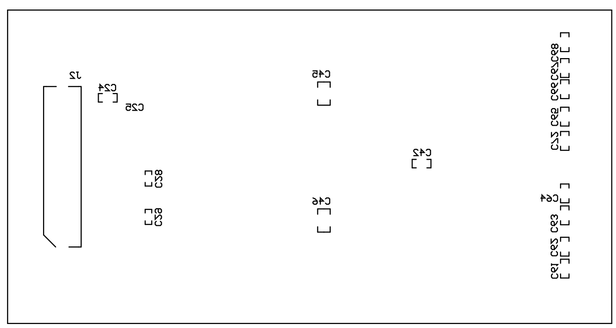
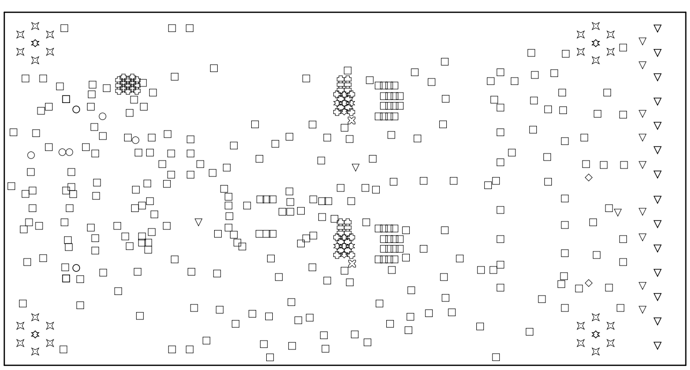


Figure 9-10. Bottom Silkscreen



Symbol	Hit Count	Tool Size	Plated	Hole Type
☼	10	7.874mil (0.2mm)	PTH	Round
○	43	8mil (0.203mm)	PTH	Round
⊠	2	10mil (0.254mm)	PTH	Round
□	274	12mil (0.305mm)	PTH	Round
○	5	16mil (0.406mm)	PTH	Round
⌘	24	19.685mil (0.5mm)	PTH	Round
▽	12	28mil (0.711mm)	PTH	Round
□	2	33mil (0.838mm)	PTH	Round
◇	2	43.307mil (1.1mm)	PTH	Round
▽	14	50mil (1.27mm)	PTH	Round
○	2	57.087mil (1.45mm)	NPTH	Round
☼	4	137.795mil (3.5mm)	PTH	Round
	394 Total			

Figure 9-11. Drill Drawing

Figure 9-12. Mechanical Dimensions

9.3.2 Layout Recommendations

The ISO6441 and ISO6421 are designed for high-speed operation. To minimize reflections and possible bit errors series resistors are added to all data and clock outputs. The corresponding areas are circled yellow in Figure 9-13.

Effective cooling of the DRV81646 requires thermal vias under the devices, circled green. On the bottom side as seen in Figure 9-14, a large contiguous copper area serves as heat sink. Users must prevent traces from unintentionally blocking heat flow. For more layout guidelines and best practices see the *Best Practices for Board Layout of Motor Drivers* application note.

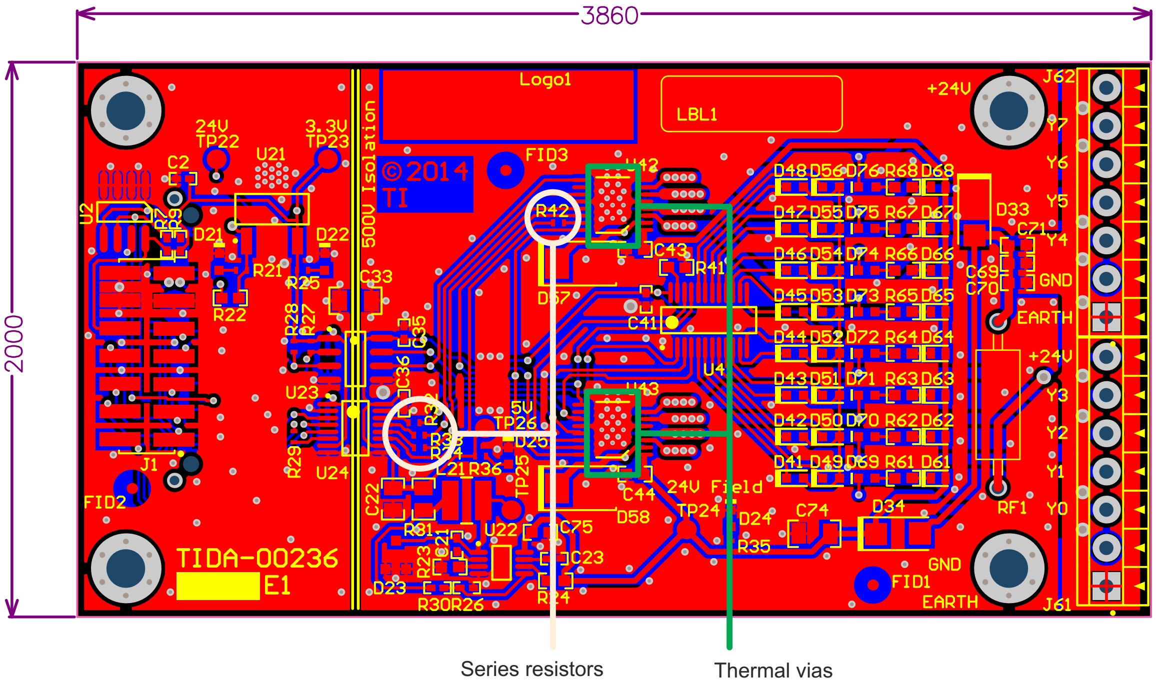


Figure 9-13. Layout Guidelines 1

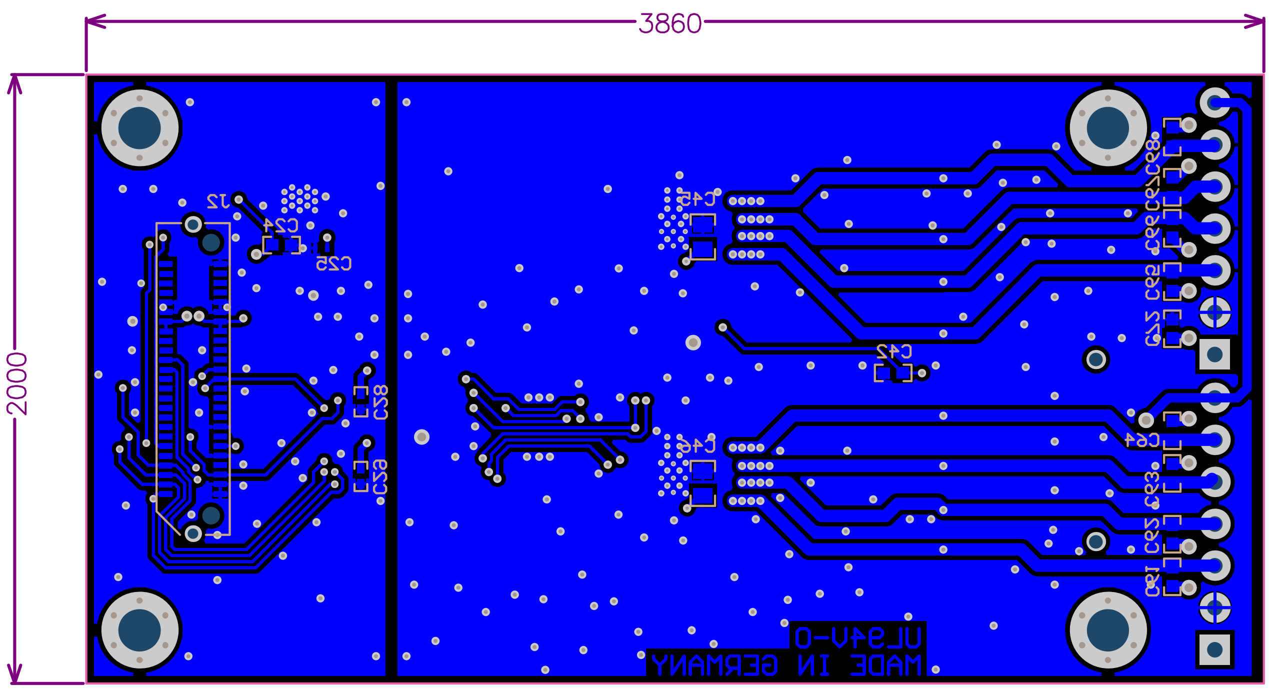


Figure 9-14. Bottom Layers

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00236.

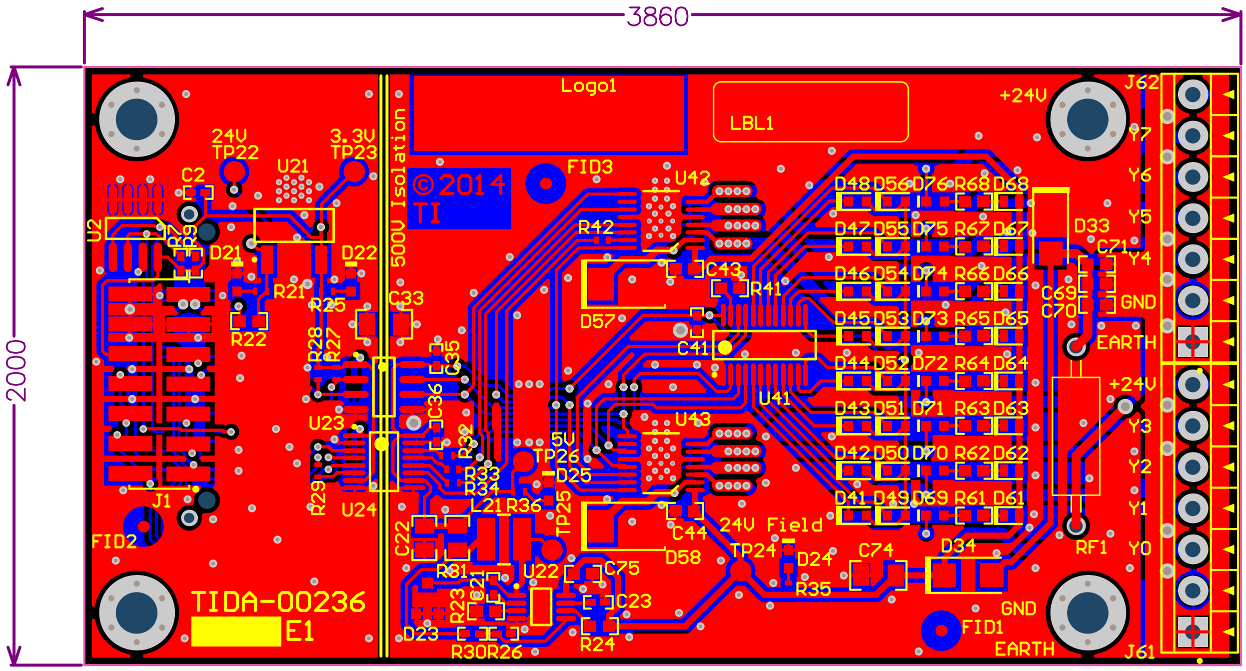


Figure 9-15. All Layers

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00236.

9.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00236.

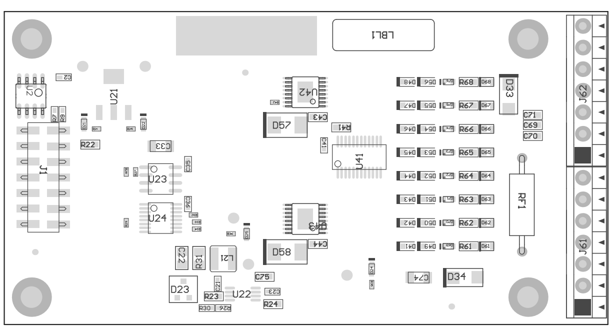


Figure 9-16. Top Side Assembly Drawing

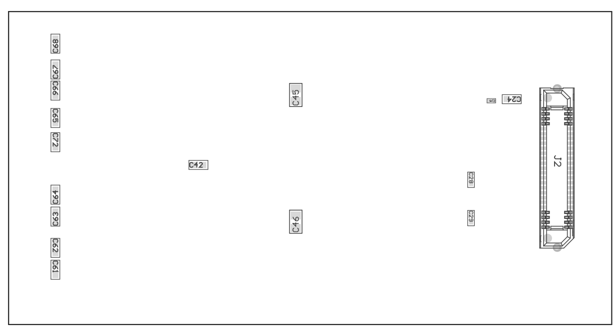


Figure 9-17. Bottom Side Assembly Drawing

9.7 Software Files

To download the software files, see the design files at TIDA-00236.

10 References

1. Texas Instruments, *PLC I/O Module Front-End Controller Using a Tiva C Series ARM Cortex-M4 MCU* Design Guide
2. Texas Instruments, *Thermal Considerations for Surface Mount Layouts* Seminar

11 About the Author

INGOLF FRANK is a systems engineer in the Texas Instruments Factory Automation and Control team, focusing on PLC I/O modules. Ingolf works across multiple product families and technologies to leverage the best designs possible for system level application design. Ingolf earned his electrical engineering degree [Dipl. Ing. (FH)] in the field of information technology at the University of Applied Sciences Bielefeld, Germany in 1991.

ANUPAM MAJJAGI is doing his master thesis at Texas Instruments in the Factory Automation and Control team. A part of his thesis involves writing test programs and firmware to test TIDA-00236 and communicate with the design. He is pursuing his master degree in embedded and microelectronics at Hochschule Darmstadt, Germany.

HENRIK MANNESSON is a system engineer at Texas Instruments Germany in the Factory Automation and Control team. Henrik earned his master of science in electrical engineering (MSEE) from Lunds University of Technology (LTH), Lund, Sweden.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2014) to Revision A (January 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed device support throughout the document from ISO7141 and ISO7421 to ISO6441 and ISO6421. Additionally, changed DRV8804 to DRV81646	1