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# Temperature Transmitter on Single Chip Mixed-Signal MCU

**TEXAS INSTRUMENTS**

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|---|---|
| TIDA-00247 | Tool Folder Containing Design Files |
| MSP430F2274 | Product Folder |
| TPS7A1601 | Product Folder |

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## Design Features

- Analog Functionality Fully Integrated Into Microcontroller (MCU)
- Sensor Input Only Compatible With Two-Wire PT100 Resistance Temperature Detector (RTD) Probes
- Temperature Range for RTD –200°C to 850°C
- Input Power Supply Range: 10- to 33-V DC
- 4- to 20-mA Current Loop Output Signal
- Maximum Measured Error: Better than ±2.5ºC
- Implements Ratiometric Measurement
- Design to Meet IEC 61000-4 Requirement
- Operating Temperature Range –40°C to 85°C

## Featured Applications

- Factory Automation and Process Control
- Sensors and Field Transmitters
- Building Automation
- Portable Instruments
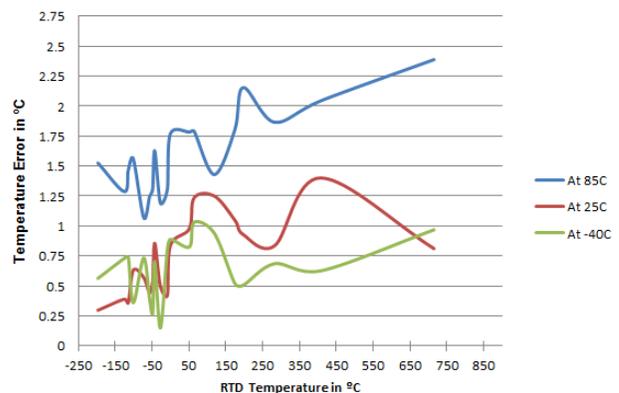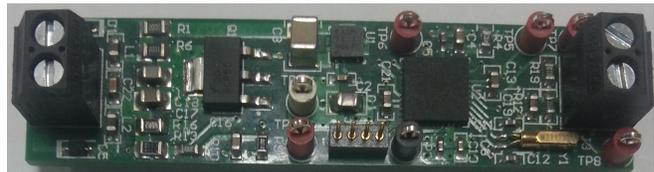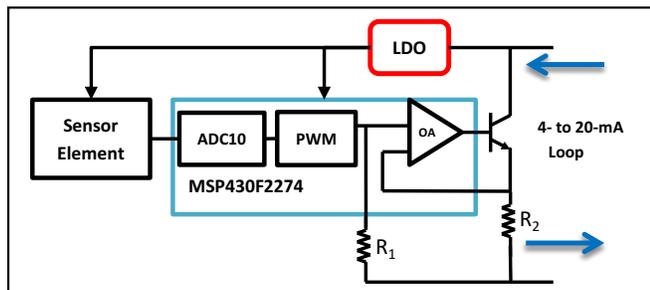






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# 1 Key System Specifications

This reference design targets the specifications and features given in Table 1.

**Table 1. Key System Specifications**

| PARAMETERS | SPECIFICATIONS AND FEATURES |
|---|---|
| Sensor type | 2-wire PT100 RTD probe only |
| Temperature range | –200°C to +850°C |
| Output signal | 2-wire, 4- to 20-mA current loop |
| Measurement type | Ratiometric |
| Power supply voltage range on loop interface terminals | 10- to 33-V DC |
| Supply current consumption | Less than 1.8 mA at 1 MHz CPU clock |
| Reverse polarity protection | Diode bridge that works with either polarity |
| Output current resolution | Approximately 2.8 µA |
| Power supply influence on output | Approximately 5.7 µA |
| System accuracy or maximum measured error (excluding sensor errors) | Better than ±2.5°C (–200°C to 850°C temperature range) |
| Calibration | Offset and gain calibration for analog-to-digital converter (ADC) and digital-to-analog converter (DAC) |
| RTD temperature linearization | –200°C to 850°C look-up table with 1°C resolution implemented in the MSP430™ firmware to resolve non-linearity of RTD |
| Surge transient immunity | IEC 61000-4-5: ±1 kV line-to-line differential mode (DM) |
| Operating temperature | –40°C to 85°C |
| Form factor (L X W) | 13.97 mm × 57.15 mm |

## 2 System Description

The system power consumption must be considered carefully for portable 2-wire, 4- to 20-mA current loop applications. The conventional approach of using a high bridge excitation voltage and an operational amplifier to achieve a full-scale ADC input voltage increases the chip count and overall power consumption. An additional external voltage regulator is also required to excite the bridge sensor and supply the microcontroller from the same voltage source. The goal for this reference design is to maintain low power consumption and low cost solutions. As the block diagram shows in Figure 1, this design utilizes the integrated ADC and operational amplifiers (OAs) of a microcontroller. To cut down on costs, the ADC and DAC use the main supply voltage as the reference voltage instead of including an external reference or selecting a more expensive ADC or DAC that features an internal reference. Leveraging the integrated peripherals of a MCU enables a low component count and lower cost for the user. This reference design is based on a mixed signal microcontroller, specifically the MSP430F2274™.

Figure 1 shows how the integrated peripherals of the MSP430F2274 have been utilized. The first integrated operational amplifier (OA0) and the integrated 10-bit successive approximation register (SAR) ADC (ADC10) are utilized as the analog front end (AFE) for the system. The second integrated operational amplifier (OA1) and the pulse-width modulation (PWM) timer are used to implement the DAC. One of the general-purpose input/outputs (GPIOs) implement the ground on/off switch for the bridge circuit for saving power.

The sensor transmitter has two external 2-pin input terminals, one for connecting the 2-wire PT100 RTD sensor and another for connecting the loop interface. The transmitter communicates back to its host, typically a PLC analog input module, by precisely controlling the magnitude of the return current. To conform to the 4- to 20-mA communication standards, the complete transmitter must consume less than 3.3 mA of current.
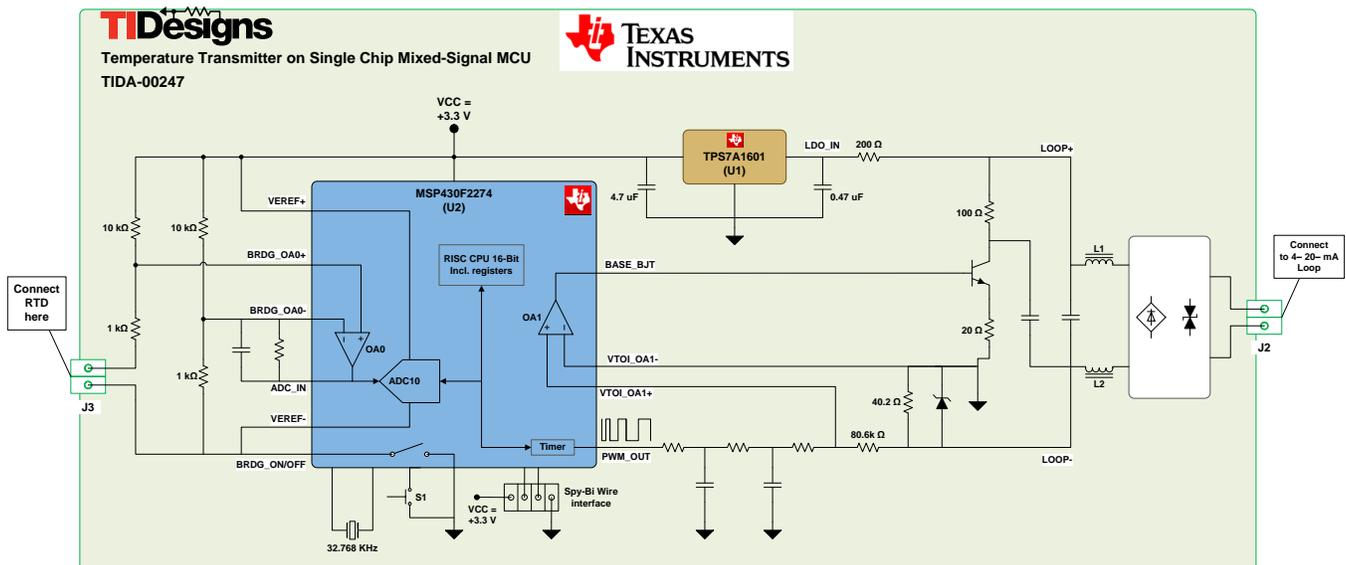


**Figure 1. System Block Diagram**

## 2.1 Analog Front End (AFE)

Platinum RTDs are mostly for use with Wheatstone bridge circuits for temperature measurement. The bridge contains the RTD at one arm and the other remaining three arms are connected with known standard resistors that ideally have a zero temperature coefficient. A bridge is generally a resistance measuring device, which converts the resistance of the RTD into an electrical signal. The bridge output voltage is an indirect indication of the RTD resistance. Determine the resistance of the RTD (fourth resistor) using the voltage differential and the three known standard resistors. To avoid subjecting the three bridge-completion resistors to the same temperature as that of the RTD, separate the RTD from the bridge with a pair of extension wires.

In Figure 2, an operational amplifier (OA0) is used in a negative feedback configuration that ensures that the potentials of the non-inverting ($V_A$) and inverting ($V_B$) input terminals are equal. In this configuration, $V_A$ can be given as:

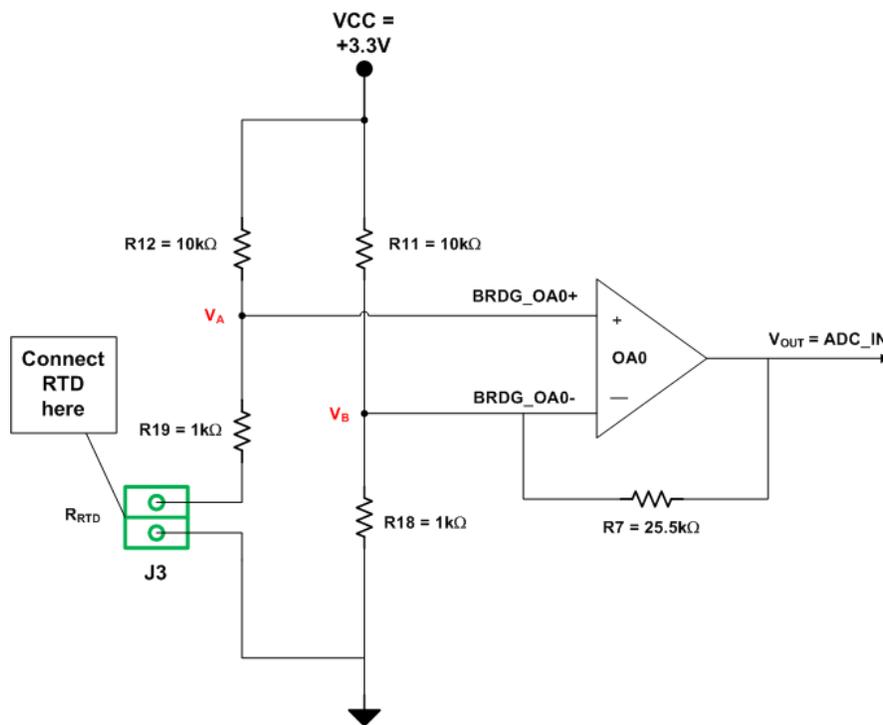$$V_A = \left[ \frac{R_{RTD} + R19}{R_{RTD} + R19 + R12} \right] \times V_{CC} = V_B$$

(1)



**Figure 2. Wheatstone Bridge Circuit**

Applying Kirchhoff's Current Law (KCL) at node B:

$$\frac{V_{CC} - V_B}{R11} + \frac{V_{OUT} - V_B}{R7} = \frac{V_B}{R18}$$

(2)

Now, substitute the value of $V_B$ from the previous Equation 1 and solve for $V_{OUT}$,

$$V_{OUT} = \left[ \left\{ \left( \frac{1}{R7} + \frac{1}{R11} + \frac{1}{R18} \right) \times \left( \frac{R_{RTD} + R19}{R_{RTD} + R19 + R12} \right) \right\} - \frac{1}{R11} \right] \times R7 \times V_{CC} = ADC\_IN$$

(3)

After the signal conditioning, the output signal ($V_{OUT}$) is provided to the integrated ADC10 of the MSP430 for further processing. The ADC10 converts $V_{OUT}$ to a 10-bit digital representation and stores the result in the ADC10MEM register. The ADC core uses voltage levels selectable by software ($V^{R+}$ and $V_{R-}$) to define the upper and lower limits of the conversion. The digital output (NADC) is full scale (03FFh) when the input signal is equal to or higher than $V_{R+}$, and zero when the input signal is equal to or lower than $V_{R-}$. In the software, $V_{CC}$ and GND are selected as $V_{R+}$ and $V_{R-}$, respectively. Selecting $V_{CC}$ as the ADC reference implements the ratiometric measurement because the bridge circuit is also excited by $V_{CC}$. The conversion formula for the ADC is given as:

$$N_{ADC} = 1023 \times \left[ \frac{ADC\_IN}{V_{REF}} \right]$$

(4)

$$N_{ADC} = 1023 \times \left[ \left\{ \left( \frac{1}{R7} + \frac{1}{R11} + \frac{1}{R18} \right) \times \left( \frac{R_{RTD} + R19}{R_{RTD} + R19 + R12} \right) \right\} - \frac{1}{R11} \right] \times R7$$

(5)

In order to get the higher accuracy from the RTD, consider the following guidelines:

- Use resistors with better tolerance. There will be less variability in the manufacturing of 0.1% resistors when compared to 1% resistors.
- Measure the known resistors with an ohmmeter. By obtaining the most accurate measurements for the known resistances, the formula results in a more accurate measurement of the RTD.
- Use a moving average when obtaining the bridge value to reduce the amount of noise in the measured signal.
- Turn off the power to the Wheatstone bridge to reduce self-heating of the RTD.

## 2.2   *PWM Digital-to-Analog Converter (DAC)*

This section describes the software and hardware implementation of a pulse-width modulation (PWM) DAC. The use of a PWM DAC is by far the most common and most popular technique to implement DAC functionality in MCUs that do not have an integrated DAC module. The PWM DAC mainly consists of two blocks:

1. A timer to generate a PWM waveform of a given period and specified duty cycle
2. A low-pass filter that converts the PWM waveform to an analog output voltage

The PWM function paired with an RC low-pass filter can be used as a simple, low-cost DAC. A PWM DAC is simple to build, easy to use, and requires very few parts (only one or two pins). Later, this voltage output is converted to current in the loop using a voltage-to-current (V to I) converter circuit. This design uses the timer B module of the MSP430F2274 to produce a PWM wave, which is output on a general-purpose port pin of the MCU. Figure 3 shows the block diagram of a voltage output PWM DAC.
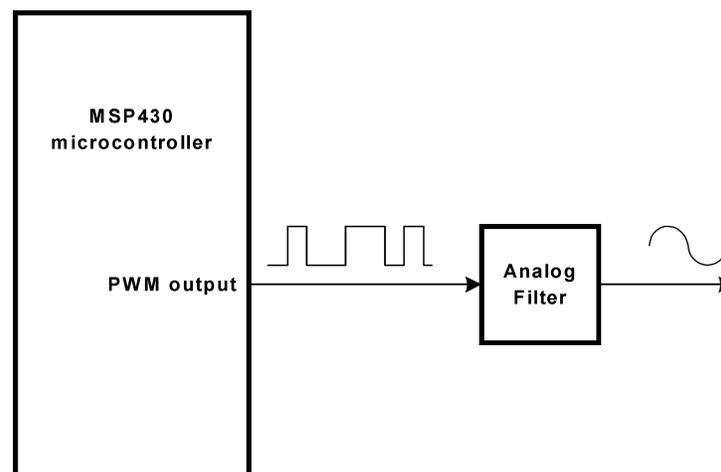


**Figure 3. PWM DAC Block Diagram**

### 2.2.1  Generating a PWM Signal

Pulse-Width Modulation (PWM) is a form of signal modulation where a high-frequency carrier is modulated by varying the width of a pulse or changing the duty cycle of a periodic waveform. A PWM signal consists of two main components that define its behavior: a duty cycle and a frequency. The duty cycle describes the amount of time the signal is in a high (ON) state as a percentage of the total time the PWM signal takes to complete one cycle. By adjusting the duty cycle of a PWM waveform, the average DC output voltage becomes easily controllable.

$$\text{Duty cycle} = \frac{T_{ON}}{T_{PWM\_PERIOD}}$$
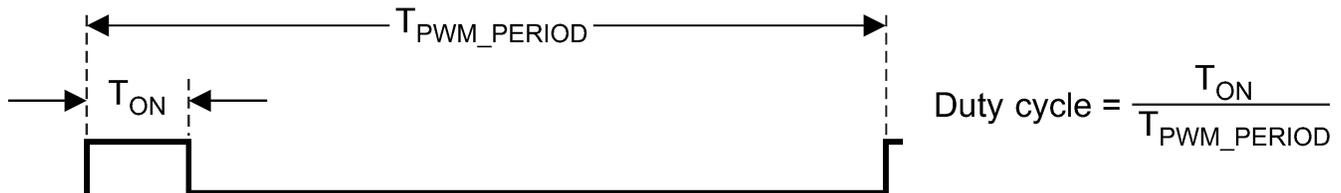
**Figure 4. PWM Signal**

In this design, the timer B module is used to toggle a general-purpose port pin to create the PWM waveform (Figure 5). The basic structure is simple and revolves around the timer B counter register, (designated as TBR). The system or CPU clock continuously increments the TBR, either directly or through a 1/2/4/8 clock divider. The timer can be used in one of three operation modes:

- Continuous mode: In continuous mode, the value of the timer counts up to its maximum value (defined by the register size of the module) before being reset by the hardware.
- Up mode: In up mode, the timer counts up to a defined value stored in the main module capture and compares the "TBCCR0" register before being reset by the hardware. If this register is set to 0, the module counts up to the maximum value by default.
- Up-down mode: In up-down mode, the timer counts up to the defined value stored in the "TBCCR0" register and then counts back down to 0.

Intermediate switching values (which define the duty cycle) of a PWM are placed into the individual timer output capture and compare registers (TBCCRx). This value (paired with the correct output modulation mode), controls the output, which is routed to the external general purpose port pin.
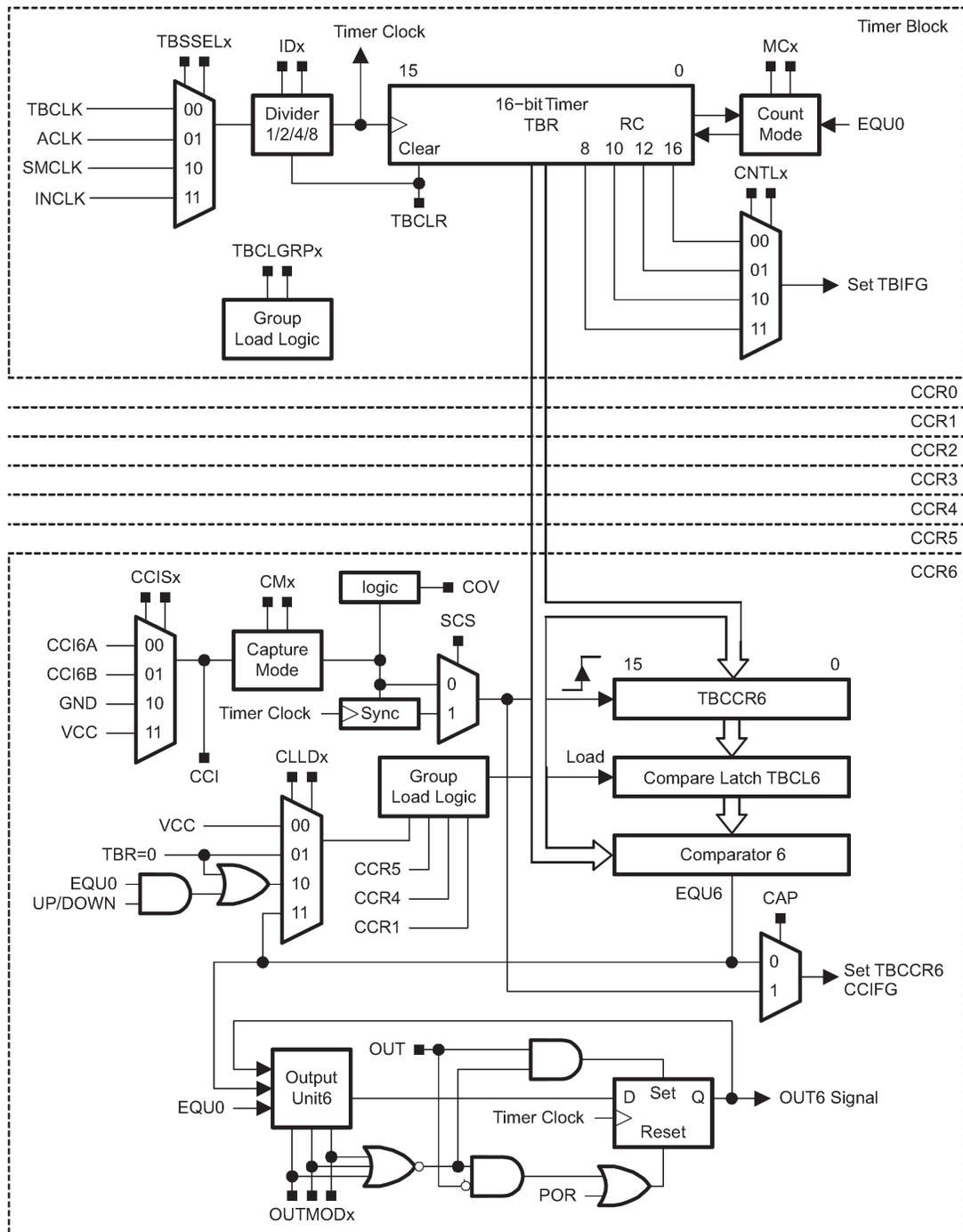
**Figure 5. Timer B Module**

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The up mode is used if the timer period must be different from the TBR(MAX) counts. The timer repeatedly counts up to the value of the compare latch TBCL0 (the value loaded from TBCCR0), which defines the period, as Figure 6 shows. The number of timer counts in the period is TBCL0+1. When the timer value equals TBCL0, the timer restarts counting from zero. If up mode is selected when the timer value is greater than TBCL0, the timer immediately restarts counting from zero.
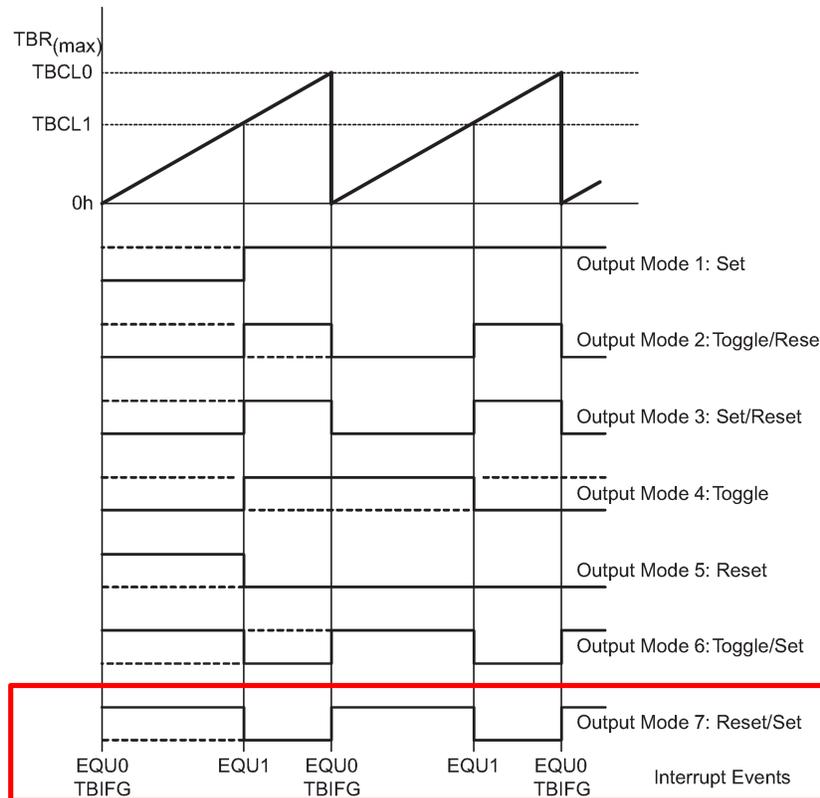


**Figure 6. Timer B in Up Mode**

The PWM duty cycle is also expressible in terms of timer B registers, as Equation 6 shows.

$$D = \frac{|TBCCR1|}{|TBCCR0|}$$

(6)

PWM signals can be decomposed into a DC component with a square-wave of the identical duty-cycle, but with a time-average amplitude of zero, as Figure 7 shows.



**Original PWM signal**          **DC Component**          **Zero average square wave**
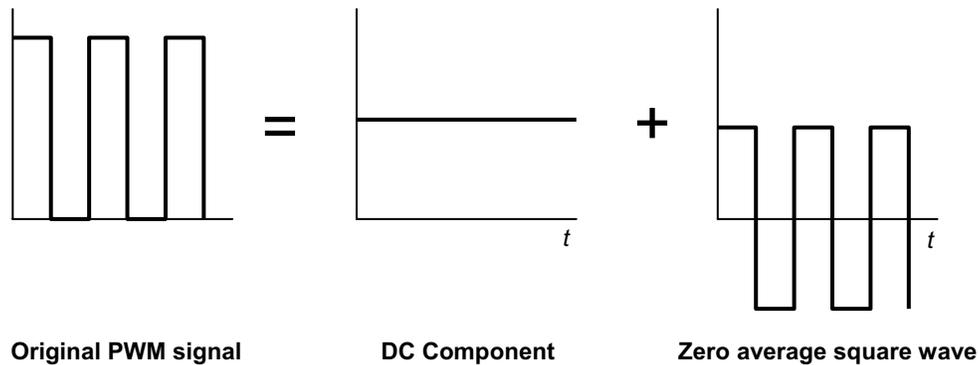
**Figure 7. Decomposition of PWM Signal**

The MSP430 timer compare blocks, in conjunction with the various output modes, can be used to generate these PWM signals with variable duty cycles. For implementing the PWM DAC, either the PWM period is fixed and the duty cycle is varied, or vice versa. In more complex applications, both parameters must be varied to achieve the required DAC output. In this application, the PWM DAC implementation with a fixed PWM period and variable duty cycles is a considerable option.

The DAC resolution is the smallest increment in the analog output voltage that corresponds to an increment in the DAC digital count. In the case of the PWM DAC, the smallest increment in the output voltage level is achieved by incrementing the PWM duty-cycle value. Therefore, in the case of the PWM DAC, the PWM duty-cycle resolution directly represents the DAC resolution.

The $F_{PWM}$ is the frequency of the PWM signal, which is generated using a timer module in an MCU that is input to the low-pass filter. The $F_{CLOCK}$ signal is the frequency of the timer clock source that functions as a timer tick to increment the timer counter. The relationship between $F_{PWM}$, $F_{CLOCK}$, and the PWM DAC duty cycle resolution is given by Equation 7.

$$N = \log_2 \left[ \frac{F_{CLOCK}}{F_{PWM}} \right]$$

where

- N = PWM DAC duty cycle resolution in bits.                                                                  (7)

According to Equation 7, there are two ways to increase the PWM DAC resolution: increasing the $F_{CLOCK}$ or decreasing the $F_{PWM}$. However, higher $F_{PWM}$ frequencies are required to lower the complexity of the external low-pass filter circuitry. Higher order filters require more external components, which increases system cost and space. Reducing the order of the low-pass filter also affects the DAC bandwidth. So, the limiting factor for achieving a higher duty cycle resolution with a higher $F_{PWM}$ frequency is the PWM timer clock source $F_{CLOCK}$. So for a given $F_{CLOCK}$ frequency, there is a clear exchange between the PWM DAC duty cycle resolution and the $F_{PWM}$ frequency.

Consider the active-mode power supply current flowing into the DVCC and AVCC of MSP430 when setting the CPU clock, because the entire transmitter must be able to power-on with less than a 4-mA supply current. As Figure 8 shows, the MSP430F2274 (excluding external circuitry) consumes slightly more than 3 mA and less than 1 mA at 8 MHz and 1 MHz, respectively. So, $F_{CLOCK}$ at 8 MHz is not likely a good choice for this situation because the total power supply current of the transmitter can exceed 4 mA (when accounting for external circuitry). As a solution, an $F_{CLOCK}$ of 1 MHz has been used in this design.
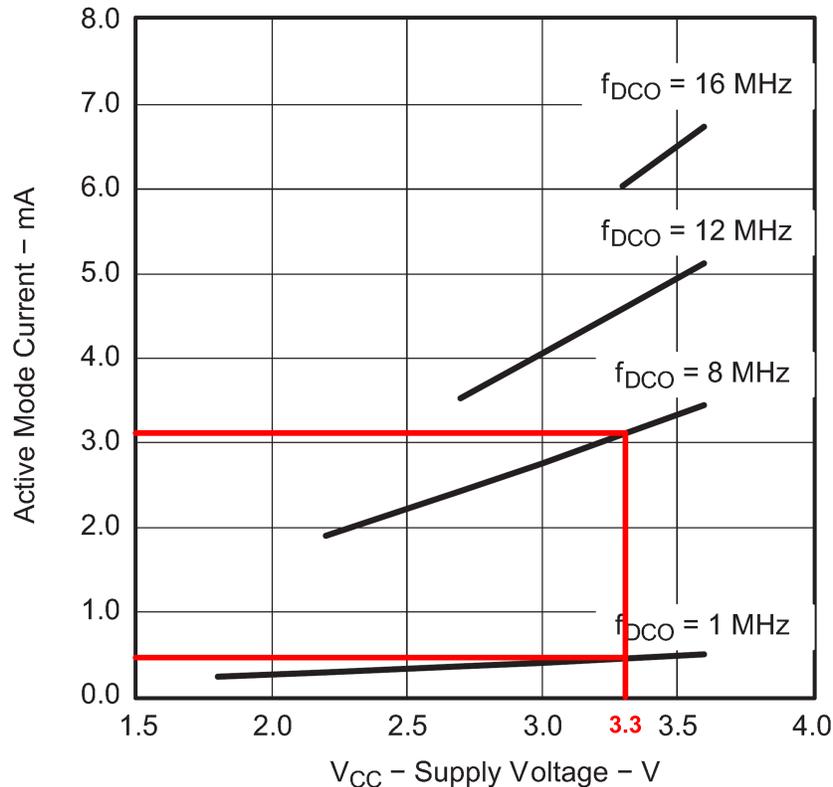


**Figure 8. MSP430F2274 Active-Mode Power Supply Current**

For example, suppose a PWM of 1-KHz frequency is desired with the timer and capture module driven by a 1-MHz CPU clock. The time-base of the PWM provides 1000 clock counts per cycle of PWM, which specifies the timer compare value and then the duty cycle. Setting a PWM of 1 KHz frequency equates to just less than a 10-bit PWM duty cycle resolution. When the PWM resolution is determined, it is possible to calculate the least significant bit (LSB) size. The LSB size depends on the PWM resolution and the full scale output voltage ($V_{FS}$) of the PWM. For a lightly-loaded complementary metal-oxide semiconductor (CMOS) output, the full scale output voltage ($V_{FS}$) is equal to the supply voltage ($V_{CC}$). The desired DC output can only be specified in steps of 3.3 mV (or, 3.3 V per 1000 counts).

Figure 9 shows the basic flow of the PWM DAC code. The code consists of a single interrupt loop that drives the PWM DAC update at a periodic rate to generate the desired PWM waveform.
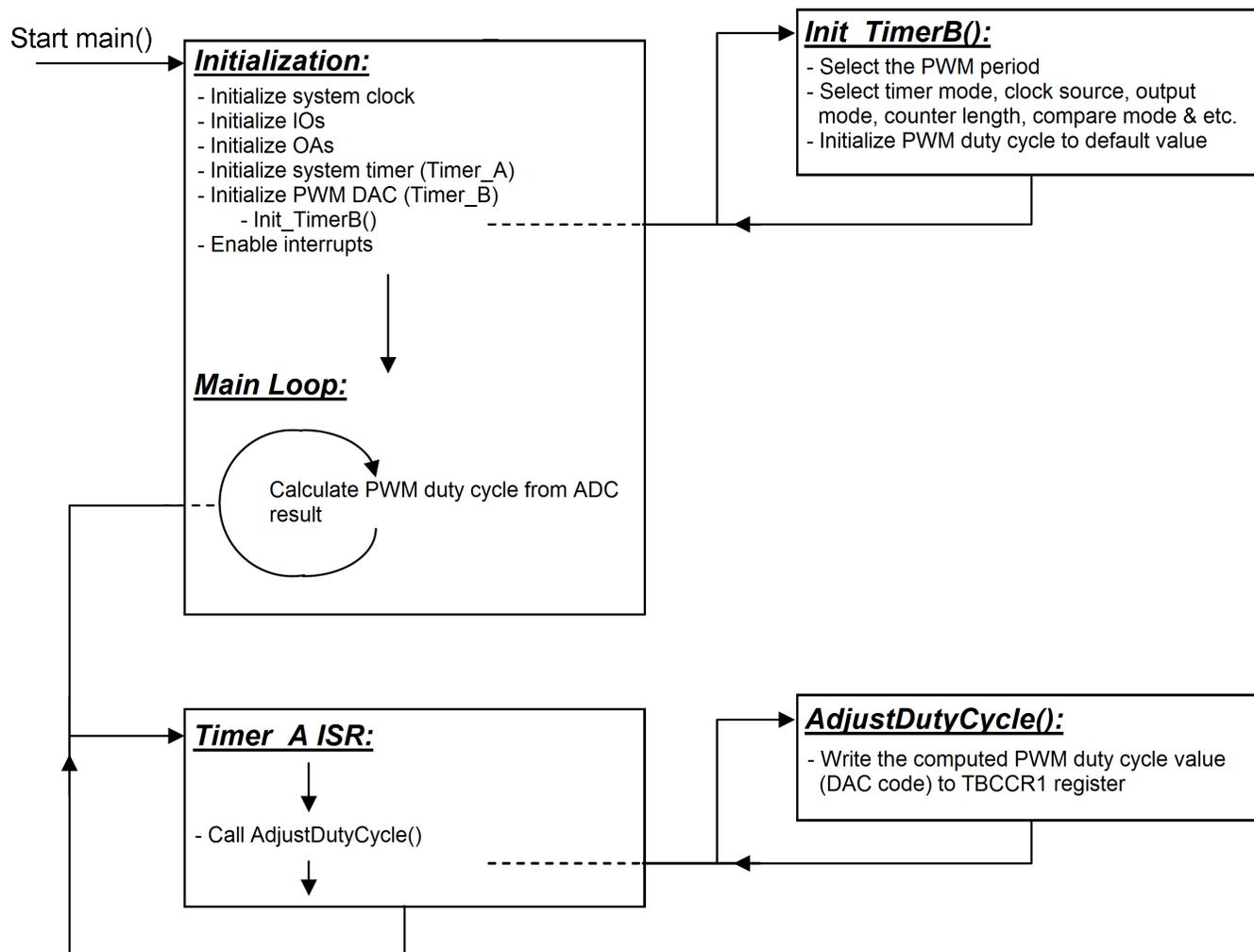


**Figure 9. PWM DAC Code Flow**

The following example code is used to initialize the timer B module and change the duty cycle of the PWM signal. The PWM duty cycle is modified inside the interrupt service routine of timer A (system timer), which generates periodic interrupts.

```
void Init_TimerB(void) {
  TBCCR0 = PWM_Period;          // PWM Period = 1000 counts
  TBCCTL1 = CLLD_1 | OUTMOD_7;    // Capture latch load when TBR is 0, TBCCR1 reset/set
  TBCCR1 = 0x0000;              // Set duty cycle to correspond to 4mA loop current
  TBCTL = TBSSEL_2 | MC_1;        // SMCLK, up mode
}

#pragma vector = TIMERA0_VECTOR
__interrupt void TimerA_ISR(void) {
  AdjustDutyCycle();           // Update duty cycle to new computed value
}
```

### 2.2.2 Analog Low-Pass Filter

An interesting step in this design is generating analog DC voltage from the PWM output signal. The simplest method to generate this voltage is to use a passive low-pass filter. Passive filters are easily implemented with resistors and capacitors. In some cases, a first-order filter works fine; however, in some applications a second order filter may be necessary. The end user must evaluate the trade-off between the filter cost and filter performance. Increase the order of the filter by simply cascading more stages. The roll-off rate becomes steeper for each additional order of the filter by an additional −20 dB/decade.

The PWM DAC performance depends heavily on the design and selection of the analog low-pass filter, particularly where the PWM carrier frequency requires filtering by the analog low-pass filter to output a steady analog voltage. The first important factor that must be defined is how much ripple voltage ($V_{RIPPLE}$) is acceptable in the analog output. The second necessary factor to define is the PWM frequency ($F_{PWM}$). When passing the PWM signal through a low-pass filter, a DC voltage with reasonable ripple generates. The ripple is caused by the charging (during PWM ON time) and discharging (during PWM OFF time) of the filter capacitors, as Figure 10 shows. This ripple represents the first harmonic of the filter and is of the same frequency of the PWM signal. Integer multiples of this PWM frequency form the higher-order harmonics in the system.
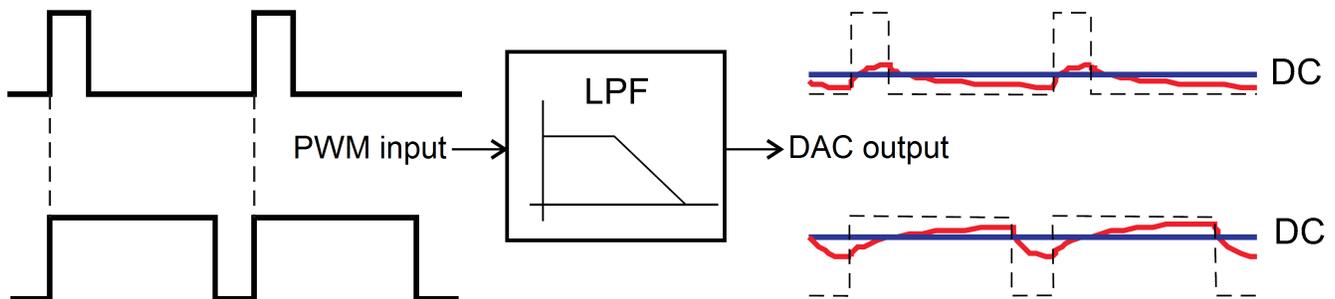


**Figure 10. Voltage Ripples on PWM DAC Output**

Once the acceptable $V_{RIPPLE}$ and $F_{PWM}$ variables are defined, determine the required attenuation using Equation 8.

$$A_{dB} = 20 \times \log_{10}\left[\frac{V_{RIPPLE}}{V_{PWM}}\right]$$

Where

- $A_{dB}$ is attenuation in dB and is a negative number.
- $V_{PWM}$ is the voltage swing of the PWM output, in this case $V_{PWM} = (3.3\ V - 0\ V) = 3.3\ V$. (8)

Once the attenuation factor is known, the user can calculate the required 3-dB frequency ($F_{3dB}$) for the filter as given by Equation 9:

$$A_{dB} = SLOPE \times \log_{10}\left[\frac{F_{PWM}}{F_{3dB}}\right]$$

where

- SLOPE is the roll-off factor of the low-pass filter, SLOPE = −20n dB/decade; n is the order of the filter.
- For the first-order low-pass filter, SLOPE = −20 dB/decade.
- For the second-order low-pass filter, SLOPE = −40 dB/decade.
- Re-arrange Equation 9 to calculate $F_{3dB}$. (9)

$$F_{3dB} = F_{PWM} \times 10^{-\frac{A_{dB}}{SLOPE}}$$ (10)

Now all of the variables have been established in order to design the required passive low-pass filter.

$F_{PWM} = 1$ KHz, as determined in the previous section.

As the output of the low-pass filter is fed to the voltage-to-current converter in the next stage, the voltage ripple in the filter output reflects as current ripples in the loop. This reflection of current ripples leads to an error in temperature measurement. To minimize the error due to ripple voltage, target a $V_{RIPPLE}$ of 1LSB / 10. Minimizing this error may require an aggressive filter cut-off at the cost of an increased settling time. This method is fine for temperature sensing applications where fast settling is not desired.

$$V_{RIPPLE} = \frac{1\,LSB}{10} = \frac{3.3\,mV}{10} = 0.33\,mV \tag{11}$$

So, the required attenuation is:

$$A_{dB} = 20 \times \log_{10}\left[\frac{0.33\,mV}{3.3\,V}\right] = -80\,dB \tag{12}$$

The next step is to determine the bandwidth of the filter.

For the first-order low-pass filter:

$$F_{3dB} = 1000\,Hz \times 10^{-\frac{80\,dB}{20}} = 0.1\,Hz \tag{13}$$

For the second-order low-pass filter:

$$F_{3dB} = 1000\,Hz \times 10^{-\frac{80\,dB}{40}} = 10\,Hz \tag{14}$$

If using a first-order low-pass filter, the user must design a filter with an $F_{3dB}$ of 0.1 Hz, which is even smaller than the bandwidth of the RTD sensor. The first-order low-pass filter clearly cannot be used for this application. A second-order filter requires an $F_{3dB}$ of 10 Hz, which is greater than the bandwidth of the RTD sensor and a better option for this application.

A second-order low-pass filter is implemented simply by cascading two first-order filters in series as Figure 11 shows. The $F_{3dB}$ of the second-order filter is given by Equation 15.

$$F_{3dB} = \frac{1}{2\pi\sqrt{R8 \times R9 \times C15 \times C16}} \tag{15}$$

If R8 = R9 = RF and C15 = C16 = CF, then

$$F_{3dB} = \frac{1}{2\pi \times RF \times CF} \tag{16}$$

Equation 17 shows that if the user chooses 1 µF for CF, then the computed RF is 15.92 kΩ. Depending upon availability, the resistor selected is 15.8 kΩ (±0.1% and 25 PPM).

$$RF = \frac{1}{2\pi \times F_{3dB} \times CF} = \frac{1}{2\pi \times 10\,Hz \times 1\,\mu F} = 15.92\,k\Omega \tag{17}$$



Figure 11. Second-Order Low-Pass Filter

## 2.3 *Voltage-to-Current (V to I) Conversion*



**Figure 12. Voltage-to-Current Converter**

In Figure 12, operational amplifier (OA1) uses negative feedback to ensure that the potentials at its inverting ($V_{OA1-}$) and non-inverting ($V_{OA1+}$) input terminals are equal. In this configuration, $V_{OA1-}$ is directly tied to the local GND; therefore the potential at the non-inverting input terminal ($V_{OA1+}$) is driven to local ground. $I_{PWM}$ can be given as:

$$I_{PWM} = \frac{D \times V_{CC}}{(R8 + R9 + R10)}$$

(18)

Operational amplifier (OA1) drives the base of the NPN BJT (Q1) to allow current to flow through R16 such that the voltage drop across resistors R13 and R16 always remains equal, ensuring that the inverting and non-inverting terminals are at the same potential. A small part of the current through R16 is sourced by the quiescent current of all of the components used in the transmitter design (like the low dropout voltage (LDO) regulator and MSP430). Because the voltage drops across R13 and R16 are equal, the different sized resistors cause different current flows through each resistor. This voltage drop can be used to apply gain to the current flow through R16 by controlling the ratio of resistor R13 to R16, as Equation 19 shows.

$$R13 \times I_{PWM} = R16 \times I_{SENSE}$$

(19)

$$I_{SENSE} = \frac{R13 \times I_{PWM}}{R16}$$

(20)

This current gain is helpful to allow a majority of the output current to come directly from the loop through Q1 instead of from the voltage-to-current converter. This advantage, in addition to low-power components, keeps the current consumption of the voltage-to-current converter low. The currents of $I_{LOOP}$ and $I_{SENSE}$ combine to form the output loop current $I_{LOOP}$, as Equation 21 shows.

$$I_{LOOP} = I_{PWM} + I_{SENSE}$$

(21)

$$I_{LOOP} = I_{PWM} \times \left(1 + \frac{R13}{R16}\right)$$

(22)

$$I_{LOOP} = \frac{D \times V_{CC}}{(R8 + R9 + R10)}\left(1 + \frac{R13}{R16}\right)$$

(23)

Finally, the complete transfer function for $I_{LOOP}$ can be arranged as a function of input code, as Equation 24 shows.

$$I_{LOOP} = \frac{CODE \times V_{CC}}{1000 \times (R8 + R9 + R10)}\left(1 + \frac{R13}{R16}\right)$$

(24)

R17 is included to reduce the gain of transistor Q1 and thereby reduce the closed-loop gain of the voltage-to-current converter and ensure a stable design. Typically, the ideal range for R17 is from 20 Ω to 120 Ω (keeping compliance voltage in mind). Resistors R10, R13, and R16 are sized based on the full-scale range of the DAC, supply voltage, and the desired loop current range of the design.

$$I_{LOOP} = \frac{CODE \times 3.3\,V}{1000 \times (15.8\,K + 15.8\,K + 240\,K)}\left(1 + \frac{80.6\,K}{0.0402\,K}\right)$$
(25)

$$I_{LOOP} = CODE \times 0.02437304$$
(26)

## 2.4 Selection of External BJT

The MPS430 PWM DAC uses an external NPN transistor (BJT). Transistor Q1 conducts the majority of the signal-dependent, 4- to 20-mA loop current. Using an external transistor avoids on-chip power dissipation and thermally induced errors. Because the external transistor is inside a feedback control loop, the characteristics of the transistor are not critical. Virtually any transistor with sufficient voltage, current, and power rating may be used. Considerations such as case style and thermal mounting often influence the choice for any given application. The basic requirements for selecting an external BJT are:

| | |
|---|---|
| $V_{CEO}$ = | 45 V minimum |
| β = | 40 minimum, and the transistor must be able to handle power dissipation |
| $P_D$ = | $V_{CE\,(MAX)} \times I_{LOOP\,(MAX)}$ |

The worst case power dissipation in Q1 is given as:

$$P_{D\_Q1} = [V_{LOOP\,(MAX)} - (100\,\Omega \times I_{LOOP\,(MAX)}) - (20\,\Omega \times I_{LOOP\,(MAX)}) - (40.2\,\Omega \times I_{LOOP\,(MAX)})] \times I_{LOOP\,(MAX)}$$

$$P_{D\_Q1} = [33\,V - (100\,\Omega \times 20\,mA) - (20\,\Omega \times 20\,mA) - (40.2\,\Omega \times 20\,mA)] \times 20\,mA$$

$$P_{D\_Q1} = 29.1552\,V \times 20\,mA = 0.59592\,W$$
(27)

The previous equations indicate that Q1 must be capable of handling 0.59592 W of power dissipation at the maximum ambient temperature of 85ºC. The BJT selected for this application is the BCP55. The total power dissipation of the BCP55 is 1.5 W at 25ºC, which derates above 25ºC at the rate of 12mW/ºC. Using simple math, the total power dissipation of the BCP55 at 85ºC equals approximately 0.78 W, which is greater than the actual power dissipation.

## 2.5 Mapping RTD Resistance to $I_{LOOP}$

In this reference design, a look-up table for the PT100 RTD with a resolution of 1°C is used for linear interpolation in the software. A standard look-up table of for RTDs consists of resistance values ($R_{LT}$) against corresponding temperature values ($T_{LT}$), where two consecutive temperatures ($T_{LT[n-1]}$ and $T_{LT[n]}$) are 1°C apart. The RTD value is used in linear interpolation of the line segment involving two surrounding points in the PT100 RTD look-up table. If additional accuracy is desired, a table with more points and with less than 1°C or more accurate curve fit can be stored as a look-up reference table.

To perform a linear interpolation using a look-up table, first compare the measured $R_{RTD}$ values with the resistance values ($R_{LT}$) given in the look-up table, until the look-up table value exceeds the measured value that is being converted. Then use Equation 28 to convert the measured $R_{RTD}$ value to the temperature value ($T_{RTD}$). This operation involves four addition, one multiplication, and one division step, respectively. This operation can be done easily on a 16-bit MSP340F2274 MCU.

$$T_{RTD} = T_{LT[n-1]} + (R_{RTD} - R_{LT[n-1]}) \times \left[\frac{(T_{LT[n]} - T_{LT[n-1]})}{(R_{LT[n]} - R_{LT[n-1]})}\right]$$
(28)

Now, convert the temperature value ($T_{RTD}$) to the equivalent loop current using Equation 29.

$$I_{LOOP} = 4 \text{ mA} + (T_{RTD} + 200°C) \times \left[\frac{16 \text{ mA}}{1050°C}\right]$$

(29)

Re-arrange the V-to-I converter transfer function in Equation 26 to find out the PWM duty cycle code,

$$\text{Duty\_cycle} = \text{DEC2HE}\left[41.029 \times I_{LOOP}\right]$$

(30)

## 2.6 Power Design

The TPS7A16xx family of ultra-low power voltage regulators offers the benefit of ultra-low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. The TPS7A16xx family of LDOs accepts a maximum input voltage of 60 V, which makes them ideal for use in industrial applications where high-voltage transients are present. The TPS7A1601 has an adjustable output voltage range from 1.194 V to 20 V. The nominal output of the device is set by two external resistors R2 and R5, as Figure 13 shows. To set the LDO output voltage, $V_{CC}$ = 3.3 V, calculate the resistor divider components using Equation 31.

$$R2 = R5 \times \left[\frac{V_{CC}}{V_{REF}} - 1\right]$$

where

- $V_{REF}$ = LDO internal reference voltage = 1.193 V (typical).

(31)

The selected values are R2 = 22.1 kΩ and R5 = 12.4 kΩ.

LDO/Power Circuitry
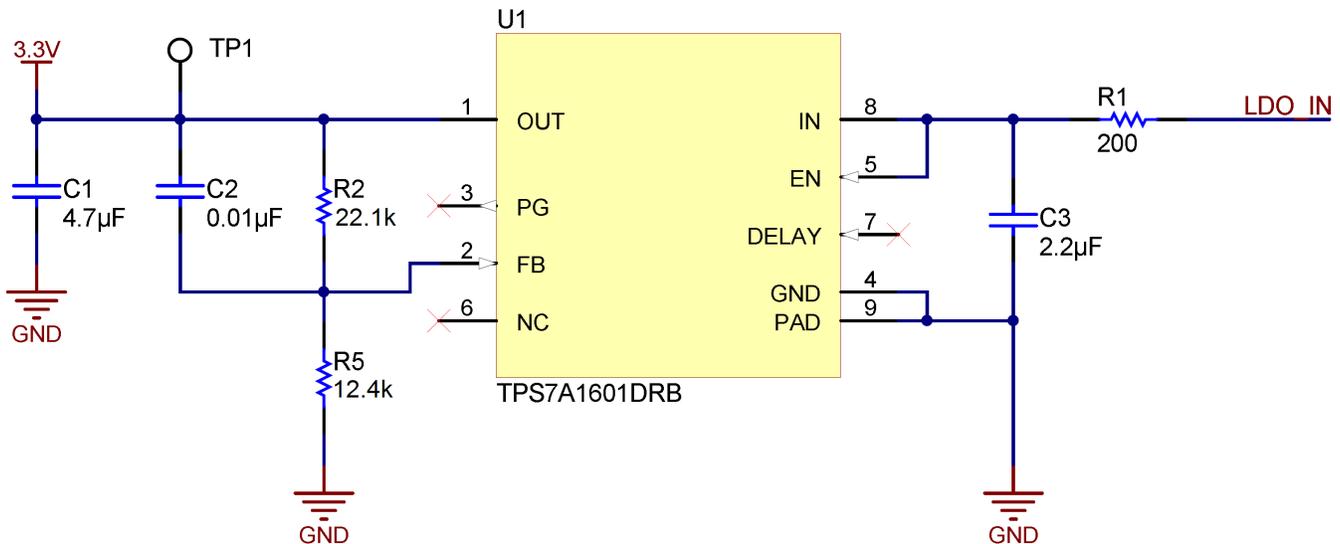


**Figure 13. LDO Circuit With Feedback for Adjustable Output**

The maximum power dissipation within the LDO is given by Equation 32:

$$P_D = (V_{INLDO} - V_{CC}) \times I_Q$$

(32)

Assume a worst-case scenario where the entire maximum loop power supply voltage, $V_{SUPPLY (MAX)}$ = 33 V, appears across the LDO input. The maximum allowed $I_Q$ = 3.3 mA.

$$P_D = (33 \text{ V} - 3.3 \text{ V}) \times 3.3 \text{ mA} = 98.01 \text{ mW}$$

(33)

The junction-to-ambient thermal resistance, $\theta_{JA}$, of the TPS7A1601 device is 44.5°C/W.

For safe operation:

$$\theta_{JA} \times P_D + T_{A\ (MAX)} < T_{J\ (MAX)} \tag{34}$$

The maximum junction temperature before the TPS7A1601 device shuts down is 170°C. From Equation 34, the worst case junction temperature of TPS7A1601 device is approximately 90°C, assuming an ambient temperature of 85°C. Therefore, a sufficient thermal-operating margin is available with the TPS7A1601 device, even accounting for the worst-case power dissipation.

## 2.7 *Diode Bridge and Protection Circuit*

The industrial environment can be dangerous for sensitive electronic components, so systems are frequently designed to be robust, including protection against incorrect wiring and immunity to environmental hazards that may lead to electrical overstress or undesirable performance. Figure 14 shows the circuit used to protect this design from the aforementioned events.

To protect against incorrect terminal connections a diode bridge is implemented. Two diodes are placed with a cathode facing the positive node of the loop transmitter and a node facing each of the terminal blocks. Similarly, two diodes are placed with a node facing the return node of the loop transmitter and a cathode facing each of the terminal blocks. This arrangement ensures that the loop connections are rectified regardless of which terminal is connected to the supply and which is connected to the return.

The selection of this diode is based on low, reverse leakage current and low forward voltage. The low, reverse leakage current is important because two diodes in the bridge configuration are always reverse-biased, allowing some leakage current, which directly impacts the accuracy. Low forward voltage is helpful because this allows for the design to achieve lower compliance voltage. The BAT46WJ, 115 diode was chosen for this design. This device features a 0.5-µA reverse leakage current at a reverse bias of 40 V and 0.4-V forward voltage at a forward current of 40 mA.
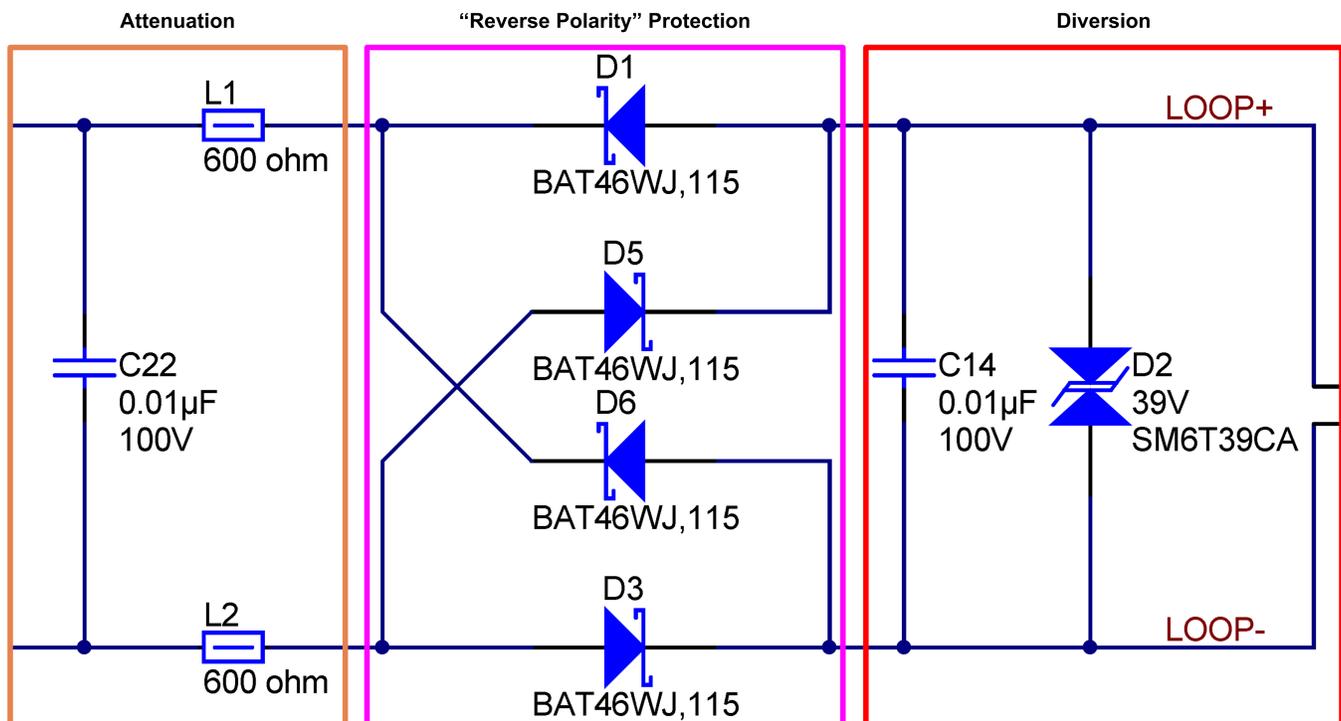


**Figure 14. Reverse Polarity Protection Using Diodes Bridge**

The IEC61000-4 transients have two main components: a high-frequency component and a high-energy component. These two properties can be leveraged with a strategy of attenuation and diversion by the protection circuitry to deliver robust immunity.

Attenuation uses passive components, primarily resistors and capacitors, to attenuate high-frequency transients and to limit series current. Ferrite beads are commonly used with voltage outputs to maintain DC accuracy while still limiting series current. Ferrite beads can also be useful for current outputs because they do not add any additional compliance voltage headroom at DC. A ferrite is included in series between each of the terminal blocks and the diode bridge along with a parallel capacitor to attenuate the high-frequency transients and limit current flow during exposure to transients.

Diversion capitalizes on the high-voltage properties of the transient signals by using diodes to clamp the transient within supply voltages or to divert the energy to ground or the return path. Transient voltage suppressor (TVS) diodes are helpful to protect against the IEC transients because the diodes break down very quickly and often feature high power ratings, which are critical to survive multiple transient strikes. A TVS diode is included in between the two terminal block connections, positioned close to the terminal blocks in the PCB layout.

A bidirectional TVS diode is used to divert high-voltage transients to ground. Base the selection of this diode on working voltage, breakdown voltage, leakage current, and power rating. The working voltage specification defines the largest reverse voltage at which the diode is meant to be continuously operated without conducting. This reverse voltage is the voltage at the "knee" of the reverse breakdown curve, which is where the diode begins to break down and exhibit some leakage current. As the voltage increases above the working voltage, more current begins to flow through the diode. The breakdown voltage defines the reverse voltage at which the diode is fully allowing current to flow. An important factor to keep in mind is that if excessive current flows through a diode, the breakdown voltage rises.

The diode breakdown voltage must be low enough to protect all of the components connected to the output terminals and to provide headroom to continue providing this protection as the breakdown voltage rises with large currents. In this design, the working voltage of the TVS diode must be at or above the upper limit of the allowed supply voltages, because any higher voltage causes leakage through the diode. For the purposes of this design, use a SM6T39CA TVS diode with a working voltage of 33.3 V, breakdown voltage of 39 V (nominal), and power rating of 600 W.

An additional parameter to consider for TVS diode selection is leakage current. At the working voltage, when the diode is not operating in its breakdown region, some current flows through the diode and can affect system accuracy. The TVS diode selected for this design features a 1-µA maximum leakage current at the working voltage.

Refer to Section 5.7.1 of TIDA-00165 for a detailed understanding on IEC-61000-4 protection and selection of the TVS diode.

## 3    Hardware PCB Assembly View



**Figure 15. Top-Side PCB Assembly View**



**Figure 16. Bottom-Side PCB Assembly View**

## 4    Software Update

This code is designed to implement a temperature transmitter application highlighting the MSP430F2274 MCU with its integrated analog peripherals (ADC10 and OAs) to receive data from an RTD temperature probe and send out the temperature reading on a 4- to 20-mA signal. The code also addresses the use of system level calibration, both offset and gain, which can improve the ADC and PWM DAC accuracy. The code includes linear interpolation to address the non-linearity of the RTD element.

TI™ recommends using Code Composer Studio™ (CCS) for MSP430 firmware updates. CCS is an integrated development environment (IDE) for TI embedded processor families. CCS comprises a suite of tools used to develop and debug embedded applications. CCS includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators, real-time operating system, and many other features. The intuitive IDE provides a single user interface that guides through each step of the application development flow. The MSP430F2274 implements an embedded emulation module (EEM) for programming and debugging. The EEM is accessible and controllable through either 4-wire Joint Test Action Group (JTAG) mode or Spy-Bi-Wire mode. This reference design only supports the Spy-Bi-Wire mode. For more details on how the features of the EEM can be used together with CCS, see Advanced Debugging Using the Enhanced Emulation Module (SLAA393). The 2-wire interface is made up of the SBWTCK (Spy-Bi-Wire test clock) and SBWTDIO (Spy-Bi-Wire test data input and output) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the RST/NMI pin of the device. The SBWTCK, SBWTDIO, VCC, and GND from the debugger must be connected on J1 for programming and debugging purposes (Figure 17).



Figure 17. Spy-Bi-Wire Interface for Debugging and Programming of MCU

With the proper connections, a MSP430 debugger interface (such as the MSP-FET Emulation Tool shown in Figure 18) can be used to program and debug code on the reference design.



**Figure 18. MSP-FET Emulation Tool**

| CAUTION |
| --- |
| Take special care during debug operations to avoid damages due to conflicts in different power domains (4- to 20-mA loop power and debugger tools power). Read the following section carefully. |

The TPS7A1601 device supplies 3.3 V to the MSP430 device if a voltage in the range of 10 V to 33 V is supplied to the 4- to 20-mA loop. Normally this 3.3 V powers the MSP430F2274.

If this local 3.3-V supply from the TPS7A1601 is used during debug operations, ensure that the VCC_Target pin from the debugger interface is connected to the $V_{CC}$ pin. If there is no local power and power from the debugger interface is used, ensure that the VCC_Tool pin from the debugger interface is connected to the $V_{CC}$ pin and disconnect the VCC_Target pin. Refer to Figure 19.
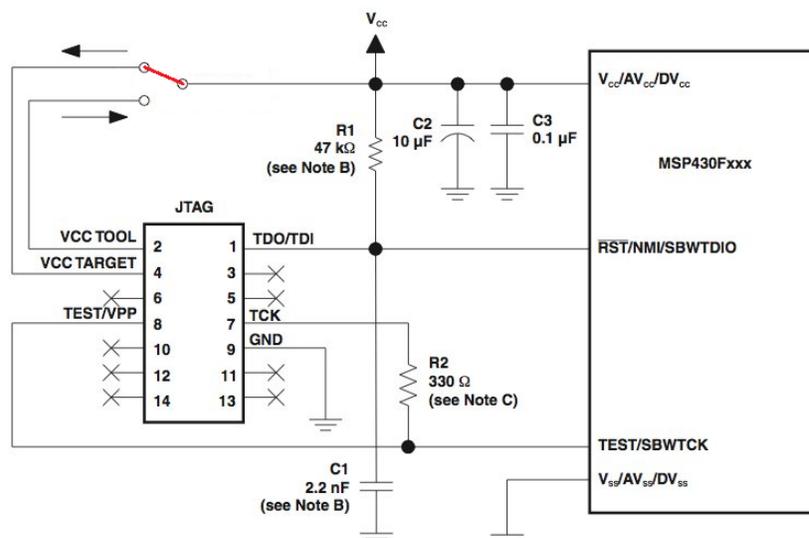


**Figure 19. Power Supply Connection During Debugging**

## 5    Test Setup
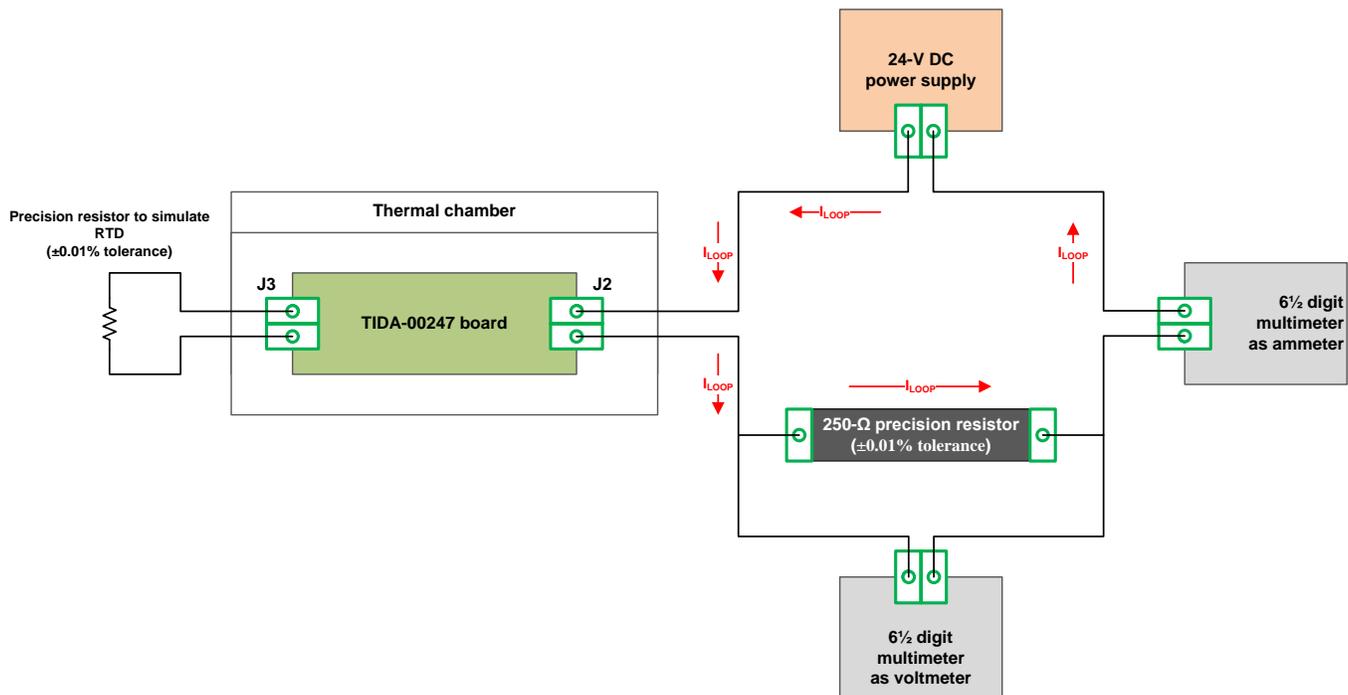


**Figure 20. Test Setup**

The following equipment was used for the testing:

1. A 24-V DV power supply with current limit set to 50 mA
2. A 6½ digit multimeter functional as a DC ammeter and connected in series with a power supply
3. An additional 6½ digit multimeter functional as a DC voltmeter
4. MSP430-FET emulation tool for programming and debugging
5. 250-Ω external load resistor connected in series with a DC power supply and ammeter
6. Set of high precision resistors (20 Ω to 350 Ω) with a ±0.01% tolerance to simulate RTD
7. A thermal chamber to vary board temperature from –40 ºC to 85ºC during calibration and testing
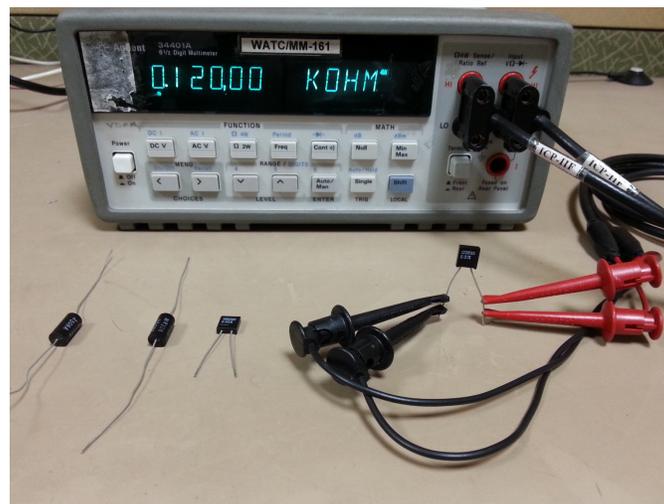


**Figure 21. 4-Wires Resistance Measurement Using 6½ Digit Multimeter**

# 6 Test Results

## 6.1 Maximum Measured Error of Complete System

After a three-point temperature calibration, a complete system characterization was performed for maximum measured error. In this setup, a power supply and 6½ digit multimeter was used to measure the loop current. As Figure 22 shows, multiple precision resistor values were used covering −200°C to 850°C of the PT100 RTD.
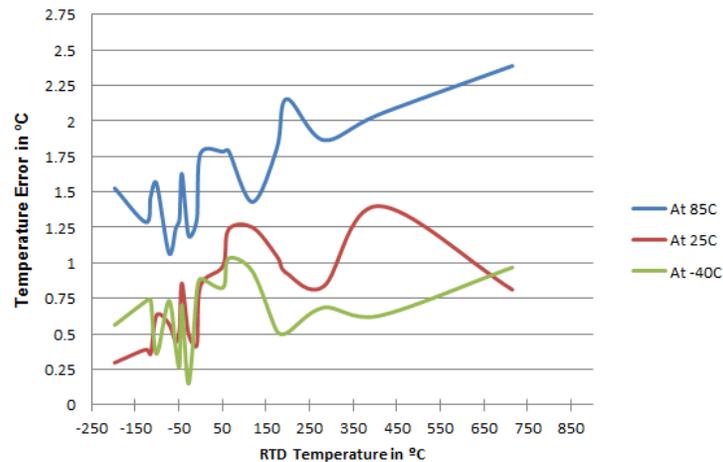


**Figure 22. Maximum Measured Error of Complete System**

## 6.2 Power Supply Influence

For the power supply influence test, the power supply was slowly varied from 10 V to 33 V and the corresponding loop-current change was recorded. The PWM DAC output was programmed for a fixed 12-mA output current for this measurement. The total deviation of loop current across the power supply range was approximately 5.7 µA.

## 6.3 Output Current Resolution

For this test, the PWM DAC output was programmed for a fixed 12-mA output current. More than 2500 samples were recorded over time using a 6½ digit multimeter. In terms of output current, the noise-free resolution was approximately 2.8 µA.

## 6.4 Power Supply Current

For this test, the voltage-to-current converter stage was disabled by generating a PWM signal with a zero duty cycle. In this condition, the power supply current of the transmitter is the same as the current flowing in the loop, which is less than 1.8 mA.

# 7 Design Files

## 7.1 Schematic

To download the schematic, see the design files at [TIDA-00247](#).
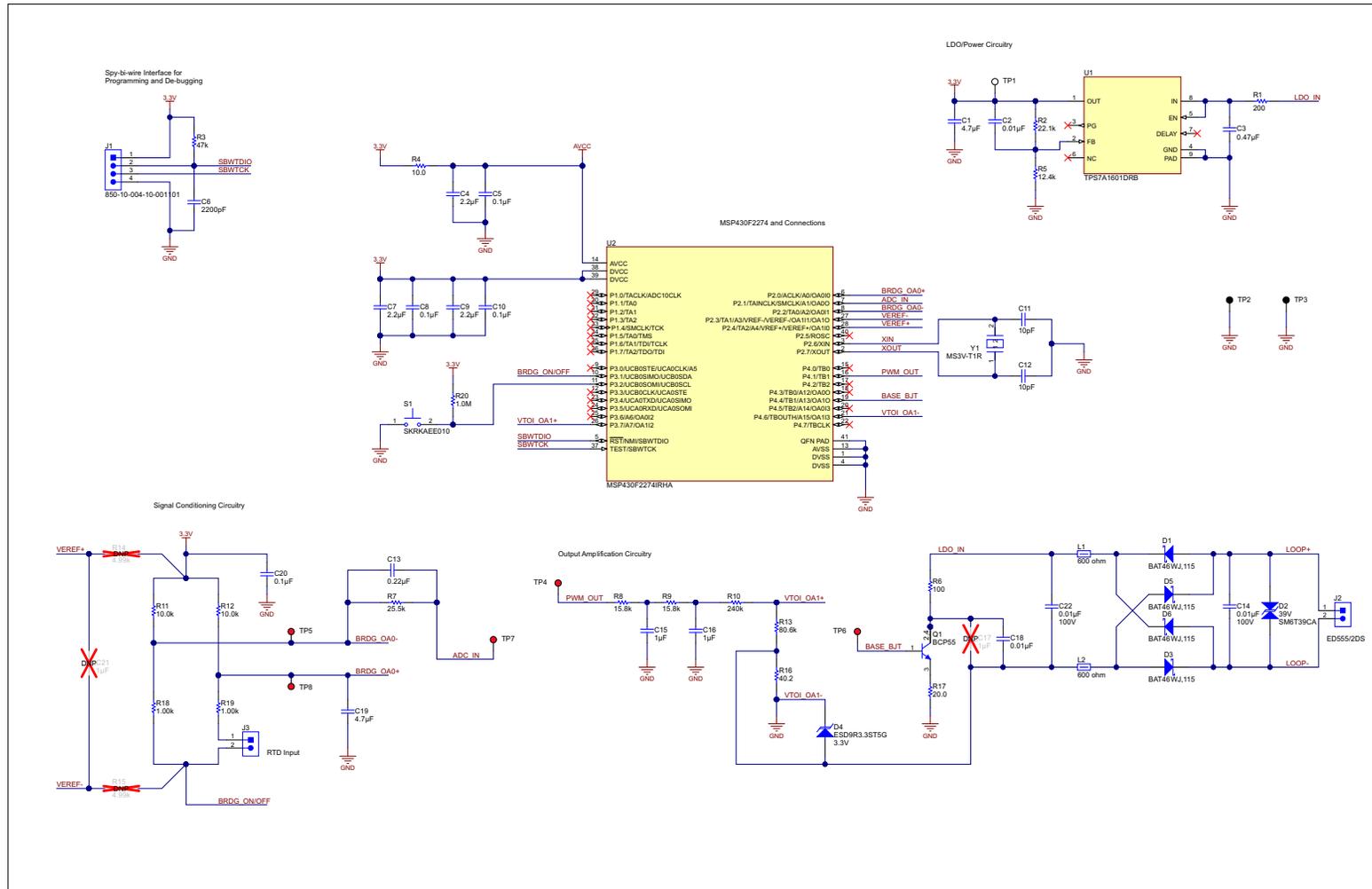


**Figure 23. TIDA-00247 Schematic**

## 7.2 Bill of Materials

To download the Bill of Materials, see the design files at TIDA-00247.

## 7.3 Layer Plots

To download the layer plots, see the design files at TIDA-00247.
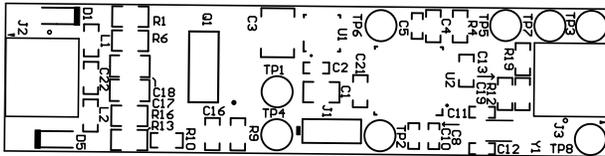


**Figure 24. Top Overlay**
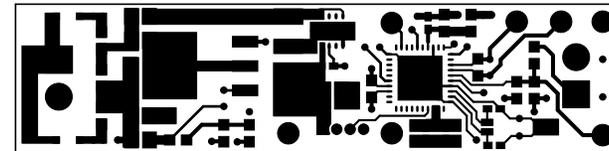


**Figure 25. Top Electric**
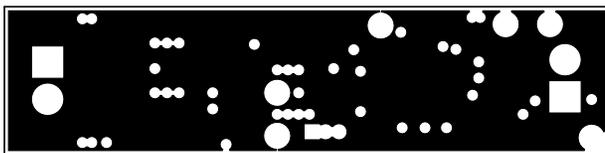


**Figure 26. Ground Plane**
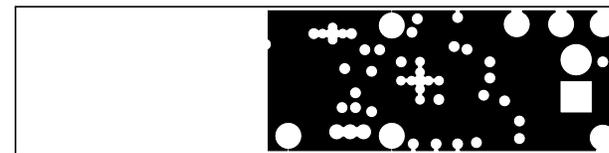


**Figure 27. Power Plane**
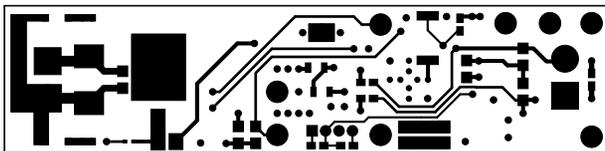


**Figure 28. Top Electric**



**Figure 29. Bottom Overlay**
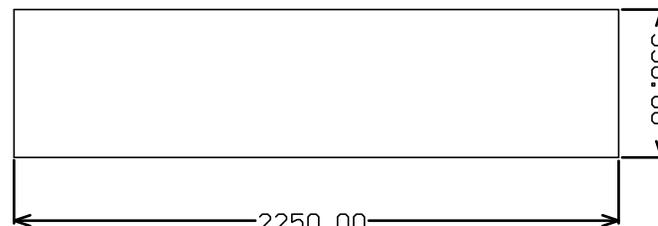


**Figure 30. Board Dimensions**

## 7.4 Altium File

To download the Altium file, see the design files at TIDA-00247.
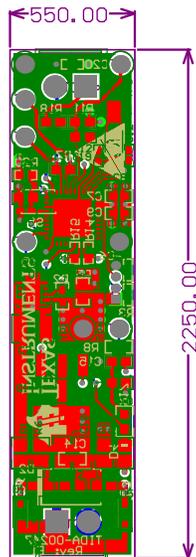
## Gerber File

To download the Gerber files, see the design files at [TIDA-00247](TIDA-00247).
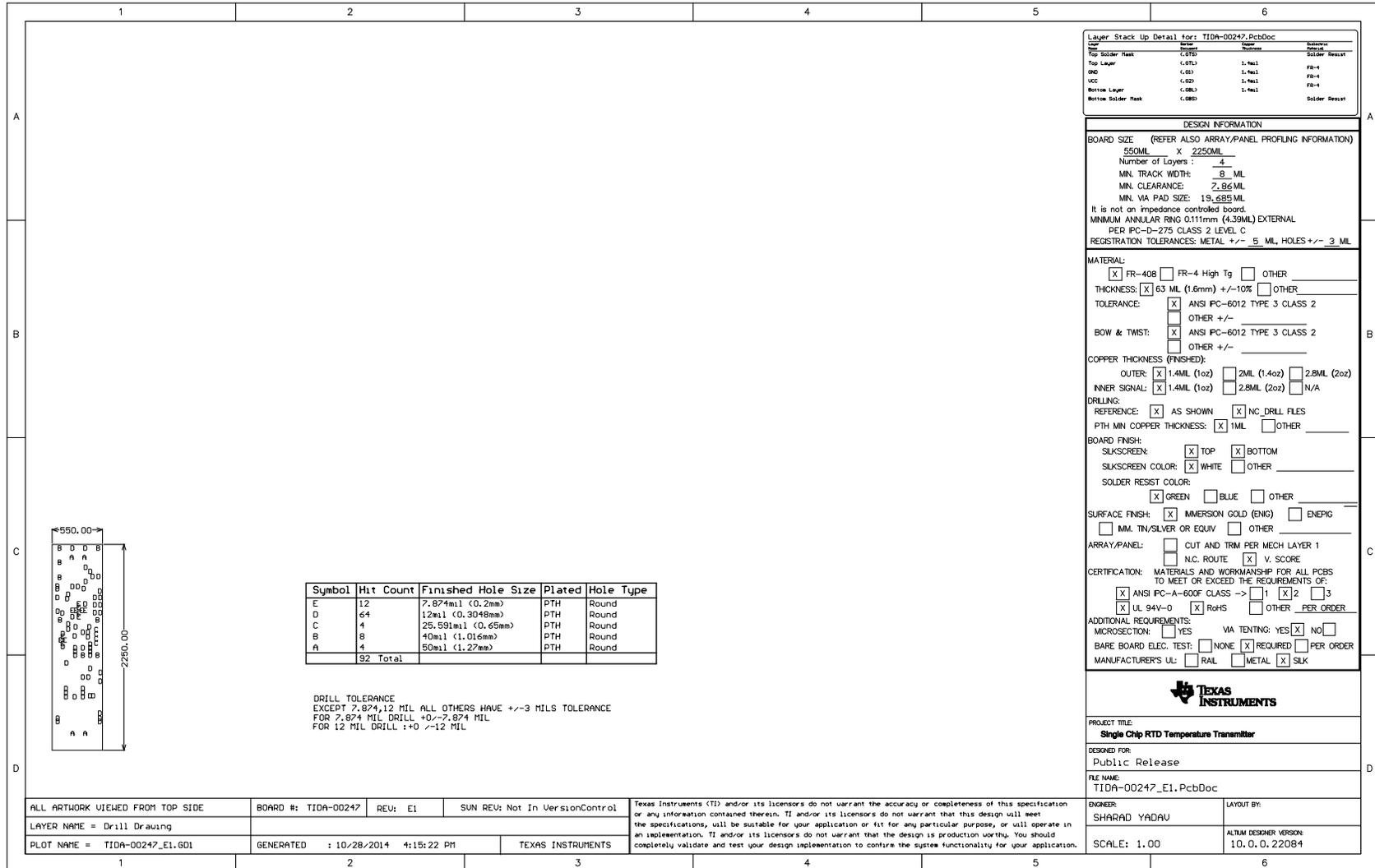
**Figure 31. Fabrication Drawing**

## 7.5 Assembly Files

To download the assembly files, see the design files at TIDA-00247.
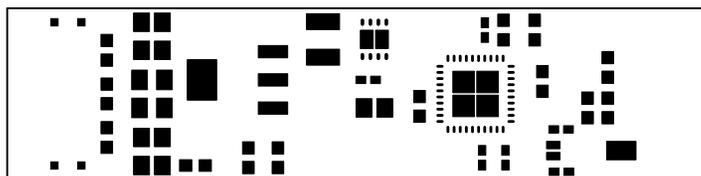


**Figure 32. Top Paste**
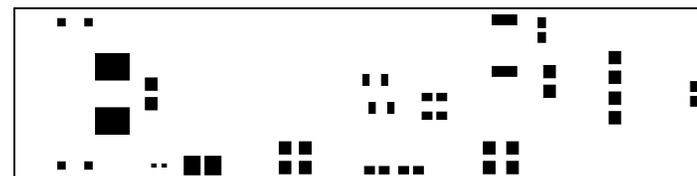


**Figure 33. Bottom Paste**
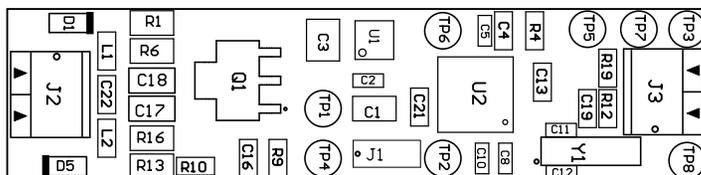


**Figure 34. Top Assembly**
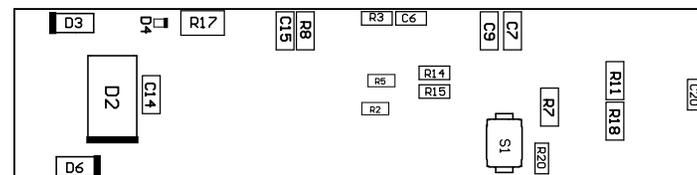


**Figure 35. Bottom Assembly**
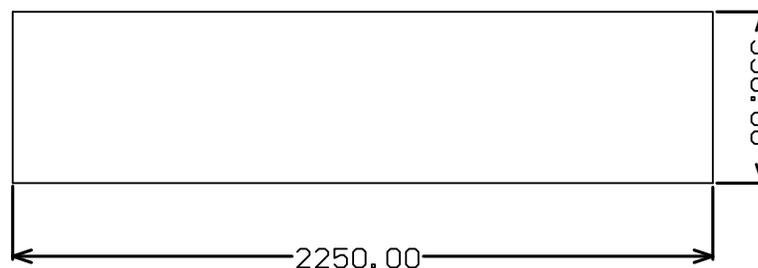


**Figure 36. Board Outline**

# 8    References

1. Texas Instruments, *Small Form Factor, 2-Wire 4 to 20mA Current Loop RTD Temperature Transmitter Reference Design*, User's Guide, (TIDU385).

2. Texas Instruments, Integrating Mixed Signal Capabilities on MSP430™ in Industrial Automation Applications, Application Report, (SLAY030).

3. Texas Instruments, *Advanced Debugging Using the Enhanced Emulation Module (EEM) With Code Composer Studio Version 6*, Application Report, (SLAA393).

4. Thermibel, *Conversion of RTD Pt100*, http://www.thermibel.be/documents/pt100/conv-rtd.xml?lang=en.

## Revision History

**Changes from Original (February 2015) to A Revision** **Page**

* Changed two connectors in system block diagram. ………………………………………………………………… 3

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.