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Design Resources

TIDA-00400	Tool Folder Containing Design Files
LM5017	Product Folder
TPS70933	Product Folder
TPS70950	Product Folder
TPS7A4700	Product Folder
TPS7A3001	Product Folder



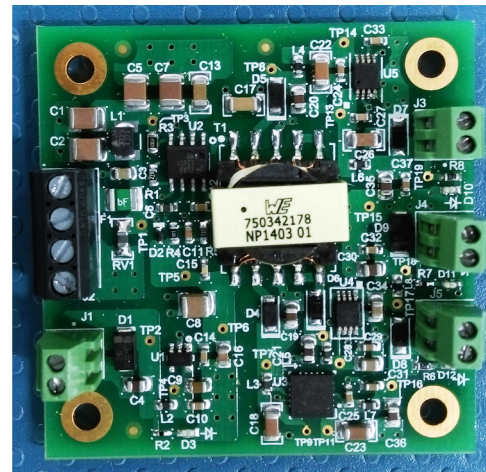
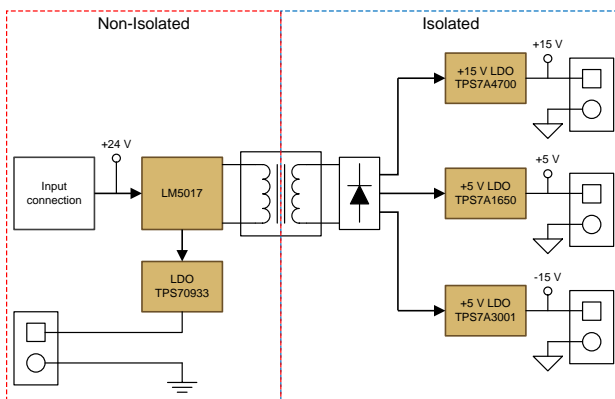
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Design Features

- Wide Input Voltage Range: 18 V to 30 V (24-V Nominal)
 - Uses LM5017 Device Capable of 9- to 100-V Input Operation for Withstanding Transients and Surge Voltage
- Non-Isolated Output: 3.3 V With 50 mA
- Three Isolated Outputs:
 - +15 V With 30 mA
 - -15 V With 30 mA
 - +5 V With 40 mA
- Small Form Factor for Space Constraint IO Cards 51 x 51 x 8 mm (L x W x H)
- Primary-Side Regulation; No Need for Optocoupler; Increases Lifetime Reliability
- Cost-Effective; Lower Bill of Materials (BOM)

Featured Applications

- Programmable Logic Controllers (PLC) and Distributed Control System (DCS) IO Modules
- Isolated Power Supply for Test and Measurement



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1 Introduction

Programmable logic controllers (PLC) and IO modules are widely used in factory automation. Currently, in the large scale automation sector, systems demand a number of IO channels on a single module with higher accuracy. The isolation is installed to break the ground loop to provide digital/analog signal isolation or channel-to-channel isolation to prevent noise interference from a common ground. The isolation can also be a mandatory safety standard to isolate the user from the hazardous voltage.

Figure 1 and Figure 2 show a typical factory automation digital and analog input module diagram.

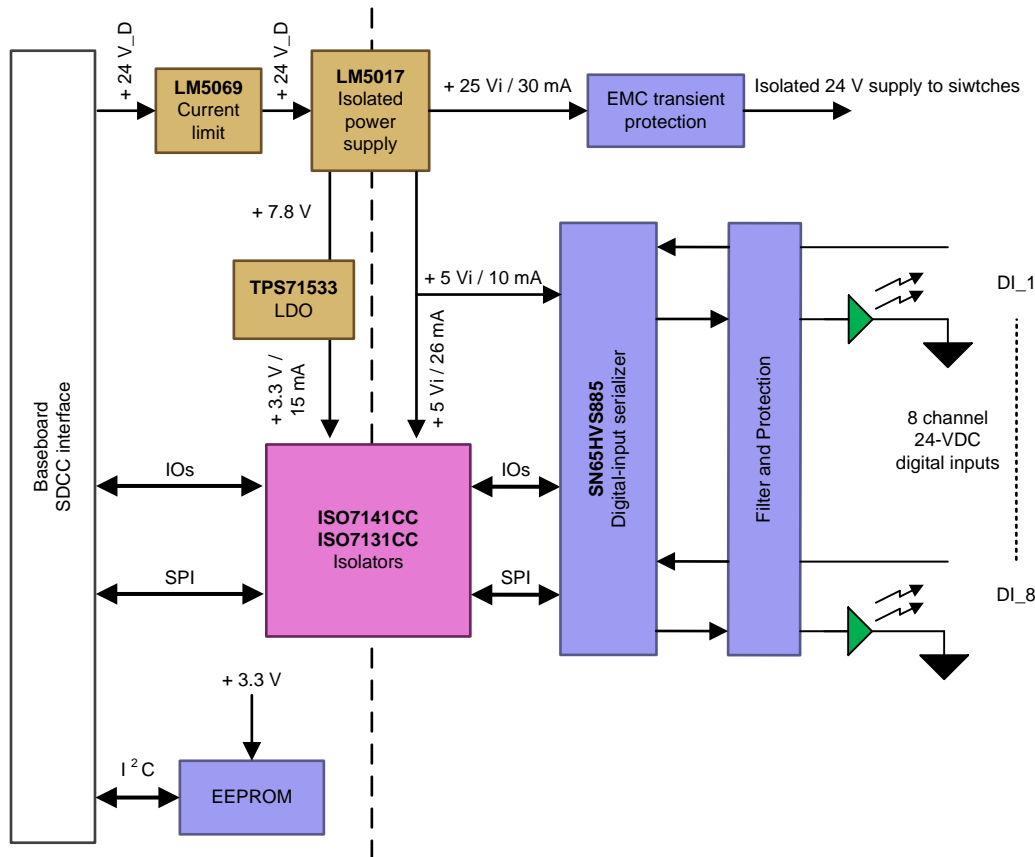


Figure 1. Digital Input Module

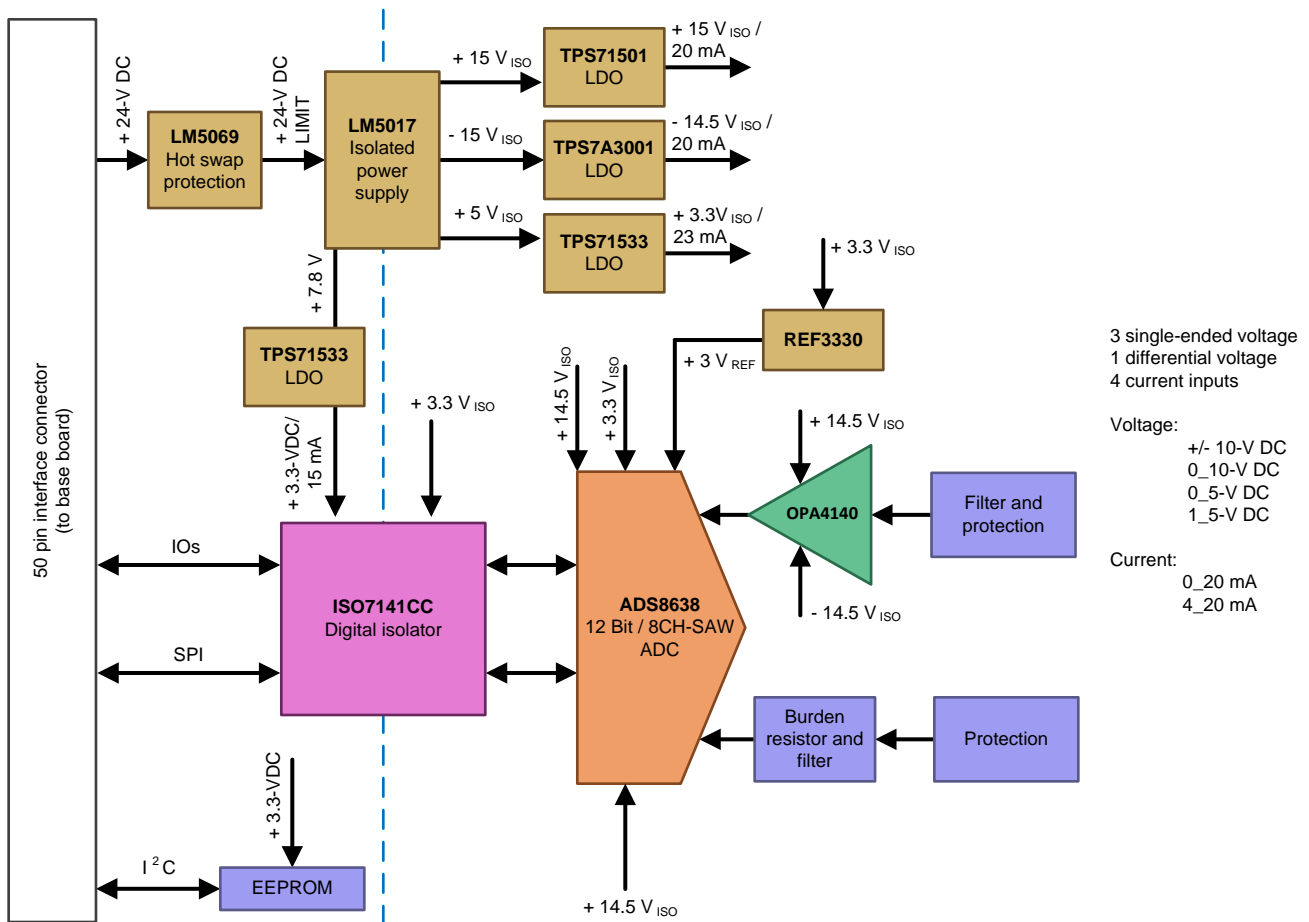


Figure 2. Analog Input Module

In IO modules, isolation is increasingly popular due to improved performance to improve the long-term reliability of the whole system. Typical bus voltage in factory automation equipment ranges from 18 V to 30 V (24 V nominal). A supply powered from the bus voltage must provide two supplies to power the controller side circuit and field side circuit.

An isolated buck converter (Fly-Buck™) uses a synchronous buck converter with coupled inductor windings to create isolated outputs. Isolated converters utilizing Fly-Buck topology use a smaller transformer for an equivalent power transfer, as the transformer primary and secondary turns ratios are better matched. The requirement for an optocoupler or auxiliary winding is unnecessary as the secondary output closely tracks the primary output voltage, resulting in smaller solution size and cost.

2 Design Specification and Features

The TIDA-00400 reference design has the following specifications.

Electrical specifications:

V_{IN}	18 to 30-V DC
V_{OUT1}	+15 V \pm 10% at 30 mA
V_{OUT2}	-15 V \pm 10% at 30 mA
V_{OUT3}	+5 V with 40 mA
Non-isolated output	+3.3 V \pm 10% at 35 mA to 50 mA
P_{OUT} is approximately	1 W
Total solution height	\leq 8 mm
Designed for IEC 61010-1 compliance (test voltage: 860-V AC)	

3 System Block Diagram

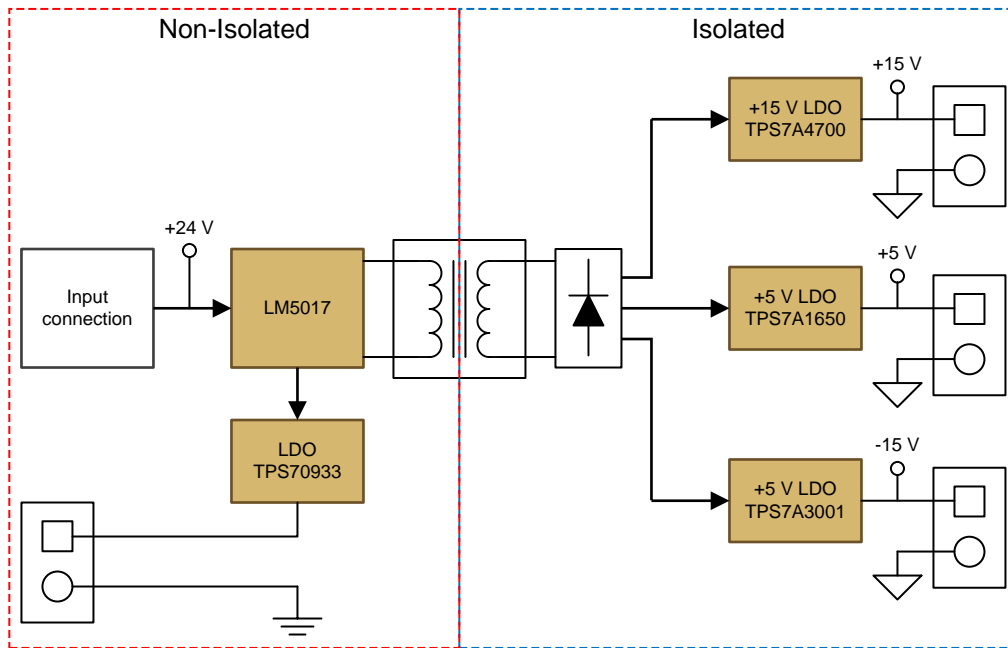


Figure 3. Top Level Block Diagram

4 Fly-Buck Converter Working

An isolated buck converter, also known as a Fly-Buck converter, is created by replacing the output filter inductor (L1) in a synchronous buck converter with a coupled inductor (X1) or flyback-type transformer, and rectifying the secondary winding voltage using a diode (D1) and a capacitor (C_{OUT2}). The topology can be extended to any number of isolated secondary outputs and can also be used to generate one or more inverting outputs.

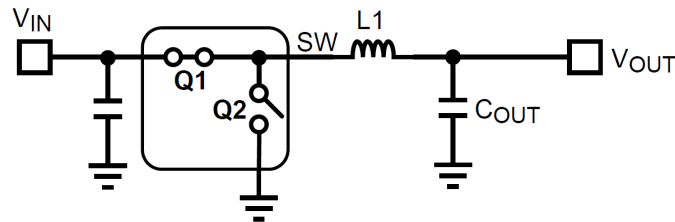


Figure 4. Synchronous Buck Converter

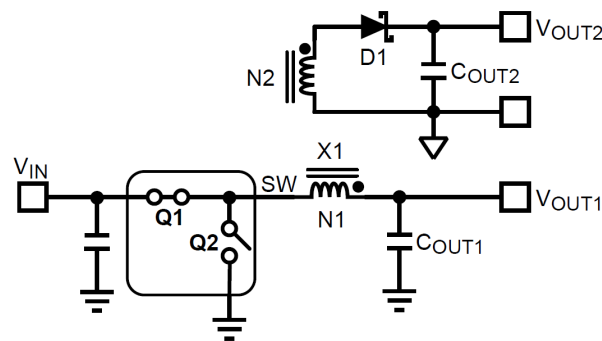


Figure 5. Isolated Buck Converter (Fly-Buck)

Creating an isolated buck converter by modifying a synchronous buck converter:

The primary output voltage equation is identical to a buck converter, which the following [Equation 1](#) shows:

$$V_{OUT1} = \frac{T_{ON}}{(T_{ON} + T_{OFF})} \times V_{IN} = D \times V_{IN} \quad (1)$$

[Equation 2](#) derives the secondary output voltage:

$$V_{OUT2} = \left(\frac{N_2}{N_1} \right) \times V_{OUT1} - V_F$$

where

- V_F is the forward voltage drop of the secondary rectifier diode,
 - N_1 is the number of turns in the primary windings,
 - N_2 is the number of turns in the secondary windings.
- (2)

The secondary output (V_{OUT2}) closely tracks the primary output voltage (V_{OUT1}) without the requirement for an additional transformer winding or an optocoupler for feedback across the isolation boundary.

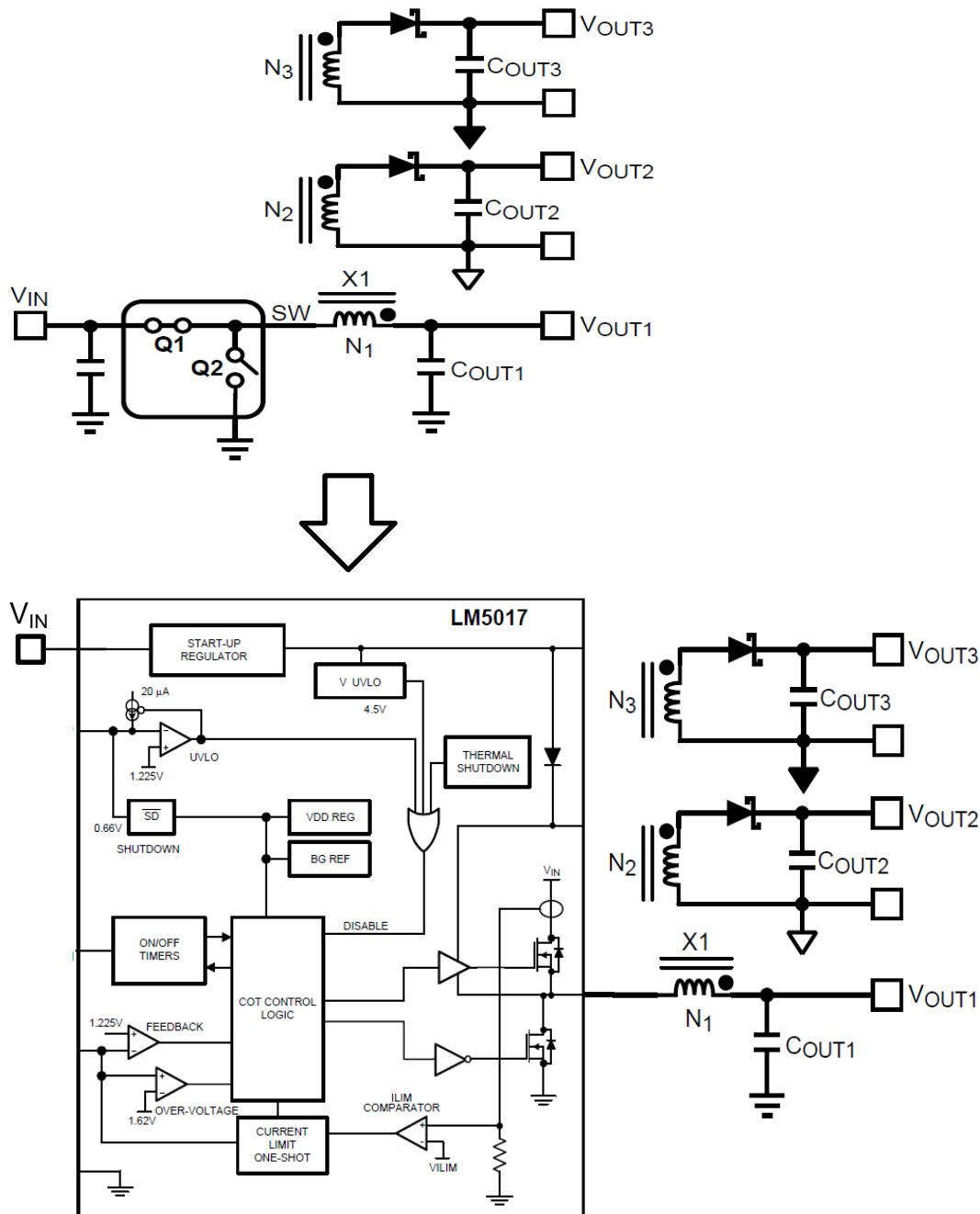


Figure 6. Simplified Overview of Fly-Buck Converter Using LM5017

In industrial systems, signals transmit from a variety of sensors to a central controller for processing and analysis. The power rails of ± 15 V, +5 V, and +3.3 V are commonly used to power up the analog-to-digital converter (ADC), digital-to-analog converter (DAC), and other signal conditioning circuitry. The LM5017 is a synchronous buck regulator with integrated MOSFET. The LM5017 is configured in Fly-Buck topology to generate non-isolated +3.3 V and isolated +5 V, +15 V, and -15 V from 24-V DC. An isolated Fly-Buck converter uses coupled inductor windings to generate isolated outputs.

5 Circuit Design and Component Selection

5.1 Fly-Buck Converter

Design specifications:

- Input voltage: 18 to 30 VDC, +24 V (nominal)
- Isolated output voltage rails:
 - +19 V, 30 mA
 - -19 V, 30 mA
 - +6.5 V, 40 mA
- Non-isolated output: +3.3 V
- Switching frequency: 1 MHz

The non-isolated output voltage ($V_{CC_NON_ISO}$) is set by two external resistors ($R1$, $R4$).

The regulated output voltage calculates as such:

$$V_{CC_NON_ISO} = 1.225 \times \left(1 + \frac{R4}{R1}\right) = 1.225 \text{ V} \times \left(1 + \frac{187 \text{ k}}{27 \text{ k}}\right) = 9.71 \text{ V} \quad (3)$$

As the LM5017 datasheet recommends, select the $C8 = 1\text{-}\mu\text{F}$, 50-V. Similarly, select the $C12 = 0.01\text{-}\mu\text{F}$, 50-V capacitor.

As [Equation 4](#) shows, the input capacitor (C_{IN}) must be large enough to limit the input voltage ripple

$$C_{IN} \geq \frac{I_{OUT(MAX)}}{4 \times f \times \Delta V_{IN}} \quad (4)$$

Choosing a $\Delta V_{IN} = 0.5 \text{ V}$ results in a minimum $C_{IN} = 0.125 \mu\text{F}$. Select a standard value of $0.22 \mu\text{F}$ is selected. A larger bulk capacitor is usually required to suppress inductive spikes in the input voltage; select a $2.2 \mu\text{F}$ bulk capacitor in this case. The input capacitor must be rated for the maximum input voltage under all conditions.

Calculate the operating frequency can be calculated as the following [Equation 5](#):

$$F_{SW} = \frac{V_{OUT}}{10^{-10} \times R_{ON}}$$

$$R_{ON} = \frac{10 \text{ V}}{10^{-10} \times 1 \text{ MHz}} \quad (5)$$

Under voltage lockout (UVLO) resistors $RFB1$ and $RFB2$ set the UVLO threshold and hysteresis according to the following relationship in [Equation 6](#) and [Equation 7](#):

$$V_{IN_HYS} = I_{HYS} \times R_{UV2} \quad (6)$$

and

$$V_{IN_UVLO} = 1.225 \text{ V} \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right)$$

where:

- $I_{HYS} = 20 \mu\text{A}$ (7)

Setting a UVLO hysteresis of 1.2 V and UVLO rising threshold of 17 V results in $R_{UV1} = 4.87 \text{ k}\Omega$ and $R_{UV2} = 60.4 \text{ k}\Omega$.

A coupled inductor or a Fly-Buck type transformer is required for this topology. Energy is transferred from primary to secondary when the synchronous switch of the buck is ON. Using the following Equation 8 for the peak inductor current, the maximum inductor current ripple that can be tolerated is given by:

$$i_{L_peak} = I_{OUT1} + \left(\frac{N2}{N1}\right)I_{OUT2} + \left(\frac{N3}{N1}\right)I_{OUT3} + \left(\frac{\Delta I_{L1}}{2}\right)$$

$$\Delta I_{L1} = 2 \times \left(i_{L_peak} - I_{OUT1} - \left(\frac{N2}{N1}\right)I_{OUT2} - \left(\frac{N3}{N1}\right)I_{OUT3} \right)$$

$$\Delta I_{L1} = 2 \times (0 - 0.050 - 0.058 - 0.136)$$

$$\Delta I_{L1} = 2 \times (0.329 - 0.050 - 0.058 - 0.135)$$

$$\Delta I_{L1} = 0.172 \text{ A}$$

where

$$i_{L1_peak} = I_{OUT} + \frac{\Delta I_{LMAX}}{2}$$

$$i_{L1_peak} = 329 \text{ mA}$$

$$L1 = \left(\frac{V_{IN_MAX} - V_{OUT}}{\Delta I_{L1} \times f_{SW}} \right) \times \left(\frac{V_{OUT}}{V_{IN_MAX}} \right)$$

$$L1 = \left(\frac{30 \text{ V} - 9.91 \text{ V}}{0.172 \text{ A} \times 960 \text{ kHz}} \right) \times \left(\frac{9.91 \text{ V}}{30 \text{ V}} \right)$$

$$L1 = 40.19 \text{ } \mu\text{H}$$

A higher value for primary inductance maintains the high-side switch current below the minimum peak current limit. For this design, a 50- μH value is selected for the primary inductance. For this chosen primary inductance, the primary inductor current ripple during T_{ON} is:

$$\Delta I_{L1} = \left(\frac{V_{IN_MAX} - V_{OUT}}{L_1 \times f_{SW}} \right) \times \left(\frac{V_{OUT}}{V_{IN_MAX}} \right)$$

$$\Delta I_{L1} = \left(\frac{30 \text{ V} - 9.91 \text{ V}}{50 \text{ } \mu\text{H} \times 960 \text{ kHz}} \right) \times \left(\frac{9.91 \text{ V}}{30 \text{ V}} \right)$$

$$\Delta I_{L1} = 0.138 \text{ A}$$

(10)

Select a 1:1.935 and 1.55:1 turns ratio for the windings:

$$V_{OUT2} = \left(\frac{N2}{N1}\right) \times V_{OUT1}$$

$$V_{OUT2} = 1.935 \times 9.91 \text{ V}$$

$$V_{OUT2} = +19.17 \text{ V}$$

similarly,

$$V_{OUT3} = -19.17 \text{ V} \tag{11}$$

and,

$$V_{OUT4} = +6.4 \text{ V} \tag{12}$$

(13)

For the rectifier diode, the voltage across the secondary diodes calculates to:

$$V_{D2,3} = \left(\frac{N2}{N1}\right) V_{IN}$$

$$V_{D2,3} = 58.05 \text{ V}$$

$$V_{D4} = 20 \text{ V} \tag{14}$$

(14)

After considering safety margin, footprint, availability, and cost, the DFLS1200-7 Schottky diode was selected for a ± 19 -V winding and the PMEG6010CEH,115 Schottky diode was selected for a +6.4-V winding.

C_{OUT1} is calculated as:

$$\Delta V_{OUT} = \frac{\Delta I_{L1}}{8 \times f \times C_{OUT1}}$$

$$C_{OUT1} = \frac{\Delta I_{L1}}{8 \times f \times \Delta V_{OUT}}$$

$$C_{OUT1} \cong 1 \mu\text{H} \tag{15}$$

(15)

The $V_{CC_NON_ISO}$ supplies the TPS70933DBVT low-dropout (LDO) that generates the +3.3V_NON_ISO and is capable of delivering 20 mA of output current. The +3.3V_NON_ISO powers an electrically erasable programmable read-only memory (EEPROM) and two digital isolators.

Selection of rectifier diode D2:

The following [Equation 16](#) shows the reverse bias voltage across D2 when the high-side buck switch is on:

$$V_{D2} = \left(\frac{N_{sec}}{N_{pri}}\right) \times V_{IN_MAX} = \left(\frac{1}{1.55}\right) \times 35 = 23 \text{ V} \tag{16}$$

(16)

With safety margins under consideration, the peak inverse voltage (PIV) of the secondary diode should be greater than 35 V, which is why this design uses the 60-V Schottky diode PMEG6010CEH,115.

The rectified output (+V_{CC_ISO}) on the secondary side is calculated as:

$$+V_{CC_ISO_1} = \left(\left(\frac{N_{sec1}}{N_{pri1}} \right) \times V_{CC_NON_ISO} \right) - V_{FD} = 6.71 - 0.3 \text{ V} = 6.41 \text{ V}$$

$$+V_{CC_ISO_2} = \left(\left(\frac{N_{sec2}}{N_{pri}} \right) \times V_{CC_NON_ISO} \right) - V_{FD} = 13.1 - 0.5 \text{ V} = 12.51 \text{ V} \tag{17}$$

Refer to the LM5017 datasheet for instructions regarding device operation and the SNVA674 application note “AN-2292 - Designing an Isolated Buck (Flyback) Converter” [1] for Fly-Buck converter design procedure and recommended printed circuit board (PCB) layout guidelines.

5.1.1 Non-Isolated +3.3 V

The TPS709xx are a series of devices that belong to a new family of next-generation voltage regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. This performance, combined with low noise, very good power supply rejection ratio (PSRR) with little (V_{IN} – V_{OUT}) headroom, makes these devices ideal for radio frequency (RF) portable applications, current limit, and thermal protection. The TPS709xx are specified from –40°C to +125°C.

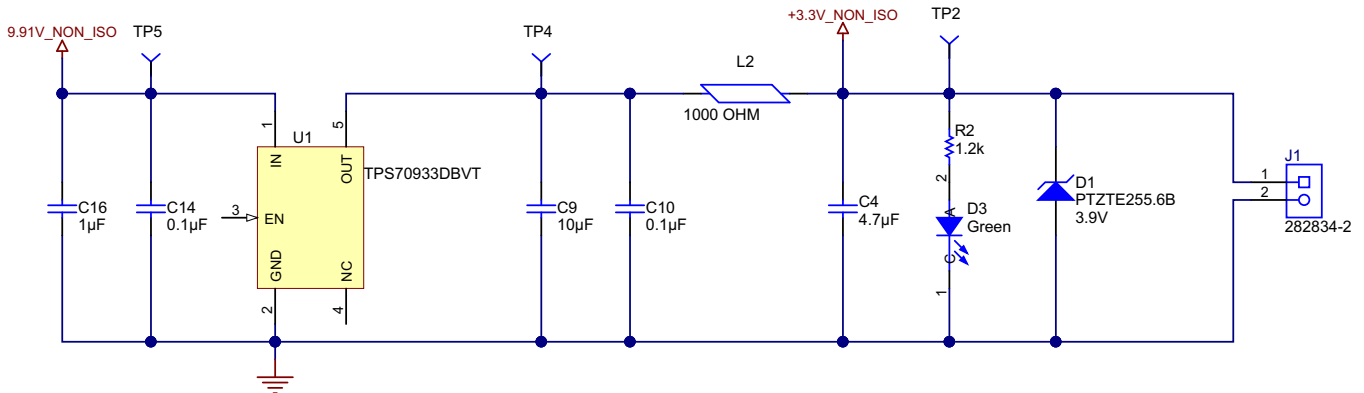


Figure 7. Non-Isolated +3.3-V LDO

Design considerations for TPS70933:

Table 1. Design Specification and Key Design Parameters for TPS70933

SR. NO.	DESIGN SPECIFICATIONS AND KEY PARAMETERS	
1	Input Voltage Range (V _{IN})	9.91-V DC
2	Output Voltage (V _{OUT})	+3.3 V (fixed)
3	Output current (I _{OUT})	50 mA
4	V _{DO}	200 mV to 300 mV at 50 mA
5	Thermal shutdown at	+165°C
6	T _{J_MAX}	+150°C
7	θ _{JA} Junction-to-ambient thermal resistance	212.1°C/W

Input and output capacitors:

The TPS709xx devices are stable with output capacitors with the minimum capacitance of 1.5 μF for output voltages equal or greater than 1.5 V. The equivalent series resistance (ESR) of the output capacitor must be between 0 Ω and 0.2 Ω for stability. The effective capacitance is the minimum capacitance value of a capacitor after taking into account variations resulting from tolerances, temperature, and DC bias effects. TI recommends X5R or X7R-type ceramic capacitors for design because these capacitors have minimal variation in value and ESR over temperature. A 10- μF , 16-V X5R output capacitor is selected to satisfy the minimum output capacitance requirement with a 3.3-V DC.

Although an input capacitor is not required for stability, good design practice is to connect a 0.1- μF capacitor and a bulk capacitor of 1- μF capacitor from INPUT to GND. These capacitors counteract reactive input source and improve transient response, input ripple, and PSRR.

Thermal protection:

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating. The TPS70933 internal protection circuitry is designed to protect against accidental overload conditions.

Power dissipation:

$$\text{Power Dissipation, PD} = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{mA}}$$

$$= (9.91 - 3.3) \times 50 \text{ mA}$$

$$= 331 \text{ mW}$$

$$T_{\text{J}} = T_{\text{A_MAX}} + (\theta_{\text{JA}} \times \text{PD})$$

$$= 70 + (212.1 \times 330 \text{ mW})$$

$$= 139^\circ\text{C}$$

$T_{\text{J}} < T_{\text{J IC}}$, which means there is no required heatsink for the TPS70933 device. (18)

The PCB thermal pads and area around the device that is free of other components move the heat from the device to ambient air. The copper plane and plated through-holes are used for the power connections to increase the effectiveness in removing heat from the TPS70933.

Refer to the TPS709xx datasheet for instructions regarding device operation and recommended PCB layout guidelines.

5.2 Post Isolated Regulators

5.2.1 +5-V Regulator

An isolated 5 V is generated using the TPS7A1650 linear regulator. The TPS7A1650 is an ultra-low power, LDO voltage regulator, which offers the benefits of ultra-low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging.

The TPS7A1650 offers an enable pin (EN) compatible with standard CMOS logic and an integrated, open-drain, active-high, power-good (PG) output with a user-programmable delay. These pins are intended for use in microcontroller-based, battery-powered applications where power rail sequencing is required. The EN pin is connected to the V_{IN} pin.

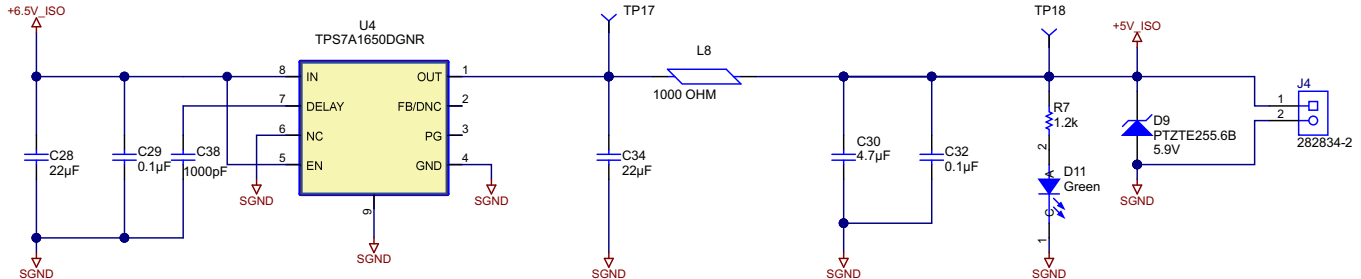


Figure 8. Isolated +5-V LDO

Design considerations for TPS7A1650:

Table 2. Design Specification and Key Design Parameters for TPS7A1650

SR. NO.	DESIGN SPECIFICATIONS AND KEY PARAMETERS	
1	Input Voltage Range (V_{IN})	6.5-V DC
2	Output Voltage (V_{OUT})	5 V (fixed)
3	Output current (I_{OUT})	40 mA
4	V_{DO}	200 mV to 300 mV at 50 mA
5	Thermal shutdown at	+170°C
6	T_{J_MAX}	+125°C
7	θ_{JA} Junction-to-ambient thermal resistance	66.2°C/W

Input and output capacitors:

The TPS7A16 family of linear regulators achieve stability with a minimum input capacitance of 0.1 μ F and an output capacitance of 2.2 μ F. The 22- μ F, X5R ceramic capacitor is connected to maximize AC performance and to achieve better stability over temperature.

An input capacitor is necessary if line transients are anticipated. In this design a 22- μ F capacitor is connected at the input. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR.

Thermal protection:

Thermal protection in the TPS7A1650 disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool. When the junction temperature cools to approximately +150°C, the output circuitry is again enabled.

Power dissipation:

$$\text{Power dissipation, } PD = (V_{IN} - V_{OUT}) \times I_{OUT}$$

$$= (6.5 - 5) \times 50 \text{ mA} = 75 \text{ mW}$$

$$T_J = T_{A_MAX} + (\theta_{JA} \times PD)$$

$$= 70 + (66.2 \times 75 \text{ mW}) = 74.97^\circ\text{C}$$

$T_J < T_J \text{ IC}$, which means there is no required heatsink for the TPS7A1650 device. (19)

Refer to the TPS7A1650 datasheet for instructions regarding device operation and recommended PCB layout guidelines.

5.2.2 +15-V Regulator

Notable features of the TPS7A4700 LDO include thermal and current limit shutdown protection, pin selectable output voltage, low dropout, and low noise (approximately $3.5 \mu\text{V}$ per $\sqrt{\text{Hz}}$). These features are critical to maximize system performance of operational amplifiers, ADCs, DACs, and other high-performance analog circuitry in critical applications such as high performance IO modules, medical, radio frequency (RF), and test-and-measurement. Output voltage is user-programmable (up to 20.5 V) using a PCB layout without the requirement of external resistors or feed-forward capacitors, which reduces the overall component count. The TPS7A4700 has a wide input voltage range from +3 V to 35 V. The TPS7A4700 device is capable of delivering up to 1 A to a dynamic load across the full recommended input and output voltage range of the LDO.

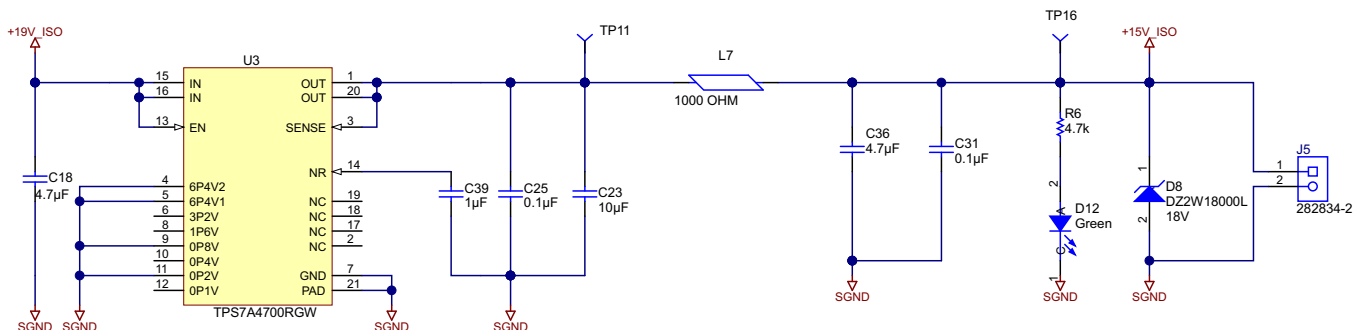


Figure 9. Isolated +15-V LDO

Design considerations for TPS7A4700:

Table 3. Design Specification and Key Design Parameters for TPS4700

SR. NO.	DESIGN SPECIFICATIONS AND KEY PARAMETERS	
1	Input Voltage Range (V_{IN})	+19-V DC
2	Output Voltage (V_{OUT})	+15 V (fixed)
3	Output current (I_{OUT})	30 mA
4	V_{DO}	450 mV
5	Thermal shutdown at	+170°C
6	T_{J_MAX}	+150°C
7	θ_{JA} Junction-to-ambient thermal resistance	32.5°C/W

Input and output capacitors:

Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended for the TPS7A4700 device. TI recommends to apply a 50% derating of the nominal capacitance in the design. The 4.7- μ F bulk input and 10- μ F output capacitors are used for better transient load response and have no detrimental influence on the stability of the device.

Noise reduction capacitor:

The noise reduction capacitor (connected to the NR pin of the TPS7A4700 device), forms an RC filter for filtering out noise that the control loop might ordinarily amplify and appear on the output voltage. Larger capacitances, such as 1 μ F, affect noise reduction at lower frequencies and also tend to further reduce noise at higher frequencies.

Thermal protection:

The TPS7A4700 device contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the main pass-FET exceeds 170°C (typical). Thermal shutdown hysteresis assures that the TPS7A4700 resets (turns on) when the temperature falls to 150°C (typical).

Power dissipation:

$$\text{Power Dissipation, PD} = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{OUT}}$$

$$= (19 - 15) \times 30 \text{ mA}$$

$$= 120 \text{ mW}$$

$$T_J = T_{\text{A_MAX}} + (\theta_{\text{JA}} \times \text{PD})$$

$$= 70 + (32.5 \times 120 \text{ mW})$$

$$= 73.9^\circ\text{C}$$

$T_J < T_J \text{ IC}$, which means there is no required heatsink for the TPS7A1650 device. (20)

Refer to the TPS7A4700 datasheet for instructions regarding device operation and recommended PCB layout guidelines.

5.2.3 -15-V Regulator

One of the primary TPS7A3001 applications is to provide ultralow noise voltage rails to high-performance analog circuitry to maximize system accuracy and precision.

The TPS7A4700 family of positive high-voltage linear regulators, in conjunction with its positive counterpart (the TPS7A3001 family of negative high voltage linear regulators), provides ultralow noise, positive and negative voltage rails for high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic of the TPS7A3001 allows for high-performance analog solutions to optimize the voltage range and maximize system accuracy.

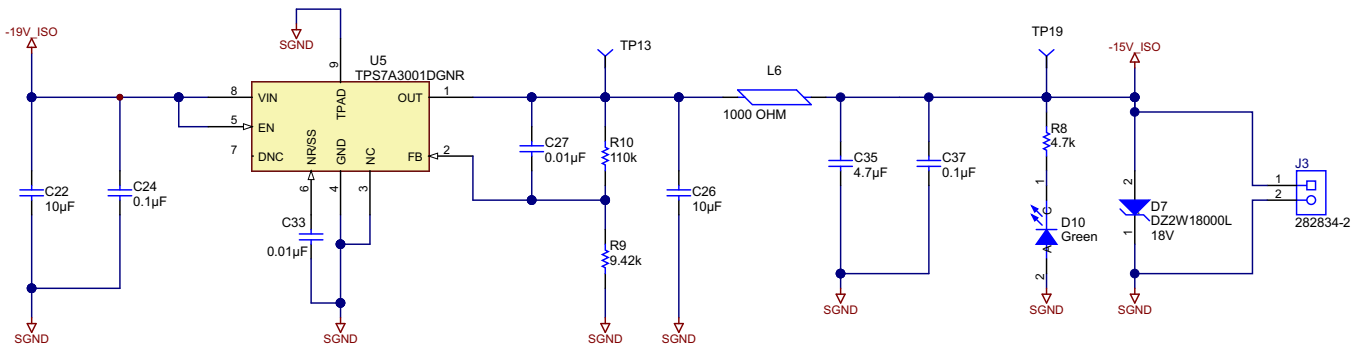


Figure 10. Isolated -15-V LDO

Design considerations for the TPS7A3001:

Table 4. Design Specification and Key Design Parameters for TPS7A3001

SR. NO.	DESIGN SPECIFICATIONS AND KEY PARAMETERS	
1	Input Voltage Range (V_{IN})	-19-V DC
2	Output Voltage (V_{OUT})	-15 V (fixed)
3	Output current (I_{OUT})	30 mA
4	V_{DO}	150 mV
5	Thermal shutdown at	+170°C
6	T_{J_MAX}	+150°C
7	θ_{JA} Junction-to-ambient thermal resistance	55.09°C/W

Input and output capacitors:

The TPS7A3001 device achieves stability with a minimum input and output capacitance of 2.2 μF ; however, TI highly recommends using a 10- μF capacitor to maximize the AC performance.

Noise reduction capacitor:

The TPS7A3001 datasheet recommends using a 0.01- μF capacitor noise reduction (between $C_{NR/SS}$ and GND) and a bypass capacitor (from the FB pin to the OUT pin) to minimize noise and maximize the AC performance.

The noise reduction capacitor serves as a filter for the internal reference. By using a 0.01- μF noise reduction capacitor, the output noise is reduced by almost 80%. This capacitor greatly improves PSRR at lower frequencies for the band from 10 Hz to 200 kHz.

The low noise and high power supply rejection of the TPS7A3001 and TPS7A4700 devices make them a good choice for powering high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

Thermal protection:

Similar to other LDOs, the TPS7A3001 contains a thermal shutdown protection circuit that turns off the output when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the main pass-FET exceeds 170°C (typical). Thermal shutdown hysteresis assures that the TPS7A3001 resets (turns on) when the temperature falls to 150°C (typical).

Feedback resistors:

Calculate R9 and R10 for any output voltage range by using the following formula from [Equation 21](#):

$$R10 = R9 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (21)$$

Set a value for R9 = 10 kΩ:

$$R10 = 10 \text{ k} \left(\frac{15 \text{ V}}{1.179 \text{ V}} - 1 \right) \quad (22)$$

$$R10 = 117.23 \text{ k}\Omega$$

Considering standard values R9 = 9.42 kΩ and R10 = 110 kΩ:

$$V_{OUT} = \left(\frac{R10}{R9} \times V_{REF} \right) - 1$$

$$V_{OUT} = 14.98 \text{ V} \quad (23)$$

Power dissipation:

$$\text{Power Dissipation, PD} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

$$= (19 - 15) \times 30 \text{ mA}$$

$$= 120 \text{ mW}$$

$$T_J = T_{A_MAX} + (\theta_{JA} \times \text{PD})$$

$$= 70 + (55.09 \times 120 \text{ mW})$$

$$= 76.6^\circ\text{C}$$

$T_J < T_J \text{ IC}$, which means there is no required heatsink for the TPS7A3001 device. (24)

Refer to the TPS7A3001 datasheet for instructions regarding device operation and recommended PCB layout guidelines.

6 Test Results

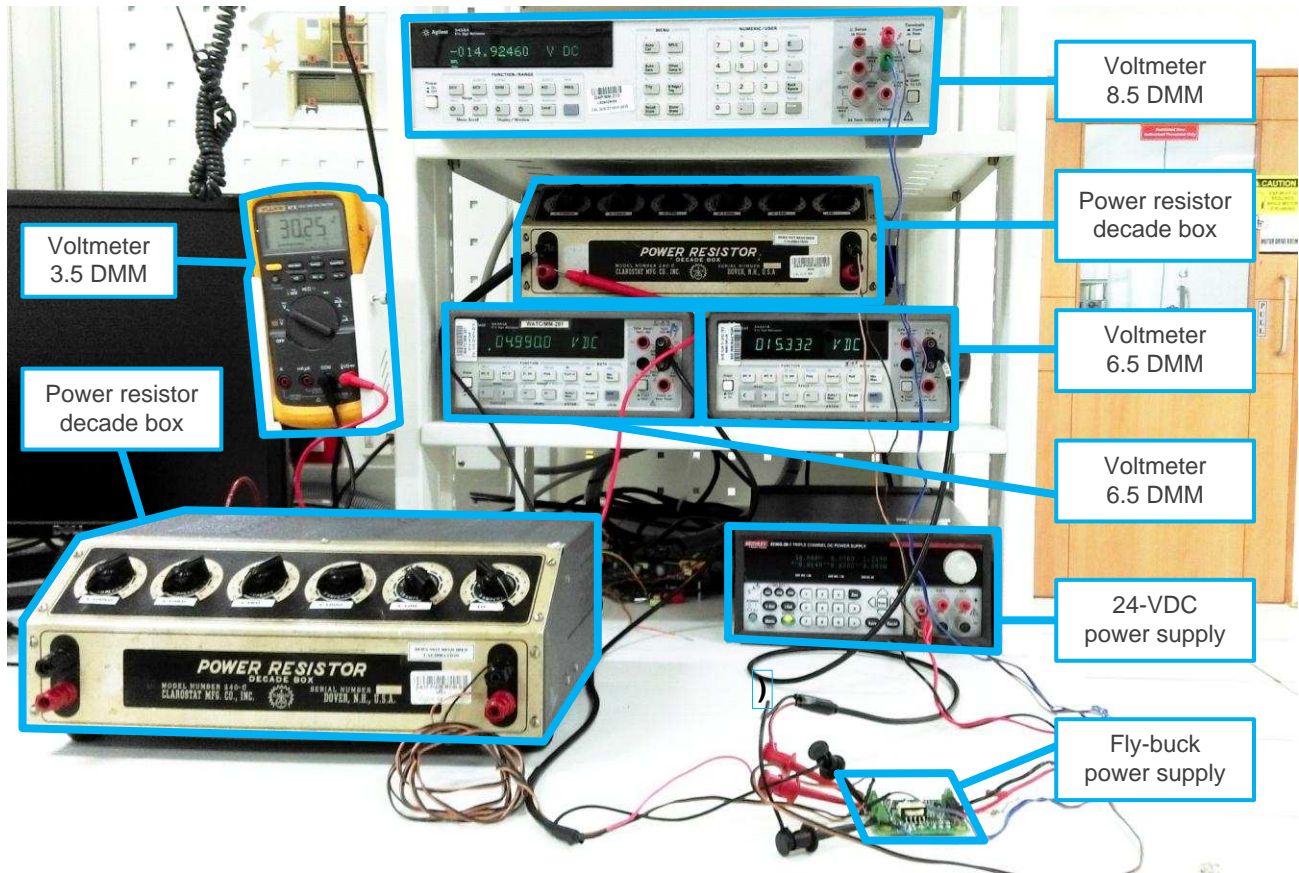


Figure 11. Test Setup

6.1 Efficiency

The efficiency is calculated for all outputs; the load current is in increments of 10% intervals, as Figure 12 shows.

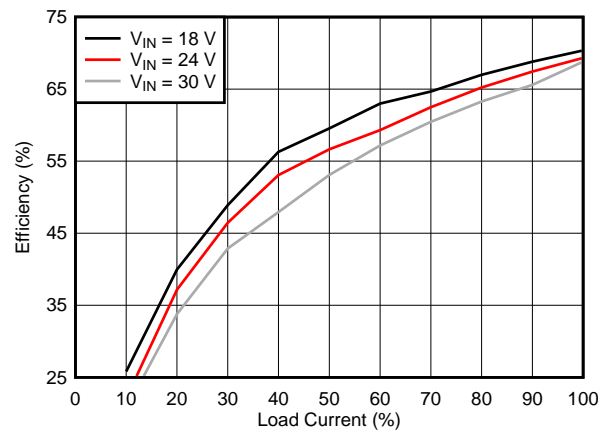


Figure 12. Efficiency Graph

V_{IN} is set to 18 V:
Table 5. Efficiency at V_{IN} = 18 V

LOAD CURRENT (%)	V _{OUT1} (V)	V _{OUT2} (V)	V _{OUT3} (V)	I _{IN} (A)	P _{IN} (W)	P _{OUT1} (W)	P _{OUT2} (W)	P _{OUT_TOTAL} (W)	EFFICIENCY
10	-14.93	4.99	15.33	0.024	0.432	0.092	0.020	0.111	25.81
20	-14.93	4.99	15.33	0.031	0.558	0.183	0.040	0.223	39.96
30	-14.93	4.99	15.33	0.038	0.684	0.275	0.060	0.334	48.89
40	-14.93	4.99	15.33	0.044	0.792	0.366	0.080	0.446	56.29
50	-14.93	4.99	15.33	0.052	0.936	0.458	0.100	0.557	59.55
60	-14.93	4.99	15.33	0.059	1.062	0.549	0.120	0.669	62.99
70	-14.93	4.99	15.33	0.067	1.206	0.641	0.139	0.780	64.67
80	-14.93	4.99	15.33	0.074	1.332	0.733	0.160	0.892	66.98
90	-14.93	4.99	15.33	0.081	1.458	0.824	0.179	1.003	68.81
100	-14.93	4.99	15.33	0.088	1.584	0.916	0.199	1.115	70.38

V_{IN} is set to 24 V:
Table 6. Efficiency at V_{IN} = 24 V

LOAD CURRENT (%)	V _{OUT1} (V)	V _{OUT2} (V)	V _{OUT3} (V)	I _{IN} (A)	P _{IN} (W)	P _{OUT1} (W)	P _{OUT2} (W)	P _{OUT_TOTAL} (W)	EFFICIENCY
10	-14.93	4.99	15.33	0.021	0.504	0.091567	0.01992	0.111	22.12
20	-14.93	4.99	15.33	0.025	0.6	0.183134	0.03984	0.223	37.16
30	-14.93	4.99	15.33	0.03	0.72	0.274728	0.059712	0.334	46.45
40	-14.93	4.99	15.33	0.035	0.84	0.366267	0.079553	0.446	53.07
50	-14.93	4.99	15.33	0.041	0.984	0.457834	0.0996	0.557	56.65
60	-14.93	4.99	15.33	0.047	1.128	0.549291	0.119712	0.669	59.31
70	-14.93	4.99	15.33	0.052	1.248	0.640775	0.139107	0.780	62.49
80	-14.93	4.99	15.33	0.057	1.368	0.732534	0.159616	0.892	65.22
90	-14.93	4.99	15.33	0.062	1.488	0.824183	0.179137	1.003	67.43
100	-14.93	4.99	15.33	0.067	1.608	0.915668	0.199201	1.115	69.33

V_{IN} is set to 30 V:
Table 7. Efficiency at V_{IN} = 30 V

LOAD CURRENT (%)	V _{OUT1} (V)	V _{OUT2} (V)	V _{OUT3} (V)	I _{IN} (A)	P _{IN} (W)	P _{OUT1} (W)	P _{OUT2} (W)	P _{OUT_TOTAL} (W)	EFFICIENCY
10	-14.93	4.99	15.33	0.018	0.54	0.091567	0.01992	0.111	20.65
20	-14.93	4.99	15.33	0.022	0.66	0.183134	0.03984	0.223	33.78
30	-14.93	4.99	15.33	0.026	0.78	0.274728	0.059712	0.334	42.88
40	-14.93	4.99	15.33	0.031	0.93	0.366267	0.079553	0.446	47.94
50	-14.93	4.99	15.33	0.035	1.05	0.457834	0.0996	0.557	53.09
60	-14.93	4.99	15.33	0.039	1.17	0.549291	0.119712	0.669	57.18
70	-14.93	4.99	15.33	0.043	1.29	0.640775	0.139107	0.780	60.46
80	-14.93	4.99	15.33	0.047	1.41	0.732534	0.159616	0.892	63.27
90	-14.93	4.99	15.33	0.051	1.53	0.824183	0.179137	1.003	65.58
100	-14.93	4.99	15.33	0.054	1.62	0.915668	0.199201	1.115	68.82

6.2 Ripple

Ripple on +15 V:

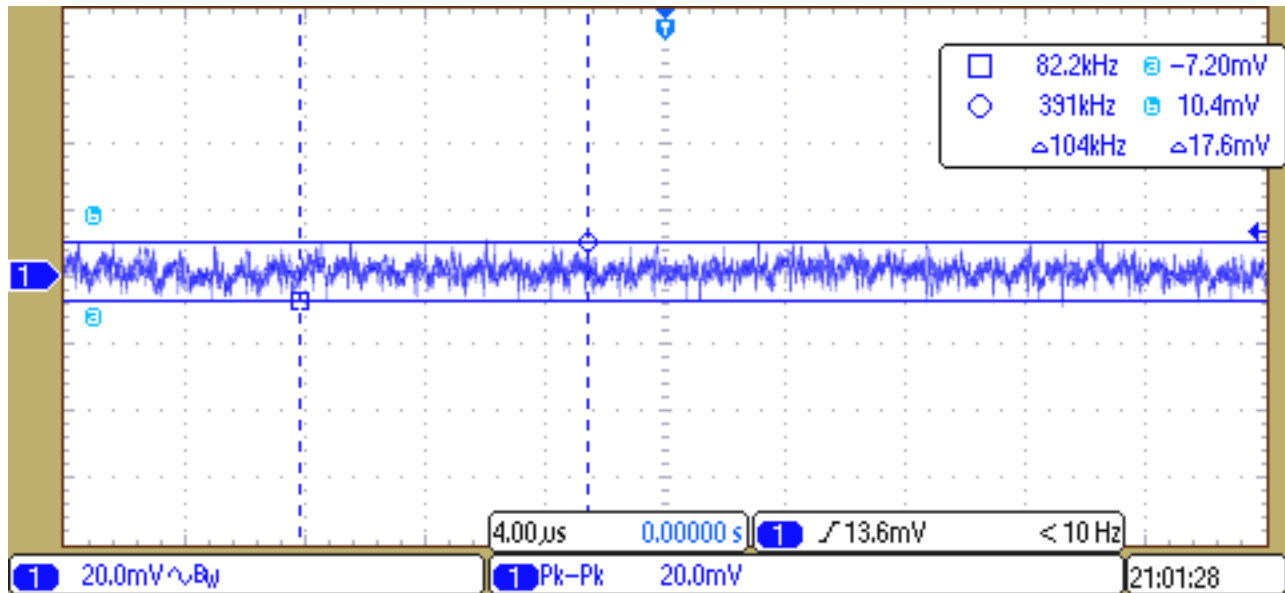


Figure 13. Isolated +15-V Ripple

Ripple on -15 V:

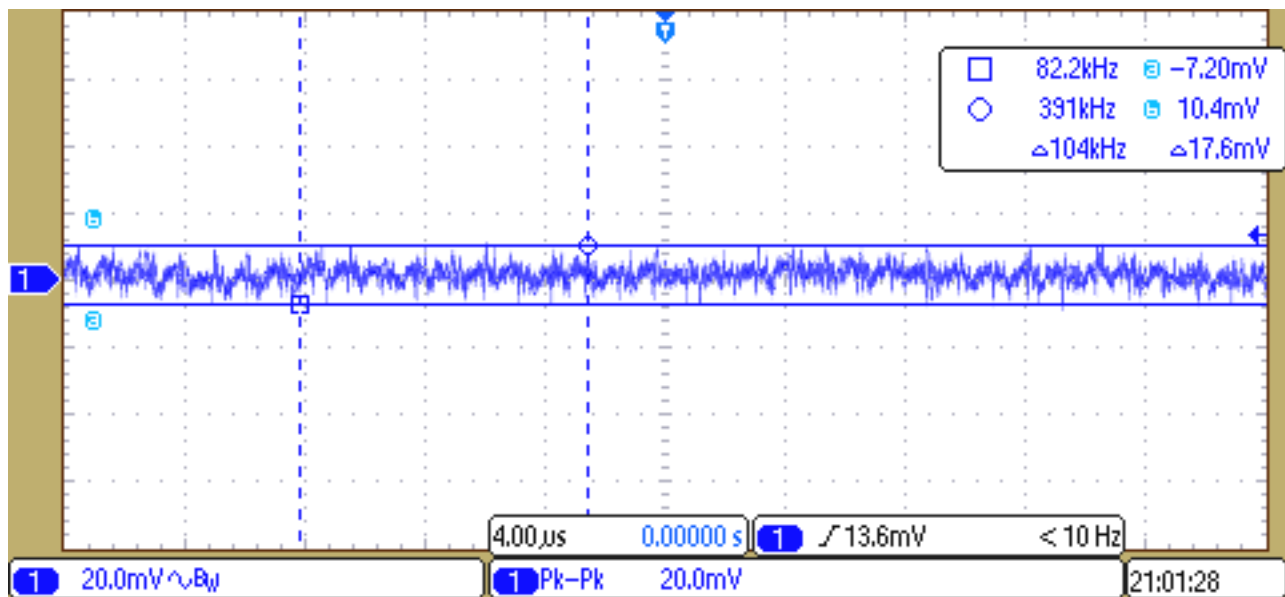


Figure 14. Isolated -15-V Ripple

Ripple on +5 V:

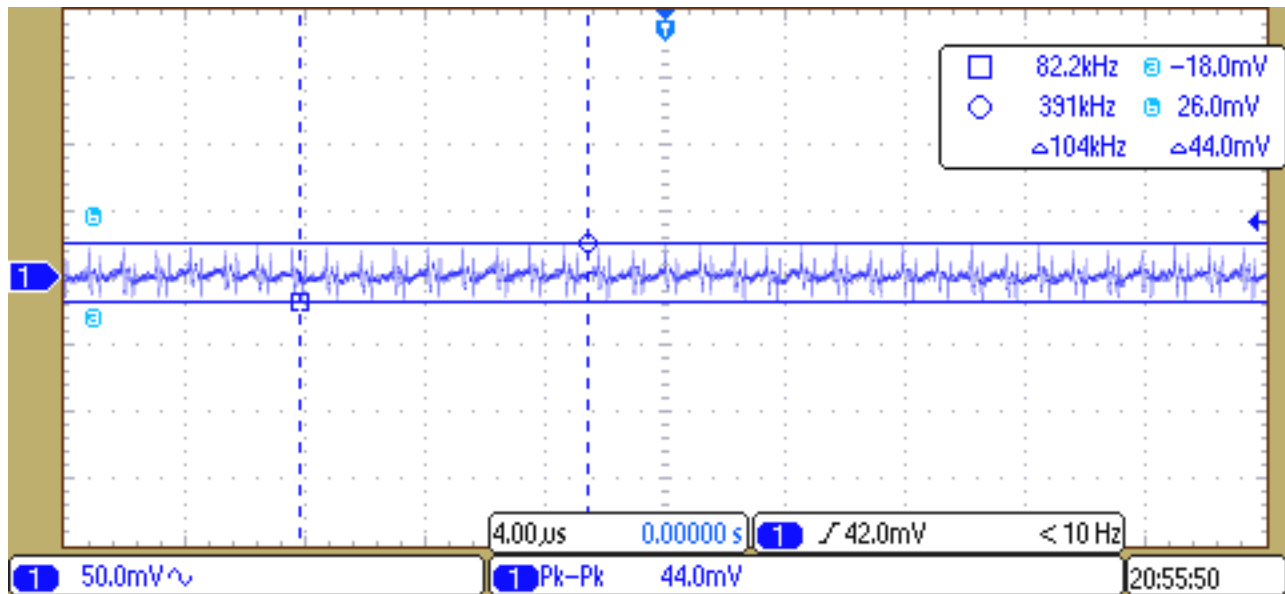


Figure 15. Isolated +5-V Ripple

6.3 Line Regulation

Each output rail is loaded with 100% load current and input voltage is varied from 18- to 30-V DC.

Table 8. Line Regulation

V _{IN}	VARIABLE		NOTE	
IL1_PRIM	0.05	3.3 V	Non-isolated 3.3 V	
IL1	0.03	-15 V	Isolated -15 V	
IL2	0.04	5 V	Isolated +5 V	
IL3	0.03	15 V	Isolated +15 V	
V _{IN} (V)	V _{OUT1_PRIM} (V)	V _{OUT1} (V)	V _{OUT2} (V)	V _{OUT3} (V)
18	3.274	-14.92	4.99	15.33
19	3.274	-14.92	4.99	15.33
20	3.274	-14.92	4.99	15.33
21	3.274	-14.92	4.99	15.33
22	3.274	-14.92	4.99	15.33
23	3.274	-14.92	4.99	15.33
24	3.273	-14.92	4.99	15.33
25	3.272	-14.92	4.99	15.33
26	3.271	-14.92	4.99	15.33
27	3.27	-14.92	4.99	15.33
28	3.26	-14.92	4.99	15.33
29	3.27	-14.92	4.99	15.33
30	3.27	-14.92	4.99	15.33

7 Design Files

7.1 Schematics

To download the schematics, see the design files at [TIDA-00400](http://www.ti.com/Design-Files/TIDA-00400).

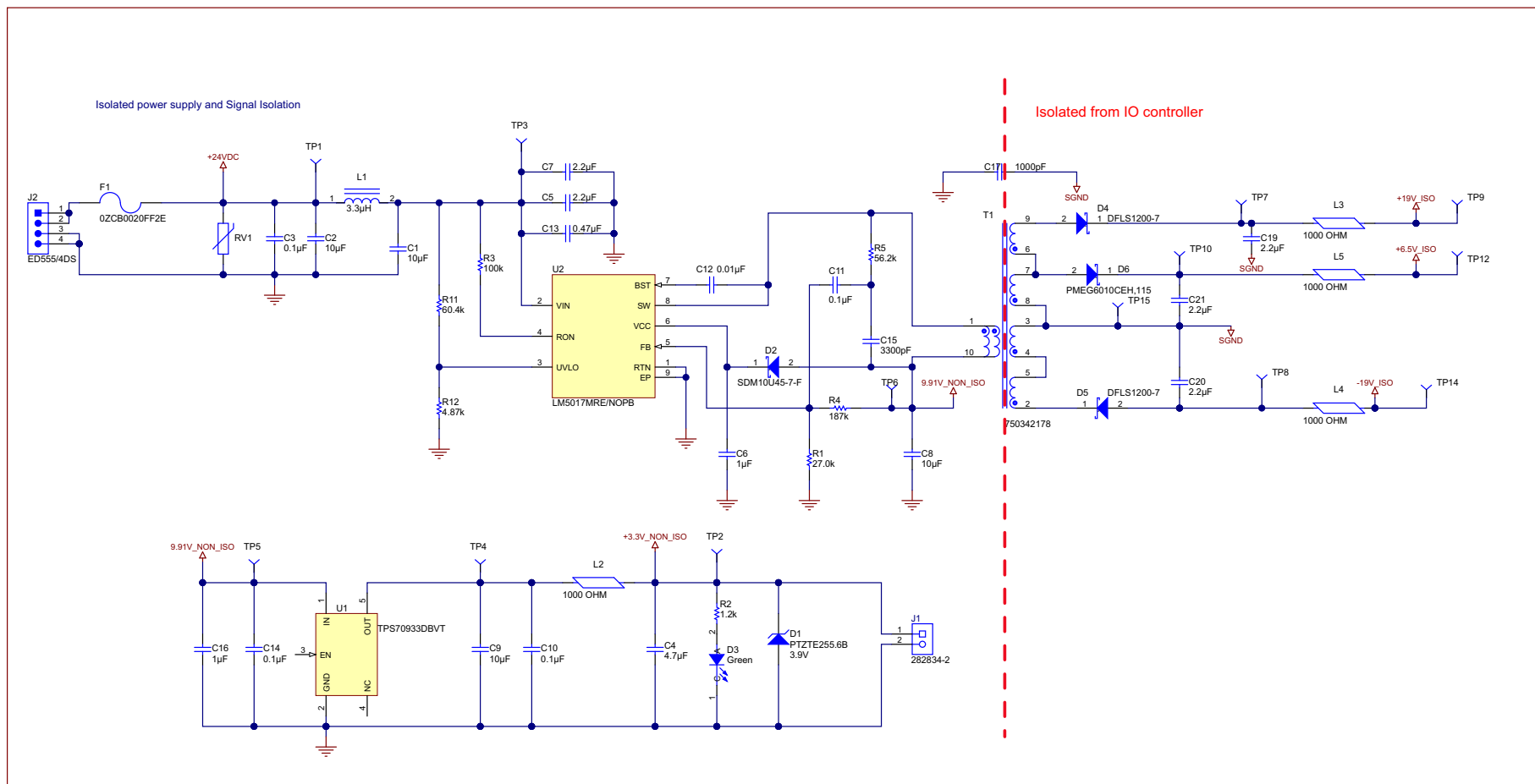


Figure 16. Fly-Buck Converter and Non-Isolated +3.3-V Regulator Schematic

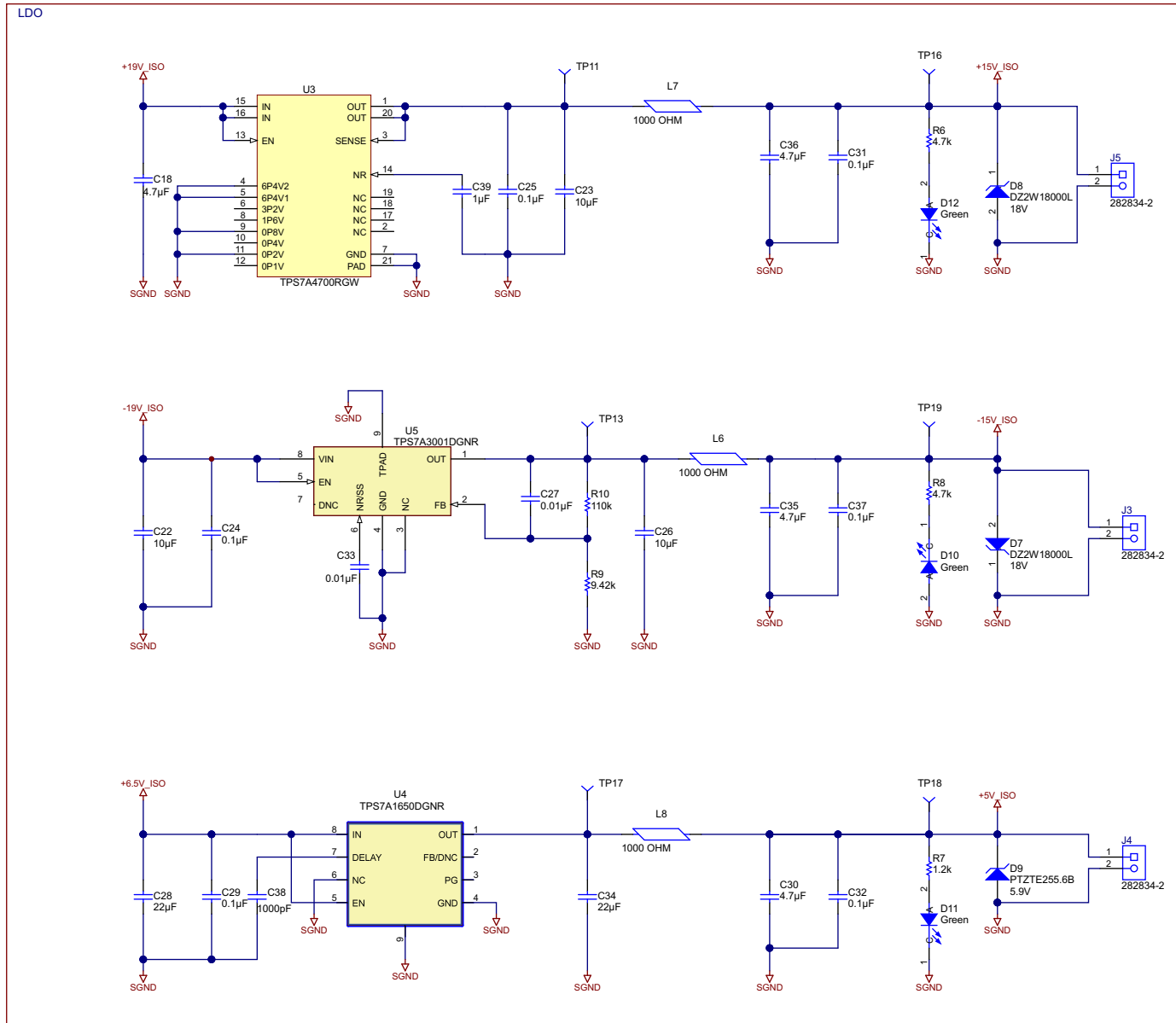


Figure 17. Post Isolation Regulator Section Schematic

7.4 Altium Project

To download the Altium project files, see the design files at [TIDA-00400](#).

7.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-00400](#).

7.6 Software Files

To download the software files, see the design files at [TIDA-00400](#).

8 References

1. Texas Instruments, *AN-2292 Designing an Isolated Buck (Fly-Buck) Converter*, Application Report, ([SNVA674](#))
2. Texas Instruments, *LM5017 Fly-Buck™ Quick Start Calculator*, Tool Resource, ([LM5017](#))

9 About the Author

AMOL GADKARI is a systems engineer at Texas Instruments India where he is responsible for developing reference design solutions for the industrial segment. Amol has eight years of experience in mixed signal board design, analog circuit designs, and EMC-protection circuit design. He can be reached at a-gadkari@ti.com.

Revision History

Changes from Original (March 2015) to A Revision	Page
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- Changed from preview page..... 1
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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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