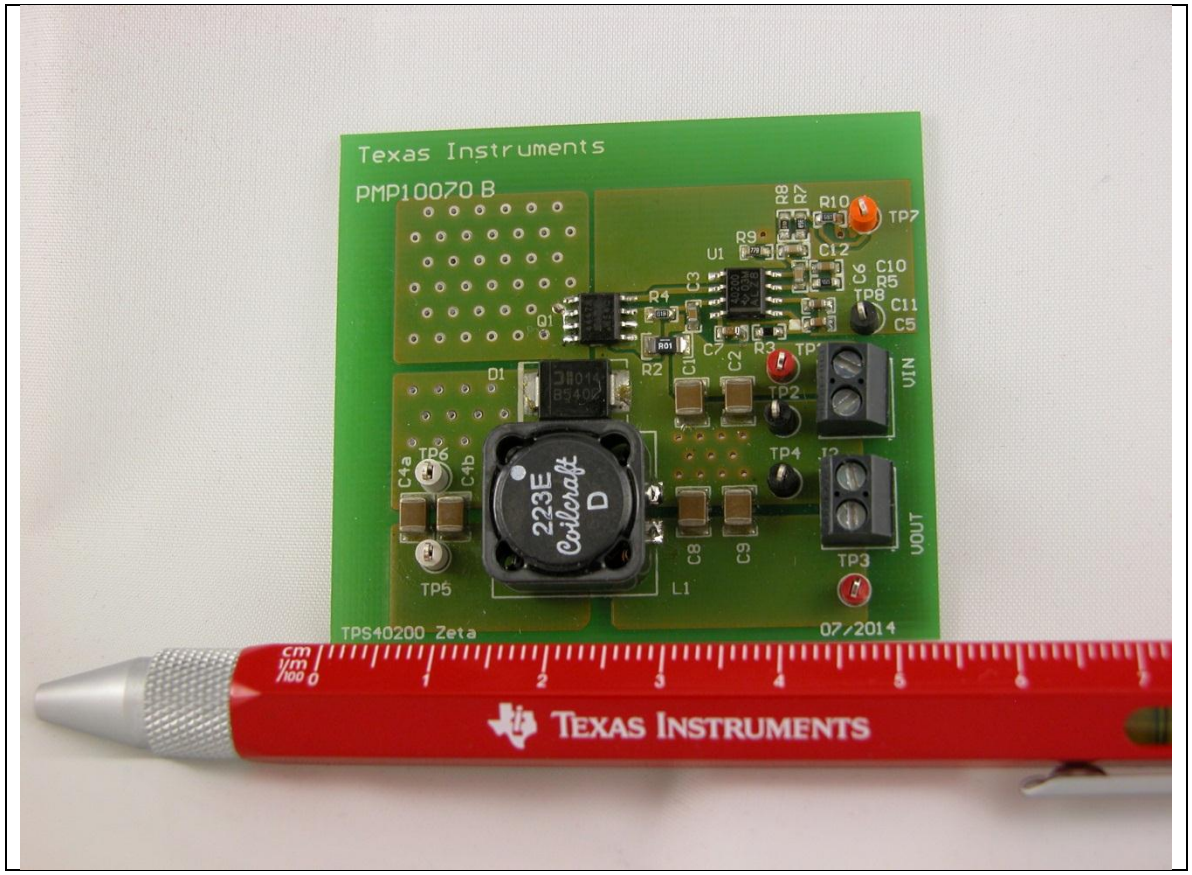
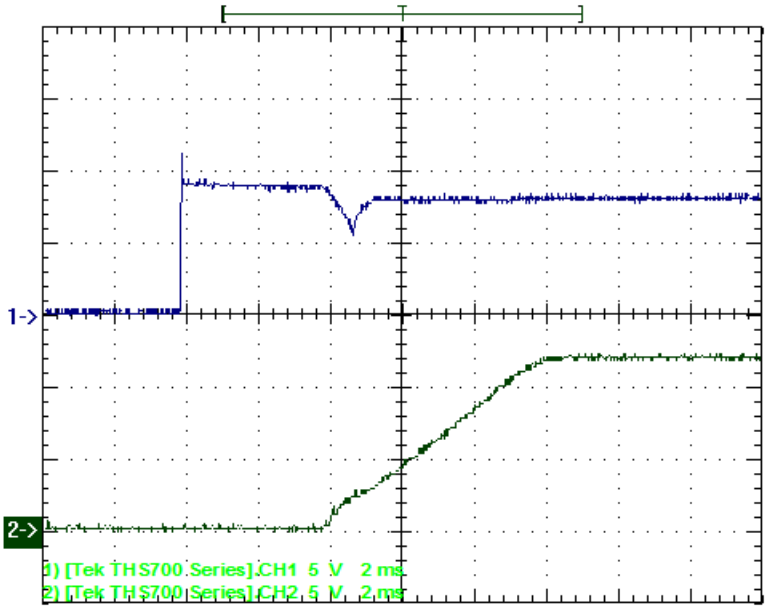
PMP10070RevB Test Results

Topology: ZETA
Device: TPS40200



1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 8V, with 1.5A load at the output.



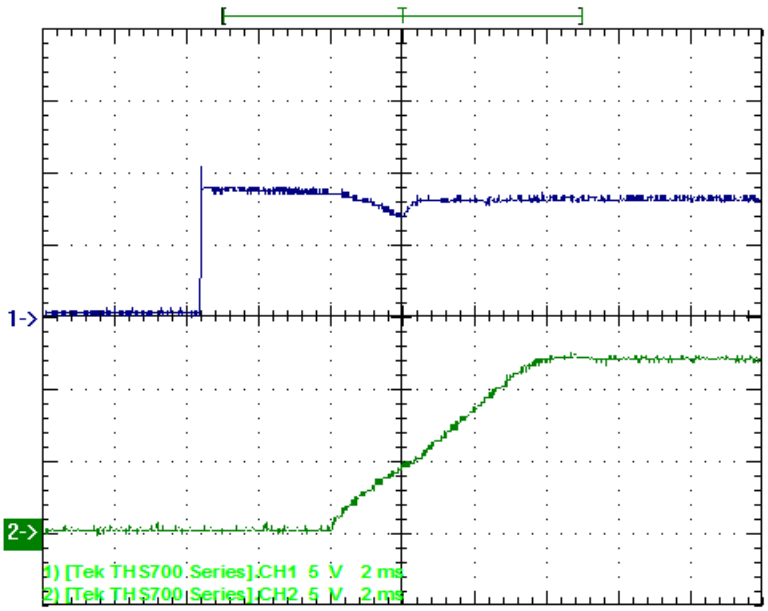
Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

2ms/div

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set at 8V, with 0.1A load at the output.



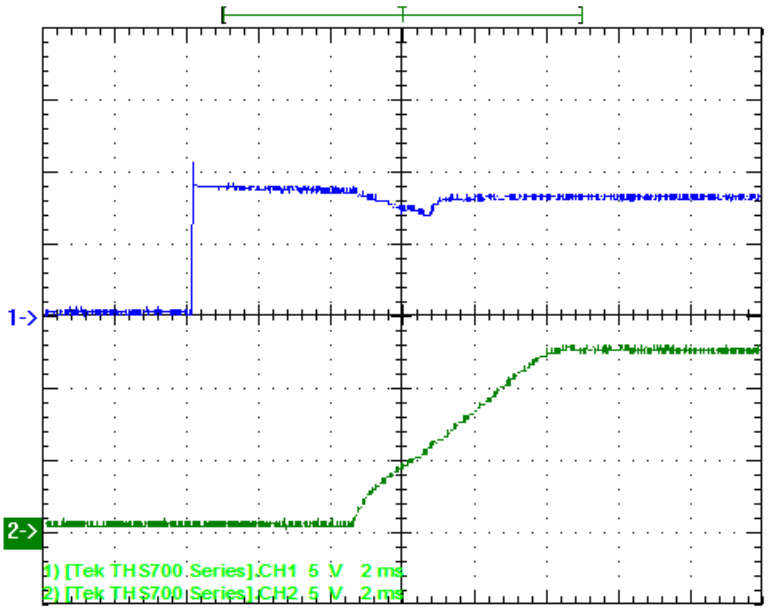
Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

2ms/div

Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set at 8V, with no load at the output.



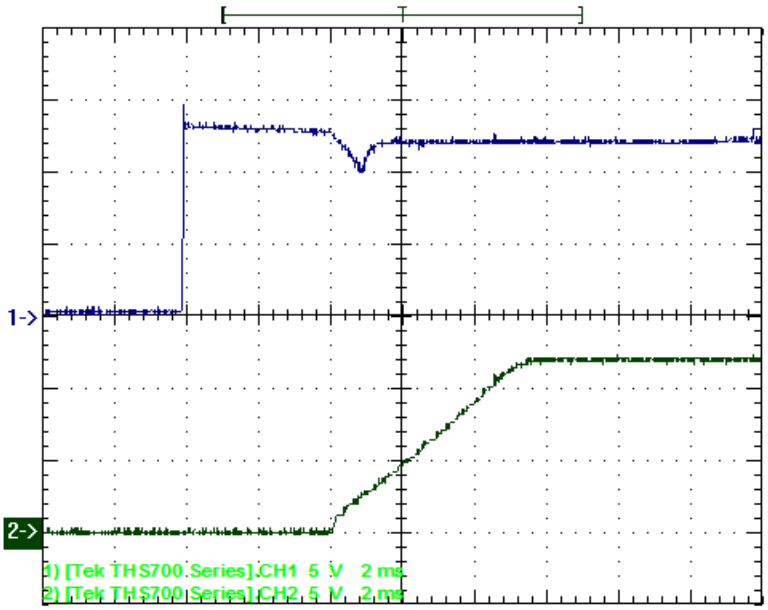
Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

2ms/div

Figure 3

The startup waveform is shown in the Figure 4. The input voltage was set at 12V, with 1.5A load at the output.



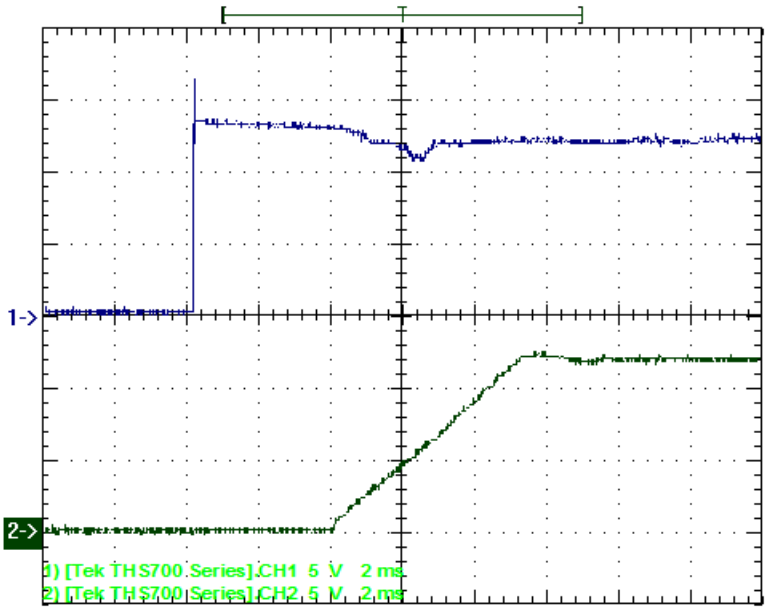
Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

2ms/div

Figure 4

The startup waveform is shown in the Figure 5. The input voltage was set at 12V, with 0.1A load at the output.



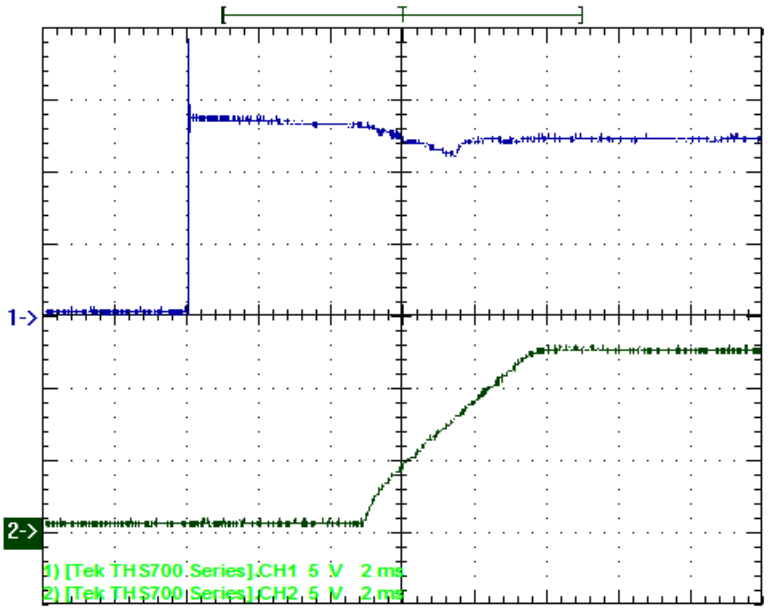
Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

2ms/div

Figure 5

The startup waveform is shown in the Figure 6. The input voltage was set at 12V, with no load at the output.



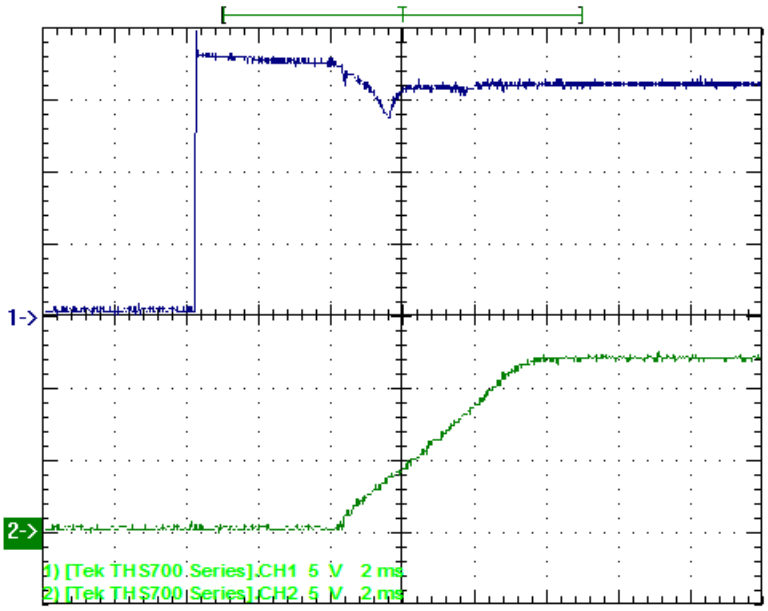
Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

2ms/div

Figure 6

The startup waveform is shown in the Figure 7. The input voltage was set at 16V, with 1.5A load at the output.



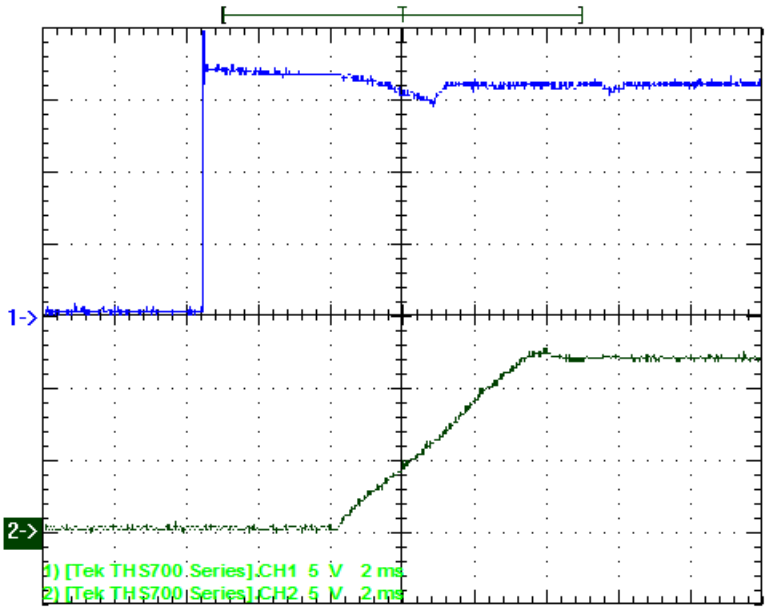
Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

2ms/div

Figure 7

The startup waveform is shown in the Figure 8. The input voltage was set at 16V, with 0.1A load at the output.



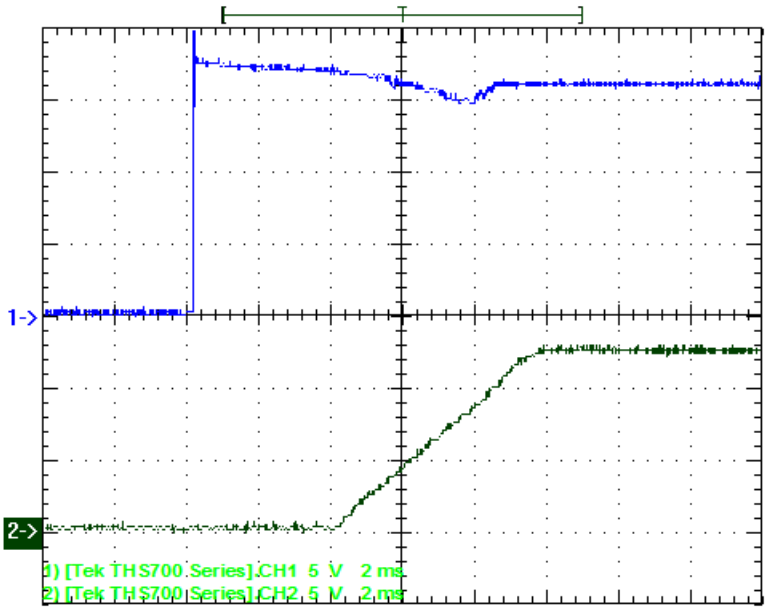
Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

2ms/div

Figure 8

The startup waveform is shown in the Figure 9. The input voltage was set at 16V, with no load at the output.



Ch1=> input voltage 5V/div

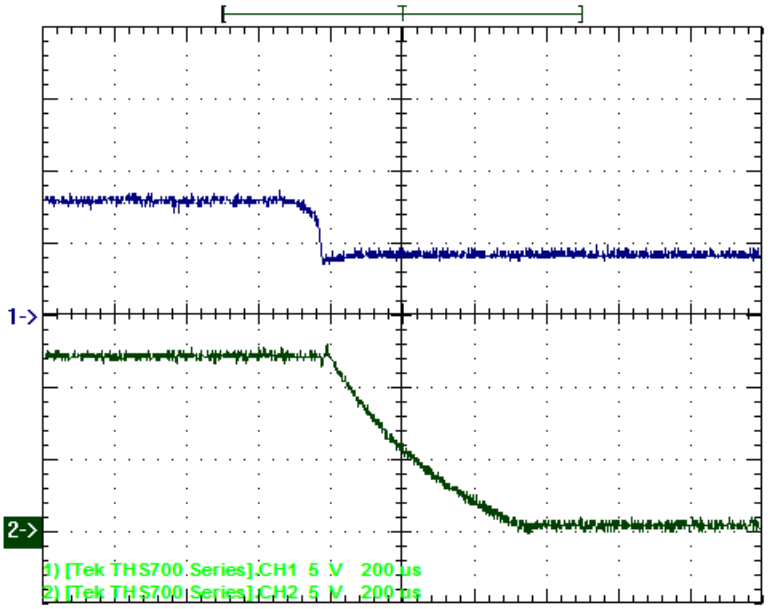
Ch2=> output voltage 5V/div

2ms/div

Figure 9

2 Shutdown

The shutdown waveform is shown in the Figure 10. The input voltage was set at 8V, with 1.5A load on the output. The power supply was disconnected.



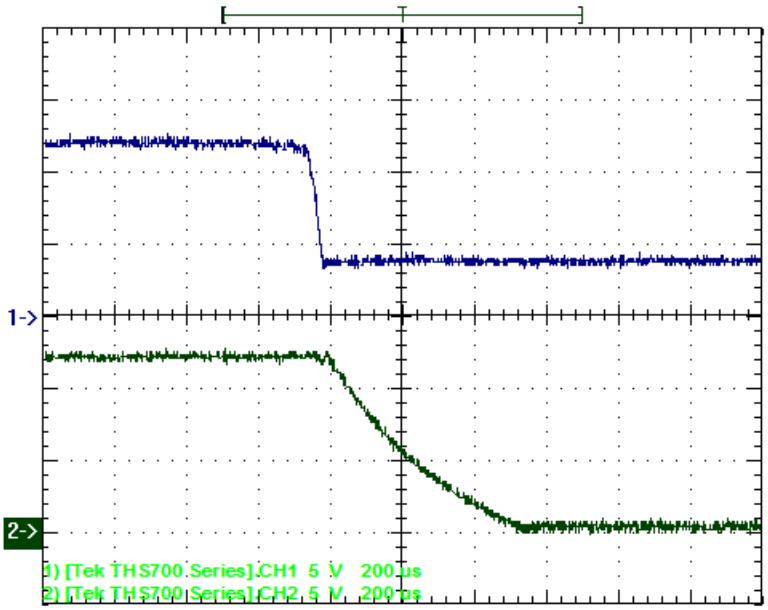
Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

200µs/div

Figure 10

The shutdown waveform is shown in the Figure 11. The input voltage was set at 12V, with 1.5A load on the output. The power supply was disconnected.



Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

200µs/div

20MHz bw

Figure 11

The shutdown waveform is shown in the Figure 12. The input voltage was set at 16V, with 1.5A load on the output. The power supply was disconnected.

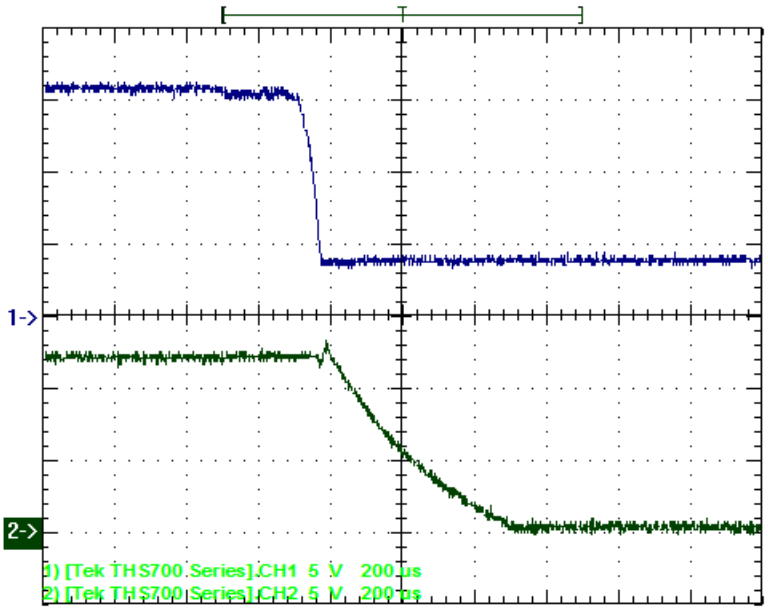


Figure 12

Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

200µs/div

20MHz bw

3 Efficiency

The efficiency is shown in the Figure 13 below. The input voltage was set to 8V, 12V and 16V.

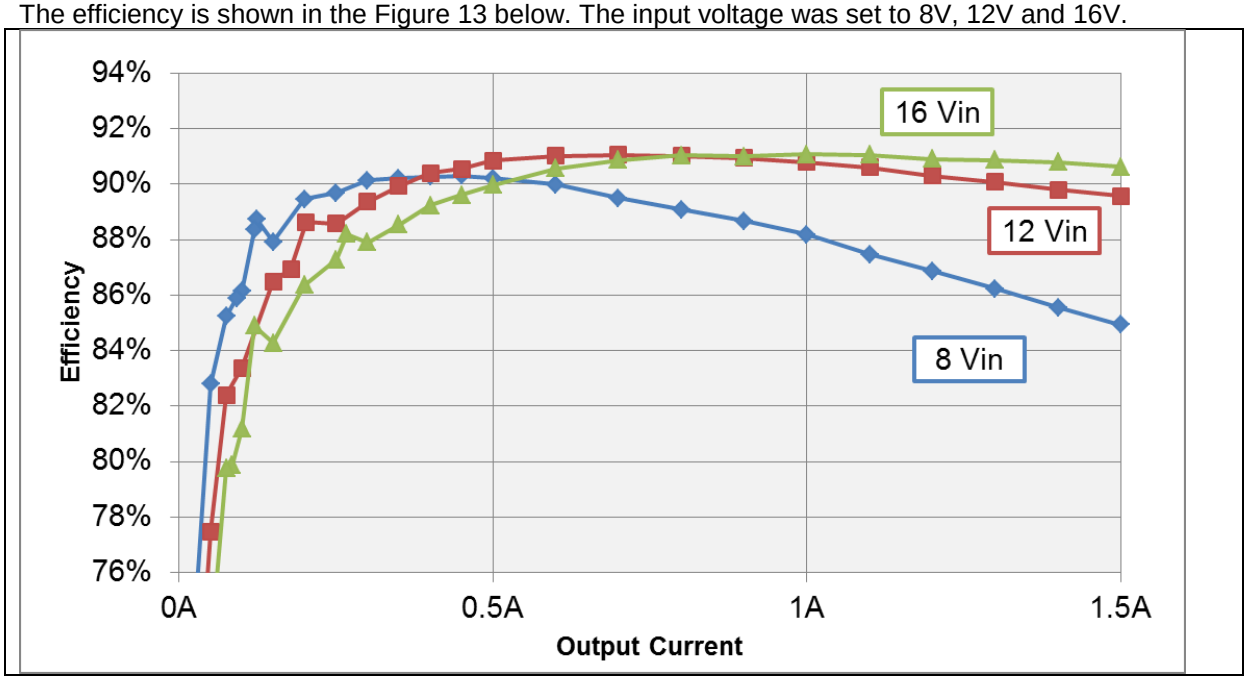


Figure 13

4 Load Regulation

The load regulation of the output is shown in the Figure 14 below. The input voltage was set to 8V, 12V and 16V.

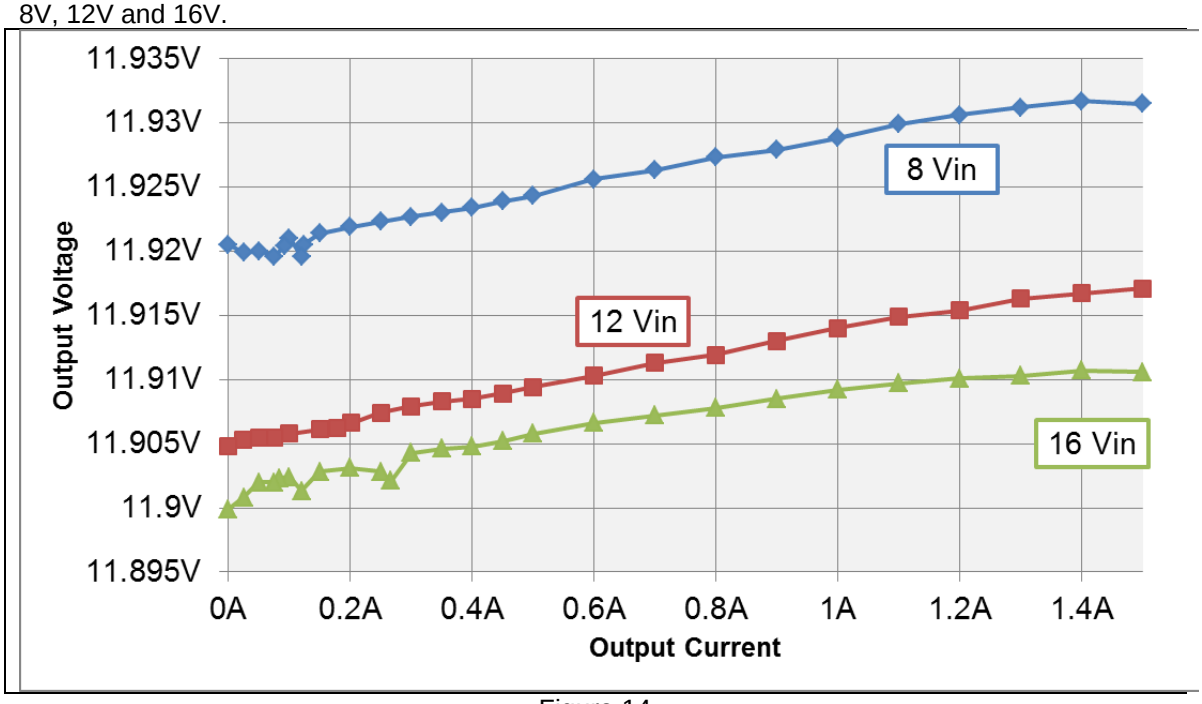


Figure 14

5 Line Regulation

The line regulation is shown in Figure 15. The output current was set to 1.5A.

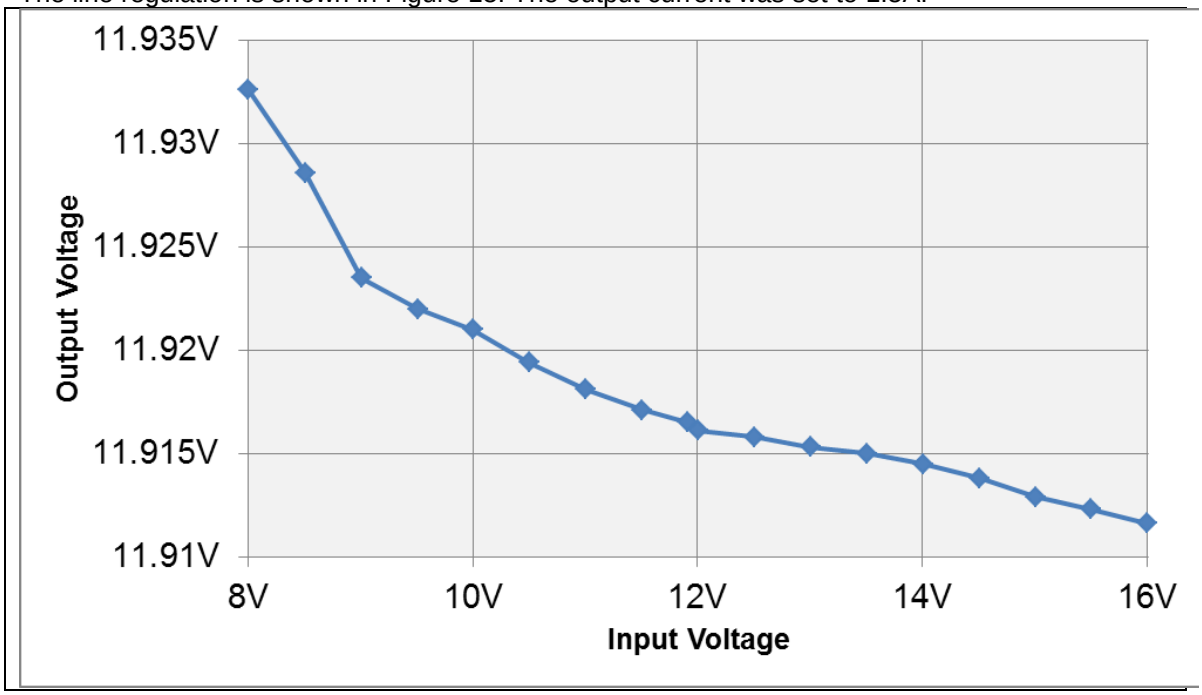


Figure 15

With the same setup the efficiencies are shown in Figure 16.

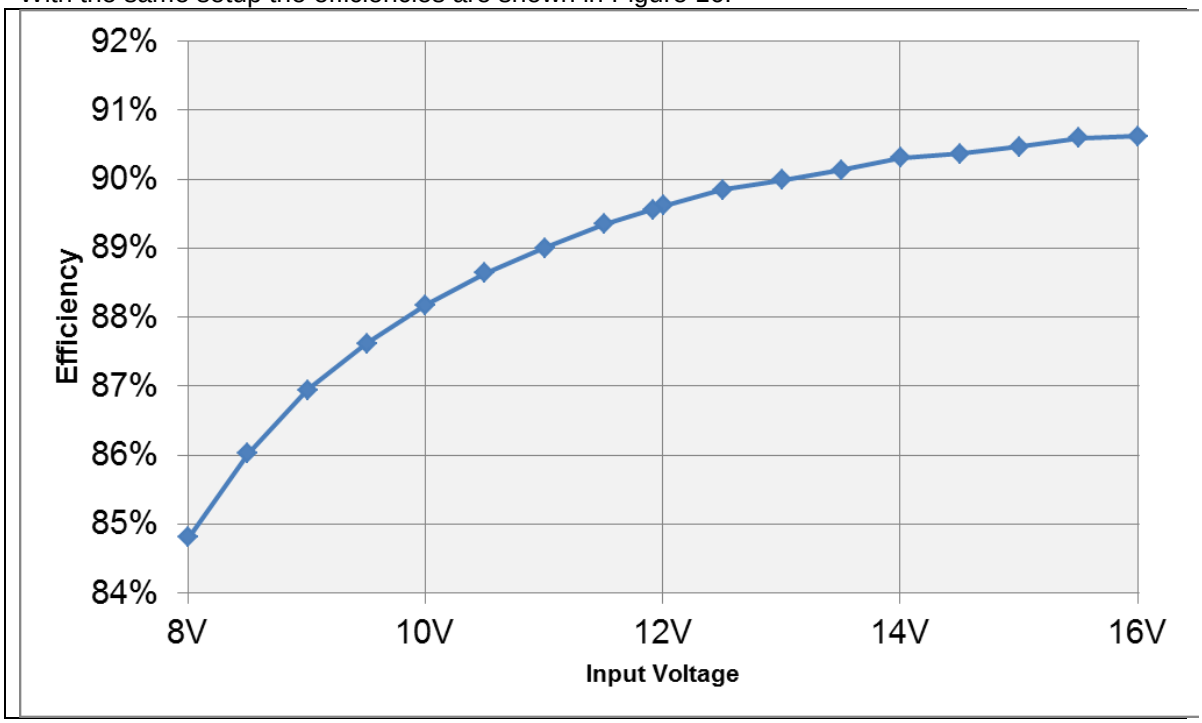
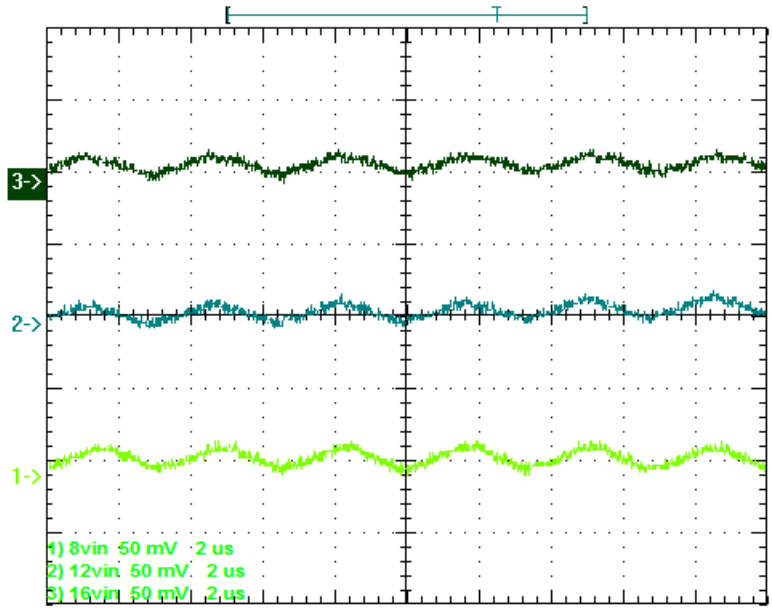


Figure 16

6 Output Ripple Voltage

The output ripple voltage is shown in Figure 17. The output current was set to 1.5A



Ch3 => output voltage@16Vin

Ch2 => output voltage@12Vin

Ch1 => output voltage@8Vin

50mV/div (!!!)

AC coupled

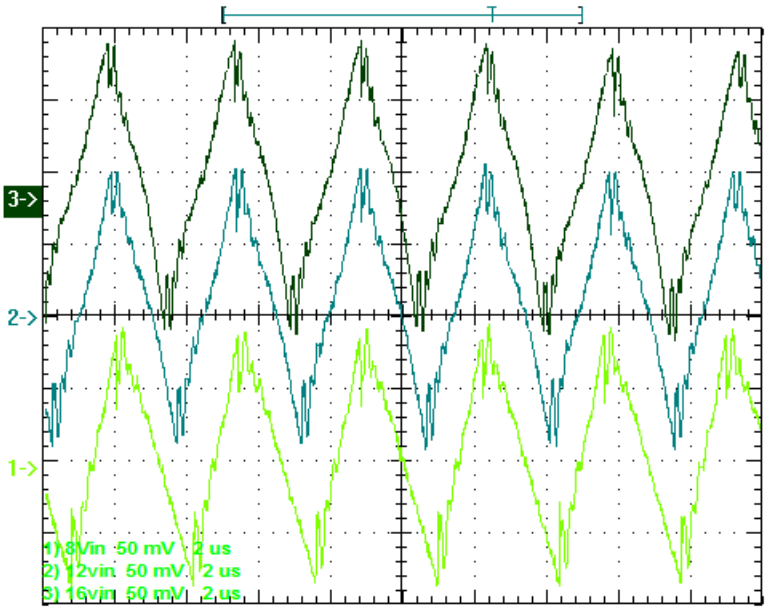
20MHz bw

2µs/div

Figure 17, continuous output current results in lowest ripple

7 Input Ripple Voltage

The input ripple voltage is shown in Figure 18. The output current was set to 1.5A



Ch3 => intput voltage@16Vin

Ch2 => input voltage@12Vin

Ch1 => input voltage@8Vin

50mV/div

AC coupled

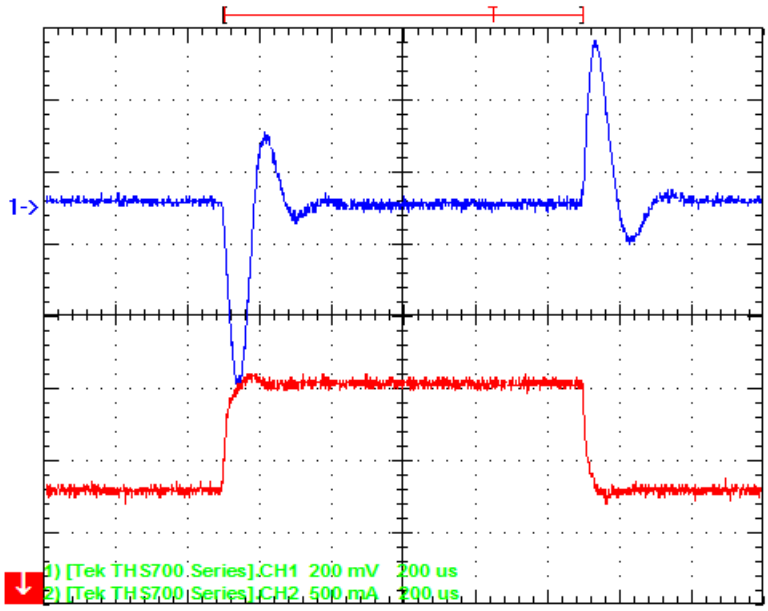
20MHz bw

2µs/div

Figure 18, pulse current across input capacitors, watch reflected ripple

8 Load Transients

The Figure 19 shows the response to load transients. The load is switching from 0.75A to 1.5A with a frequency of 500Hz. The input voltage was set to 8V, transient response du = 4%.



Ch1 => output voltage 200mV/div

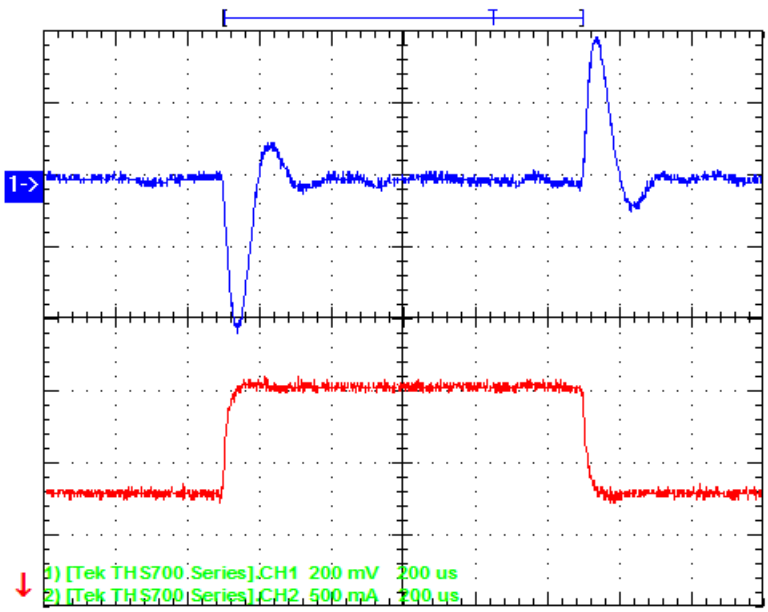
20MHz bandwidth setting

Ch2 => output current 500mA/div

200µs/div

Figure 19

The Figure 20 shows the response to load transients. The load is switching from 0.75A to 1.5A with a frequency of 500Hz. The input voltage was set to 12V



Ch1 => output voltage 200mV/div

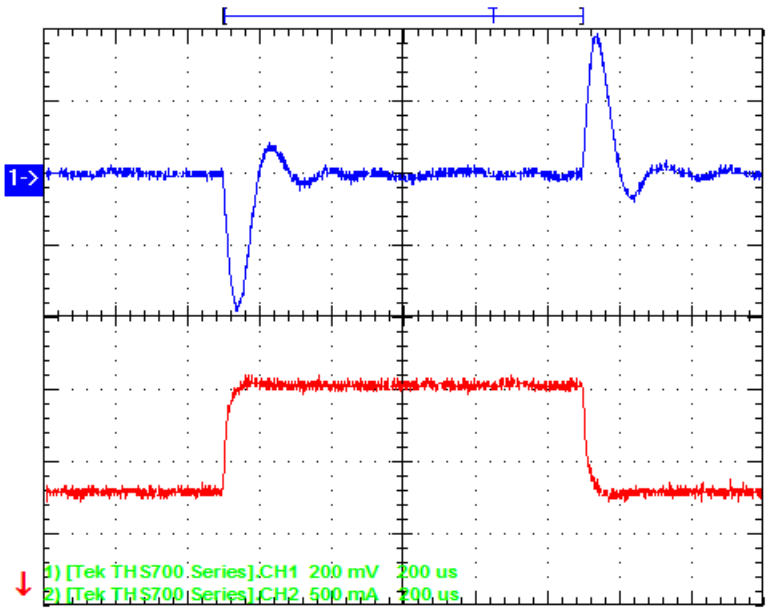
20MHz bandwidth setting

Ch2 => output current 500mA/div

200µs/div

Figure 20

The Figure 21 shows the response to load transients. The load is switching from 0.75A to 1.5A with a frequency of 100Hz. The input voltage was set to 16V



Ch1 => output voltage 200mV/div

20MHz bandwidth setting

Ch2 => output current 500mA/div

200µs/div

Figure 21

9 Control Loop Frequency Response

Figure 22 shows the loop response. 1.5A-load applied. The input voltage was set to 8V.

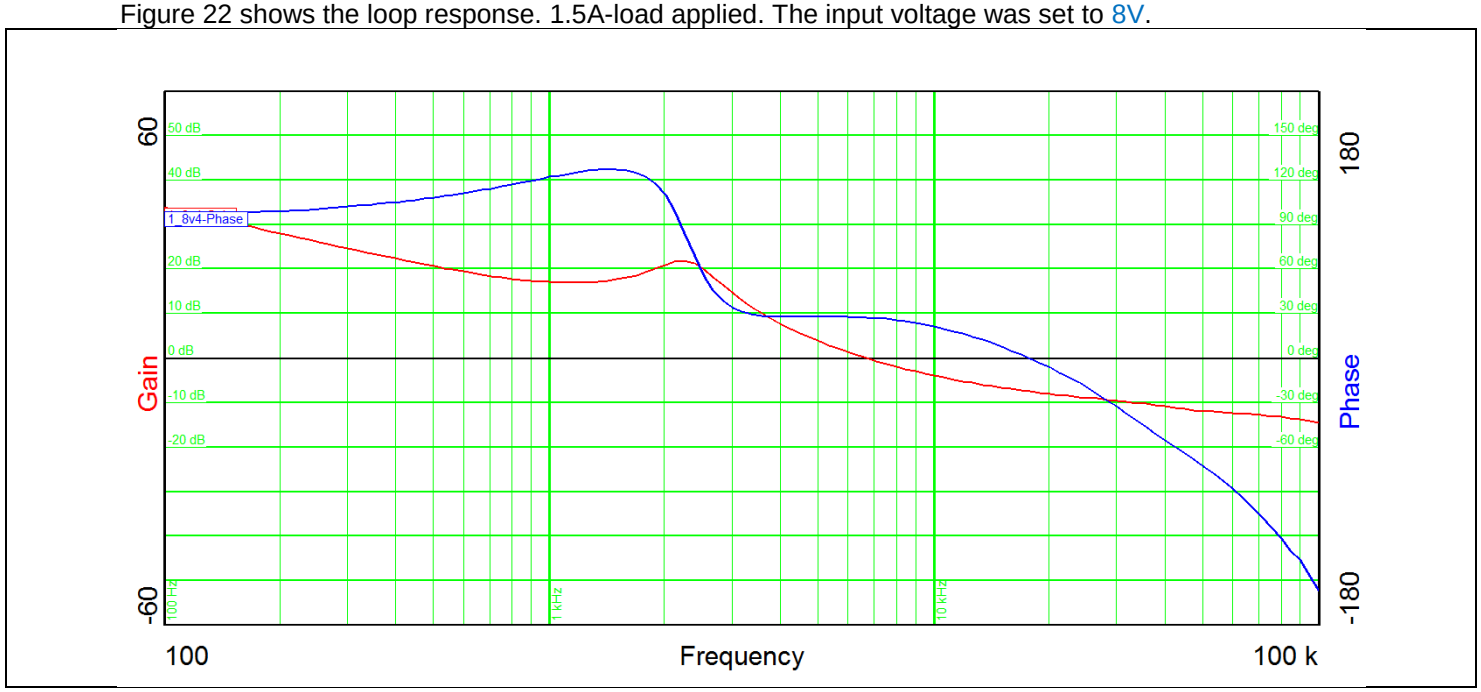


Figure 22

Figure 23 shows the loop response. 1.5A-load applied. The input voltage was set to 12V.

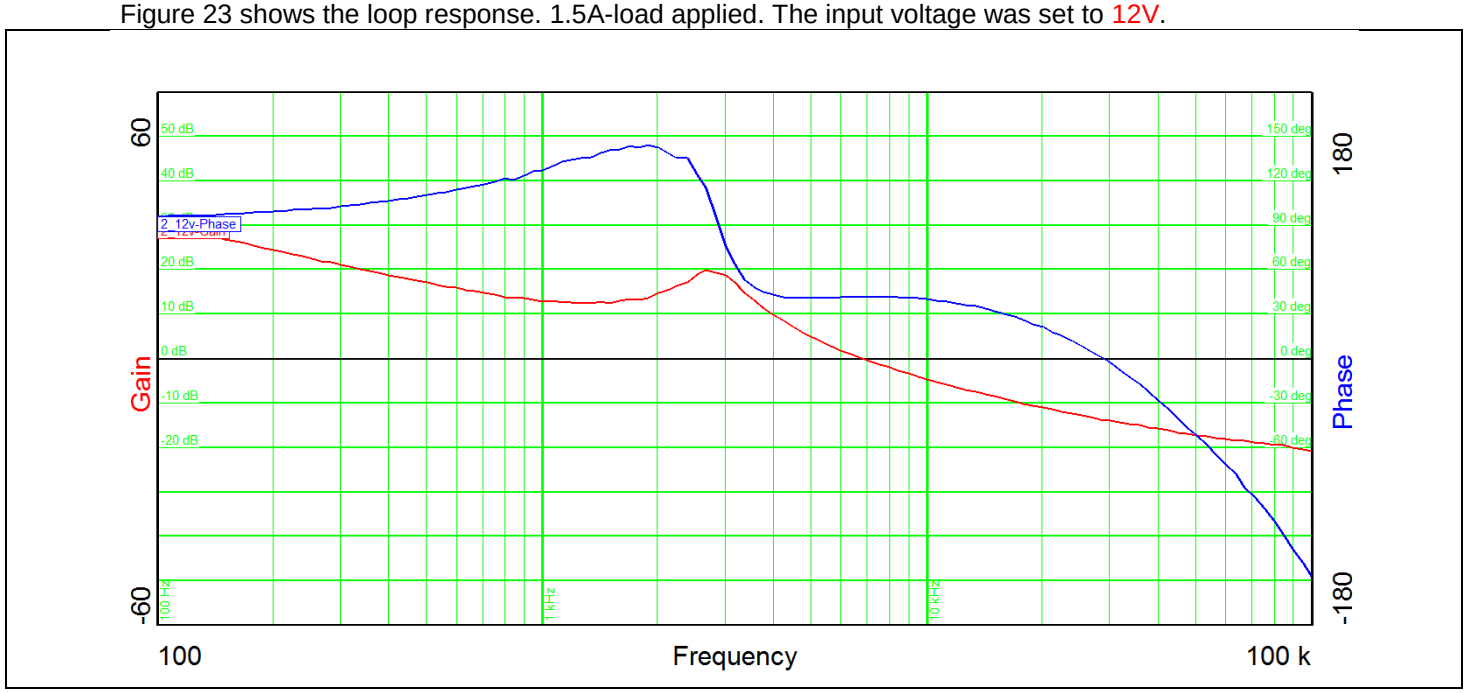


Figure 23

Figure 24 shows the loop response. 1.5A-load applied. The input voltage was set to 16V.

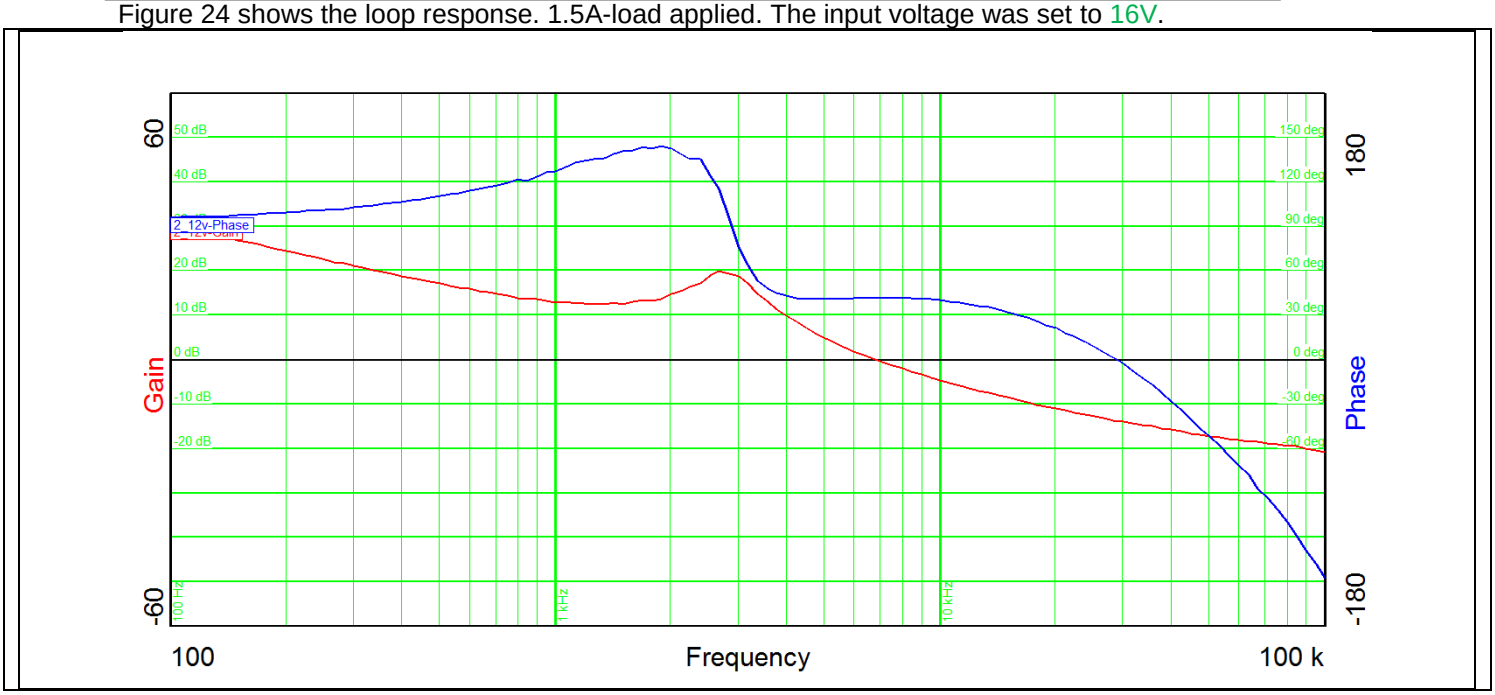


Figure 24

Table 1 summarizes the results from Figure 22 Figure 23 and Figure 24.

Vin	8V	12V	16V
Bandwidth (kHz)	6.7	6.8	7.07
Phase margin	27°	41.6°	48.5°
slope (20dB/decade)	-1.3	-1.48	-1.77
gain margin (dB)	-7.5	-13.7	-17.7
slope (20dB/decade)	-0.56	-0.75	-1.0
freq (kHz)	17.8	28.8	37.9

Table 1

Hard to compensate a Voltage Mode device for ZETA topology:

- **use a current mode device**
- **for a high Q filter use RC damping across coupling capacitors**

10 Miscellaneous Waveforms

The waveform of the voltage on Q1 drain-source is shown in Figure 25. Input voltage was set to 8V and output current to 1.5A.

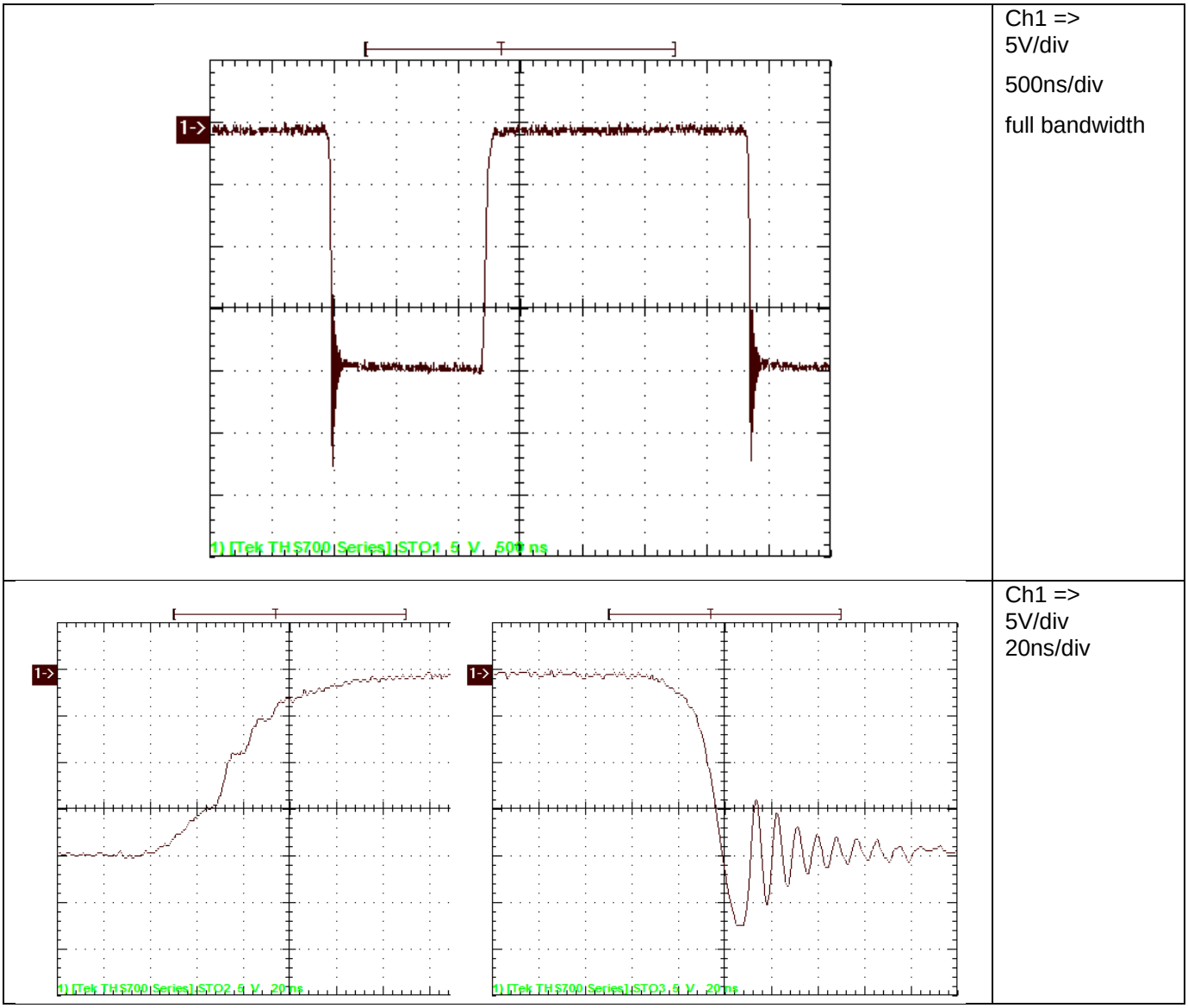


Figure 25

The waveform of the voltage on the gate to source is shown in Figure 26. Input voltage was set to 8V and output current to 1.5A.

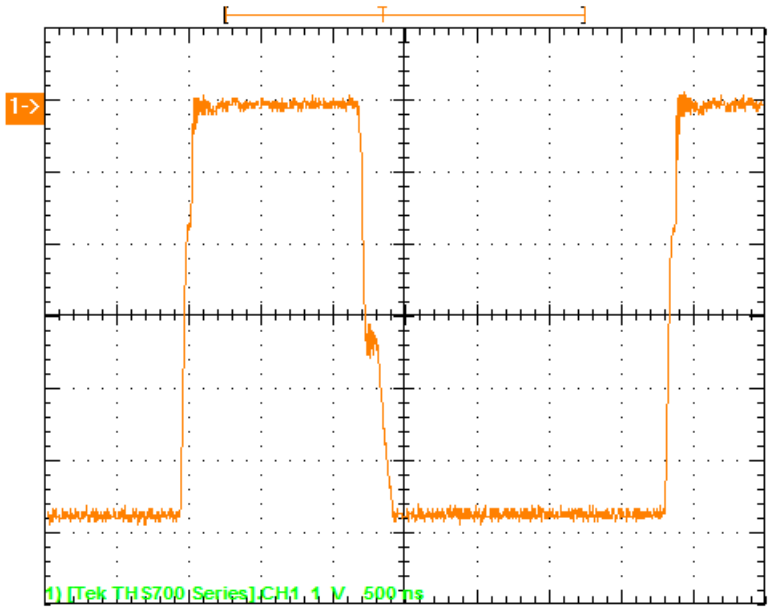
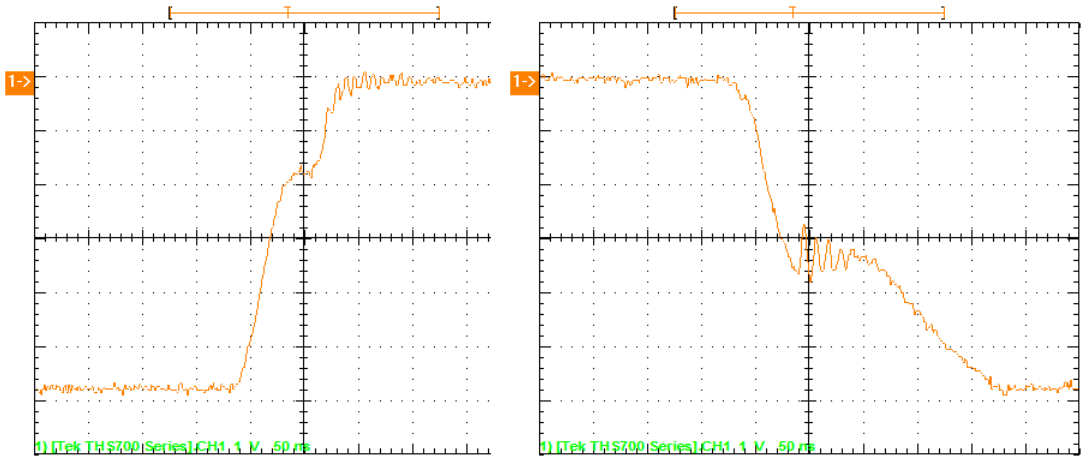
	Ch1 => 1V/div 500ns/div full bandwidth
	Ch1 => 1V/div 50ns/div

Figure 26

The waveform of the voltage on diode D1 is shown in Figure 27. Input voltage was set to 8V and output current to 1.5A.

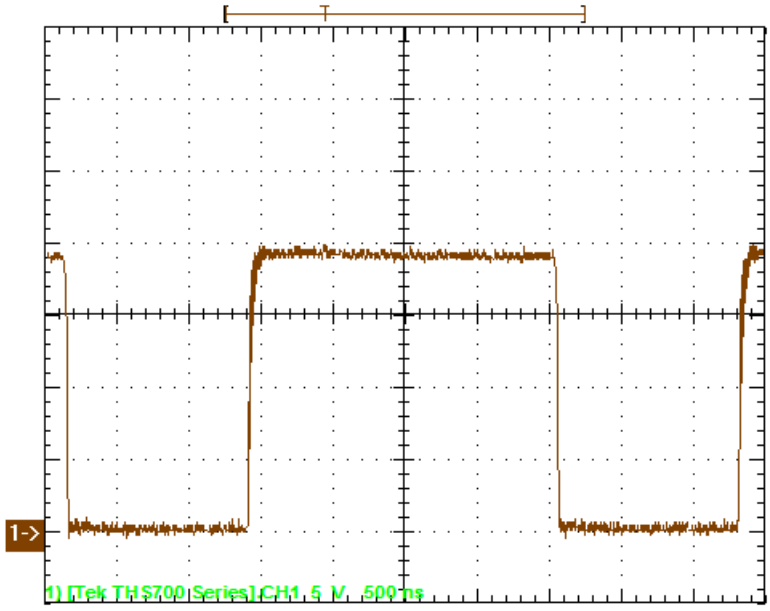
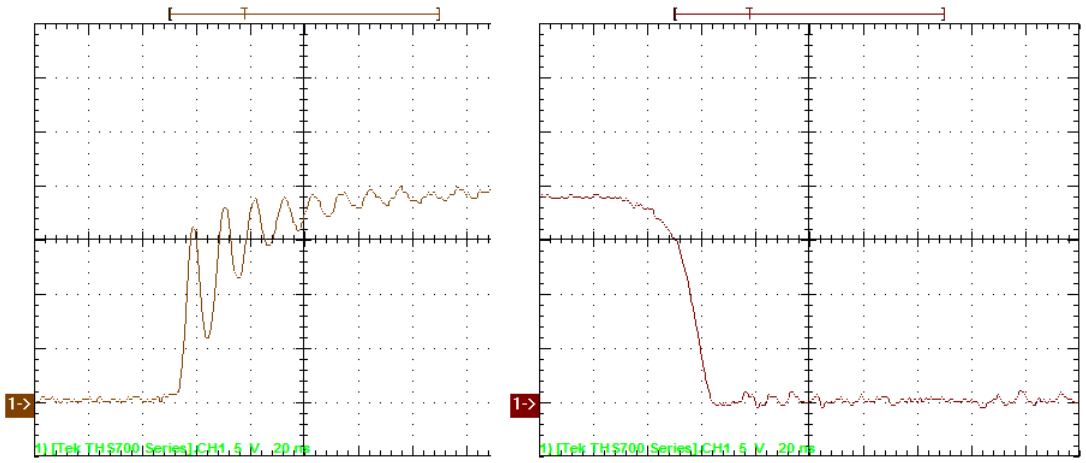
	Ch1 => 5V/div 500ns/div full bandwidth
	Ch1 => 5V/div 20ns/div

Figure 27

The waveform of the voltage on Q1 drain-source is shown in Figure 28. Input voltage was set to 12V and output current to 1.5A.

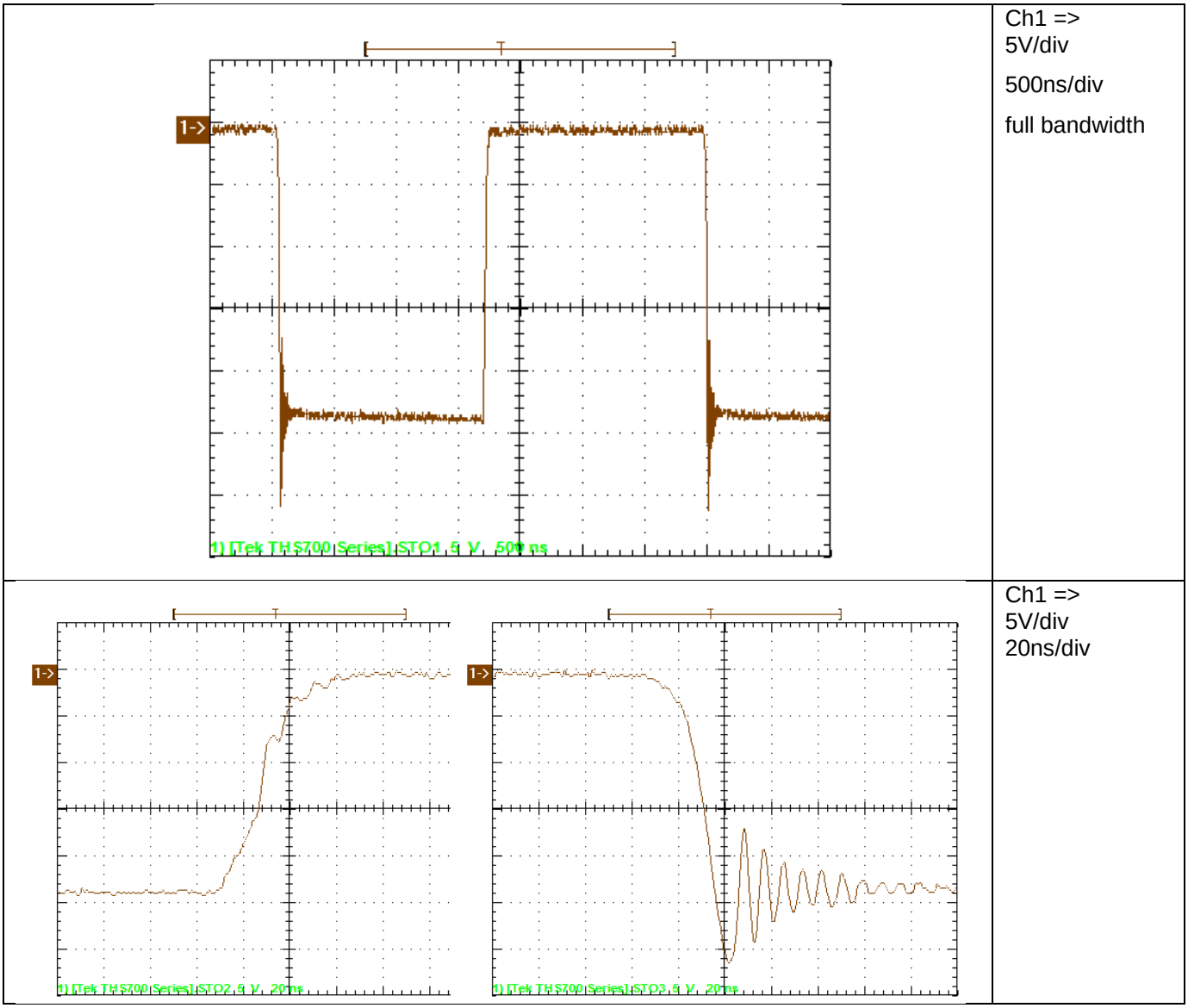


Figure 28

The waveform of the voltage on the gate to source is shown in Figure 29. Input voltage was set to 12V and output current to 1.5A.

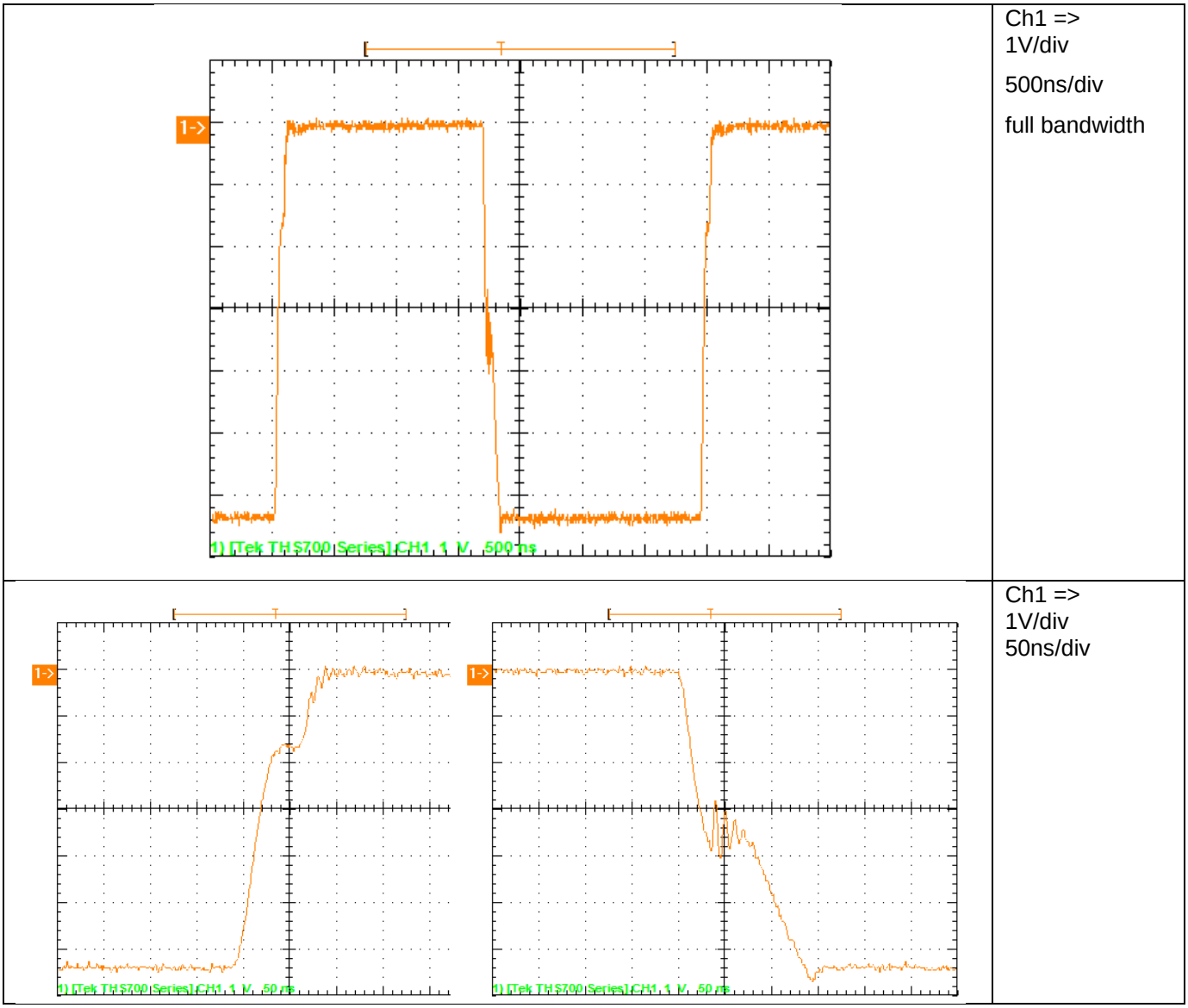


Figure 29

The waveform of the voltage on diode D1 is shown in Figure 30. Input voltage was set to 12V and output current to 1.5A.

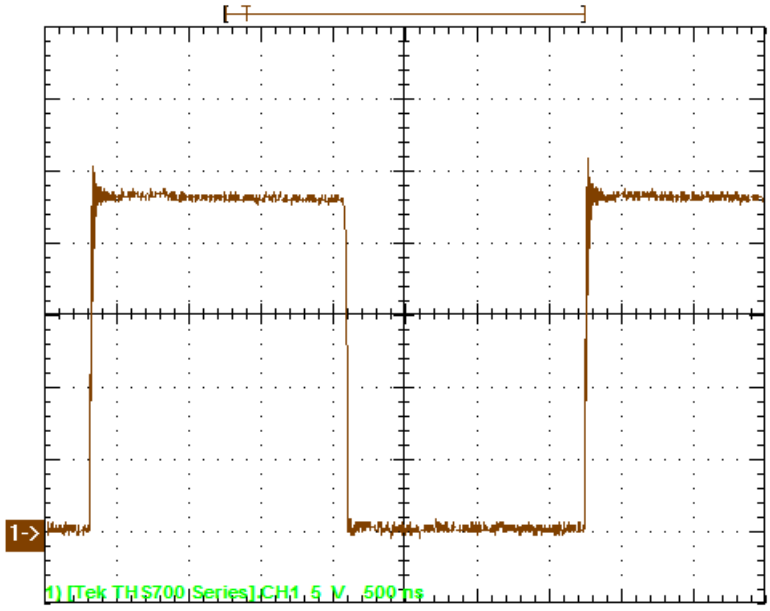
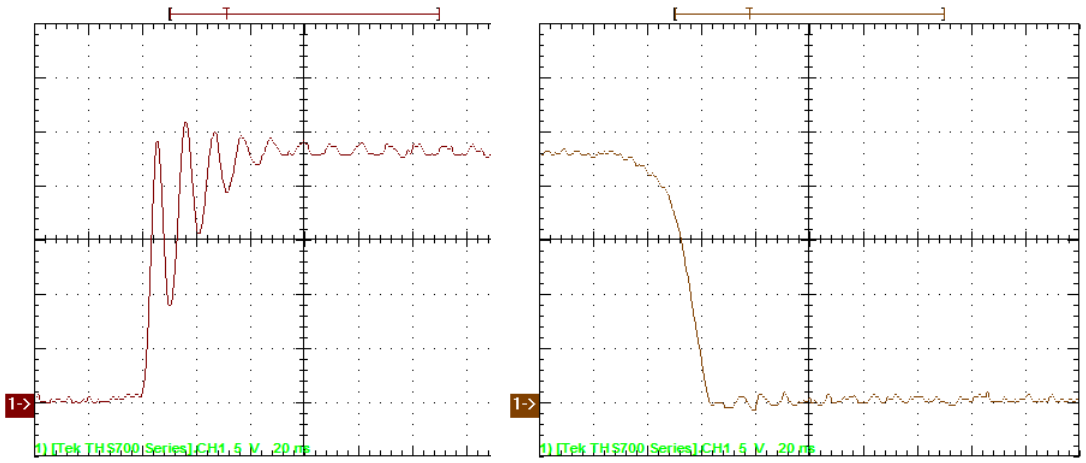
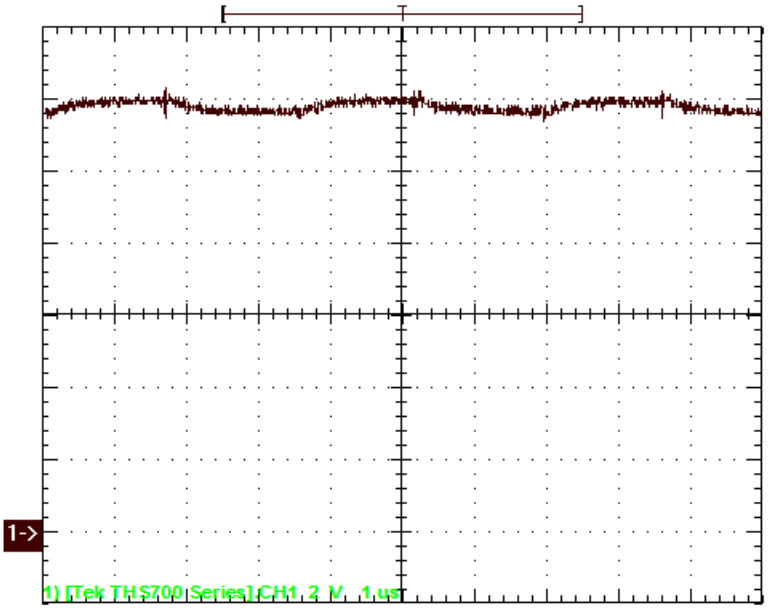
	Ch1 => 5V/div 500ns/div full bandwidth
	Ch1 => 5V/div 50ns/div

Figure 30

Figure 31 shows the waveform at capacitor C4 ("ZETA-capacitor"). Input voltage was set to 12V with 1.5A load current.

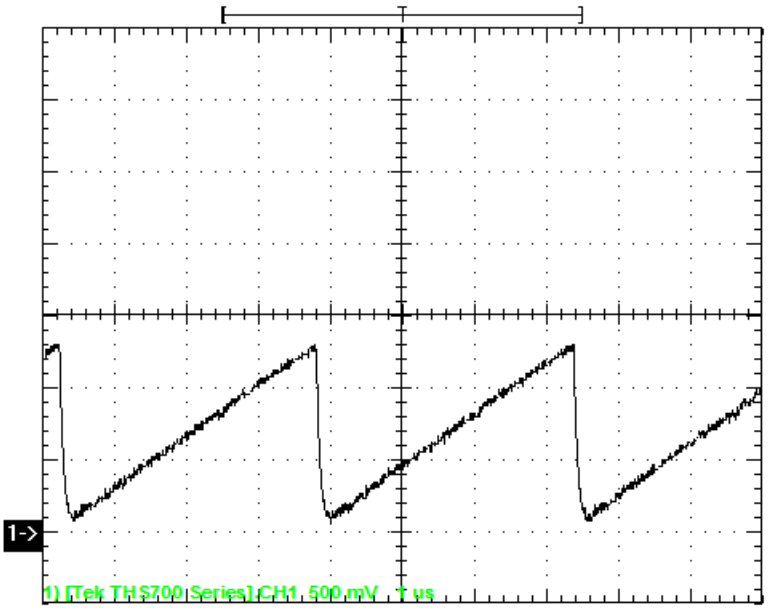


Ch1 =>
2V/div

1µs/div

Figure 31, voltage stress at clamping capacitors is equal to input voltage

Figure 32 shows the waveform at the timing capacitor C11. Input voltage was set to 12V with 1.5A load current.



Ch1 =>
500mV/div

1µs/div

measured with standard probe

20MHz bandwidth

Figure 32, ramp at RC oscillator

The waveform of the voltage on Q1 (drain-source) is shown in Figure 33. Input voltage was set to 16V and output current to 1.5A.

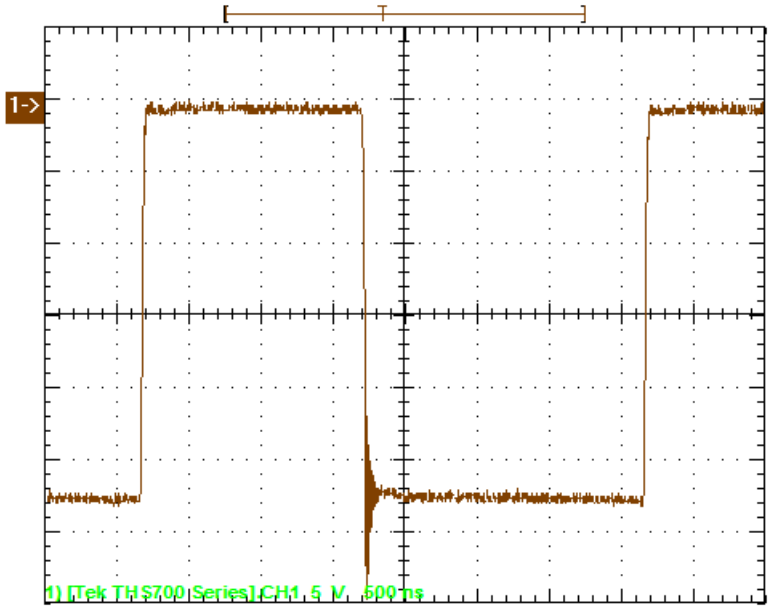
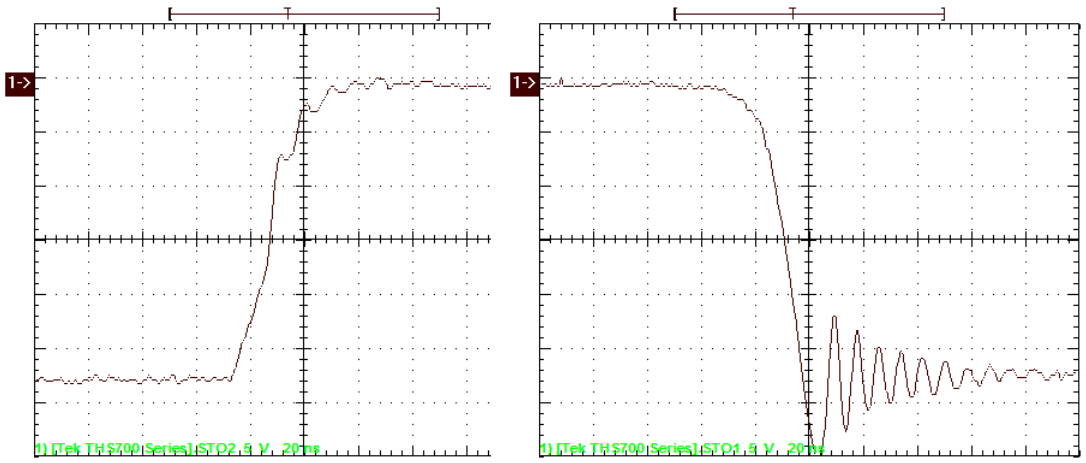
	Ch1 => 5V/div 500ns/div full bandwidth
	Ch1 => 5V/div 20ns/div

Figure 33

The waveform of the voltage on the gate to source is shown in Figure 34. Input voltage was set to 16V and output current to 1.5A.

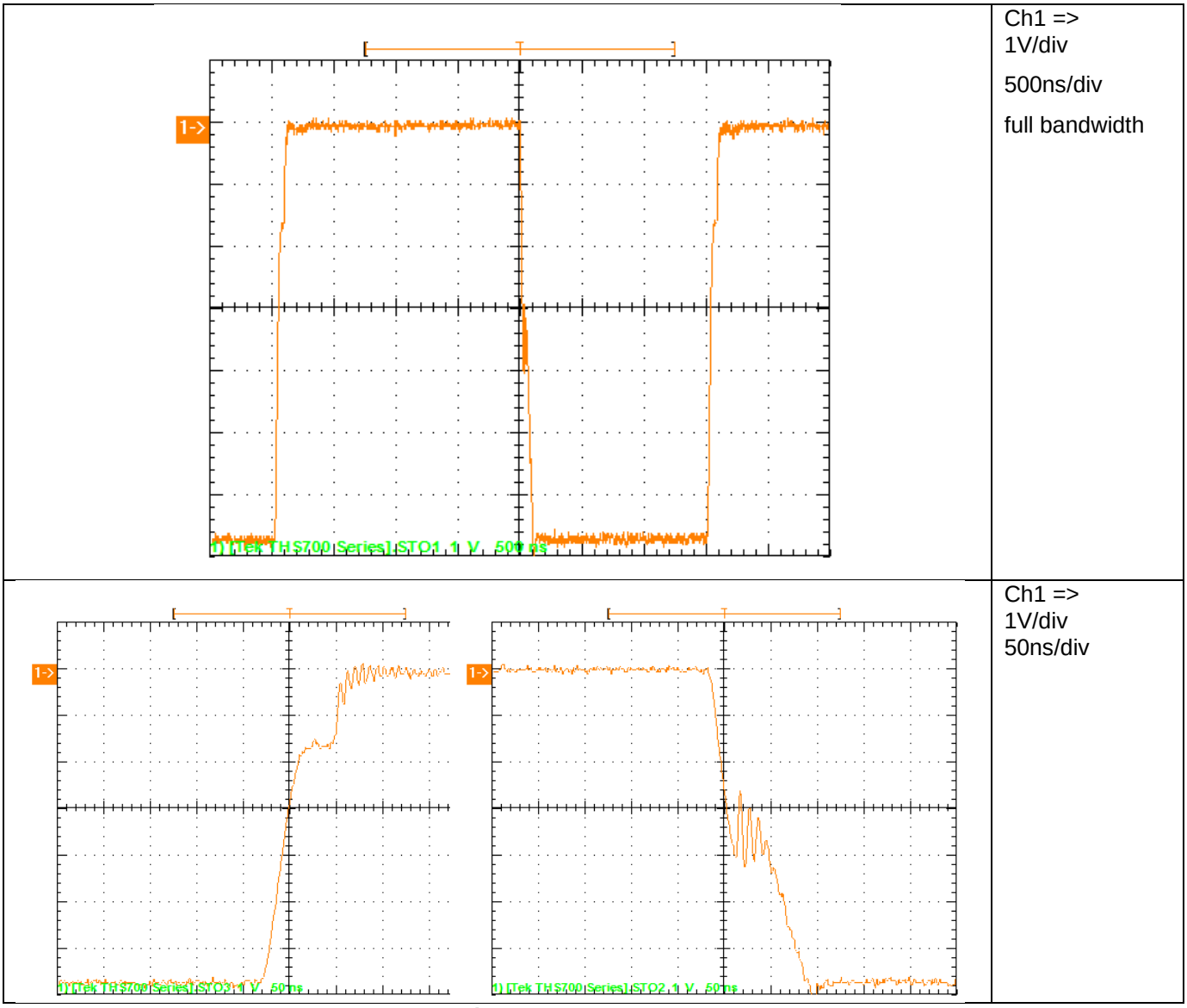


Figure 34

11 Thermal Image

Figure 35 shows the thermal image at 12V input voltage and 1A output current.

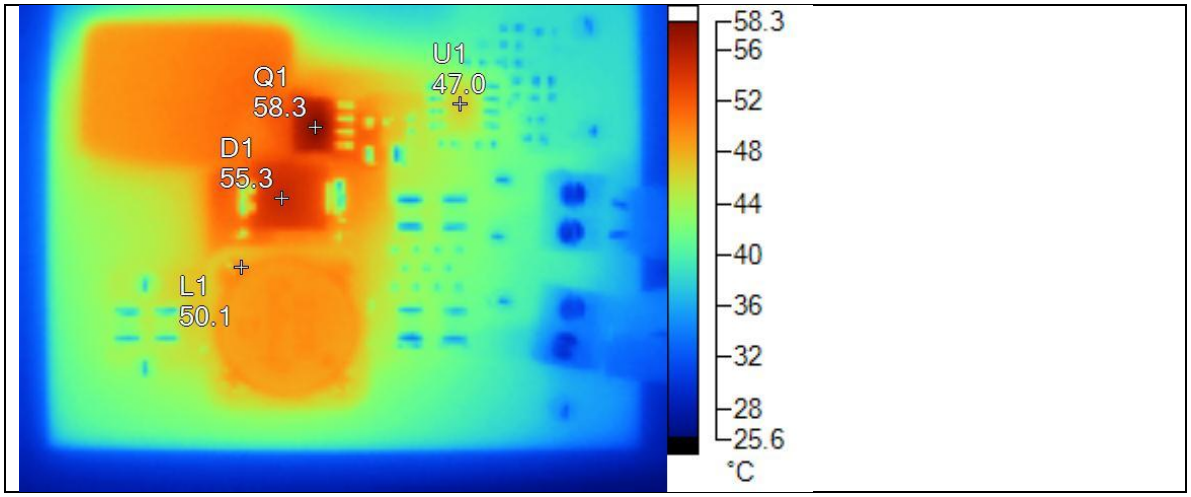


Figure 35

Name	Temperature
Q1	58.3°C
D1	55.3°C
U1	47.0°C
L1	50.1°C

Figure 36 shows the thermal image at 12V input voltage and 1.5A output current.

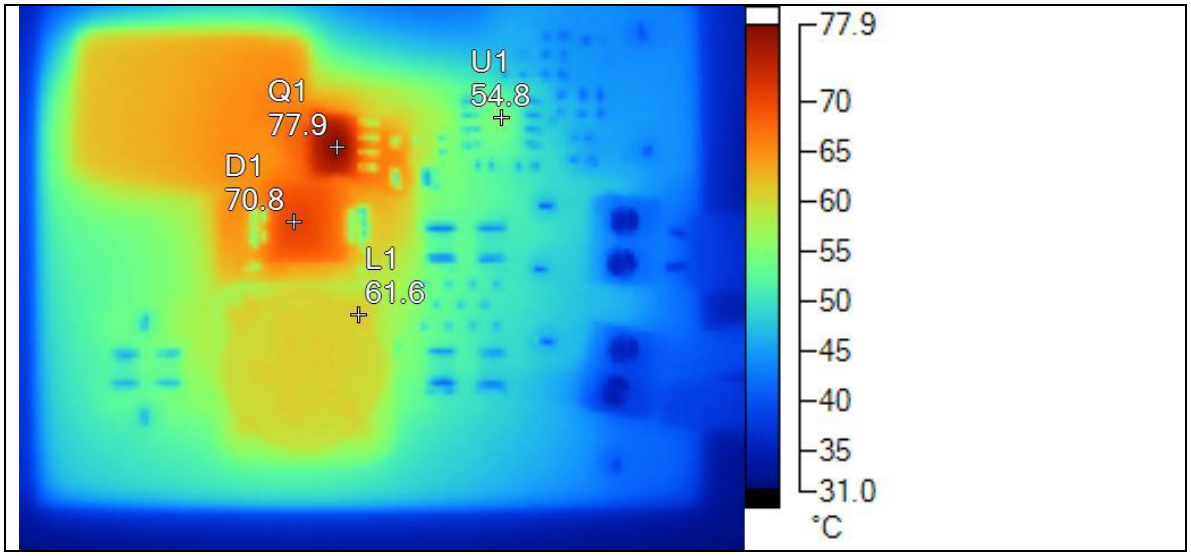


Figure 36

Name	Temperature
Q1	77.9°C
D1	70.8°C
U1	54.8°C
L1	61.6°C

For 1.5Amps continuous output current copper area at Q1/D1 will be increased, see layout Rev B

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