TIDA-00539 UPOE High-Efficiency Flyback Converter (19V/2.3A) for Forced 4-Pair PoE PD Applications

1 Introduction

TIDA-00539 is a high power four-pair solution for Power-over-Ethernet (PoE) applications requiring power in excess as defined in the current IEEE 802.3at standard. It is compliant with Cisco UPOE Forced Four-Pair designs.

2 Configurable features

1.1 Features

- Excellent efficiency, driven, synchronous flyback design.
- Forced Four-Pair UPOE compliant
- 19V @ 2.3A DC output (2.9A capable)

1.2 Applications

- Universal Power Over Ethernet (UPOE) Compliant Devices
- Video and VoIP telephones
- Multiband access points
- Security cameras
- Pico-base stations

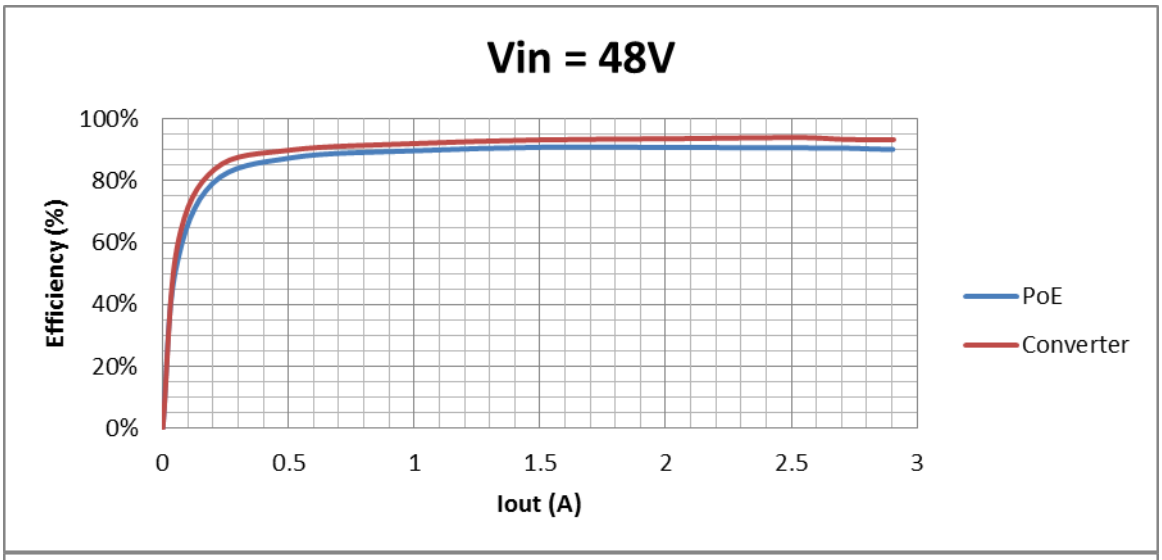
3 Electrical specifications

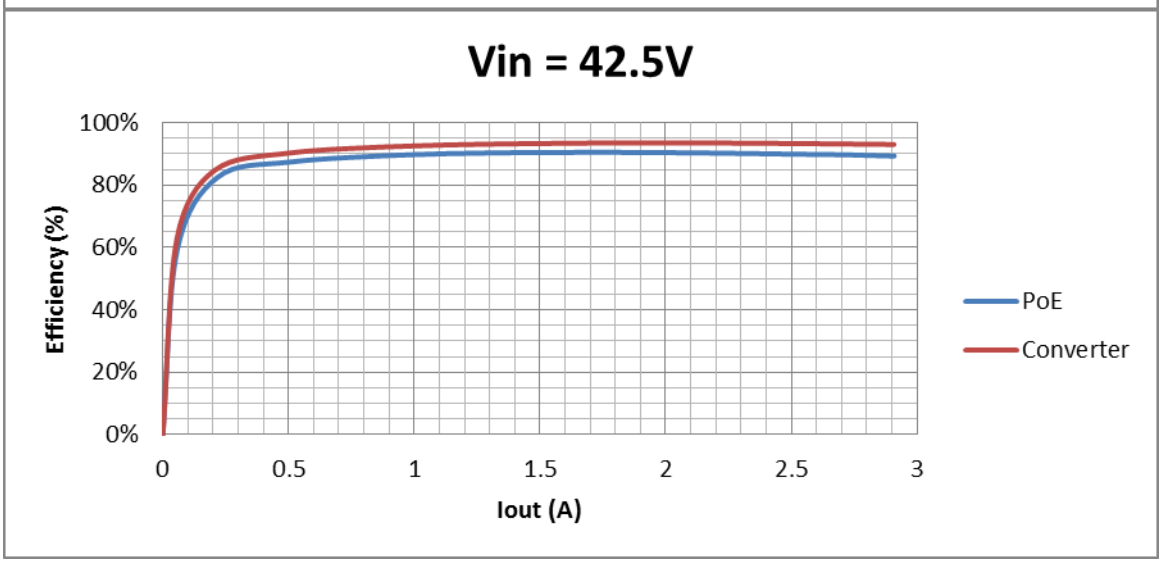
TIDA-00539 Electrical and Performance Specifications

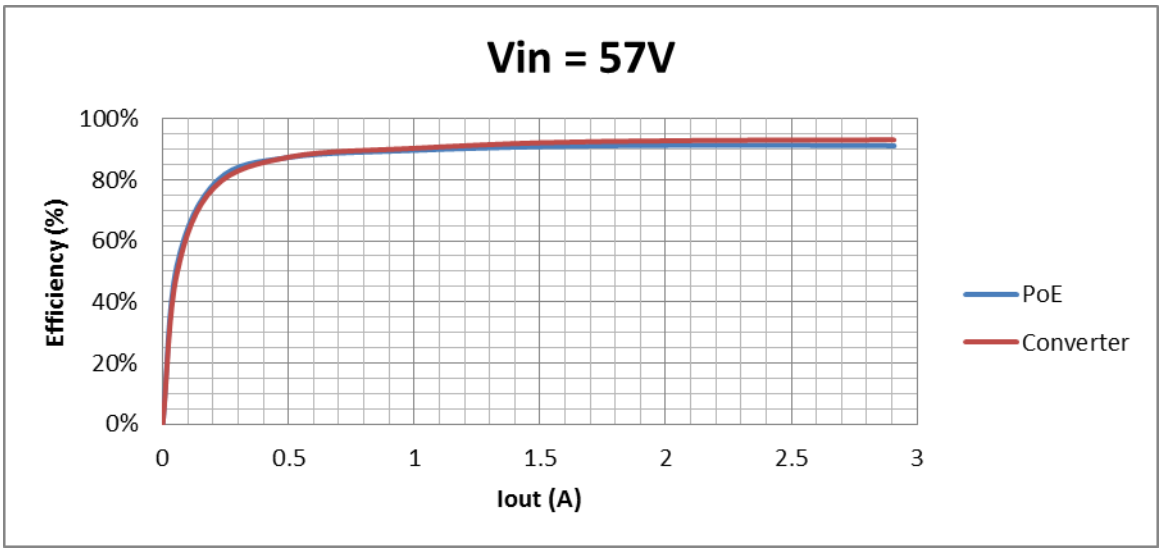
(1)Per TPS2378 PD

Parameter	Condition		Min	Typ	Max	Units
Power Interface						
Input Voltage	Applied to the power pins of connectors J1 or J3		42.5	-	57	Volts
Operating Voltage (1)	After start up.		30	-	57	
Input UVLO, POE input J1 (1)	Rising input voltage		-	-	40	
	Falling input voltage		30	-	-	
Detection voltage (1)	@ device terminals		1.4	-	10.1	
Classification voltage (1)	@ device terminals		11.9	-	23.0	
Classification current (1)	Rclass = 63.4 ohms		38	-	42	mA
Inrush current-limit (1)			100	-	180	
Operating current-limit (1)			850	-	1200	
DC/DC Converter						
Output Voltage	42.5 ≤ Vin ≤ 57V, ILOAD ≤ ILOAD (max)	19V output	19.01	19.04	19.07	Volts
Output Current	42.5 ≤ Vin ≤ 57V	19V output	-	-	2.9	Amps
Output ripple voltage, pk-to-pk	Vin = 48V, ILOAD = 2.9A	19V output	-	225	-	mV
Efficiency, dc-dc converter	Vin = 48V, ILOAD = 2.9A	19V output	-	93	-	%
Efficiency, end-to-end	Vin = 48V, ILOAD = 2.9A	19V output	-	90	-	%
Switching frequency			225	-	270	kHz

4 Efficiency

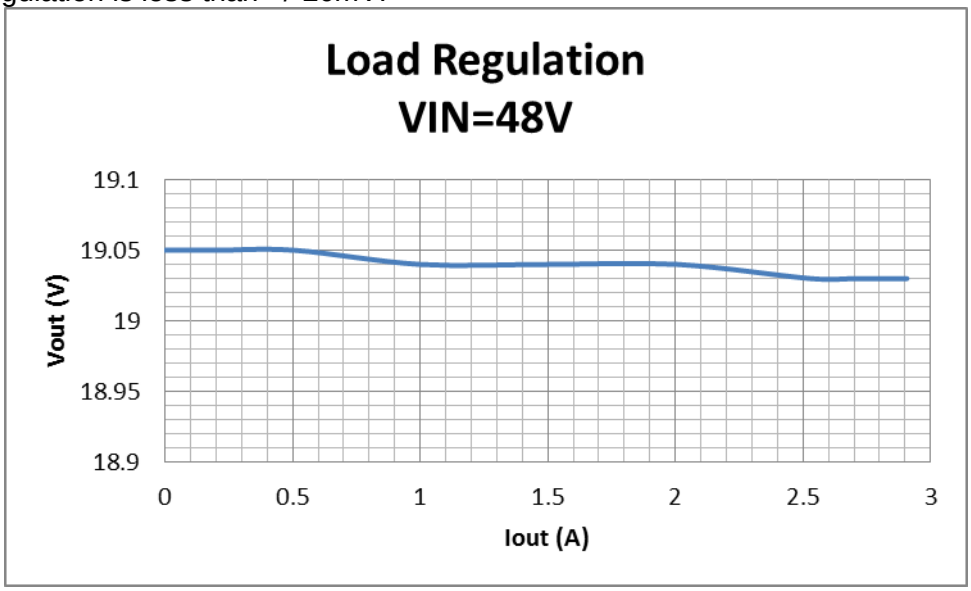




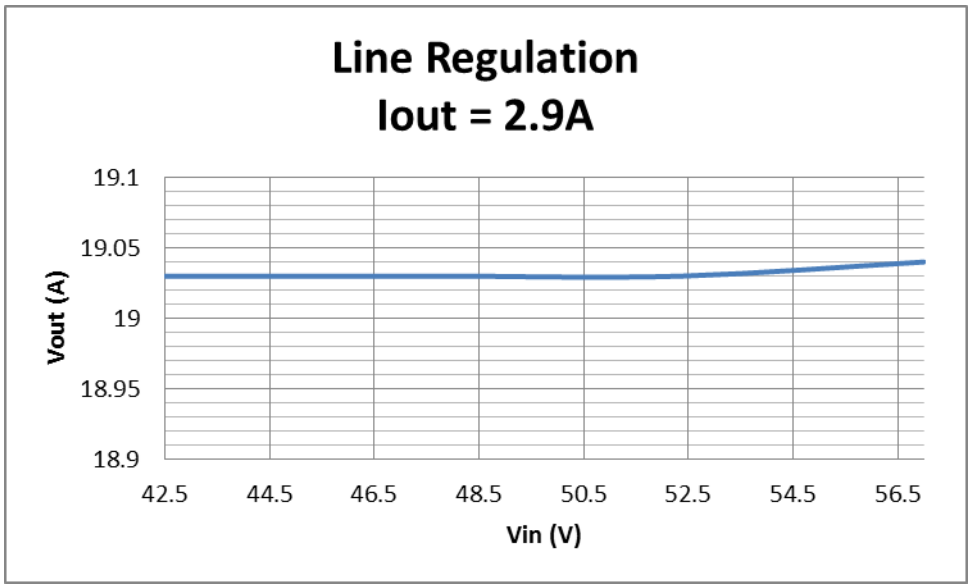


5 Load Regulation

Load regulation is less than +/-20mV.

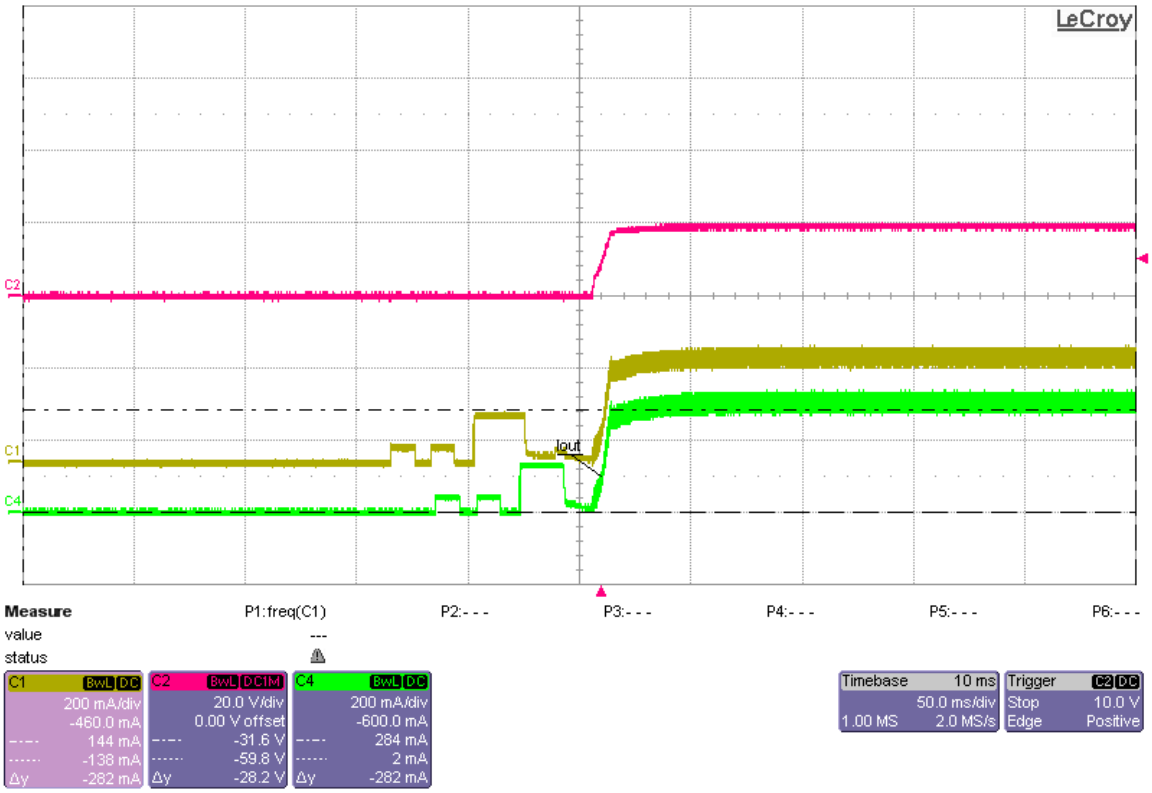


6 Line Regulation



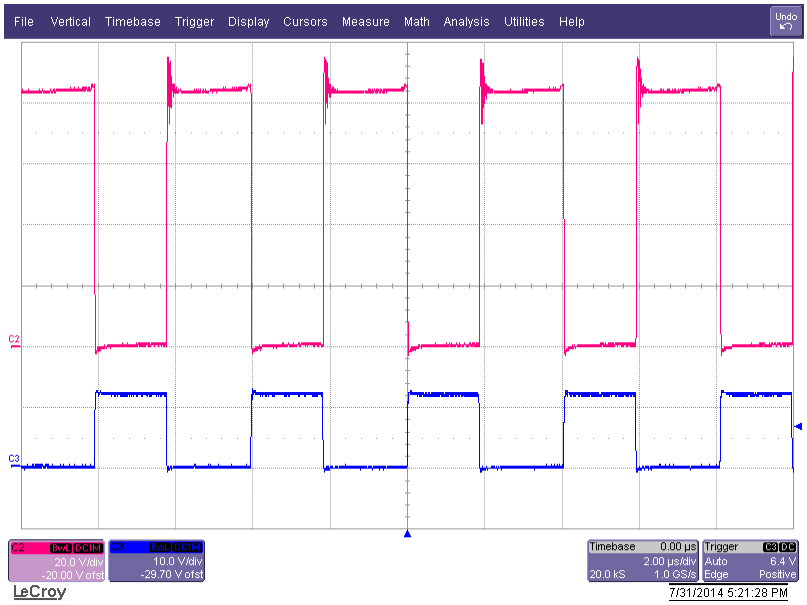
7 Start up

The below graph shows startup of the converter and subsequent current starting between the two PDs for a 26W output load.

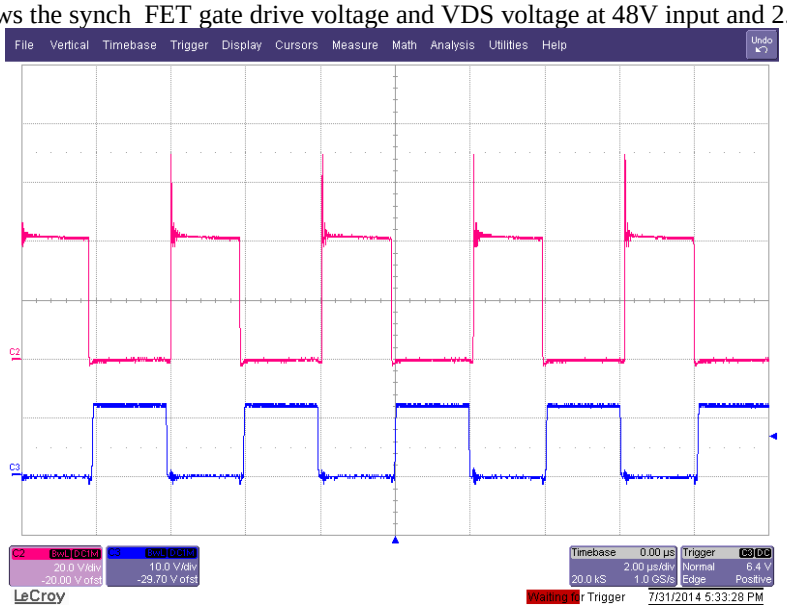


8 Switch Node Waveforms

The below waveform shows the primary FET gate drive voltage and VDS voltage at 48V input and 2.9A output current.

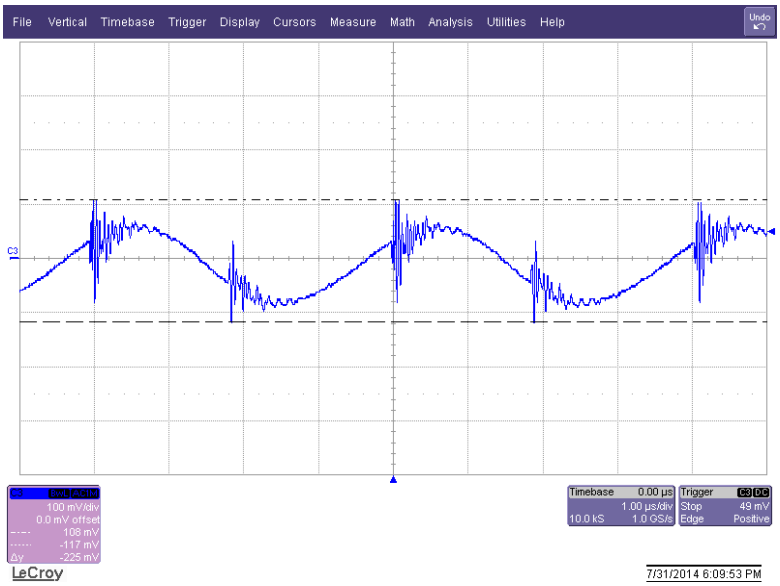


The below waveform shows the synch FET gate drive voltage and VDS voltage at 48V input and 2.9A output current.



9 Output Ripple Voltage

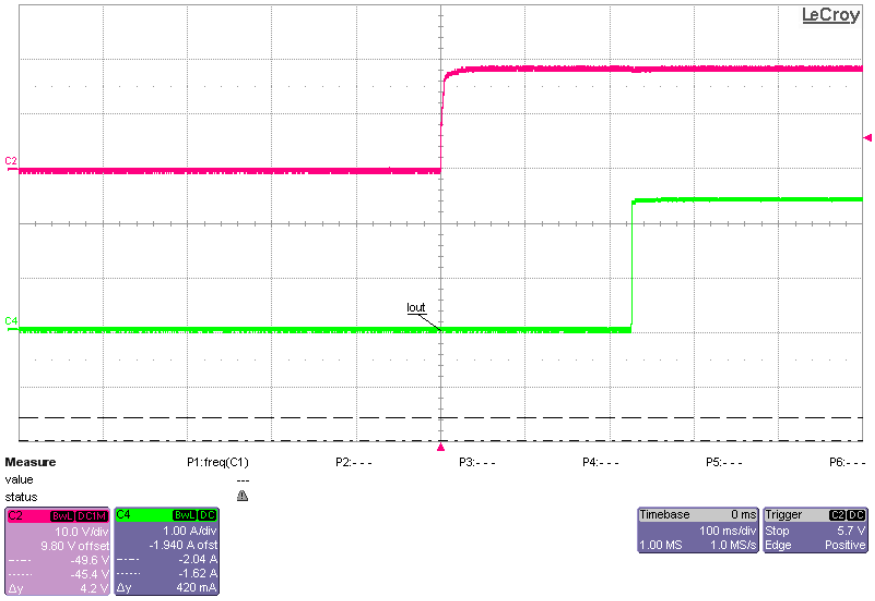
The 19V output ripple voltage is shown in the scope plot below. The waveform was taken with the output loaded to 2.9A.Vin = 48V.



10 Load Delay Circuit

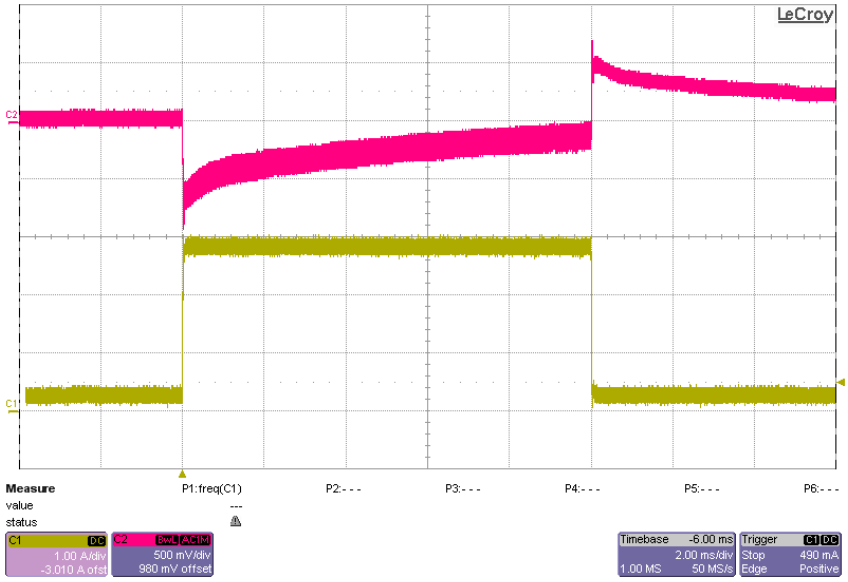
IEEE standard requires at startup, the PD does not consume more than 13W for 80ms. Typically, there are provisions (startup delays) in the end-product load that satisfies this requirement.
Resistive loads are typically used for evaluation. The main purpose of the Load Delay Circuit is to delay a high-current resistive load and prevent PSE hiccup during startup.

The 19V output voltage is shown in the scope plot below. There is 230ms delay before the load current is enabled. This can be adjusted through C39. The waveform was taken with the output loaded to 2.4A and the Load Delay Circuit enabled. Vin = 48V.



11 Load Transients

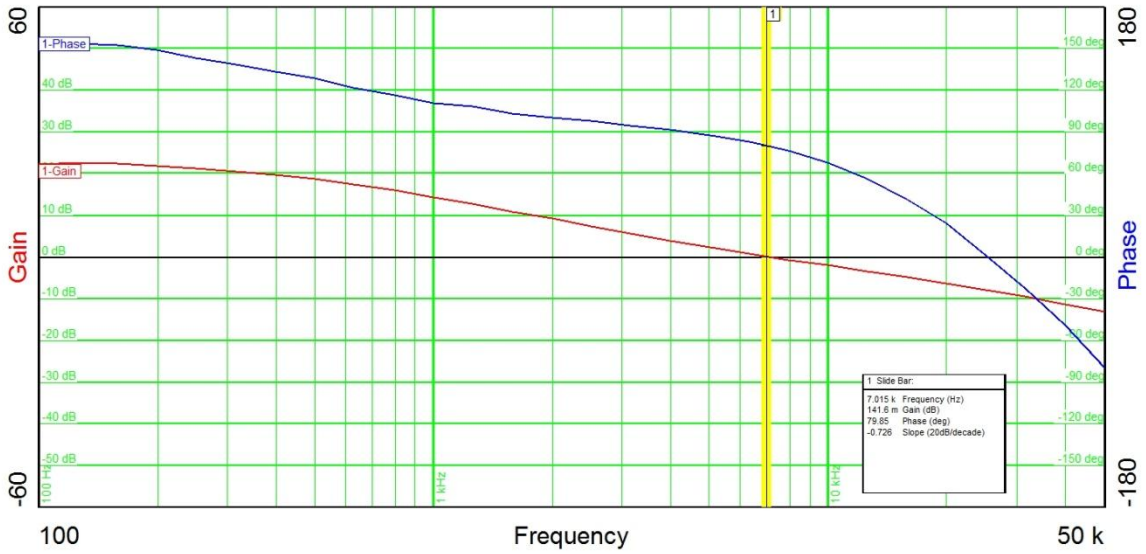
The scope plots below shows the 19V output voltage when the load current is pulsed from 0.29 to 2.9A at a 300A/ms slew rate. Vin = 48V.



12 Control Loop Gain / Stability

The table below shows the loop gain and phase margin. The output was loaded to 2.9A with a resistive load.

Input voltage	48VDC	
Gain/Phase	Crossover	Phase Margin
TIDA-00539	7kHz	80°


60
-60
Gain
180
-180
Phase
1-Phase
1-Gain
40 dB
30 dB
10 dB
0 dB
-10 dB
-20 dB
-30 dB
-40 dB
-50 dB
150 deg
120 deg
90 deg
60 deg
30 deg
0 deg
-30 deg
-90 deg
-120 deg
-150 deg
100 Hz
1 kHz
10 kHz
1
1 Slide Bar:
7.015 k Frequency (Hz)
141.6 m Gain (dB)
79.85 Phase (deg)
-0.726 Slope (20dB/decade)
100
Frequency
50 k

13 Thermal

The image below shows the thermal performance of TIDA-00539 at full load with 48V input.

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