TI Designs

Highly Efficient Power and Data Transmission Design for Isolated Low Power Applications

TI Designs

The TIDA-00459 provides a turnkey solution for the design and evaluation of sensor transmitters and other applications requiring isolated data transmission and isolated power conversion. The design is based on the LaunchPad™ form factor and showcases a unique power saving method for transmitting the data across the isolation barrier. The highly efficient onboard isolated DC/DC converter enables its use in low power applications and applications with limited input power budget like 4- to 20-mA loop powered systems.

Design Resources

TIDA-00459	Design Folder
MSP430FR5969	Product Folder
TPS60402	Product Folder
TPS62125	Product Folder
TPS715A33	Product Folder
TIDA-00245	Tools Folder
TIDA-00349	Tools Folder
TIDA-00167	Tools Folder
TIDA-00189	Tools Folder

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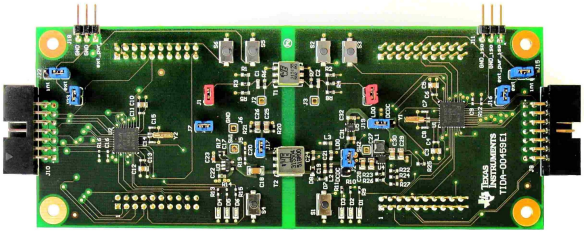
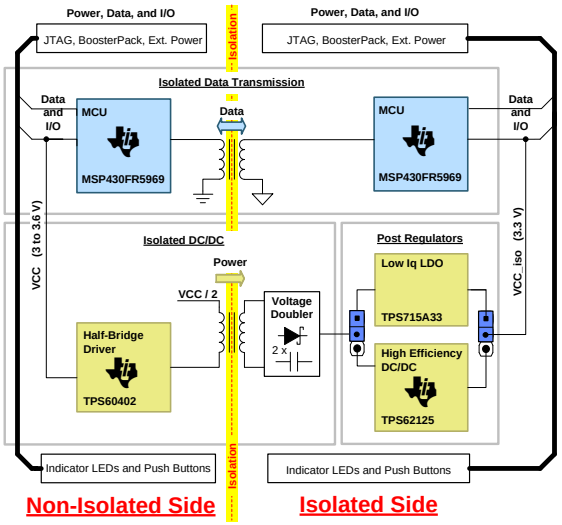
Design Features

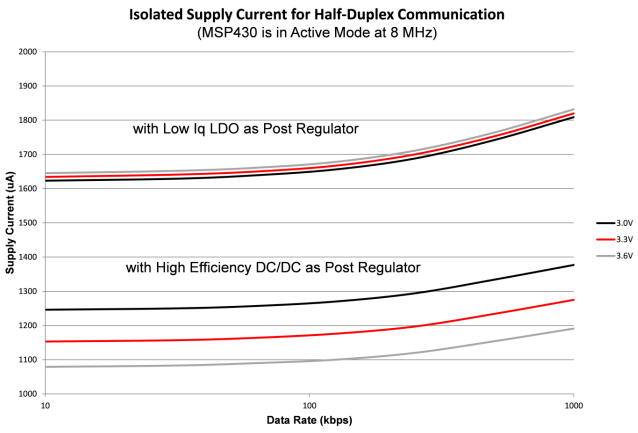
- Low-Power Isolated Single Wire Bidirectional Data Transmission up to 1 Mbps
- Highly Efficient, Optocoupler-Less Isolated DC/DC Converter With 3.3-V Output
- Fully Characterized Over 3- to 3.6-V Input and for Load Currents up to 10 mA
- Easily Configurable Board With LaunchPad Form Factor, Expandable by BoosterPack™ Plug-In Boards
- Flexible Use by Multiple Power Options and Programmable MCUs on Non-Isolated and Isolated Side

Featured Applications

- Factory Automation and Process Control
- Loop Powered 4- to 20-mA Transmitters, Other Sensors, and Field Transmitters
- Building Automation
- Portable Instrumentation







1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	3		3.6	V
T_A	Operating free-air temperature	–40		85	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)			16	MHz

Table 2. Isolated Data Transmission Path

PARAMETER	SPECIFICATION	MIN	TYP	MAX	UNIT
Data rate				1	Mbps
Overall system supply current for half-duplex communication with low Iq LDO as post regulator	Both CPUs in active mode at 8 MHz and bidirectional communication with 1 MBaud at 3.3 V		2750		µA
Overall system supply current for half-duplex communication with high efficiency DC/DC as post regulator	Both CPUs in Active Mode at 8 MHz and bidirectional communication with 1 MBaud at 3.3 V		2200		µA
Standby current with low Iq LDO as post regulator	System standby in LPM0 and receive ready at 3.3 V		605		µA
	System standby in LPM3 and receive ready at 3.3 V		175		µA
Standby current with high efficiency DC/DC as post regulator	System standby in LPM0 and receive ready at 3.3 V		530		µA
	System standby in LPM3 and receive ready at 3.3 V		195		µA
Shutdown current with low Iq LDO as post regulator	System shutdown current at 3.3 V		112		µA
Shutdown current with high efficiency DC/DC as post regulator	System shutdown current at 3.3 V		150		µA
FRAM write speed				8	MBps

Table 3. Total Power Path

ISOLATED DC/DC + LOW Iq LDO AS POST REGULATOR					
PARAMETER	**SPECIFICATION**	**OUTPUT VOLTAGE[1]**			**UNIT**
		MIN	**TYP**	**MAX**	
VOUT_LDO		3.135	3.300	3.465	V
PARAMETER	**SPECIFICATION**	**TYPICAL OUTPUT VOLTAGE / TYPICAL EFFICIENCY**			**UNIT**
		T_A = –40°C	**T_A = 25°C**	**T_A = 85°C**	
VOUT_LDO / η	VIN = 3 V, J19_IOUT = 10 µA	3.325 / 9.4	3.334 / 9.8	3.328 / 7.6	V / %
	VIN = 3 V, J19_IOUT = 100 µA	3.323 / 39.4	3.332 / 40.3	3.324 / 36.5	V / %
	VIN = 3 V, J19_IOUT = 1 mA	3.321 / 58.3	3.329 / 58.6	3.319 / 57.6	V / %
	VIN = 3 V, J19_IOUT = 10 mA	3.317 / 61.1	3.321 / 61.2	3.309 / 60.9	V / %
	VIN = 3.6 V, J19_IOUT = 10 µA	3.324 / 6.5	3.335 / 6.9	3.328 / 5.4	V / %
	VIN = 3.6 V, J19_IOUT = 100 µA	3.323 / 30.1	3.332 / 31.2	3.324 / 27.6	V / %
	VIN = 3.6 V, J19_IOUT = 1 mA	3.321 / 47.9	3.329 / 48.3	3.319 / 47.2	V / %
	VIN = 3.6 V, J19_IOUT = 10 mA	3.317 / 50.9	3.322 / 51.0	3.309 / 50.7	V / %
ISOLATED DC/DC + HIGH EFFICIENCY DC/DC AS POST REGULATOR					
PARAMETER	**SPECIFICATION**	**OUTPUT VOLTAGE[1]**			**UNIT**
		MIN	**TYP**	**MAX**	
VOUT_DCDC		3.200	3.333	3.469	V
PARAMETER	**SPECIFICATION**	**TYPICAL OUTPUT VOLTAGE / TYPICAL EFFICIENCY**			**UNIT**
		T_A = –40°C	**T_A = 25°C**	**T_A = 85°C**	
VOUT_DCDC / η	VIN = 3 V, J19_IOUT = 10 µA	3.334 / 8.1	3.326 / 7.9	3.324 / 6.1	V / %
	VIN = 3 V, J19_IOUT = 100 µA	3.333 / 43.0	3.325 / 43.3	3.323 / 38.1	V / %
	VIN = 3 V, J19_IOUT = 1 mA	3.332 / 74.4	3.323 / 76.3	3.321 / 76.1	V / %
	VIN = 3 V, J19_IOUT = 10 mA	3.332 / 73.6	3.324 / 74.3	3.321 / 74.6	V / %
	VIN = 3.6 V, J19_IOUT = 10 µA	3.336 / 5.8	3.326 / 5.8	3.324 / 4.4	V / %
	VIN = 3.6 V, J19_IOUT = 100 µA	3.335 / 35.6	3.325 / 36.0	3.324 / 30.6	V / %
	VIN = 3.6 V, J19_IOUT = 1 mA	3.333 / 72.5	3.324 / 74.3	3.322 / 72.8	V / %
	VIN = 3.6 V, J19_IOUT = 10 mA	3.333 / 76.5	3.323 / 77.5	3.321 / 77.8	V / %

(1) Based on the datasheet specifications of the post regulators used

Table 4. Isolated DC/DC

PARAMETER	COMMENT				
Type of converter	Half-bridge on primary, voltage doubler on secondary				
Loop control	Open-loop, optocoupler-less				
Transformer insulation dielectric	Functional, 1500-V AC 1 min, 1875-V AC 1 sec				
PARAMETER	**SPECIFICATION**	**VALUE**			**UNIT**
		MIN	**TYP**	**MAX**	
VCC_IN	Input voltage range	3.0		3.6	V
PARAMETER	**SPECIFICATION**	**TYPICAL OUTPUT VOLTAGE / TYPICAL EFFICIENCY**			**UNIT**
		T_A = –40°C	**T_A = 25°C**	**T_A = 85°C**	
J24_VOUT / $\eta_{IsolatedDC/DC}$	VIN = 3 V, J24_IOUT = 10 µA	5.6 / 16.0	5.8 / 18.5	5.5 / 12.7	V / %
	VIN = 3 V, J24_IOUT = 100 µA	4.8 / 58.5	5.0 / 63.0	5.2 / 59.6	V / %
	VIN = 3 V, J24_IOUT = 1 mA	4.6 / 81.4	4.8 / 85.1	5.0 / 86.9	V / %
	VIN = 3 V, J24_IOUT = 10 mA	4.1 / 75.4	4.2 / 77.3	4.2 / 78.0	V / %
	VIN = 3.6 V, J24_IOUT = 10 µA	7.0 / 14.4	7.3 / 16.5	6.7 / 11.0	V / %
	VIN = 3.6 V, J24_IOUT = 100 µA	5.9 / 55.4	6.1 / 59.0	6.3 / 54.0	V / %
	VIN = 3.6 V, J24_IOUT = 1 mA	5.7 / 82.6	5.9 / 85.9	6.1 / 87.0	V / %
	VIN = 3.6 V, J24_IOUT = 10 mA	5.2 / 79.5	5.3 / 81.1	5.3 / 81.8	V / %

Table 5. Post Regulator

PARAMETER	COMMENT				
Type of post regulator	Low Iq LDO or high efficiency DC/DC; selectable by jumper				
J24_VIN	Input voltage; equal to output voltage of isolated DC/DC (J24_VOUT)				
LOW Iq LDO					
PARAMETER	**SPECIFICATION**	**VALUE(1)**			**UNIT**
		MIN	**TYP**	**MAX**	
VIN_operating	Operating input voltage range	3.6		24	V
Iq	Ground pin current		3.2	5.8	V
VOUT	Output voltage (VIN > 4.3 V)	3.135	3.3	3.465	V
V_{DO}	Dropout voltage (IOUT = 10 mA; VOUT = $VOUT_{(NOM)}$ – 0.1 V)		84	140	V
η	Efficiency	See Section 7.1.5			
HIGH EFFICIENCY DC/DC					
PARAMETER	**SPECIFICATION**	**VALUE(1)**			**UNIT**
		MIN	**TYP**	**MAX**	
VIN_operating	Operating input voltage range	3		17	V
VIN_startup	VIN at which converter starts	4.122	4.32	4.535	V
VIN_stop	VIN at which converter stops	3.012	3.133	3.283	V
VOUT	Output voltage	3.2	3.333	3.469	V
η	Efficiency	See Section 7.1.4			

(1) Based on the datasheet specifications of the post regulators used

2 System Description

The main purpose of this design is to provide a highly efficient low-power solution for avoiding ground loops in signal conditioning and bidirectional data transmission applications by providing isolation for the power path as well as for the data transmission path.

Because ground potential differences are common in a large variety of different applications such as factory automation, process control, building automation, energy harvesting and portable instrumentation, some sensors (like thermocouple sensors) and signal conditioning circuitry must be galvanically isolated from the ground. In such isolated sensor transmitters, both the power supply and the data transmission path have to be isolated (Figure 1).

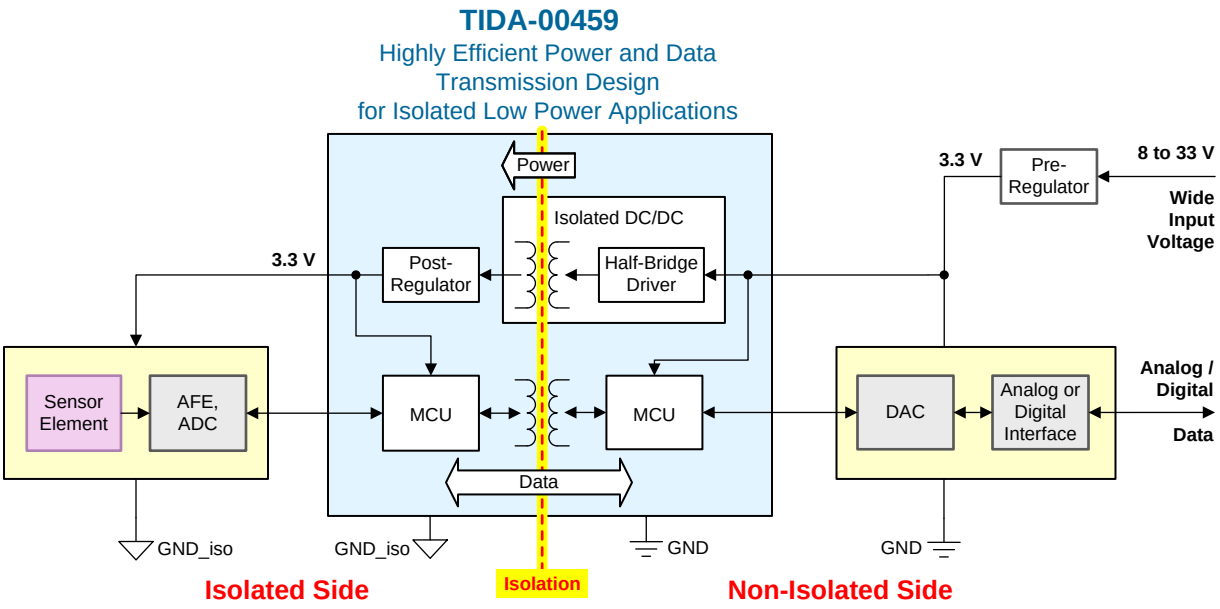


Figure 1. TIDA-00459 Used in Isolated Sensor Transmitter System

The data transmission path in such applications can be either unidirectional or bidirectional, of which the bidirectional is more challenging.

A bidirectional communication is needed in systems in which not only the isolated sensor side sends the data, but also the host provides (for example, configuration data to the isolated sensor side). The main challenge of such a solution is the limited size within industry standard sensor transmitters and, in case of a loop-powered system, the overall current consumption.

A single-wire interface is crucial to ensure space and power consumption constrains. In the real application, one MCU (placed on the isolated side) takes care of the signal conditioning (linearization, calibration, data acquisition routine) while the second MCU (placed on the non-isolated side) takes care of the communication (in case of HART or more complex communications than just 4 to 20 mA) and sending different configurations to the isolated sensor side.

The other challenge is related to the low power level of such applications, often ranging from tens of milliwatts down into the sub-milliwatt range. While solutions are already available for high efficiency isolated DC/DC converters addressing an output power range above hundreds of milliwatts [1], the required isolated power solution needs to be uniquely efficient even at much lower power levels as previously mentioned. A high power efficiency enables applications with limited input power or input current budgets such as loop powered 4- to 20-mA transmitters or bus powered applications where the bus power is limited.

Figure 1 shows a typical fully isolated sensor transmitter system where the TIDA-00459 is powered on the non-isolated system side by a pre-regulated non-isolated 3.3-V rail. The TIDA-00459 is then used to power the signal conditioning and signal processing of the isolated side. The isolated rail generated by the TIDA-00459 is a well regulated isolated 3.3 V, eliminating the need for an additional 3.3-V post regulator on the isolated side.

The galvanic isolation of the TIDA-00459 is transformer based and has an inherent life span advantage over an optocoupler isolator. Industrial devices typically operate for much longer periods of time than consumer electronics. Therefore, maintenance of effective isolation over a period of over 15 years is important. In systems requiring galvanic isolation between the transmitter and the receiver, the commonly used coupling element are therefore transformers.

The TIDA-00459 provides functional isolation for the data transmission and power path between the non-isolated and the isolated system side. The design can also be used in similar applications where the functional isolation of the used transformers is sufficient. Other use cases may require modified transformers to fulfill more stringent isolation requirements.

3 Block Diagram

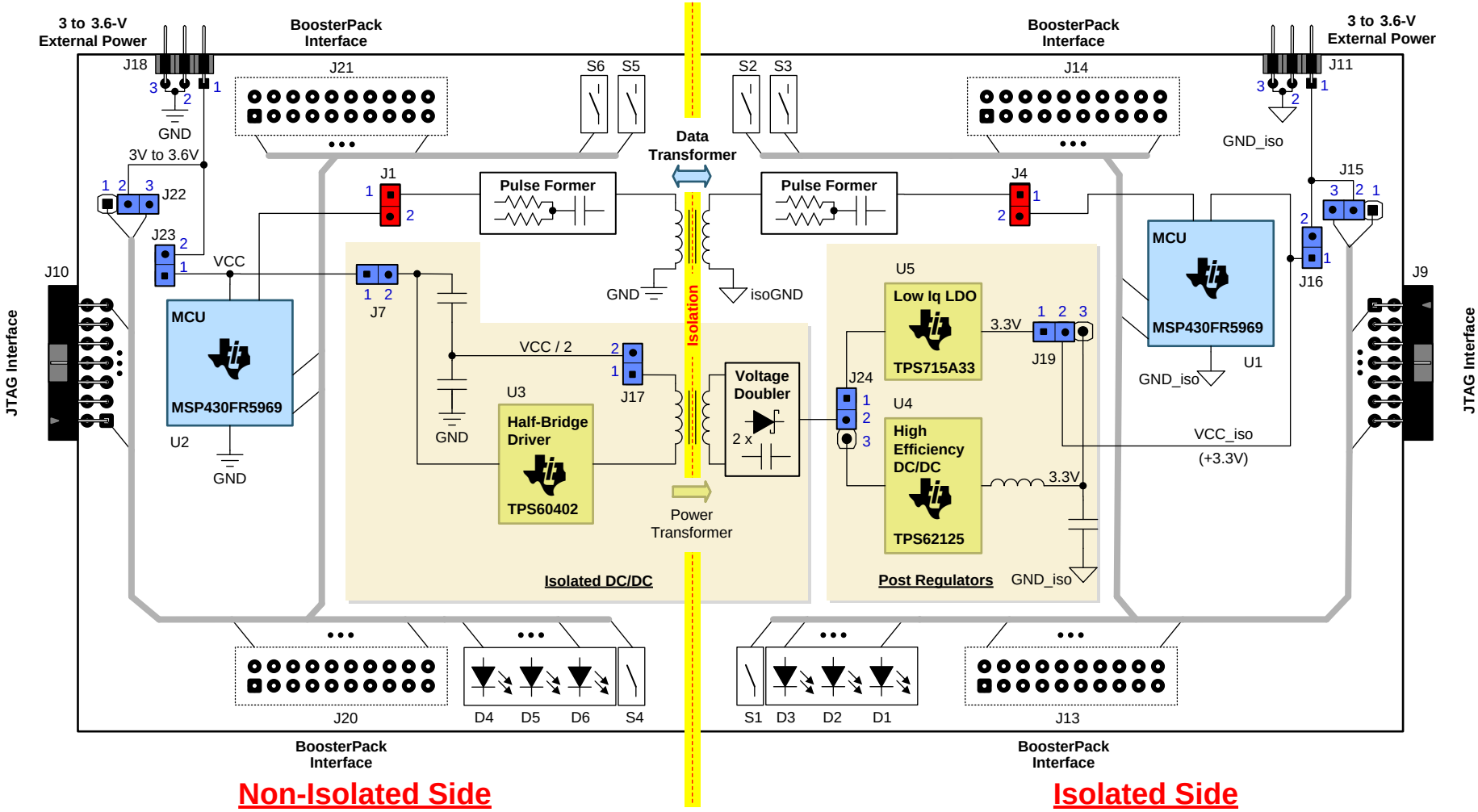


Figure 2. TIDA-00459 Block Diagram

Figure 2 shows the block diagram of the TIDA-00459. The design consists of:

- the isolated bidirectional data transmission path
- the isolated power path
- the peripherals and interface components

The block diagram is split into the non-isolated and the isolated side, both separated from each other by the isolation barrier. Each side has a dedicated ground (GND on the non-isolated side, GND_iso on the isolated side).

Isolated Bidirectional Data Transmission Path

This design provides a method for transmitting digital data bidirectional over an isolation boundary from one MCU to another MCU using a single isolation component, a pulse transformer. The use of the transformers to cross the isolation boundary is typical in industrial applications due to their robustness, low-power consumption, and low cost. The challenge of such a solution is first of all the limited size within sensor transmitters (industry standard) and in case of a loop-powered system the overall current consumption.

For the MCUs, the MSP430FR5969 has been chosen because of its ULP system architecture, integrated comparator, and integrated UART module, which is used for the isolated data transmission.

Isolated Power Path

The power path of the design spans from the header J7 on the non-isolated side to the header J19 on the isolated side. The input voltage on the non-isolated side is a 3.3-V rail, which can range from 3 to 3.6 V and can be provided either by the JTAG interface (J10) or by the connector J18. The isolation barrier is crossed by the power transformer of the isolated DC/DC. The isolated DC/DC is using a half-bridge topology on the primary side and uses a voltage doubler on the secondary. The half bridge is running with a fixed frequency and with a fixed 50% duty cycle. It uses an open-loop control approach, which makes the use of optocoupler needles. The design offers two different user-selectable post regulators on the isolated side: a low Iq LDO (U5) as well as a high efficiency DC/DC (U4). The selection of the post regulator is done by a simple jumper setting (J24, J19). The output voltage on the isolated side of the power path is a regulated 3.3-V, which can be loaded with up to 10 mA. It is used to power the MCU (U1) on the isolated side. This isolated and regulated 3.3-V rail is brought out on the connector J11 and the BoosterPack connector J13 to power external circuits (sensor element, AFE, ADC, and so on) on the isolated side as shown in Figure 1.

Peripherals and Interface Components

To showcase the functionality, the hardware of the TIDA-00459 includes BoosterPack connectors on both sides of the isolation. BoosterPack plug-in modules allow the user to extend the functionality of the hardware and add features like wireless connectivity, capacitive touch, temperature sensing, displays, and much more (www.ti.com/boosterpack). The design files include design considerations, block diagrams, schematics, bill of materials (BOM), layer plots, Altium files, Gerber files, and MSP430™ firmware.

3.1 Highlighted Products

3.1.1 MSP430FR5969

The TIDA-00459 reference design uses the MSP430 ULP ferroelectric RAM (FRAM) platform. The MSP430 combines a uniquely embedded FRAM and a holistic ULP system architecture, allowing innovators to increase performance at lowered energy budgets. FRAM is much faster to write to than flash and has near infinite endurance, which means that in a remote sensor, data could be written more often for improved data accuracy, or it could collect data for a longer period of time. Due to the lack of a charge pump, FRAM enables lower average and peak power during writes. Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current is included in the active mode current consumption numbers already.

The bitwise programmable memory can be used at the programmer's convenience for data or program storage. It also does not require things like pre-erasure of segments before a write. Security is another area where FRAM can offer advantages. FRAM is inherently more secure due to its makeup, and de-layering is not effective. FRAM is also resistant to alpha radiation and SER effects. There are two main differences between FRAM and static RAM (SRAM):

- FRAM is nonvolatile; that is, it retains contents on loss of power.
- The embedded FRAM on MSP430 devices can be accessed (read or write) at a maximum speed of 8 MHz.

In comparison to MSP430 flash, FRAM:

- Is very easy to use
- Requires no setup or preparation such as unlocking of control registers
- Is not segmented and each bit is individually erasable, writable, and addressable
- Does not require an erase before a write
- Allows low-power write accesses (does not require a charge pump)
- Can be written to across the full voltage range (1.8 to 3.6 V)
- Can be written to at speeds close to 8MBps (maximum flash write speed including the erase time is approximately 14 kBps)

Writing to FRAM does not require additional power when compared to reading from FRAM. The FRAM read current is included in the active mode current consumption numbers already. Table 6 summarizes the FRAM advantages versus other memory technologies.

Table 6. FRAM Advantages

SPECIFICATION	FRAM	SRAM	FLASH
Write speed per word	125 ns	< 125 ns	85 us
Erase time	No pre-erase required	No pre-erase required	23 ms for 512 bytes
Bit-wise programmable	Yes	Yes	No
Write endurance	10^{15} write per erase cycle	N/A	10^{15} write per erase cycle
Nonvolatile	Yes	No	Yes
Internal write voltage	1.5 V	1.5 V	12 to 14 V (charge pump required)

Features:

- Embedded microcontroller
  - 16-bit RISC architecture up to 16-MHz clock
  - Wide supply voltage range (1.8 to 3.6 V; Minimum supply voltage is restricted by SVS levels.)
- Optimized ULP modes
  - Active mode: Approximately 100 µA/MHz
  - Standby (LPM3 with VLO): 0.4 µA (typical)
  - Real-time clock (LPM3.5): 0.25 µA (typical; RTC is clocked by a 3.7-pF crystal.)
  - Shutdown (LPM4.5): 0.02 µA (typical)

- ULP FRAM
  - Up to 64KB of nonvolatile memory
  - ULP writes
  - Fast write at 125 ns per word (64KB in 4 ms)
  - Unified memory = Program + Data + Storage in one single space
  - 10^{15} write cycle endurance
  - Radiation resistant and nonmagnetic
- Intelligent digital peripherals
  - 32-bit hardware multiplier (MPY)
  - Three-channel internal DMA
  - RTC with calendar and alarm functions
  - Five 16-bit timers with up to seven capture/compare registers each
  - 16-bit cyclic redundancy checker (CRC)
- High-performance analog
  - 16-channel analog comparator
  - 12-bit analog-to-digital converter (ADC) with internal reference and sample-and-hold and up to 16 external input channels
- Multifunction I/O ports
  - All pins support capacitive touch capability with no need for external components
  - Accessible bit-, byte-, and word-wise (in pairs)
  - Edge-selectable wake from LPM on all ports
  - Programmable pullup and pulldown on all ports
- Code security and encryption
  - 128-bit or 256-bit AES security encryption and decryption coprocessor
  - Random number seed for random number generation algorithms
- Enhanced serial communication
  - eUSCI_A0 and eUSCI_A1 support
    - UART with automatic baud-rate detection
    - IrDA encode and decode
    - SPI at rates up to 10 Mbps
  - eUSCI_B0 supports
    - I^2C with multiple slave addressing
    - SPI at rates up to 8Mbps
  - Hardware UART and I^2C bootstrap loader (BSL)
- Flexible clock system
  - Fixed-frequency DCO with 10 selectable factory-trimmed frequencies
  - Low-power low-frequency internal clock source (VLO)
  - 32-kHz crystals (LFXT)
  - High-frequency crystals (HFXT)
- Development tools and software
  - Free professional development environments with EnergyTrace™++ technology development kit (MSP-TS430RGZ48C)

For complete module descriptions, See the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* (SLAU367).

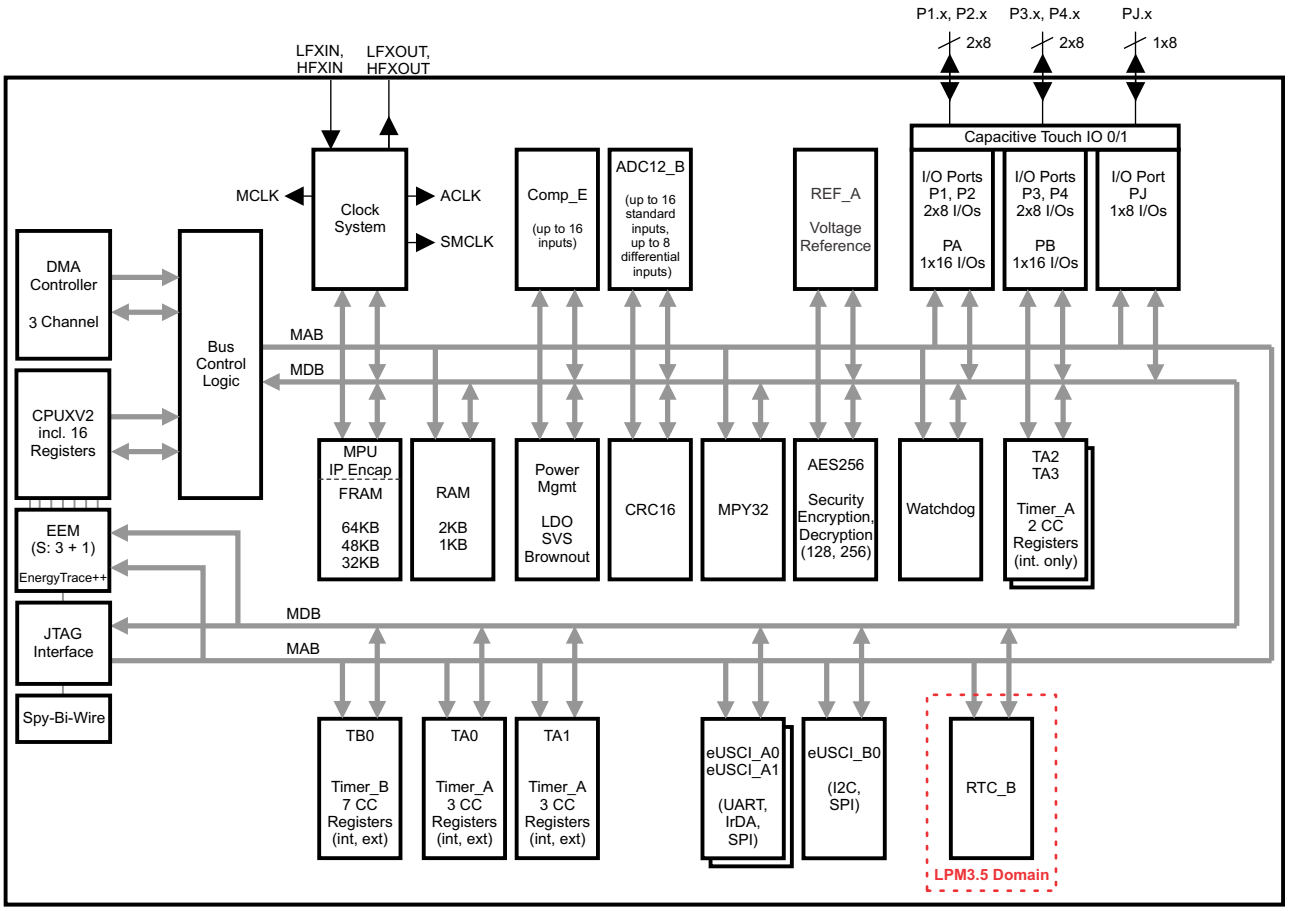


Figure 3. MSP430FR5969 Block Diagram

The MSP430 ULP FRAM portfolio consists of a diverse set of devices featuring FRAM, the ULP 16-bit MSP430 CPU, and intelligent peripherals targeted for various applications. The Comparator_E (COMP_E) and the eUSCI_A modules are used in this application.

The COMP_E module supports precision slope ADCs, supply voltage supervision, and monitoring of external analog signals. Features of COMP_E include:

- Inverting and non-inverting terminal input multiplexer
- Software-selectable RC filter for the comparator output
- Output provided to Timer_A capture input
- Software control of the port input buffer
- Interrupt capability
- Selectable reference voltage generator and voltage hysteresis generator
- Reference voltage input from shared reference
- ULP comparator mode
- Interrupt driven measurement system for low-power operation support

The enhanced universal serial communication interface A (eUSCI_A) supports multiple serial communication modes with one hardware module. In this design, the UART mode is used. UART mode features include:

- 7-bit or 8-bit data with odd, even, or non-parity
- Independent transmit and receive shift registers
- Separate transmit and receive buffer registers
- LSB-first or MSB-first data transmit and receive
- Built-in idle-line and address-bit communication protocols for multiprocessor systems
- Receiver start-edge detection for auto wake up from LPMx modes (wake up from LPMx.5 is not supported)
- Programmable baud rate with modulation for fractional baud-rate support
- Status flags for error detection and suppression
- Status flags for address detection
- Independent interrupt capability for receive, transmit, start bit received, and transmit complete

3.1.2 TPS60402

The TPS60402 [6] is used in a modified way to drive the power transformer T2 of the open loop isolated DC/DC in this TIDA-00459 reference design. The device was selected due to its integrated FETs which are sized for such low power application and which are usable as half-bridge driver. The TPS60402 comes furthermore with an internal oscillator generating the complementary 50% duty cycle control signal for the half-bridge FETs (Q1 and Q2) as illustrated in Figure 4. Finally, the device features a low quiescent current, which is mandatory to use in this design.

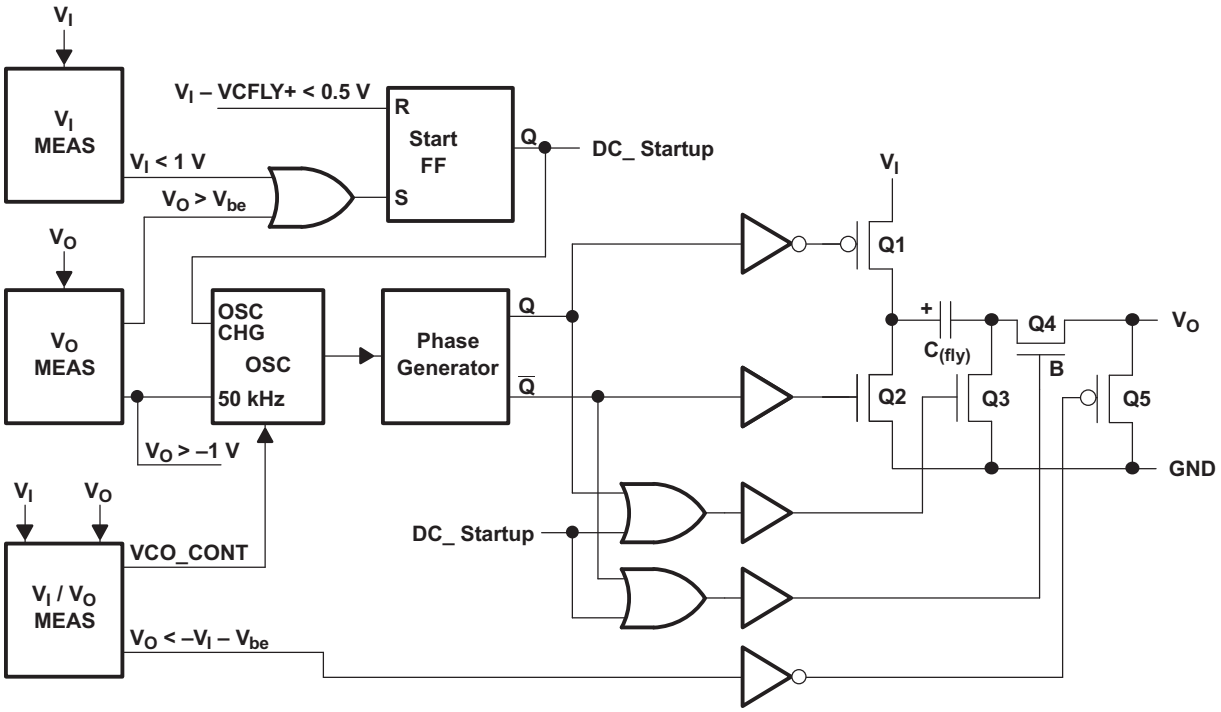


Figure 4. TPS60400 Family—Functional Block Diagram

The primary applicable and beneficial specifications of the TPS60400 device family can be summarized as follows:

- Input voltage range from 1.6 to 5.5 V
- Small 5-pin SOT23 package
- Integrated switches (FETs)
- Internal fixed frequency oscillator (for TPS60401 to TPS60403)
- Multiple switching frequency versions, as shown in Table 7
- Devices available with quiescent current down to 65 µA

Table 7. TPS60400 Family—Device Versions

PARAMETER	TPS60400	TPS60401	TPS60402	TPS60403
Switching frequency (typ)	Variable switching frequency 50 to 250 kHz	20 kHz	50 kHz	250 kHz
Quiescent current (typ)	125 µA	65 µA	120 µA	425 µA

The TPS60402 was selected from the TPS60400 family. With a 50-kHz switching frequency, the TPS60402 offers a good trade-off between efficiency and solution size.

3.1.3 TPS715A33

The TPS715A33 [2] is an low Iq LDO, used as one of the two user selectable post regulators, generating a well regulated 3.3-V rail from the open-loop, isolated DC/DC's non-regulated output. An LDO-based post regulator is by far the simplest, less complex, and the most cost effective approach for doing the required post regulation. The specific device was selected due to its wide input voltage range, its low and load independent quiescent current (Iq), and the fact that the accuracy of its output voltage is specified down to 0 mA. The fixed 3.3-V output voltage version was chosen to simplify the design and to eliminate the additional tolerances and temperature drift of the external voltage setting resistors otherwise needed when the adjustable version would have been used (see Figure 5 and Figure 6).

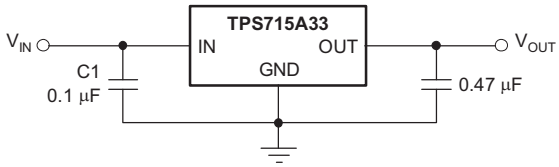


Figure 5. Typical Application Circuit (Fixed-Voltage Version)

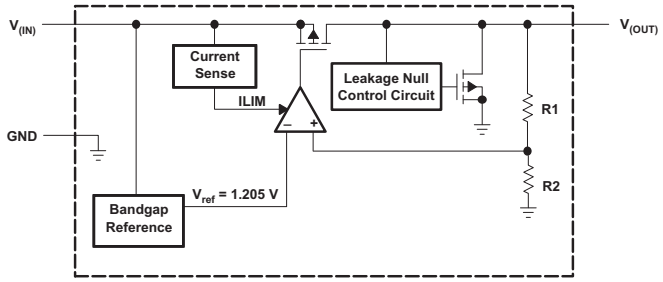


Figure 6. Functional Block Diagram (Fixed Version)

The TPS715A low-dropout voltage regulators (LDO) offer the benefits of high input voltage, low-dropout voltage, low-power operation, and miniaturized packaging. The devices, which operate over an input range of 2.5 to 24 V, are stable with any capacitor (> 0.47 µF). The high maximum input voltage combined with excellent power dissipation capability makes this part particularly well-suited to industrial and automotive applications. A PMOS pass element behaves as a low-value resistor. The low-dropout voltage, typically 670 mV at 80 mA of load current, is directly proportional to the load current. The low quiescent current (3.2 µA typically) is nearly constant over the entire range of output load current (0 to 80 mA). The TPS715A is available in 3×3-mm package ideal for high power dissipation and small 2×2-mm package ideal for handheld and ultra-portable applications. The 3×3-mm package is also available as a non-magnetic package for medical imaging applications.

Features:

- 24-V maximum input voltage
- Low 3.2-µA quiescent current at 80 mA
- Stable with any capacitor (≥ 0.47 µF)
- 80-mA specified current
- Available in fixed and adjustable (1.2 to 15 V) versions
- Specified current limit
- 3×3-mm and 2×2-mm SON packages
- –40°C to 125°C specified junction temperature range

3.1.4 TPS62125

The TPS62125 [3] is a high efficiency DC/DC buck converter, used as the other of the two user selectable post regulators, generating a well regulated 3.3-V rail from the open-loop, isolated DC/DC's non-regulated output. The use of this switching regulator provides a total power conversion efficiency of the complete power path, which is almost up to 30% higher (see Figure 44 to Figure 47) compared to the use of the low Iq LDO. The specific buck converter was selected due to its wide input voltage range, its user programmable undervoltage lockout (UVLO) and hysteresis, its ability to operate with 100% duty cycle, and its power good output (see Figure 7).

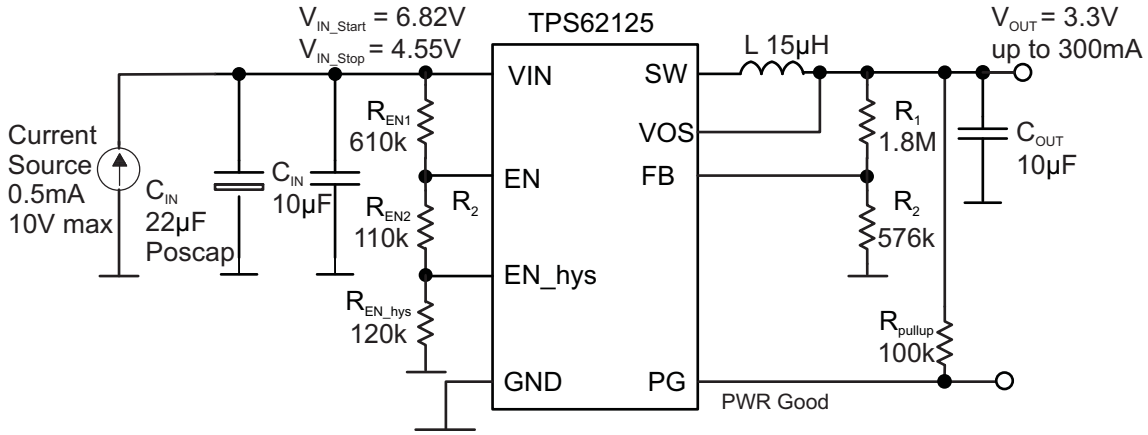


Figure 7. TPS62125 Operation From a Storage Capacitor Charged From a 0.5-mA Current Source

The user programmable UVLO and hysteresis can be helpful to support a smooth start-up of the DC/DC converter when it is powered from input sources with limited current budget. Similarly sources with an output current dependent output voltage are sensitive, when powering DC/DC converters. The isolated DC/DC can be considered as such an input source because its output voltage rises under extreme light or no-load conditions (see Figure 52 to Figure 55).

The maximum recommended supply voltage of 17 V provides more than enough of a margin, even when powered from the isolated DC/DC under no-load conditions. The feature set of the TPS62125 is furthermore complemented by an impressive high efficiency, even for low output currents ranging from the sub-mA range up to 10 mA and higher as illustrated by Figure 8.

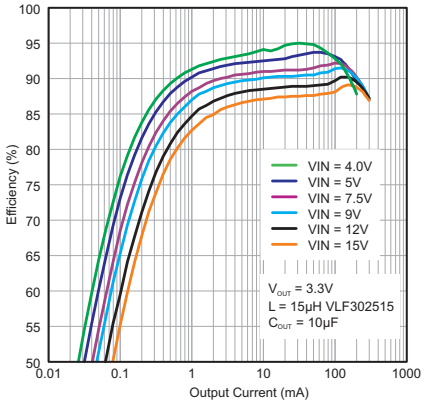


Figure 8. Efficiency versus Output Current, V_{OUT} = 3.3 V

The TPS62125 is a high efficiency synchronous step-down converter optimized for low and ultra-low power applications providing up to a 300-mA output current. The wide input voltage range of 3 to 17-V supports four cell alkaline and 1- to 4-cell Li-Ion batteries in series configuration as well as 9-V to 15-V powered applications. The device includes a precise low-power enable comparator that can be used as an input supply voltage supervisor (SVS) to address system specific power up and down requirements. The enable comparator consumes only 6-µA quiescent current and features an accurate threshold of 1.2 V typical as well as an adjustable hysteresis. With this feature, the converter can generate a power supply rail by extracting energy from a storage capacitor fed from high impedance sources such as solar panels or current loops. With its DCS-Control™ scheme the converter provides power save mode operation to maintain highest efficiency over the entire load current range. At light loads, the converter operates in PFM mode (pulse frequency modulation) and transitions seamlessly and automatically in pulse width modulation (PWM) mode at higher load currents. The DCS-Control scheme is optimized for low output ripple voltage in PFM mode in order to reduce output noise to a minimum and features excellent AC load regulation. An open drain power good output indicates once the output voltage is in regulation.

Features:

- Wide input voltage range: 3 to 17 V
- Input SVS with adjustable threshold / hysteresis
- Wide output voltage range: 1.2 to 10 V
- Typical 13-µA quiescent current
- 350-nA typical shutdown current
- Seamless power save mode transition
- DCS-Control scheme
- Low output ripple voltage
- Up to 1-MHz switching frequency
- Highest efficiency over wide VIN and VOUT range
- 100% duty cycle mode
- Power good open drain output
- Output discharge function
- Small 2×2-mm^2 SON 8-pin package

4 System Design Theory

4.1 Isolated Data Transmission Using MSP430FR5969

The UART square waveform for the data transmission is generated with the eUSCI_A module. The transmitter's DC component is blocked by a capacitor and the transformer passes only the AC components of the UART square waveform resulting in an impulse train across the secondary winding. The square waveform then needs to be recovered from the impulse train on the secondary winding. For restoring the signal, the internal Comparator_E of the MSP430FR5969 is used. The Comparator_E has a feature to generate a hysteresis for the output signal, which is used to restore the square waveform from the impulse train. The port pin of the MSP430 connected to the transmission circuit is P1.1. This pin is multiplexed with several functions like comparator output COUT and comparator input C1. When the MSP430 is configured as the transceiver, this pin is configured as COUT, and when the MSP430 is configured as the receiver this pin is configured as C1. Because the transformer is a symmetrical device (particularly one with 1:1 winding ratio) and the circuit is symmetrical as well, it is simple to reverse the data flow through it. In general, the transformers developed for T1/E1 telecom applications are well suited as the interface element in a galvanically isolated industrial transmitter. A number of suggested off the shelf transformers are listed in Table 8.

Table 8. Transformers

MANUFACTURER	P/N	MIN INDUCTANCE (µH)	ISOLATION
Würth Elektronik	750315105	400	1500-V AC
Würth Elektronik	750315155	400	1500-V AC
Coilcraft	S5394–CLB	400	1500-V AC

The functional diagram for the isolated data transmission can be seen in Figure 9.

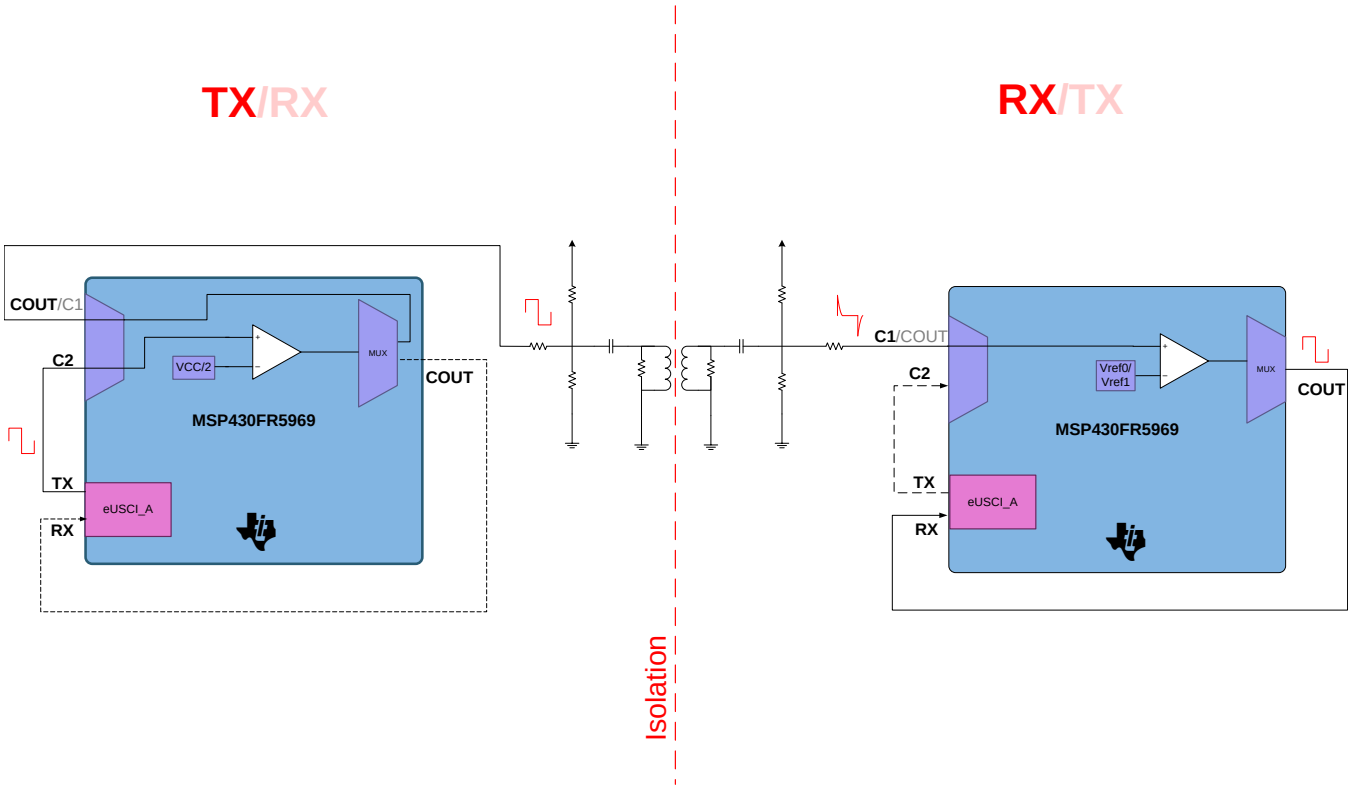


Figure 9. TIDA-00459 Functional Diagram for Isolated Data Transmission

4.1.1 Receiving Data

If the MSP430 is in receiving mode, the P1.1 pin connected to the transmission circuit is configured as comparator input C1. The comparator output COUT is mapped to a different pin P3.5, which is externally connected to the UART RX pin (see Figure 10).

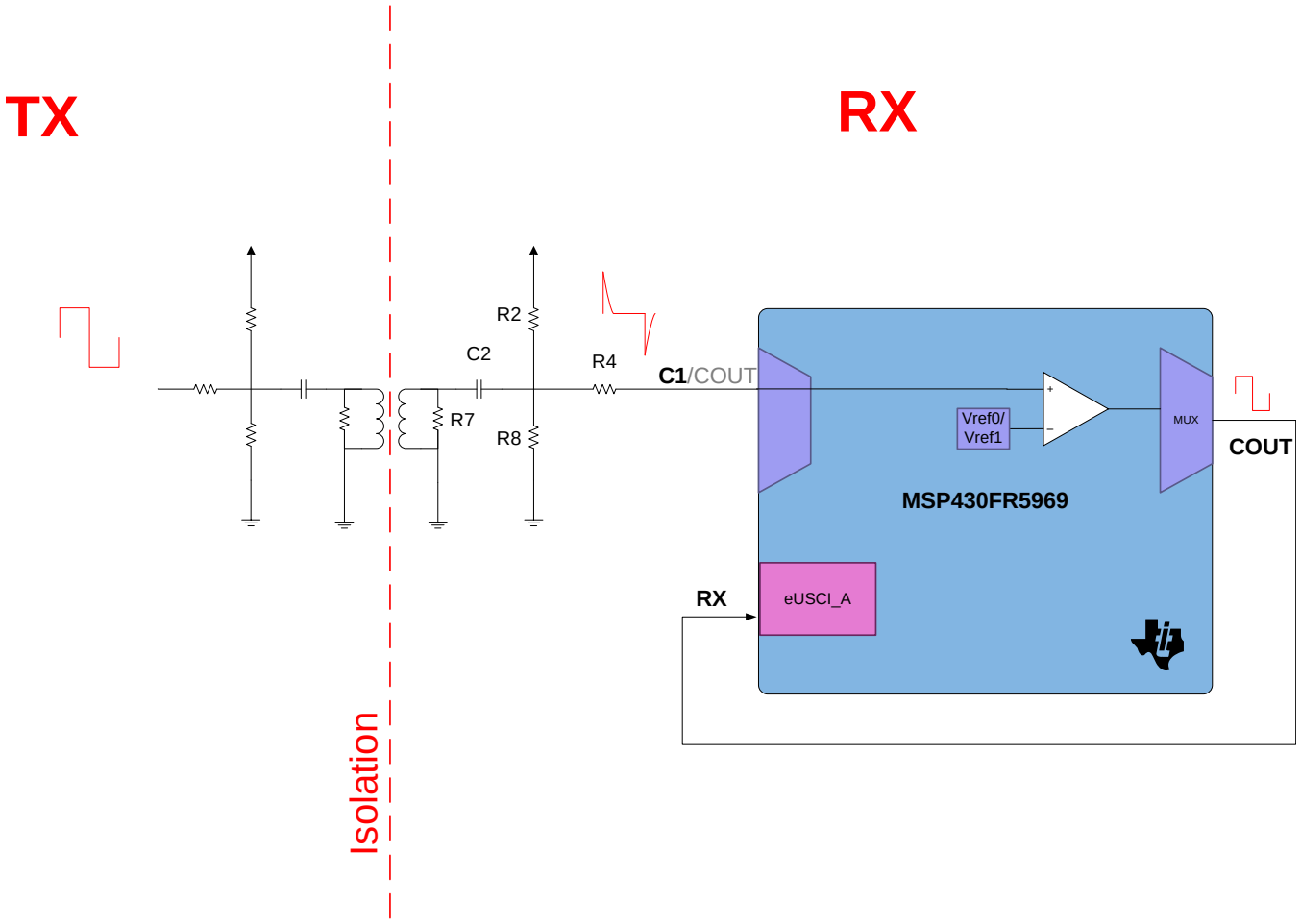


Figure 10. Receiving Block Diagram

The internal comparator of the MSP430 has two different reference voltages, Vref0 and Vref1. Vref1 is used while the output signal COUT of the comparator is 1, and Vref0 is used while COUT is 0. This allows the generation of a hysteresis without using external components. If the magnitude of the positive impulse exceeds the threshold Vref0 of the comparator, COUT goes high. This new COUT state will persist until an opposite polarity impulse appears across the secondary winding and exceeds the threshold Vref1 of the comparator. COUT will go low and this state will again persist until another positive pulse will occur. If no data is transmitted and no pulses occur, the voltage on the comparator input will be $V_{CC}/2$. As Vref0 is above $V_{CC}/2$ and Vref1 is below $V_{CC}/2$ the comparator output COUT will keep its state until a pulse in the opposite direction occurs. Figure 11 shows the output signal of the comparator depending on the pulses on the comparator input C1. The output signal of the comparator COUT on the receiver side looks again like the TX signal on the transmitter side. This COUT signal is then fed into the eUSCI_A module RX pin and the eUSCI_A module is used to decode the UART protocol.

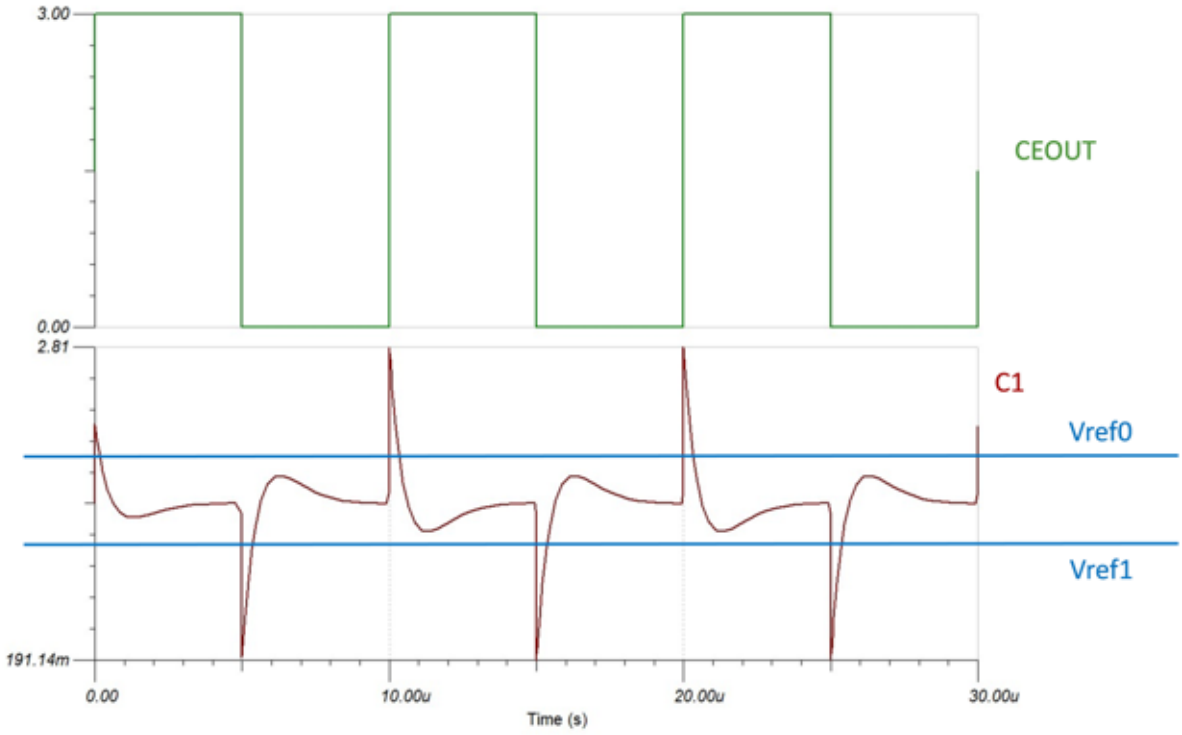


Figure 11. Comparator Input and Output Signal

4.1.2 Sending Data

In this circuit, the default VCC level on the connected MCU pin is VCC/2 when no data is transmitted. This is necessary to have the negative pulses not be going below 0 V as the I/O pins of the MSP430 do not accept negative voltage. But when voltage levels around VCC / 2 are applied to digital CMOS gates, parasitic current can flow from VCC to GND inside the pin. This parasitic current occurs if the input voltage is near the transition level of the gate. As the TX pin of the eUSCI module is a digital CMOS gate, it should not be directly connected to the transmission circuitry as parasitic current would flow from VCC to GND inside the pin. But on the P1.1/COUT/C1 pin, the port pin buffer can be disabled and this eliminates the parasitic current flow. Therefore, P1.1/COUT/C1 pin is connected to the transmission circuit. For transmitting, P1.1 is configured as comparator output COUT and the TX signal of the eUSCI module is connected to the comparator input pin C2 (see Figure 12). The inverting input of the comparator is connected to VCC/2 as a reference and the comparator output signal COUT then follows directly the TX signal on pin C2. To transmit data, the eUSCI_A module is used in UART mode. The transmitter's DC component is blocked by a capacitor and only the AC components of the TX square waveform are passed to the secondary winding of the transformer.

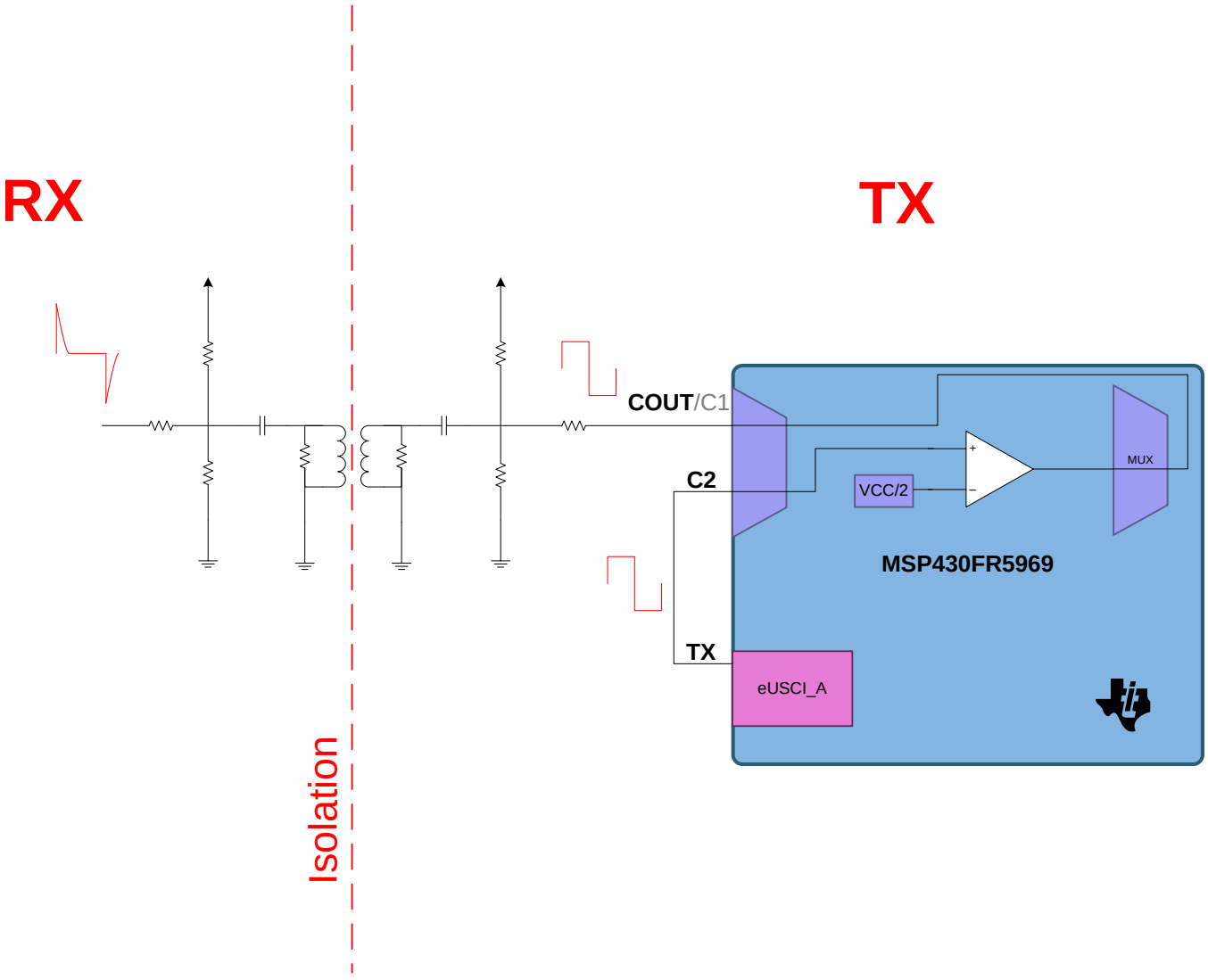


Figure 12. Transmitting Block Diagram

When one side of the MSP430FR5969 isolation is configured for RX and the other MSP430FR5969 on the other side is configured for TX, data transmission in one direction can be done continuously without any delay (see Figure 13). The turquoise signal is the transmitted data, and the green signal is the received signal on the other side of the isolation.

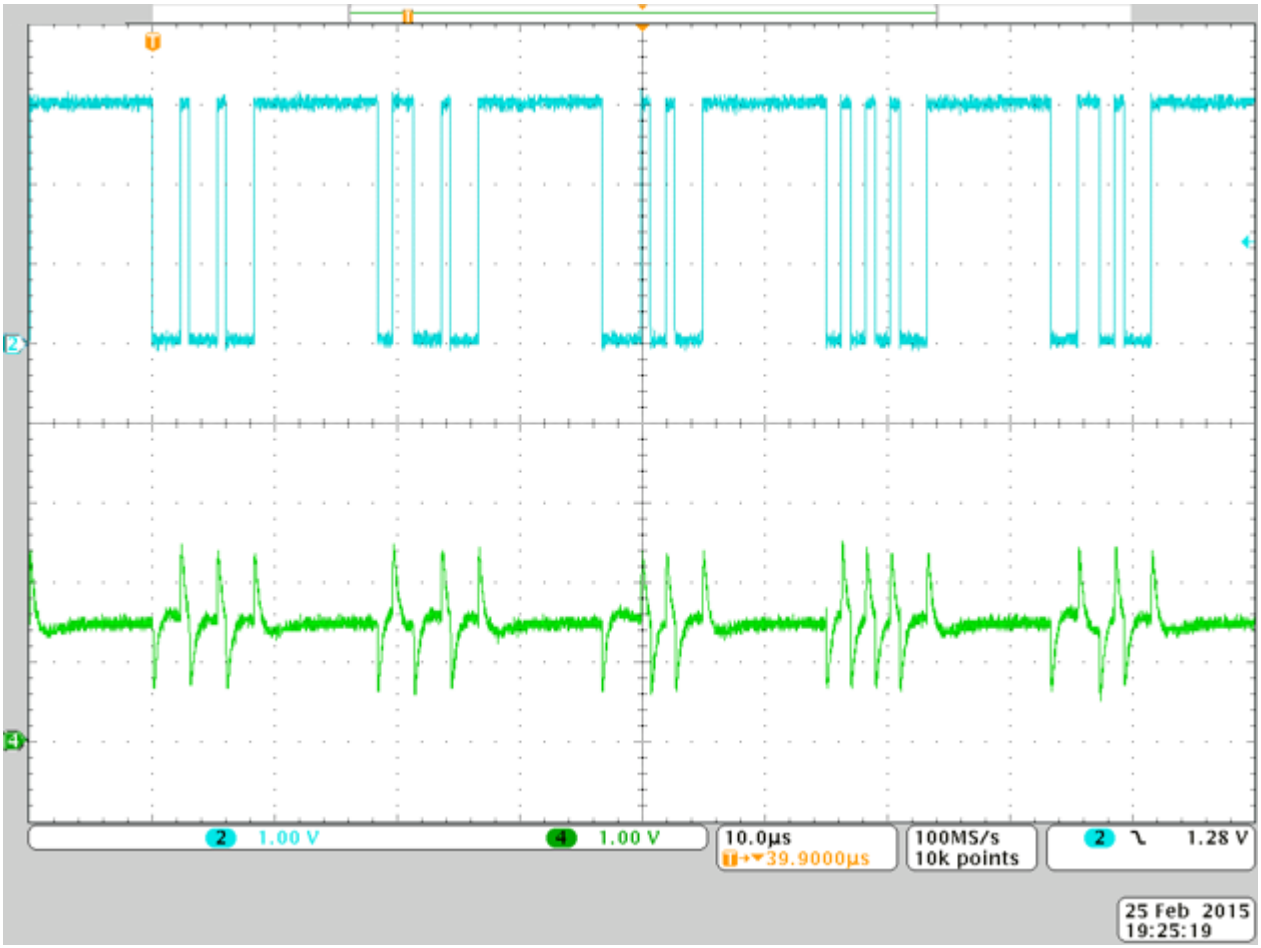


Figure 13. Transmitting Data

4.1.3 Half-Duplex Data Communication

Because the used transformer is a symmetrical device (1:1 winding ratio) and the circuit is symmetrical as well, data transmission can be done in both directions. The only thing that needs to be considered is to change the configuration of the MSP430FR5969 pins from transmitting to receiving and vice versa. When changing from transmitting to receiving, the capacitor C1 or C2 has to be discharged first and the voltage needs to settle at VCC/2 for receiving. This takes less than 10 µs. Then the transmission can start again in the other direction (see Figure 14). If the CPU is running with 8 MHz, this equates to about 80 CPU cycles. So this time should not be a problem as after receiving the last byte it usually takes much more CPU cycles until the received byte has been processed and a new transmission gets started. This idle time needs only be adhered to when changing the communication direction. Figure 14 shows the delay. The blue signal is restored from the turquoise signal on one side of the isolation, and the purple signal is restored from the green signal on the other side of the isolation. The turquoise and the green signals are the signals on the pins C1/COUT. The blue and the purple signals are the signals on the eUSCI input.

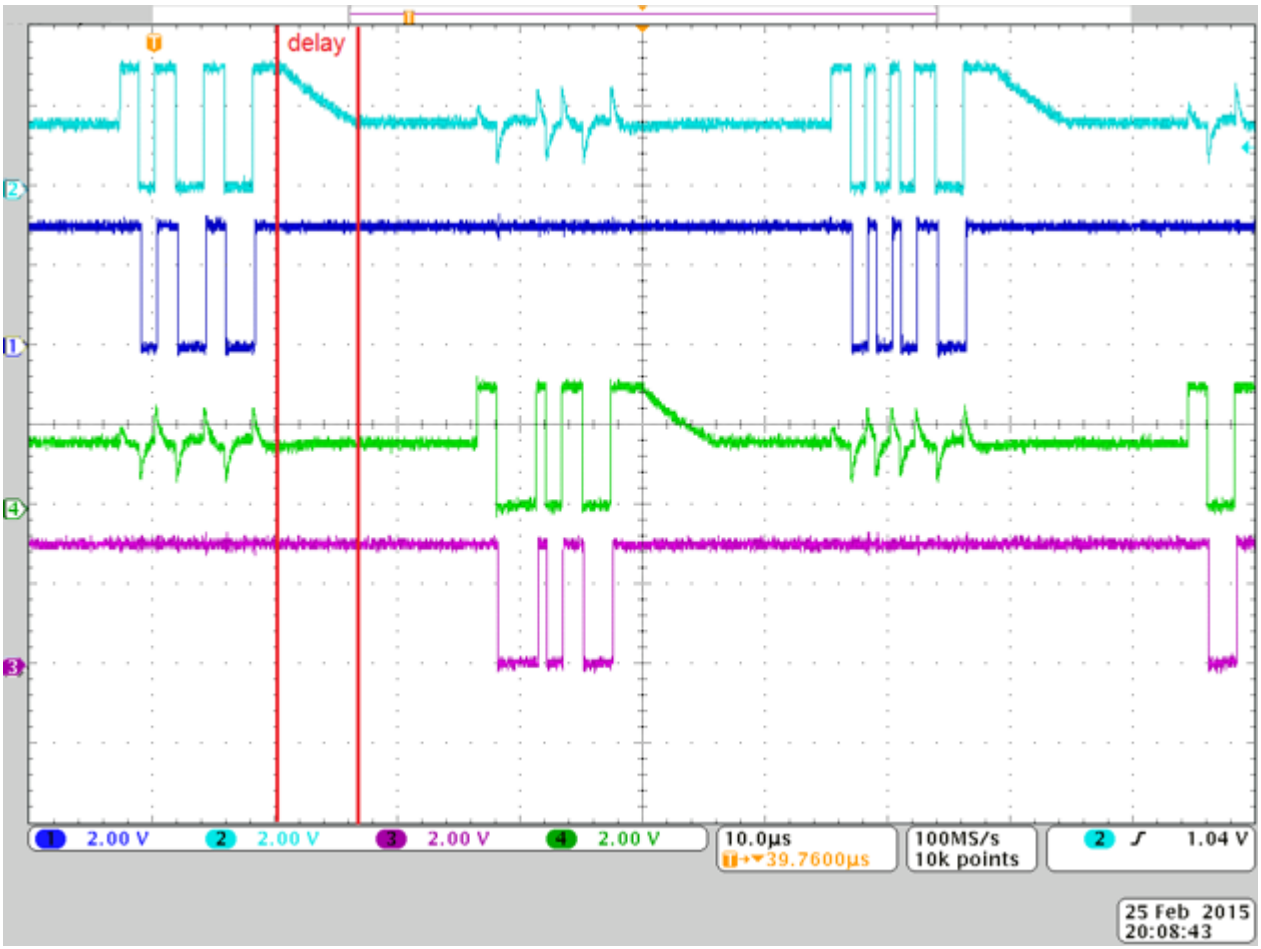


Figure 14. Half-Duplex Data Communication

4.1.4 Automated Baud-Rate Detection and Break and Synch Sequence Feature

The automatic baud-rate (ABR) detection feature of the eUSCI module allows matching of baud rates between the different isolations sides. For ABR detection, a data frame is preceded by a synchronization sequence that consists of a break and a synch field. A break is detected when 11 or more continuous zeros (spaces) are received. If the length of the break exceeds 21 bit times, the break timeout error flag UCBTOE is set. The synch field follows the break as shown in Figure 15.

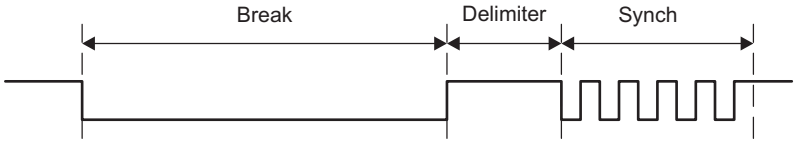


Figure 15. ABR Detection—Break/Synch Sequence

The synch field consists of the data 055h inside a byte field (see Figure 16). The synchronization is based on the time measurement between the first and the last falling edge of the pattern. The result of the measurement is transferred into the baud-rate control registers.

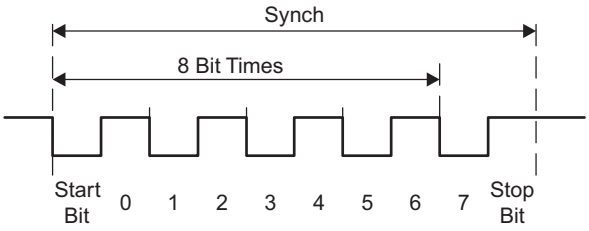


Figure 16. ABR Detection—Synch Field

The break field can be used to detect the beginning of a new frame. The UCDORM bit is used to control data reception in this mode. When UCDORM is set, all characters are received but not transferred into the eUSCI receive buffer UCA0RXBUF, and interrupts are not generated. When UCDORM is set, in UART mode with ABR detection, only the combination of a break and synch field sets the UCRXIFG. When a break/synch field is detected, the character following the break/synch field is transferred into UCA0RXBUF and the UCRXIFG interrupt flag is set. When a break/synch field is received, user software must reset UCDORM to continue receiving data. If UCDORM remains set, only the character after the next reception of a break/synch field is received. This feature can make the communication really robust in noisy environments. In addition the MSP430FR5969 includes a hardware CRC module (CRC16). The CRC16 produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

Figure 17 shows a scope screenshot of the communication using the ABR Detection and Break/Synch Sequence Feature followed by one data byte.

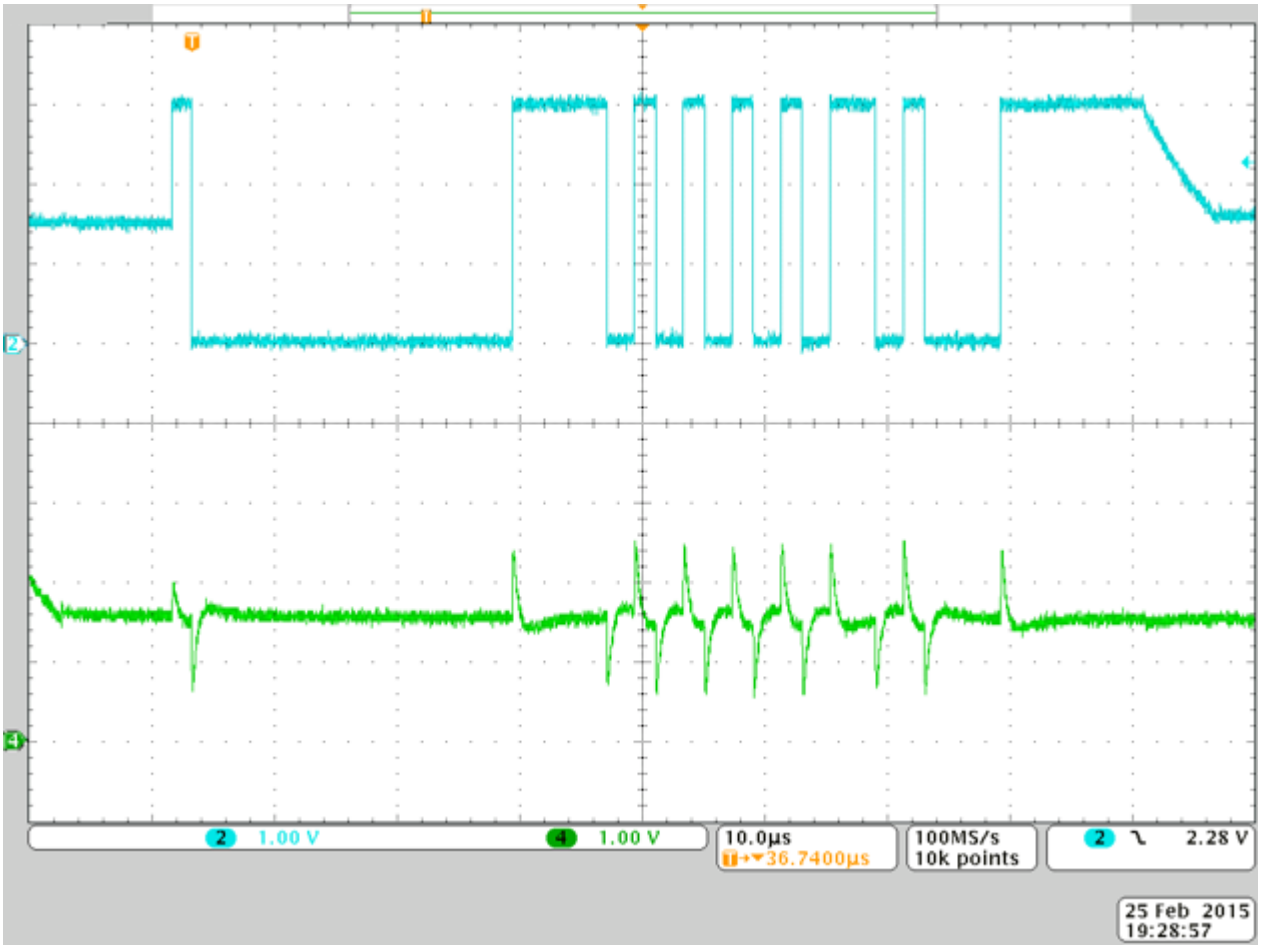


Figure 17. ABR Detection — Break/Synch Sequence Plus One Data Byte

4.2 Isolated Data Transmission Using an MSP430 With Port Mapping Functionality

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port pins. The port mapping is configured with user software. If an MSP430 with port mapping functionality (for example, MSP430F5172) is used for the isolated data transmission, the TX function of the eUSCI module can be directly mapped to the same pin as the comparator input C1. This makes the half-duplex data transmission easier as the comparator is only needed for receiving data. (see Figure 18).

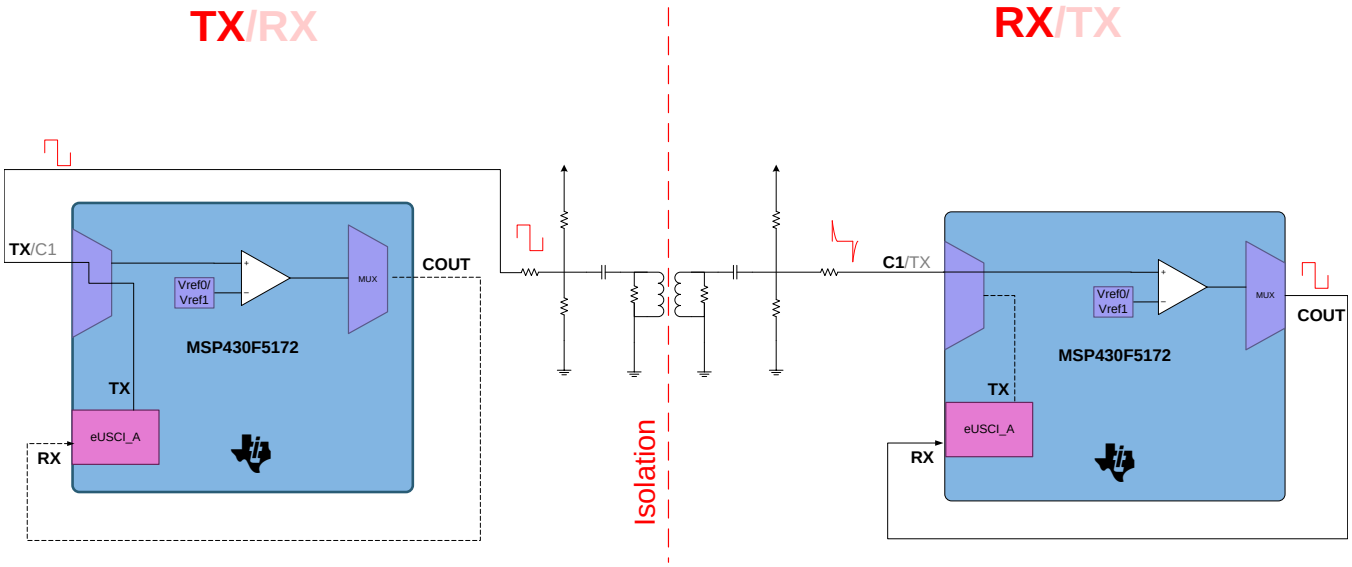


Figure 18. Isolated Data Transmission With MSP430F5172

4.3 Isolated Power Conversion

As outlined in Section 3, the complete power path consists of the isolated DC/DC converter and two different post regulators. The post regulator to be used can be selected by the user.

4.3.1 Isolated DC/DC Converter

The isolated DC/DC converter uses the 3.3-V VCC_IN, which can vary between 3 and 3.6 V as its input voltage VIN and converts it into the isolated VOUT, labeled as VOUT_isoDCDC in Figure 19.

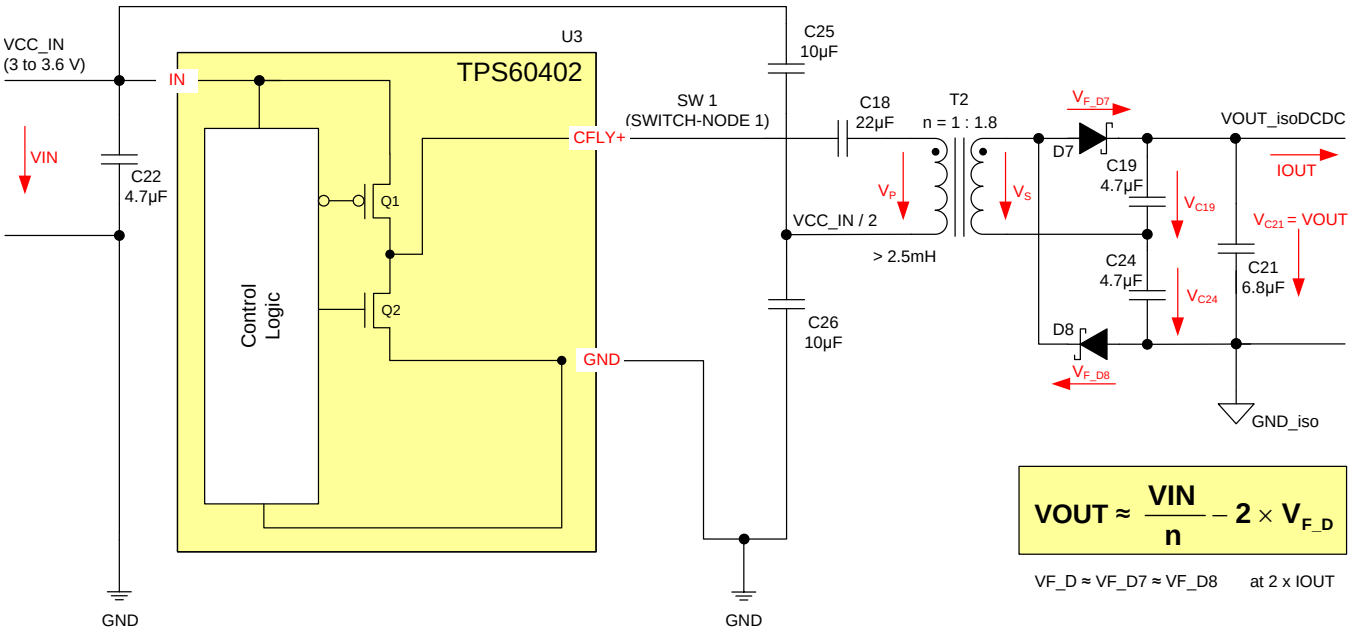


Figure 19. Simplified Schematic of Isolated DC/DC

C22 serves as an input bypass capacitor. C25 and C26 are the capacitors of the capacitive voltage divider, providing a fixed voltage of VCC/2 to one end of the primary winding of the transformer. The other end of the winding is driven by an integrated half-bridge stage inside the half-bridge driver. C18 serves as DC blocking capacitor, blocking any DC voltage on the primary winding that might otherwise cause flux walking and saturation of the transformer core. The transformer T2 is the main passive component of the design and provides the isolation between the primary (non-isolated) side and the secondary (isolated) side. The transformer construction determines the class of isolation, which is functional isolation in the case of this design.

Full details of the selection of the power topology, component selection, theory of operation, and the design procedure can be found in the related TI Designs TIDA-00349 [7] and TIDA-00167 [8]. The topology and design for the isolated DC/DC have been selected and was done with keeping the goal for achieving highest efficiency at ultra-low output power levels in mind.

To best utilize the transformer and to achieve a high efficiency, this reference design uses an open-loop control approach and a half-bridge topology on the primary side. The primary winding of the half-bridge transformer T2 is driven with a fixed 50% duty cycle in both directions of the hysteresis curve of the core of the transformer. The fixed 50% duty cycle and the open-loop control ensures that the isolated DC/DC converter is always working at an optimal operating condition—energy transfer from the primary to the secondary side of the transformer takes place over the full period of the switching frequency. As a result, the output voltage VOUT of the isolated DC/DC depends mainly on its input voltage VIN, on the turns ratio n of the transformer, and on the forward voltage V_{F_D} of the diodes D7 and D8.

Beside the optimal core utilization, the half-bridge topology does not need a tapped primary side winding as the push-pull topology requires. So the half-bridge topology ensures an optimal copper utilization of the primary winding as well.

To further keep the goal of getting a maximum efficiency at the ultra-low power levels, all losses need to be minimized. The quiescent current of almost all ICs with integrated power MOSFETs targeted for low-power isolated DC/DC converters is too high (hundreds of microamps up to milliamps) to finally provide a high enough efficiency. Even worse, in most cases the quiescent current is specified with the devices not even switching. As soon as they start switching, their switching losses will raise or lower the efficiency significantly—the higher the switching frequency, the higher the switching losses will be (which lowers the efficiency). Therefore, switching frequencies in the range of tens of kilohertz are better suited than using hundreds of kilohertz.

While a low switching frequency reduces the switching losses, another challenge appears as outlined in greater detail in Section 5.3 of the TIDA-00349 reference design [7]: The primary winding of the transformer, which represents the magnetizing inductance Lm, sees almost the full primary voltage $V_{Lm} \approx V_P$, which is applied for a relatively long time when operated at a low switching frequency. This leads to a high $\int V_{Lm} dt$, also called the V-s product. The transformer used in the isolated DC/DC needs to withstand this V-s product without going into saturation. This is best demonstrated in Figure 21.

The gray hysteresis curve in Figure 21 is also known as the B-H curve and is used to characterize the core material of the transformer itself. The slope of the curve represents the permeability, μ in this case. Applying the "Transformation of Axes" as described in Section 1 of the *Magnetics Design Handbook* [9], the vertical axis can also be used for the V-s applied to a specific inductor when the horizontal axis is used for the current flowing through this specific inductor. This specific inductor is in this case the magnetizing inductance L_m of the transformer and is then represented by the slope of the hysteresis curve as well. The horizontal axis is then specifically showing the magnetizing current I_m. The blue curve between A and A' represents the so-called minor loop that is the practical range of excursion used in real applications.

If the applied V-s product (or the flux-density B) violates a certain limit (the red dotted lines), then the slope changes from a linear to a nonlinear behavior. Any further increase in the applied V-s will cause a drastic increase of the magnetizing current. The inductive characteristic diminishes, leaving finally only the copper resistance of the winding. A drastic increase of the magnetizing current also causes shorting of the primary side of the ideal transformer block used in the simplified model of the real transformer (Figure 20).

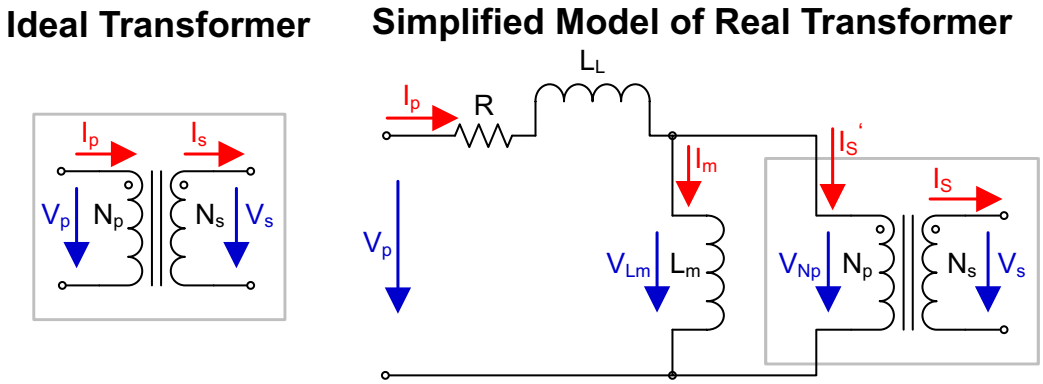


Figure 20. Ideal Transformer versus Simplified Model of Real Transformer

Any voltage applied to the magnetizing inductance can cause such an effect, no matter how small. The question is just how long the voltage is applied. This information explains why transformers can work for AC signals, but not for DC signals.

Even AC signals can cause this effect if the AC signals violate the V-s limit of the specific inductor. Such a violation can happen, if the magnitude of the voltage is too large or the time the voltage is applied is too long (for example, when operated at low frequency). The violation can also happen if the AC signal has a DC voltage superimposed. To avoid this situation, the V-s applied to an inductor (or the flux in the core) needs to be balanced. Therefore, any positive V-s excursion in one direction needs to be cancelled out by exactly the same excursion in the opposite direction. Otherwise, flux walking can happen driving the core earlier or later into saturation.

By adding a DC blocking capacitor (C18 in Figure 19), a potential flux walking can be addressed and avoided effectively in a half-bridge topology—a significant advantage compared to the push-pull.

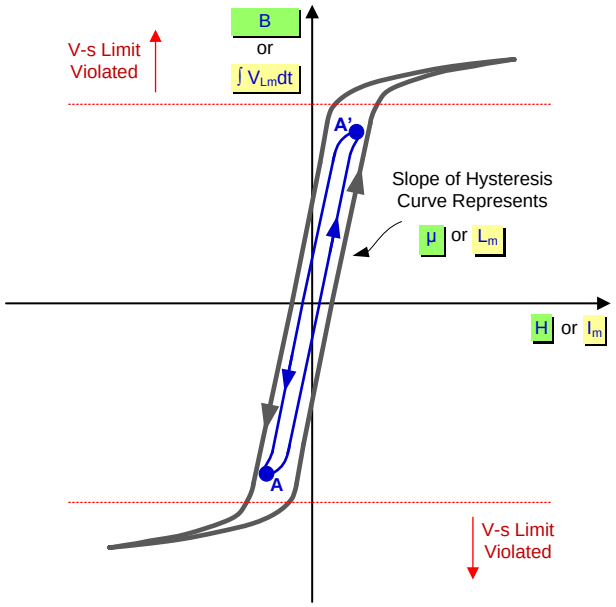


Figure 21. Hysteresis Curve of Ferrite and Specific Inductor

The applied V-s product can be reduced only by reducing the ON-time t_{ON} of the integrated switches or the voltage V_{Lm} respectively V_P applied to the magnetizing inductance. The ON-time is determined by the switching frequency and equals to almost 50% of the switching period and the applied voltage V_P is determined by the input voltage VCC_IN. The use of the half-bridge topology to drive the transformer excels the push-pull in respect of the applied voltage V_P as well: it drives the primary winding with one half of VCC_IN only instead of the full voltage, which is applied in case of a push-pull. This reduces the needed V-s capability of the transformer used in a half-bridge configuration to one half compared to a push-pull operated with the same switching frequency.

On the other side, providing only half the VCC_IN to the primary winding of transformer T2 will transfer only half of the voltage to the secondary winding. This can be compensated by adapting the turns ratio n of the transformer or by the used rectifier topology on the secondary side.

Because the output voltage of the isolated DC/DC needs to incorporate enough headroom for the following 3.3-V post regulators, an additional boost of that output voltage is required. Using solely the modification of the turns ratio of the transformer to achieve this boost and to compensate for driving the primary winding of the transformer with only VCC_IN / 2 might complicate the transformer design more. More number of turns and even additional layers on the secondary would be required, increasing the copper resistance of the winding and making the coupling and capacity between primary and secondary worse.

Therefore, the design uses a voltage doubler topology for the rectification on the secondary side to compensate for the half-voltage drive on the primary. The voltage doubler consists of D7, D8, C19, and C24. The modification of the transformers turns ratio is used to address the need for the post regulators' headroom voltage as well as for the compensation of the forward voltage drops in the diodes and the other losses in the parasitic elements of the circuit. In the special case of this design, the primary-to-secondary side turns ratio n was chosen to be 1:1.8, resulting in enough headroom voltage to enable both post regulators to operate with their full dynamic performance under all load and temperature conditions.

4.3.1.1 Isolated DC/DC Converter—Design Equations

This section presents the design equations for selecting the transformer and the diodes of the isolated DC/DC converter. Adequate margins have to be factored in when selecting the components and values needs to be confirmed by real measurements to see the effects of parasitics and non-ideal circuit behavior and to adapt the circuit and components selection accordingly. Additional details can be found in the respective section of the TIDA-00349 reference design [7].

The basic voltage conversion of the isolated DC/DC converter is described by Equation 1. It outlines very clearly the dependency of the output voltage on the input voltage of the isolated DC/DC converter. The diodes' forward voltage is one of the main contributor of losses as well as of the dependency of the output voltage on the output current and temperature. All those dependencies are a typical characteristic of any open loop converter not incorporating a control mechanism.

$$VOUT\_isoDCDC = \frac{VCC\_IN}{n} - 2 \times V_{F\_D} \quad (1)$$

where

- VOUT_isoDCDC is the output voltage of the isolated DC/DC
- VCC_IN is the input voltage of the isolated DC/DC
- V_{F_D} is the forward voltage drop of each diode D7 and D8 at twice the output current IOUT of the isolated DC/DC
- n is the *primary-to-secondary* turns ratio of transformer T2

NOTE: This is only one possible way to define the turns ratio. Some literature or transformer manufacturer define the turns ratio to the exact contrary as a secondary-to-primary turns ratio.

The diodes D7 and D8 need to be selected by their reverse voltage, average, and repetitive forward current. Their forward voltage, reverse current, diode capacitance, and reverse recovery times should be as small as possible to maximize efficiency. When deciding, consider their behavior at temperature extremes.

$$VR_D = VOUT\_isoDCDC + V_{F\_D} \quad (2)$$

where

- VR_D is the minimum required reverse voltage of each of the diodes D7 and D8

$$I_{F(AV)} = IOUT \quad (3)$$

where

- $I_{F(AV)}$ is the minimum required average forward current of each diodes D7 and D8

$$I_{FRM\_D} > 2 \times IOUT \quad (4)$$

where

- I_{FRM_D} is the minimum required repetitive peak forward current of each of the diodes D7 and D8.

Re-arranging Equation 1 and knowing the diodes' forward voltages at the respective current levels allows the calculation of the needed turns ratio for the transformer. Considering the worst case condition, Equation 1 can be re-arranged to

$$n = \frac{VCC\_IN\_min}{VOUT\_isoDCDC\_min + 2 \times V_{F\_D\_max\_T\_min}} \quad (5)$$

where

- VOUT_isoDCDC_min is the minimum output voltage of the isolated DC/DC needed to ensure proper operation of the post regulators
- VCC_IN_min is the minimum available input voltage of the isolated DC/DC
- $V_{F\_D\_max\_T\_min}$ is the maximum forward voltage drop at the minimum temperature of each of the diodes D7 and D8 at twice the output current IOUT of the isolated DC/DC
- n is the primary-to-secondary turns ratio of transformer T2

To avoid saturation of the transformer, the transformer must be able to withstand the maximum V-s product, which can happen in the design.

$$Vt > \frac{VCC\_IN\_max}{4 \times f\_min} \quad (6)$$

where

- Vt is the V-s product the transformer must be able to operate over the full temperature range without going into saturation.
- VCC_IN_max is the maximum input voltage, which might be applied to the isolated DC/DC
- f_min is the minimum switching frequency; 30 kHz for TPS60402

Beside the V-s product, there is another key design parameter for the transformer: the magnetizing current, I_m. This current does not contribute to the energy transfer from the primary to the secondary, but is circulating in the primary circuits contributing to conduction losses and switching losses. This is especially important for the light load efficiency of the isolated DC/DC converter. The specification of I_m finally allows to calculate a value for the magnetizing inductance L_m of the primary winding.

The maximum peak-to-peak and rms value of the magnetizing current can be calculated as shown in Equation 7 and Equation 8.

$$I_{m\_pp\_max} = \frac{VCC\_IN\_max}{4 \times f\_min \times L_{m\_min}} = \frac{Vt\_max}{L_{m\_min}} \quad (7)$$

$$I_{m\_rms\_max} = \frac{I_{m\_pp\_max}}{2 \times \sqrt{3}} = \frac{Vt\_max}{2 \times \sqrt{3} \times L_{m\_min}} = \frac{VCC\_IN\_max}{8 \times \sqrt{3} \times f\_min \times L_{m\_min}} \quad (8)$$

where

- L_{m_min} is the minimum value of the magnetizing inductance, in most cases applicable for the lowest temperature
- V_{t_max} is the maximum V-s product the transformer is driven with
- $I_{m\_pp\_max}$ is the maximum peak-peak value of the magnetizing current (triangular waveform)
- $I_{m\_rms\_max}$ is the maximum RMS value of the magnetizing current (triangular waveform)

Re-arranging Equation 7 leads to Equation 9, which calculates a minimum magnetizing inductance to keep the magnetizing current below its targeted maximum value.

$$L_{m\_min} = \frac{VCC\_IN\_max}{4 \times f\_min \times I_{m\_pp\_max}} = \frac{Vt\_max}{I_{m\_pp\_max}} \quad (9)$$

Note that the magnetic properties of a transformer's core have a certain dependency on temperature. This should be factored in by applying an adequate margin when calculating L_{m_min}.

4.3.1.2 Isolated DC/DC Converter—Circuit Implementation

Figure 19 only shows a simplified schematic of the isolated DC/DC converter. The real circuitry implemented on the board is provided in Figure 22. This circuitry adds the following list of additional components and tweaks to ease the test and enable user-specific modifications:

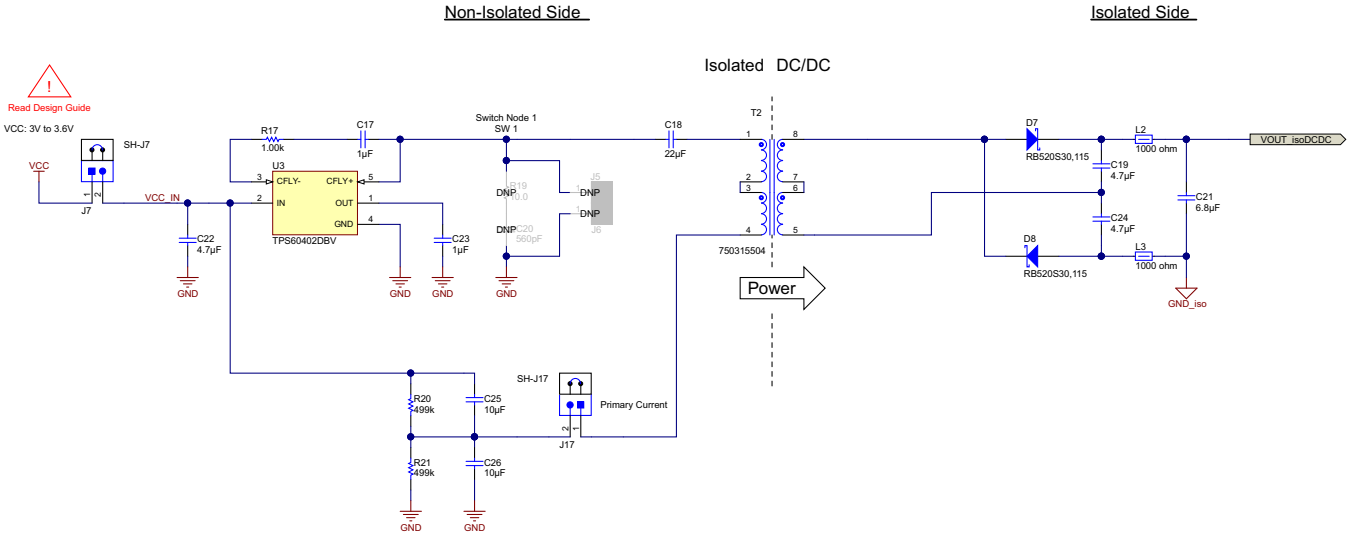


Figure 22. Isolated DC/DC—Real Implementation

- C17, C23, and R17: The TPS60402 requires a negative voltage on its OUT pin (pin 1) to ensure proper operation. This is because the device's main use case is operation as an inverting charge pump. C17 can be therefore considered as the flying capacitor of the charge pump, C23 as its output capacitor for the negative voltage and R17 to reduce the peak currents related to the charge pump operation inside the TPS60402. Besides the added R17, the capacitance values of C17 and C23 have been reduced compared to the standard application of the TPS60402 as outlined in its datasheet.
- Header J17 provides an easy way of measuring the primary current of the transformer by combining a standard current probe with a self-made adapter (Figure 23). The self-made adapter must be plugged on header J17 instead of the respective jumper SH-J17.

Figure 23. Combination of Current Probe With Self-Made Adapter for Primary Side Current Measurement

- R19 and C20 are placeholders for a snubber circuitry, which is required in case the peaks and spikes of the voltage waveform on the switch node (SW1) exceed the voltage rating of the TPS60402 CFLY+ pin. The snubber reduces peaking, dampens a possible ringing, and reduces radiated noise on that node of the circuit at the expense of a reduced efficiency of the power conversion.

  Because this isolated DC/DC is powered with a maximum of 3.6 V on VCC_IN, it is unlikely that the voltage rating of the TPS60402 will be exceeded. This was proven by measurement of the SW1 voltage waveform; there had been no peaking on SW1 observed (see Figure 29). Therefore, these components have not been populated. If these components are needed, separate testing is required to evaluate the effectiveness of the snubber and its influence on the DC/DC converter efficiency. The values given are placeholder values and must be adapted according to the specific case. The value of the capacitor C20 is usually chosen so that the ringing frequency on the switch node is halved with C20 compared to the case without C20. R19 must be a short (or a 0-Ω resistor) for finding the right value for C20. If the best fitting capacitance value has been found and C20 has been populated with a capacitor with this optimal value, R19 can be varied to find the best compromise between ringing reduction and best efficiency.

  The test must be conducted by connecting the oscilloscope probe (high impedance, low capacitance) with the shortest possible grounding wire.

  The header pins of J5 and J6 are not populated. The respective vias, labeled on the board with "SW1" and "GND", can instead be used as a test point and GND connection to plug in the tip and the ground spring of the oscilloscope probe. Figure 24 provides an example for a standard 10:1 oscilloscope probe, which comes with a probe tip cover, a long ground lead, and an alligator clip (on the left side of Figure 24). The use of such standard probes for measuring switching regulators is notorious for its noise pick-up. The right half of the figure shows the same probe but with a removed ground lead and probe tip cover. The ground lead is replaced by a ground spring, ensuring the shortest possible ground connection and avoiding noise pick-up by this. Figure 25 shows the dedicated vias on the PCB, labeled with SW1 and GND, to which the tip of the probe and its ground spring needs to be connected.

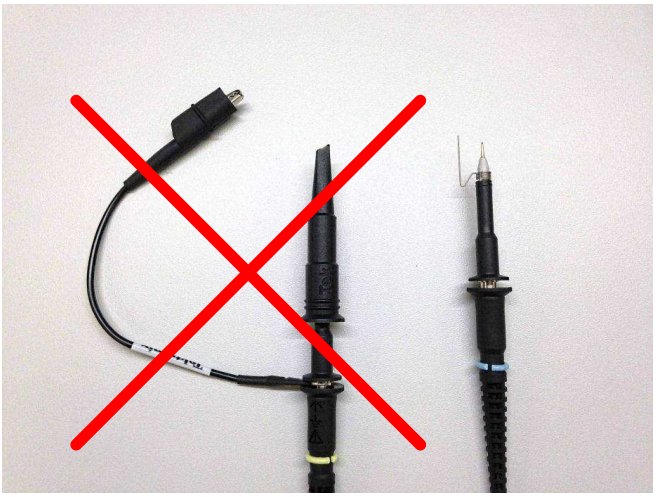


Figure 24. Probe With Long Ground Lead and Alligator Clip versus Probe With Ground Spring

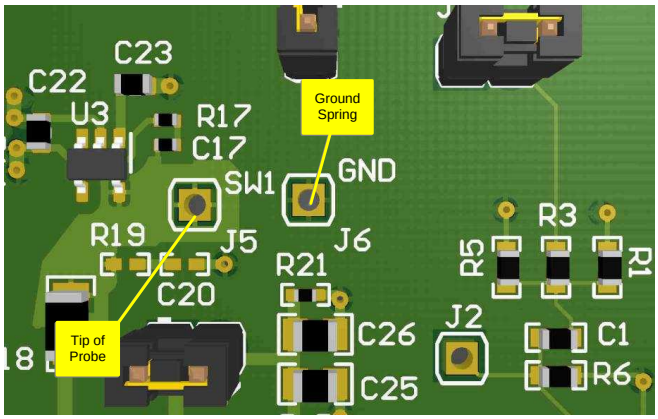


Figure 25. Test Setup for SW1—Special Vias for Connecting Tip and Ground Spring

A comparison of the same switch-node signal measured with the standard probe configuration or with the approach using the modified probe with the ground spring is shown in Figure 27 and Figure 29, respectively. The latter method provides a clean waveform compared to the standard probe usage, which shows peaking and ringing (highlighted by the red circles in Figure 27).The real measurement setup is shown in Figure 26 and Figure 28, respectively.

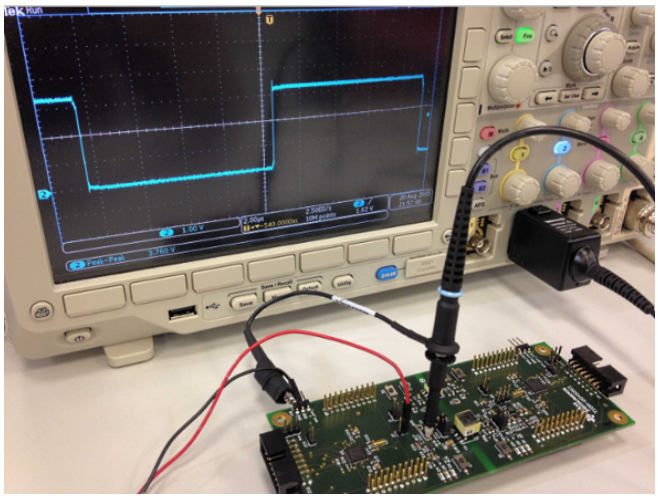


Figure 26. Test Setup for SW1—Switch Node Voltage; Using Probe With Long Ground Lead and Alligator Clip

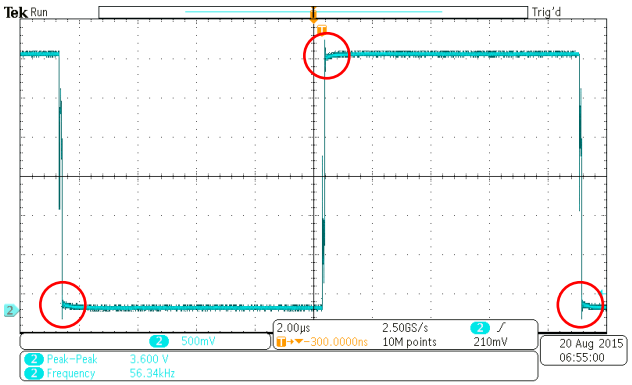


Figure 27. SW1—Switch Node Voltage Waveform Using Probe With Long Ground Lead and Alligator Clip

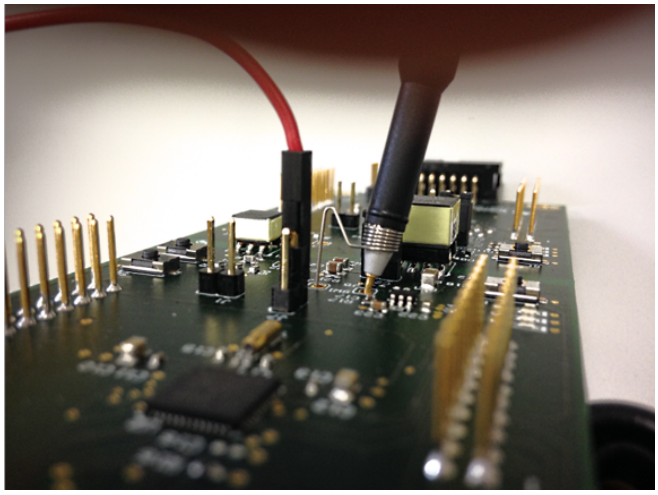


Figure 28. Test Setup for SW1—Switch Node Voltage Using Probe With Ground Spring

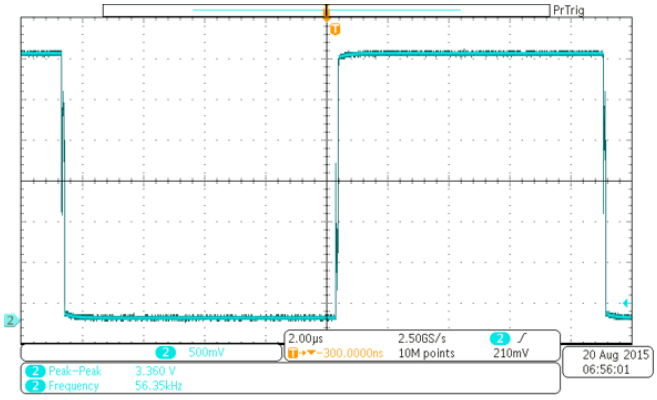


Figure 29. SW1—Switch Node Voltage Waveform Using Probe With Ground Spring

- R20 and R21 are used to keep the capacitive divider C25 and C26 balanced to cancel out their possible tolerances.
- L2 and L3 are ferrite beads used to filter high frequency noise (spikes with the switching frequency of the isolated DC/DC), which can be observed on C19+C24 but should be kept from C21.

4.3.2 Post Regulators

The design offers the user the ability to select either a TPS715A33 as low Iq LDO (U5) or a high-efficiency DC/DC converter based on a TPS62125 (U4) switching regulator as post regulator solution (see Figure 30). The LDO solution is by far the simplest solution for the implementation of the post regulator as long as the reduced efficiency compared to the switching regulator solution is acceptable.

The post regulators are powered off VOUT_isoDCDC, the non-regulated output of the isolated DC/DC converter. Both post regulators are able to provide a stable and well regulated 3.3 V on their outputs VOUT_LDO or VOUT_DCDC. The design is characterized for output currents up to 10 mA.

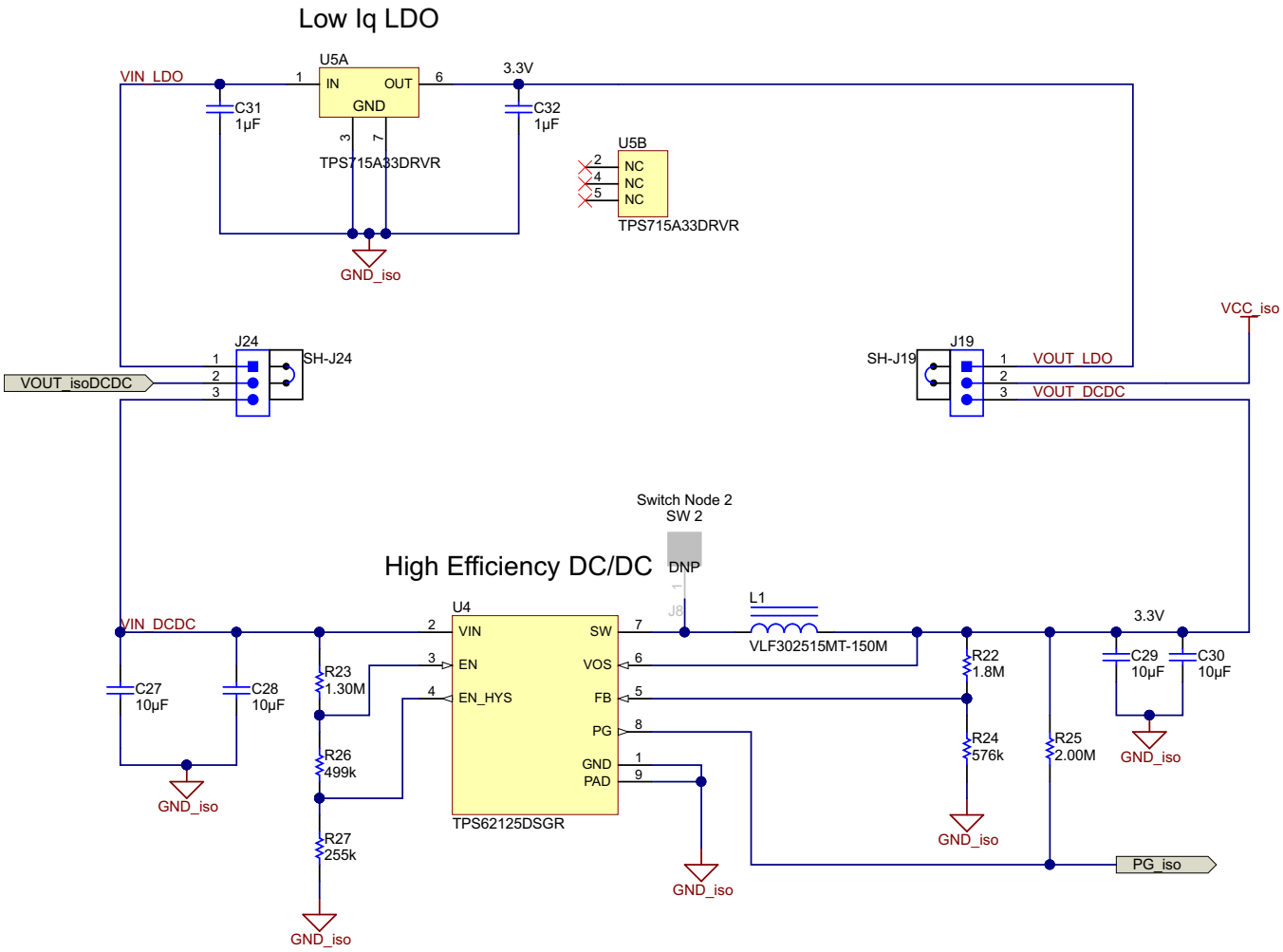


Figure 30. Post Regulators—Real Implementation

The selection of the post regulators is done by simple jumper setting. Jumper J24 connects the output of the isolated DC/DC converter with the input V_{IN_LDO} or V_{IN_DCDC} of the selected post regulators. The 3.3-V output of the selected post regulator is connected through jumper J19 to V_{CC_iso} on the isolated side. The detailed jumper settings applicable for the different power options and including the settings for J15 are described in Section 5.2 and Table 11.

4.3.2.1 Low Iq LDO—Circuit Implementation

The TPS715A33 is shown as U5A and U5B in the schematic of Figure 30, where U5A is representing the LDO functionality and U5B is symbolizing the not connected pins of the device. The used LDO is a fixed 3.3-V version, not needing any additional resistors to set up the output voltage. Tolerances and temperature coefficients of external voltage setting resistors, as would be needed with the adjustable version, do not need to be considered with the fixed 3.3-V device. The datasheet gives the output voltage accuracy spec for the used 3.3-V version over the complete full input voltage (4.3 to 24 V), output current (0 to 80 mA) and operating junction temperature range (–40°C to 125°C). The circuit design follows the guidelines and recommendations of the datasheet.

External Capacitors

C31 and C32 are the bypass capacitors of the LDO's input and output. 1-µF X5R capacitors have been selected, fulfilling the datasheet recommendations of 0.47 µF with a reasonable margin. The voltage rating for the capacitors is 16 V for the input capacitor C31 and 10 V for the output capacitor C32 to reduce the effects of DC bias (up to about 9 V for C31, 3.3 V for C32) on the capacitance values. Both capacitors are placed as close as possible on the respective pins of the LDO as shown in Figure 31. The input and output of the LDO are forced to pass through the pads of the bypass caps. The GND pin of the LDO (pin 3 of U5) is directly connected with C31 and C32 too. The LDO, the two bypass capacitors and their interconnections are placed on the same side of the PCB, not relying on vias for the electrical connections. Vias are used only to connect the "GND-iso" net of the circuit and the PowerPAD of the LDO to the "GND_iso" plane inside the PCB.

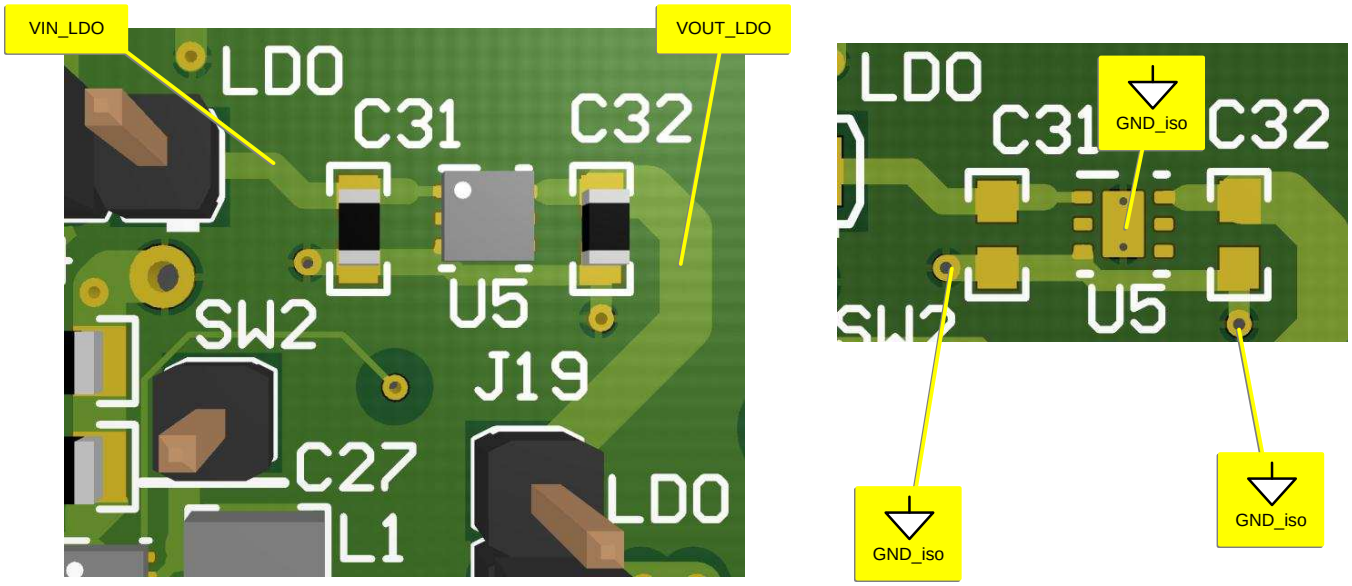


Figure 31. Low Iq LDO—Board Layout and LDO's Grounding

Dropout Voltage

As outlined in the TPS715A datasheet, the specification of the dropout voltage V_{DO} is valid for the condition when the pass-FET of the LDO is fully enhanced, so the LDO is performing under the V_{DO} test condition more as a (FET-) switch with a given $R_{DS(ON)}$ than a real voltage regulator. The V_{DO} at an output current of 80 mA, which the LDO is rated for, is given in the datasheet with a typical value of 670 mV at 25°C and a maximum value of 1.12 V at 125°C. The V_{DO} can be scaled down for lower output currents as illustrated in Figure 32, giving also a typical value of roughly 100 mV at 125°C for an output current of 10 mA.

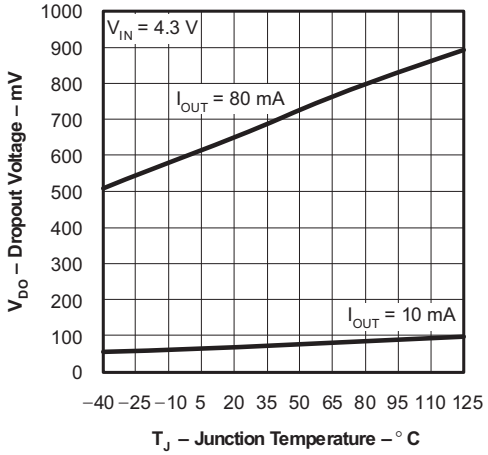


Figure 32. TPS715A Dropout Voltage versus Junction

Applying the same ratio $V_{DO\_max\_125C\_80mA}/V_{DO\_typ\_25C\_80mA}$ as given for the 80-mA output current to the 100 mV given as $V_{DO\_typ\_25C\_10mA}$ will lead to an estimated maximum value for the dropout voltage at 10-mA output current and 125°C.

$$V_{DO\_max\_125C\_10mA} \approx \frac{V_{DO\_max\_125C\_80mA}}{V_{DO\_typ\_25C\_80mA}} \times V_{DO\_typ\_25C\_10mA} = \frac{1120\ mV}{670\ mV} \times 100\ mV = 167\ mV \quad (10)$$

The 100 mV used as $V_{DO\_typ\_25C\_10mA}$ in Equation 10 are valid for an input voltage of the LDO ≥ 4.3 V. The value of the LDO's V_{DO} goes up with a lower input voltage as highlighted in Figure 33.

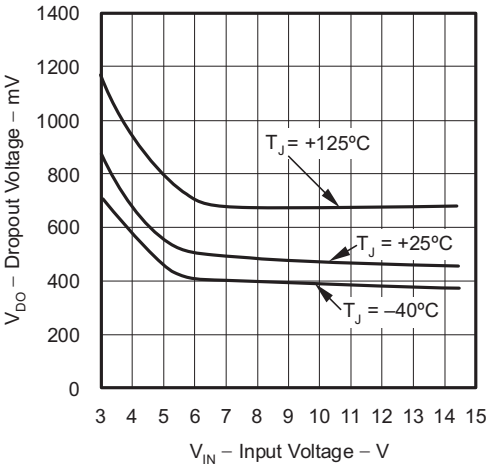


Figure 33. TPS715A Dropout Voltage versus Input Voltage

Nevertheless, as can be seen in the following section, the V_{DO} is much smaller than VHR and does not therefore need any further considerations in this design.

Headroom Voltage

Besides the dropout voltage, there is the so called headroom voltage V_{HR} = VIN – VOUT, which needs to be considered to get the full dynamical performance out of the LDO, namely the power supply ripple rejection (PSRR), as specified in the datasheet. In the case of the TPS715A, a 1-V headroom voltage was used to perform PSRR measurements and to get the PSRR specifications as given in the electrical characteristics table and the PSRR versus Frequency graph of its datasheet. The needed V_{HR} is related to the output current, similarly as the V_{DO} is. With the 10-mA output current specification of this design, the needed V_{HR} can be scaled down from its 1-V value given in the datasheet for the full 80-mA output current, but the down-scaling is not linear with IOUT as it can be done for the V_{DO}. For this design, the down-scaling was not applied.

Minimum Input Voltage

Because the main targeted applications of this design are loop-powered 4- to 20-mA transmitters, the goal is to ensure the best dynamic performance of the LDO for output currents of up to 3 mA. Therefore, the minimum needed input voltage of the LDO, $VIN\_LDO\_min_{\_-40C\_3mA}$ at the 3-mA level, and at –40°C were in the range of 4.5 V as shown in Equation 11:

$$VIN\_LDO\_min_{\_-40C\_3mA} = V_{HR} + VOUT\_LDO\_max = 1\,V + 3.465\,V = 4.465\,V \approx 4.5\,V \quad (11)$$

The voltage was defined at –40°C, because the output voltage of the isolated DC/DC (which is the input voltage of the LDO) is going down with lower temperatures. This is due to the negative temperature coefficient of the output diodes used in the isolated DC/DC. Furthermore, this voltage level needs to be generated by the isolated DC/DC even at its lowest input voltage, VCC_IN_min of 3.0 V (see the black V_{OUT} curve in Figure 52).

Power Dissipation

The LDO's power dissipation P_D needs to be calculated under worst case conditions, which are $VIN\_LDO\_max_{\_+85C\_10mA}$, VOUT_LDO_min, and IOUT_LDO_max.

$$P_D = \left(VIN\_LDO\_max_{\_+85C\_10mA} - VOUT\_LDO\_min\right) \times IOUT_{LDO_{max}} = (5.3\,V - 3.135\,V) \times 10\,mA \approx 22\,mW \quad (12)$$

where

- $VIN\_LDO\_max_{\_+85C\_10mA}$ is the maximum input voltage applied on the LDO at 85°C and at a 10-mA output current. It equals the VOUT_isoDCDC at the respective temperature and current conditions and at an input voltage of the isolated DC/DC VCC_IN of 3.6 V
- VOUT_LDO_min is the minimum output voltage of the LDO as given in the TPS715A33 datasheet under "Output Voltage Accuracy" in the "Electrical Characteristics" section of its datasheet
- IOUT_LDO_max is the maximum output current the LDO is providing in this design (10 mA)

The 22-mW power dissipation is much smaller than the dissipation ratings given in the respective section of the LDO's datasheet.

4.3.2.2 High Efficiency DC/DC—Circuit Implementation

The circuitry of the high efficiency DC/DC converter follows the datasheet recommendation. C27 and C28 are the input bypass capacitors; C29, C30, and L1 are the respective components of output filter, using the values of Table 3 inside the TPS62125 datasheet. R22 and R24 are used to set the output voltage according to Table 2 in the datasheet to the desired 3.3 V.

R23 (1.3M), R26 (499k), and R27 (255k) provide an easy way to define a precise level for VIN_DCDC at which the high efficiency DC/DC converter starts switching, but defines also a stop-voltage level. By having those two voltages programmable, a certain hysteresis can be implemented for the start and stop of the converter. With the values given for the three resistors, the startup- and stop-values as shown in Table 9 have been achieved for the high efficiency DC/DC converter's input voltage. The minimum and maximum values are based on the worst case scenario, using the datasheet min and max values for the ON and OFF threshold voltages as well as applying 1% and –1% tolerance to the resistor values.

Table 9. VIN_DCDC: Minimum, Typical, and Maximum Values for Startup and Stop Voltage

	MINIMUM	TYPICAL	MAXIMUM
VIN_DCDC_startup (V)	4.122	4.32	4.53
VIN_DCDC_stop (V)	3.012	3.133	3.283

The board layout (Figure 34 and Figure 35) follows consequently the considerations given in the datasheet.

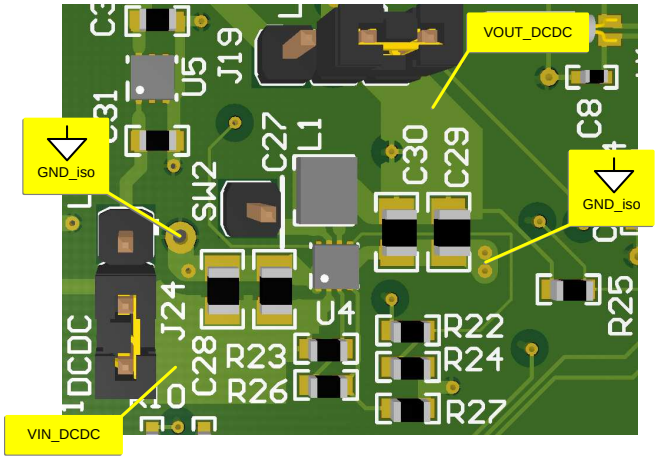


Figure 34. High Efficiency DC/DC—Board Layout

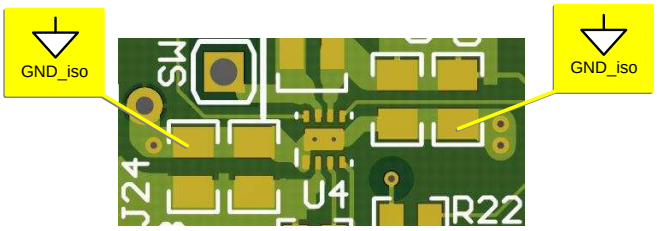


Figure 35. High Efficiency DC/DC—U4's Grounding

For any sensitive measurement, use probes equipped with ground springs instead of the standard long ground lead and alligator clip. The significant impact can be seen on Figure 36, Figure 37, Figure 40, and Figure 41 providing the SW2 – Switch Node waveforms. The first two figures cover the no-load case, and the latter two figures the case of the DC/DC converter loaded with a resistor causing 10 mA of output current. Figure 36 was taken with the standard probe, the three other figures with the probe modified by using the ground spring.

All waveforms have been generated powering the isolated DC/DC converter with 3.3 V and having the high efficiency DC/DC converter selected as the post-regulator. So the VIN_DCDC is connected to the VOUT_isoDCDC and is therefore slightly load dependent. It goes down with increasing load current, following the "VOUT" curves shown in Figure 53.

The real test setup is shown by Figure 38, whereas Figure 39 provides a clear guideline where on the board the tip and the ground spring needs to be plugged-in.

Due to the low output current, the high efficiency low-power synchronous buck converter TPS62125 is going to operate in discontinuous current mode (DCM). This can be seen on all the oscilloscope plots and can be explained by using Figure 36.

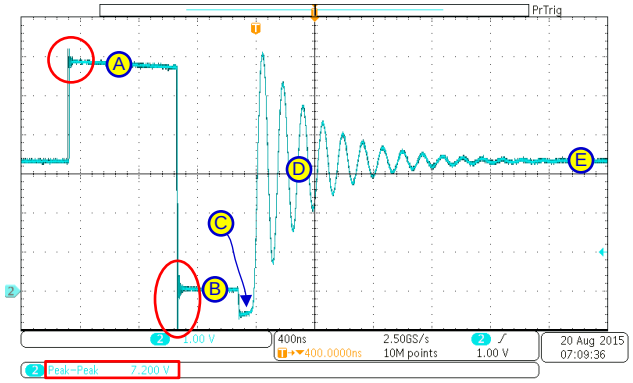


Figure 36. SW2—Switch Node Voltage Waveform Using Probe With Long Ground Lead and Alligator Clip; VCC_IN = 3.3 V, IOUT_DCDC = 0 (No Load), 400 ns

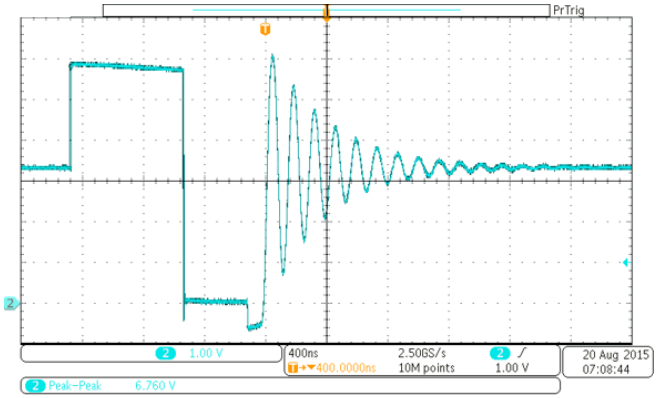


Figure 37. SW2—Switch Node Voltage Waveform Using Probe With Ground Spring; VCC_IN = 3.3 V, IOUT_DCDC = 0 (No Load), 400 ns

The red encircled areas of Figure 36 are related to the fact that switching noise was coupling into the long ground lead of the standard probe. There is a severe peaking in that areas. The resulting peak-to-peak voltage is shown with 7.2 V inside the red encircled rectangle. By using the modified probe, this peak-to-peak voltage on SW2 had been reduced to 6.76 V as demonstrated in Figure 37.

To show the DCM, Figure 36 provides a good orientation by different states labeled with A to E.

- **A**: The high-side FET (between the VIN pin and SW pin) is ON. As a result, the VIN_DCDC can be measured on the switch node SW2, and inductor current flows through the high-side FET and rises.
- **B**: The high-side FET goes OFF, and the low-side FET (also called Sync-FET) is ON, basically connecting SW2 to GND_iso through its low $R_{DS(ON)}$, inductor current flows through the low-side FET and declines.
- **C**: Both FETs are OFF, and inductor needs to flow through the body diode of the low-side FET, causing a negative voltage on SW2 that equals the forward voltage of this body diode.
- **D**: Both FETs are OFF, the inductor current has declined to zero, and the inductor forms together with the parasitic capacitances connected to the inductor a resonant tank. The resonant ringing, which is a characteristic for any switching converter operating in DCM, starts and decreases with the diminishing energy of the resonant tank. Due to the small inductance and capacitance values, the energy is limited and does not usually create EMI issues. The average or DC-level of the ringing equals the output voltage V_{OUT_DCDC} (which is connected to the other side of the inductor).
- **E**: All the energy of the resonant tank is dissipated. Ringing has stopped. Both FETs are OFF. The output voltage is still connected to the inductor and can therefore be seen on SW2.

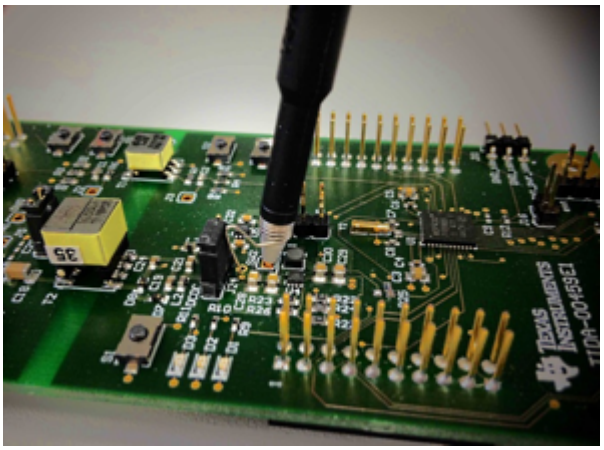


Figure 38. Test Setup for SW2—Switch Node Voltage Using Probe With Ground Spring

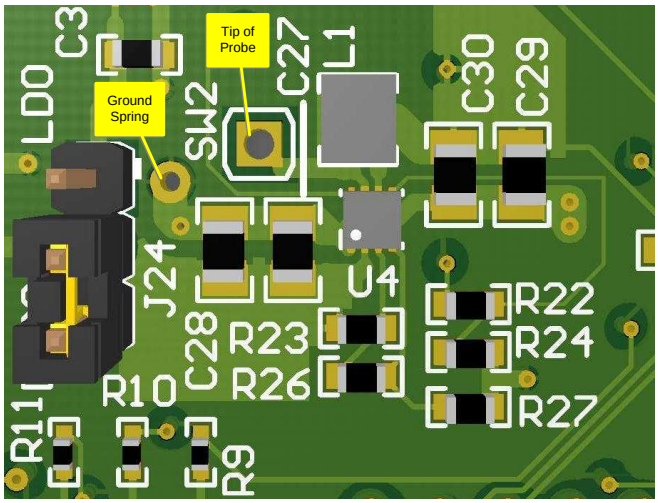


Figure 39. Test Setup for SW2—Dedicated "Vias" for Connecting Tip and Ground Spring

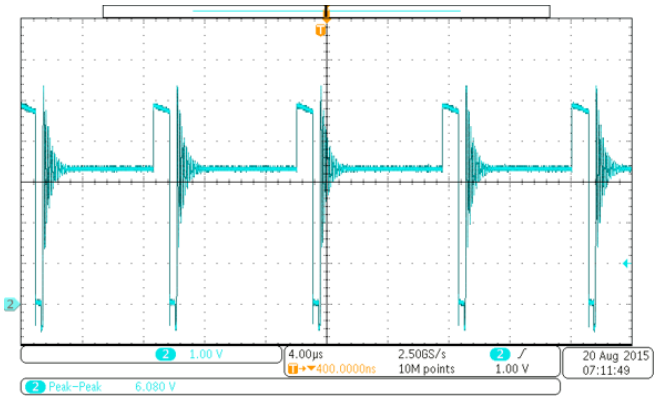


Figure 40. SW2—Switch Node Voltage Waveform Using Probe With Ground Spring; VCC_IN = 3.3 V, IOUT_DCDC = 10 mA, 4 µs

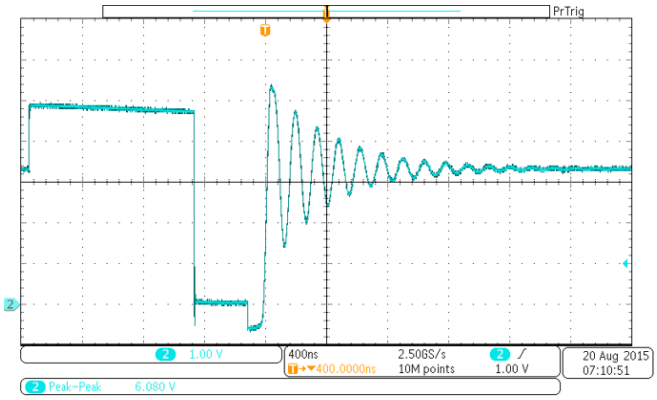


Figure 41. SW2—Switch Node Voltage Waveform Using Probe With Ground Spring; VCC_IN = 3.3 V, IOUT_DCDC = 10 mA, 400 ns

Figure 40 and Figure 41 show the SW2 waveform for output currents of 10 mA. Figure 41 is similar to Figure 37; the time of state A is slightly prolonged and the voltage level during state A is reduced in Figure 41 due to the load dependency of the isolated DC/DC's output voltage. Figure 40 covers the same condition as Figure 41 but was taken with a larger time scale, allowing to see now the switching frequency of the high efficiency DC/DC converter as well. Because the device is operating in DCM, the switching frequency is a function of the load current as well.

5 Getting Started Hardware

5.1 Headers and Jumper Locations

Figure 42 shows the jumpers found on TIDA-00459.

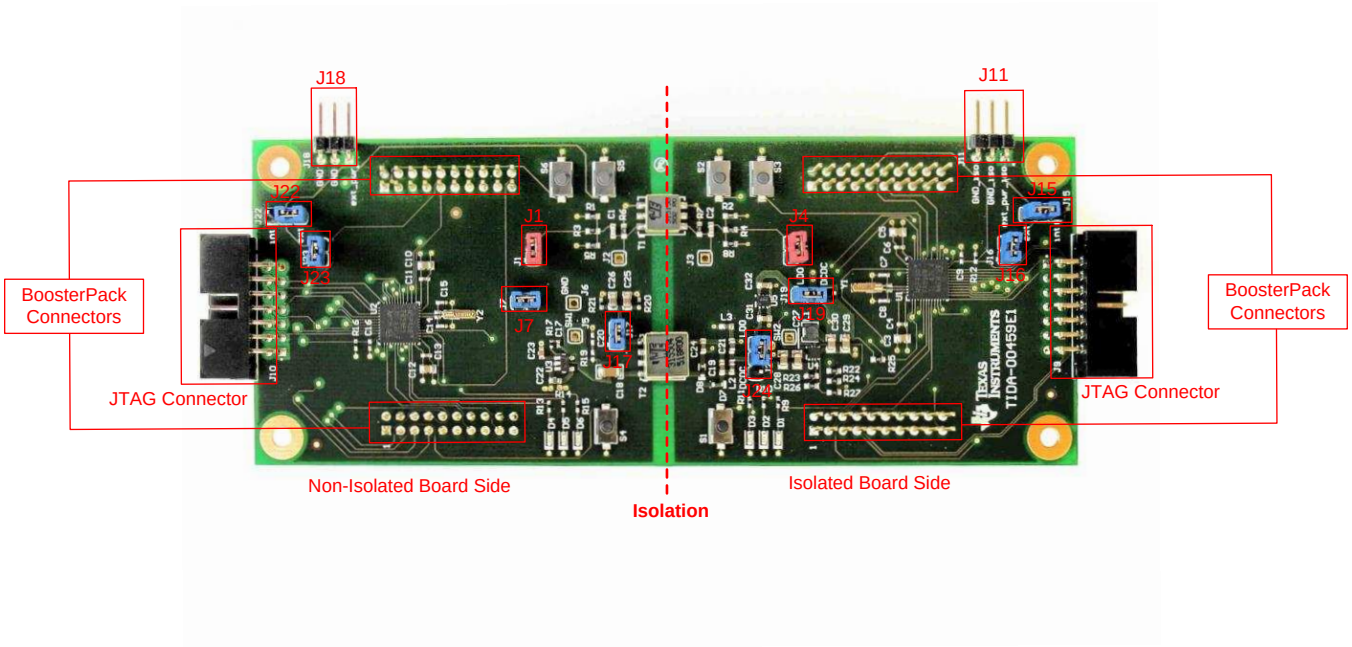


Figure 42. TIDA-00459 Jumper Locations

Table 10 shows the different functions of the headers.

Table 10. Jumper Functions

HEADERS	DESCRIPTION
J1, J4	J1 and J4 can be used to disconnect the two MSP430FR5969 from the isolation circuitry and the transformer on the board. Instead, the jumpers can be used to connect different isolation circuits and transformers.
J7	J7 can be used to measure the current into the isolated side.
J11	Isolated VCC and GND connection.
J15	If the MSP430 on the isolated side is not powered from the MSP-FET Debugger, make sure pin 2 and pin 3 are connected on header J15. If power from the MSP-FET Debugger must be used, make sure pin 1 and pin 2 are connected on header J15.
J16	J16 can be used to measure the current on the isolated side if the isolated side is powered from external VCC or MSP-FET Debugger.
J17	J17 can be used to measure the current on the primary side of the power transformer.
J18	Non-isolated VCC and GND connection.
J19	The LDO is selected for the isolated VCC if pin 1 and pin 2 are connected on J19. The DC/DC is selected for the isolated VCC if pin 2 and pin 3 are connected on J19.
J22	If the MSP430 on the non-isolated side is not powered from the MSP-FET Debugger, make sure pin 2 and pin 3 are connected on jumper J22. If power from the MSP-FET Debugger must be used, make sure pin 1 and pin 2 are connected on header J22.
J23	J23 can be used to measure the overall current of the board.
J24	The DC/DC is powered if pin 1 and pin 2 are connected on J24. The LDO is powered if pin 2 and pin 3 are connected on J24.

5.2 Power Options

On the TIDA-00459 are different power options for the non-isolated side and the isolated side. The non-isolated side can be powered from the external VCC on header J18 or from the JTAG MSP-FET Debugger.

The isolated side can be powered from the LDO, from the high efficiency DC/DC, from the external VCC on header J11, or from the MSP-FET Debugger.

If an external power supply is used during debug, make sure pin 2 and pin 3 are connected on header J22 for the non-isolated side and respectively on header J15 for the isolated side. If there is no external power connected and power from the MSP-FET Debugger Interface should be used, make sure pin 1 and pin 2 are connected on header J22 and respectively on header J15. The different jumper settings for the power options on the isolated side can be found in Table 11.

Table 11. Power Options on Isolated Side

POWER OPTIONS ON ISOLATED SIDE	JUMPER PLACEMENT ON HEADERS		
	J15	J19	J24
Power from LDO	2→3	1→2	1→2
Power from high efficiency DC/DC	2→3	2→3	2→3
Power from external VCC on J11	2→3	—	—
Power from MSP-FET Debugger on J9	1→2	—	—

6 Getting Started Firmware

To download the software files for this reference design, please see the link at http://www.ti.com/tool/TIDA-00459.

6.1 Software Setup

1. Install Code Composer Studio™ (CCS) before connecting the MSP-FET to PC. While CCS installs, USB drivers are installed automatically. Make sure to use the latest CCS version; otherwise, the USB drivers might not be able to recognize the MSP-FET.
2. Connect the MSP-FET to a USB port on the PC with the provided USB cable.
3. The following procedure applies when using Windows®:
   (a) After connecting to the PC, the MSP-FET should be recognized automatically, as the USB device driver has been already installed together with the IDE.
   (b) If the driver has not been installed yet, the Found New Hardware wizard starts. Follow the instructions and point the wizard to the driver files.
   (c) The default location for CCS is c:\ti\ccsv6\ccs_base\emulation\drivers\msp430\USB_CDC.
4. After connecting to a PC, the MSP-FET performs a self-test. If the self-test passes successfully, the green LED stays on.
5. If an external power supply is used during debug, make sure pin 2 and pin 3 are connected on jumper J15 and respectively on jumper J22. If there is no external power connected and power from the MSP-FET Debugger Interface should be used, make sure pin 1 and pin 2 are connected on jumper J15 and respectively on jumper J22.
6. Connect the MSP-FET with the 14-conductor cable to the JTAG connector J10 on the non-isolated side of the TIDA-00459 board.
7. Import the CCS project (TIDA-00459) into CCS.
8. Make sure following line has been commented out in the file main.h:
   // #define MSP430_IS_ON_ISOLATED_SIDE
9. Compile and download the firmware to the MSP430FR5969 on the non-isolated side of the TIDA-00459 board.
10. Connect the MSP-FET with the 14-conductor cable to the JTAG connector J9 on the isolated side of the TIDA-00459 board.
11. Make sure following line has been uncommented in the file main.h:
    #define MSP430_IS_ON_ISOLATED_SIDE
12. Compile and download the firmware to the MSP430FR5969 on the isolated side of the TIDA-00459 board.
13. To start the data transmission from the non-isolated side, hit the button S4. To start the data transmission from the isolated side, hit the button S1.

6.2 Software Function Documentation

The file swif.c contains the functions for the data transmission:

- *void initCompE(void)*
  This function is called to configure the Comparator_E
- *void config_USCIA0_UART(uint16_t div)*
  This function is called to configure the eUSCIA0 module in UART mode.
- *void sendByte(uint8_t x)*
  This function is called to send the break/synch field plus one byte. The parameter x is the byte to send.
- *void sendByte_RX(uint8_t x)*
  This function is called to send the break/synch field plus one byte. After transmission is completed, the MSP430 is configured for receive again. The parameter x is the byte to send.
- *void prepareTX(void)*
  This function is called to prepare the MSP430 for TX mode.
- *void prepareRX(void)*
  This function is called to prepare the MSP430 for RX mode.

6.3 Demo Software: Bidirectional Communication

The software files can be downloaded at http://www.ti.com/tool/TIDA-00459. The CCS project TIDA-00459_bidirectional is an example project for bidirectional communication.

The transmission starts on the non-isolated side with the button S4 or on the isolated side with the button S1. The value for the first transmitted byte is 0x00. When the byte has been received on the other side of the isolation, it is echoed back. The value is then incremented by one and sent again. If the value of the echoed back byte is not the same as the transmitted byte, the red LED lights up to show an error. After transmitting 1k bytes, the green LED toggles. The transmission can be stopped with button S1 or S4. The LEDs can be disabled with the buttons S2 and S3 or S5 and S6 to measure the current consumption of the data transmission.

7 Test Setup and Test Data

Several tests have been conducted. The complete isolated power path as well as the isolated data transmission have been first tested separately from each other, followed by the test of the complete board.

7.1 Power Path

The test of the complete power path includes the performance evaluation of all power blocks of this design at ambient temperatures of –40°C, 25°C, and 85°C:

- Isolated DC/DC
- Post regulators
  - Low Iq LDO
  - High efficiency DC/DC

The test was conducted by measuring and recording the input voltage and current on the input header J7 of the open loop isolated DC/DC. SMU 1 was used as programmable power supply, the output voltage of SMU1 was stepped from 3 to 3.6 V in 300-mV steps to evaluate the performance over the full input voltage range as specified in Section 1.

The regulated 3.3-V output voltage and current of the two different post regulators were measured and recorded on the respective pins of header J19 (see Table 13). This output currents can be considered as the load current of the post regulators. A second SMU (SMU 2) was set up to sweep this load current from 1 µA up to 10 mA. By using such a wide output current range for this test, the performance of the power path can be evaluated for the different load situation commonly seen in applicable applications, ranging from low power modes (Shutdown, Standby) up to maximum load situation (active mode at different clock speed + additional application specific current consumption). In addition the voltage and currents on the interface header J24, connecting the output of the isolated DC/DC with the input of the post regulators, have been recorded. The current measurement was done by DMM 1, a high-resolution voltmeter using an external 1-Ω precision resistor as a current sense shunt. This approach was preferred versus the normal way of configuring the DMM as an ammeter. The latter ammeter configuration would have been causing higher voltage drops based on the larger internal precision shunt (often 5 Ω) and the protection fuses (often two fuses: one inside the DMM, the other one a replaceable fuse located on the DMM's rear panel). These protection fuses are connected in series to the internal precision shunt but their resistance is not specified at all.

By having all the voltages and currents on the input (J7), on the output (J19), and on the interface header (J24), the performance of the total power path (isolated DC/DC + post regulator) as well of the separate power blocks can be evaluated and characterized.

The detailed test setup is described in Table 12, Table 13, and Figure 43. Additional information is provided in the sections presenting the test data.

Table 12. Basic Steps to Prepare the Board and Setup the Test of the Power Path

ITEM	DESCRIPTION	COMMENT
1	Remove all jumpers with the exception of J17 from the board	Basic prerequisite to enable the exclusive evaluation of the power path. All other circuit blocks (MCUs and data transmission circuits) will be disconnected from power after that.
2	Desolder the Power Good pullup resistor R25	Avoids, that the MCU on the isolated side of the design is powered via pin 1 of U1 and its internal ESD protection structure
3	Place the 1-Ω precision resistor as a current sense shunt directly on the respective pins of J24	Specific pins depend on which post regulator is intended to be evaluated
4	Connect all SMUs and DMMs, all channels should be floating	The floating of the inputs ensure that non-isolated side and isolated side of the board stays isolated from each other
5	Configure SMU 1 to provide the desired input voltage to the isolated DC/DC, set a current limit of 50 mA	The current limit reduces inrush currents and risk of damage in case of miswiring or shorts
6	Configure SMU 2 to sink the desired output current from the post regulator selected, be sure that SD 1 is connected to SMU 2's output in cases where the SMU is able to generate a negative output voltage.	SMU 2 might generate a negative output voltage in all cases when it is not able to sink the current it was set up to. This can happen for example, when the selected post regulator doesn't provide its positive output voltage. The external low forward voltage and low leakage schottky diode SD 1 clamps the output of SMU 2 to a negative voltage equal to SD 1's forward voltage.
7	Switch SMU 1 and both DMMs ON	
8	Switch SMU 2 ON	Keeping the sequence, that SMU 2 will always be switched ON after and switched OFF before SMU1 reduces furthermore the risk that the post regulator's output is driven negative by SMU 2

Table 13. Selection of the Desired Post Regulator for Evaluation

EVALUATION OF	J24			J19	
	PIN 1	PIN 2	PIN 3	PIN 1	PIN 3
Low Iq LDO	1 Ω DMM 1 LOW DMM 2 HIGH	DMM 1 HIGH		SMU 2 HIGH	
High efficiency DC/DC		1 Ω DMM 1 HIGH	DMM 1 LOW DMM 2 HIGH		SMU 2 HIGH

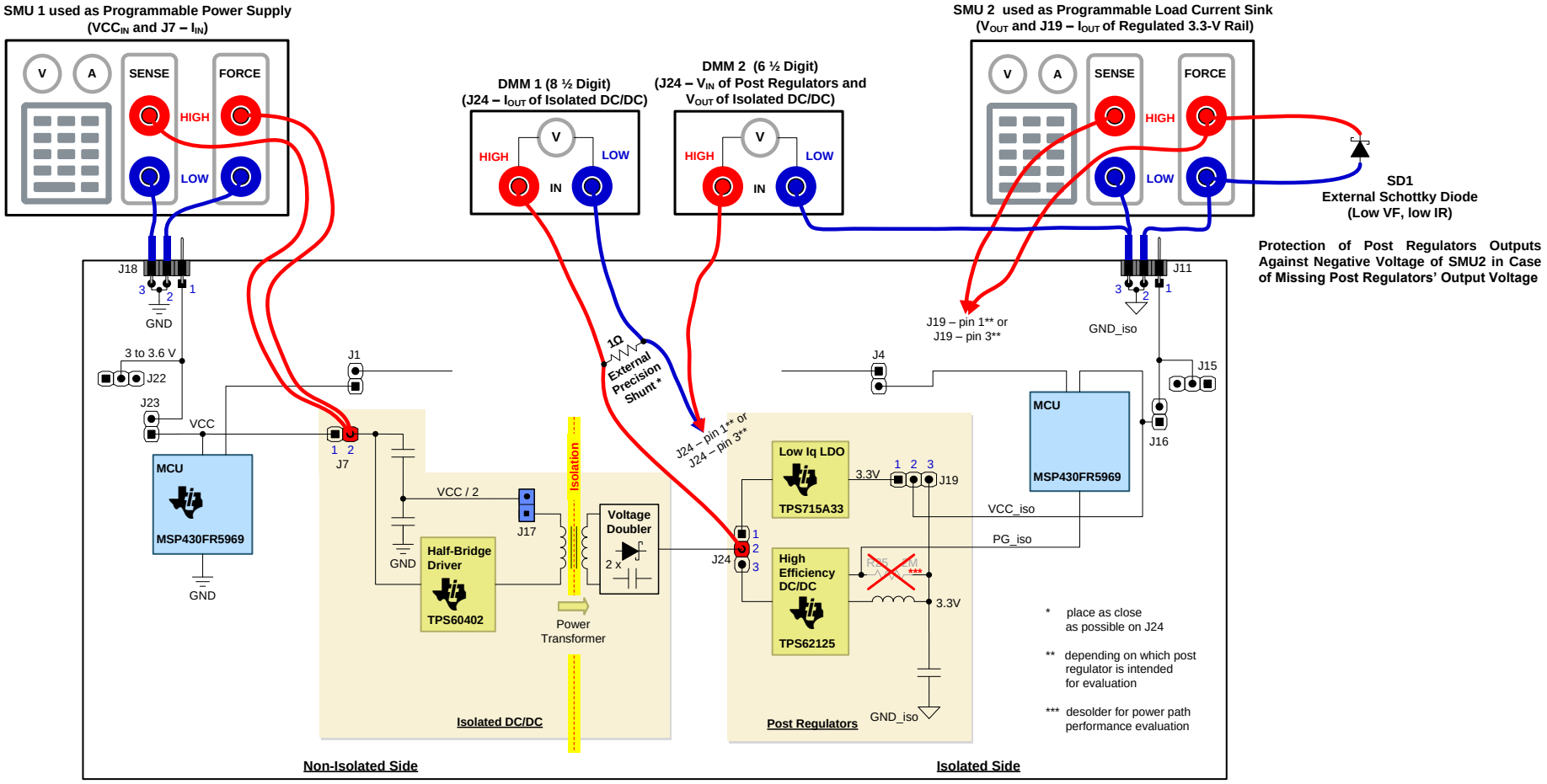


Figure 43. Test Setup for Evaluation of the Power Path

7.1.1 Efficiency of Complete Power Path

Figure 44 to Figure 47 present the total efficiency numbers of the complete power path ranging from the input of the isolated DC/DC (J7) to the output of the selected post regulator (J19). Each of the charts shows the curves taken with the high efficiency DC/DC as well as with the low Iq LDO as post regulator for easy comparison. The post regulators are set up to provide an output voltage of 3.3 V.

In Figure 44 to Figure 46, the three curves provided for each version of the selected post regulator represent the performance at the three different input voltages VCC_{IN} (3, 3.3, and 3.6 V) of the isolated DC/DC. The version using the high efficiency DC/DC provides a better efficiency, especially for output currents larger than 100 µA. The efficiency improvement is up to 30% for output currents exceeding a 2-mA level. Figure 47 highlights the temperature dependency of the efficiency at the nominal input voltage of 3.3 V.

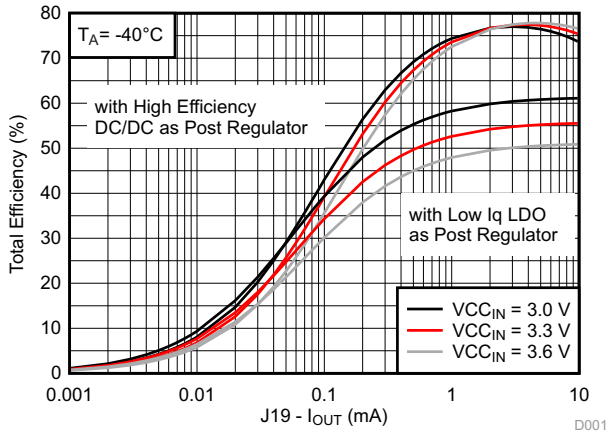


Figure 44. Total Efficiency at T_A = –40°C

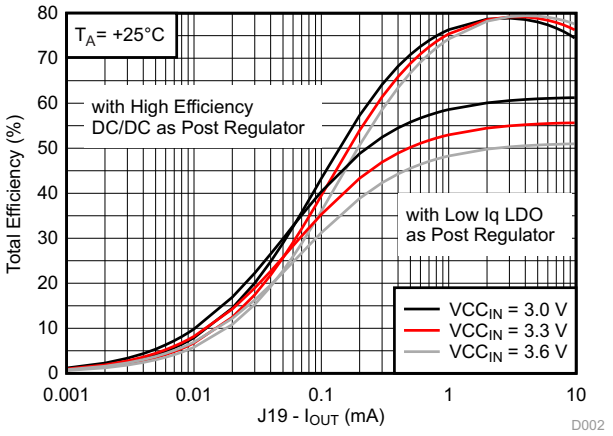


Figure 45. Total Efficiency at T_A = 25°C

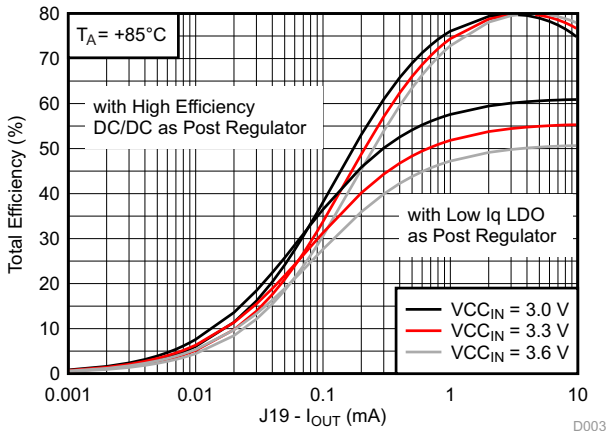


Figure 46. Total Efficiency at T_A = 85°C

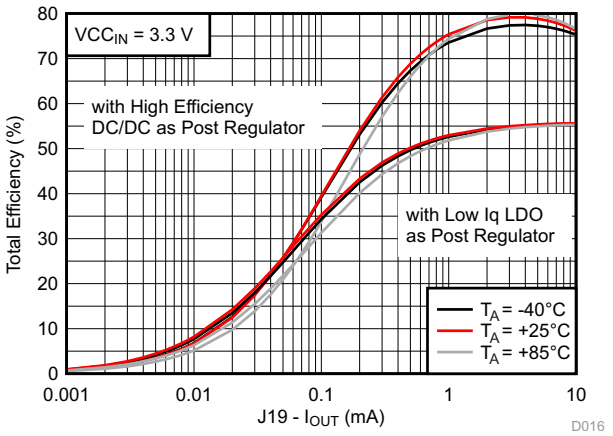


Figure 47. Total Efficiency at VCC_{IN} = 3.3 V

7.1.2 Input Current Consumption of the Complete Power Path

Figure 48 to Figure 50 present the total input current J7 – I_{IN}, which is drawn by the complete power path.

The graphs provide a straight-forward way to cross check whether the current consumption will stay below a certain value for a given output current. This is especially helpful in applications with a limited current budget, such as loop-powered 4- to 20-mA sensor transmitters, metering applications, or systems using energy harvesting. The input current is measured by SMU 1, which feeds the isolated DC/DC converter with an input voltage VCC_{IN} of 3, 3.3, and 3.6 V. J19-IOUT is the output current of the selected post regulator, which is controlled by SMU 2 operating as current sink.

The plotted curves using solid lines to present the total input current when using the high efficiency DC/DC as post regulator. The case of using the low Iq LDO as post regulator is represented by the curves using different dashed and dotted lines. Figure 51 highlights the temperature dependency of the input current consumption of the complete power path at the nominal input voltage of 3.3 V.

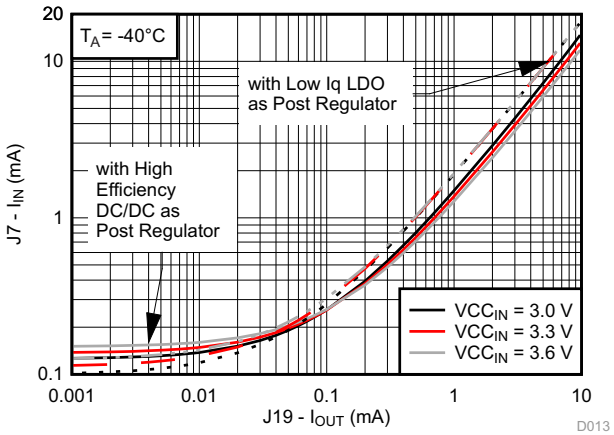


Figure 48. Total Input Current at T_A = –40°C

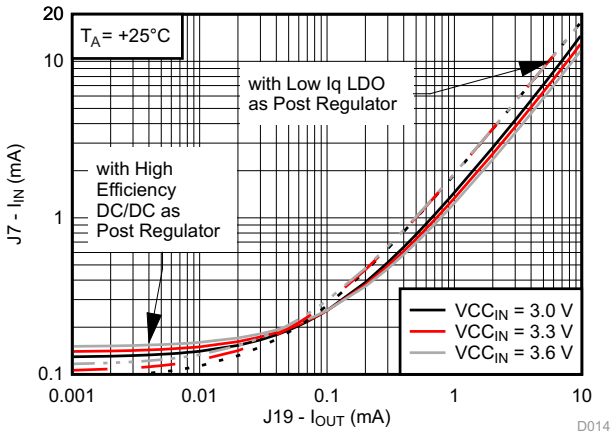


Figure 49. Total Input Current at T_A = 25°C

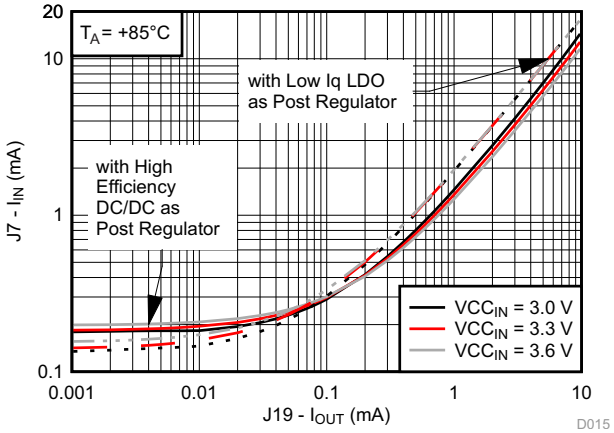


Figure 50. Total Input Current at T_A = 85°C

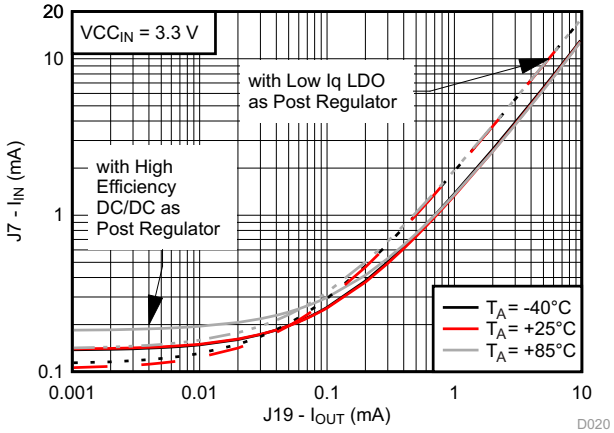


Figure 51. Total Input Current at VCC_{IN} = 3.3 V

7.1.3 Efficiency and Output Voltage of Isolated DC/DC

Figure 52 to Figure 55 present the curves for the efficiency and for the output voltage of the isolated DC/DC, based on the measurements of SMU 1, DMM 1, and DMM 2. The SMU 1 sets the input voltage (VCC_{IN} of 3, 3.3, and 3.6 V) and measures the input current J7 – I_{IN} to get the total input power.

To load the isolated DC/DC, the complete power path was used as described in Section 7.1.1 and Section 7.1.2. The low Iq LDO was selected as post regulator by adequate J24 and J19 setup and configuration according to Table 13. SMU 2 was used to sink a current from the post regulator's output from 1 µA up to 10 mA. SMU 2 was used in this case for controlling the sinking current only. The voltage and current values measured by SMU 2 have not been used in this case, because they do not represent the output voltage and output current of the isolated DC/DC but the values on the output of the post regulator.

The output current of the isolated DC/DC is derived instead by the voltage drop measured with DMM1 across the external 1-Ω precision shunt resistor. The output voltage of the isolated DC/DC (J24-VOUT) is measured with DMM 2 on the input of the low Iq LDO. This voltage differs at 10-mA current flow through the 1-Ω shunt only by 10 mV from the real voltage at the output of the isolated DC/DC. This small 10-mV error is neglectable at the respective output voltage level of at least 4 V.

The derived output voltage and current of the isolated DC/DC was used to calculate its output power and finally to calculate its efficiency by factoring in the before calculated input power. Beside the efficiency, the output voltage (J24-VOUT) is plotted into the same graphs to show the output voltage's load, input voltage, and temperature dependency. The light or no load output voltage is especially important to know when it comes to the selection of a linear or switching post regulator. The post regulator needs to be able to withstand the high output voltage of the isolated DC/DC under such load conditions. Factor in an additional adequate margin.

Figure 55 highlights the temperature dependency of the isolated DC/DC's efficiency and output voltage at the nominal input voltage of 3.3 V.

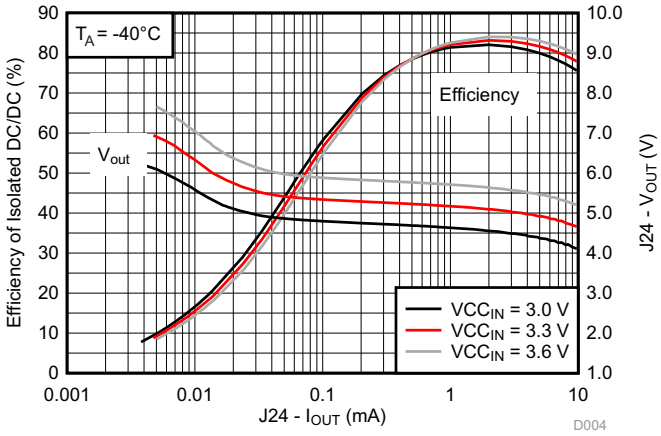


Figure 52. Efficiency and Output Voltage of Isolated DC/DC at T_A = –40°C

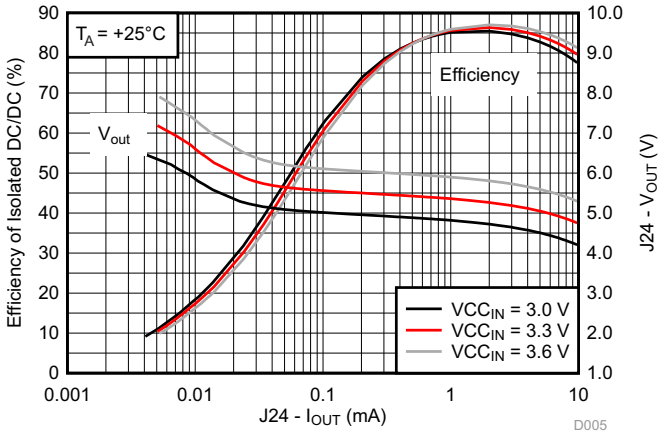


Figure 53. Efficiency and Output Voltage of Isolated DC/DC at T_A = 25°C

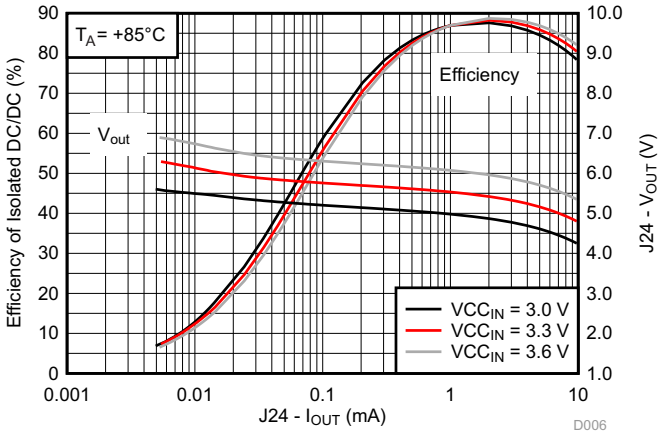


Figure 54. Efficiency and Output Voltage of Isolated DC/DC at T_A = 85°C

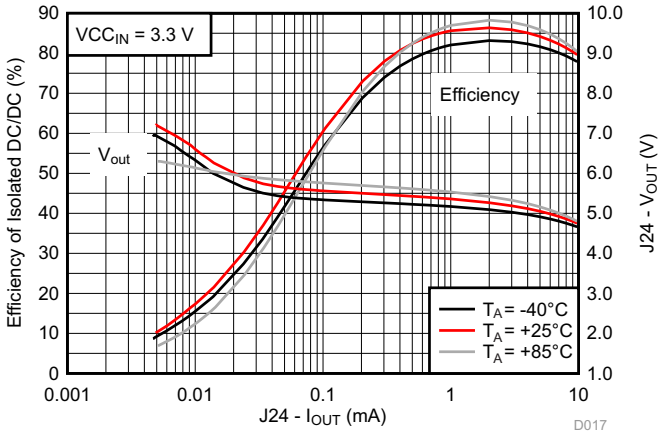


Figure 55. Efficiency and Output Voltage of Isolated DC/DC at VCC_{IN} = 3.3 V

7.1.4 Efficiency and Output Voltage of High Efficiency DC/DC

Figure 56 to Figure 59 present the curves for the efficiency and for the output voltage of the high efficiency DC/DC, based on the measurements of SMU 1, DMM 1, DMM 2, and SMU 2. The high efficiency DC/DC was selected as post regulator by adequate J24 and J19 setup and configuration according to Table 13.

The SMU 1 sets the input voltage (VCC_{IN} of 3, 3.3, and 3.6 V) of the isolated DC/DC applied to pin 2 of J7. SMU 2 was used to sink a current from 1 µA up to 10 mA as load current from the output of the high efficiency DC/DC. This load current (J19-IOUT) was used together with the output voltage (J19-VOUT) measured by SMU 2 to calculate the output power of the high efficiency DC/DC.

The input power of the high efficiency DC/DC have been derived by using the voltage drop measured with DMM1 across the external 1-Ω precision shunt resistor as input current. The input voltage of the high efficiency DC/DC was measured with DMM 2 on the pin 3 of J24.

The measured values of SMU 1 of the input voltage and input current on J7 have not been used in this case to create the efficiency curves directly because they do not represent the input power of the high efficiency DC/DC but the input power of the isolated DC/DC. Nevertheless, the three different values that SMU 1 was set up to provide as VCC_{IN} have been finally used to create for each chart three different efficiency and VOUT curves. Those three different curves can be used to characterize the input voltage dependency of the high efficiency DC/DC. VCC_{IN} is the input voltage applied to the isolated DC/DC but not the real input voltage of the high efficiency DC/DC. The input voltage of the high efficiency DC/DC basically equals the output voltage of the isolated DC/DC, so it changes with loading of the isolated DC/DC as shown in Figure 52 to Figure 55. This restriction is based on the fact that all the performance evaluation and data collection had been done for the complete power path but not for the single power blocks separately. The real input voltage of the high efficiency DC/DC can be approximated by using the different test data graphs using the following steps:

1. Know the following parameters and conditions: ambient temperature T, input voltage VCC_{IN} applied to J7-pin 2, output load current J19-IOUT.

   Example: T = 25°C, VCC_{IN} = 3.3 V, J19-IOUT = 100 µA
2. Determine the efficiency $\eta_{High\ Efficiency\ DC/DC}$ of the high efficiency DC/DC at the given conditions using the respective graphs provided in Section 7.1.4.

   Example: using Figure 57; $\eta_{High\ Efficiency\ DC/DC} \approx 68\%$
3. Determine the total efficiency η_{Total} of the complete power path at the given conditions using the "with High Efficiency DC/DC as Post Regulator" curves of the respective graphs provided in Section 7.1.1.

   Example: using Figure 45; $\eta_{Total} \approx 39.5\%$

4. Calculate the efficiency $\eta_{Isolated\ DC/DC}$ of the isolated DC/DC using

$$\eta_{IsolatedDC/DC} = \frac{\eta_{Total}}{\eta_{High\,Efficiency\,DC/DC}} \quad (13)$$

$$\eta_{IsolatedDC/DC} = \frac{\eta_{Total}}{\eta_{High\ Efficiency\ DC/DC}} \approx \frac{0.395}{0.68} \approx 0.58$$

5. Use the graphs provided in Section 7.1.3 to determine an approximated value for the input voltage of the high efficiency DC/DC (J24-VIN), which is equal to the J24-VOUT value shown on the right vertical axis of the graphs. If the graphs and curves for the applicable ambient temperature T and input voltage VCC_{IN} are used, the J24-VIN can be found on the VOUT curves at the J24-IOUT value resulting in the efficiency $\eta_{Isolated\ DC/DC}$ of the isolated DC/DC as calculated in the previous step. See the following example:
   - Using the efficiency curves of Figure 53 to find J24-IOUT at which $\eta_{Isolated\ DC/DC} \approx 0.58$ J24-IOUT = 90 µA
   - Using VOUT curves of Figure 53 to determine the VOUT at the previously found J24-IOUT: VOUT ≈ 5.55 V at J24-IOUT = 90 µA

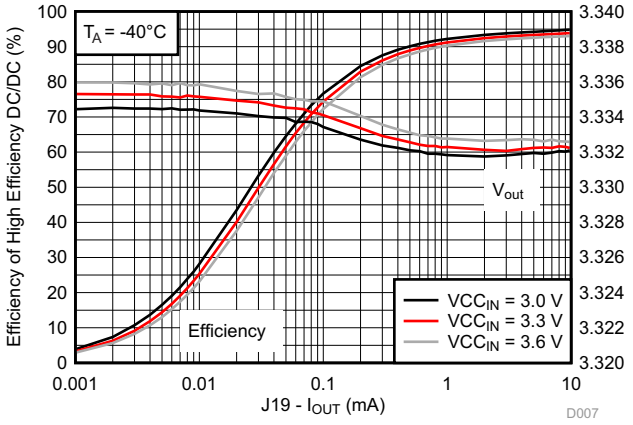


Figure 56. Efficiency and Output Voltage of High Efficiency DC/DC at T_A = –40°C

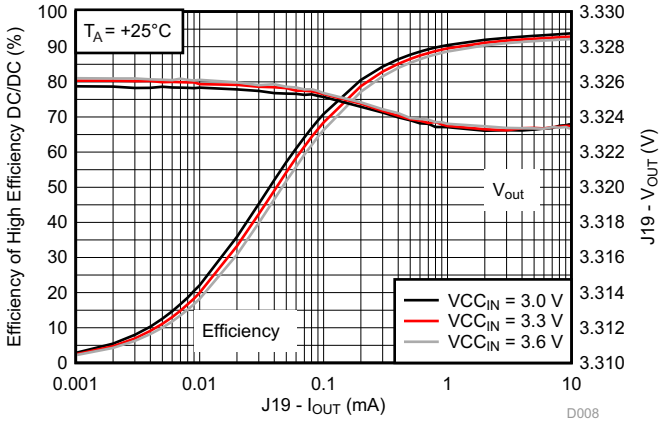


Figure 57. Efficiency and Output Voltage of High Efficiency DC/DC at T_A = 25°C

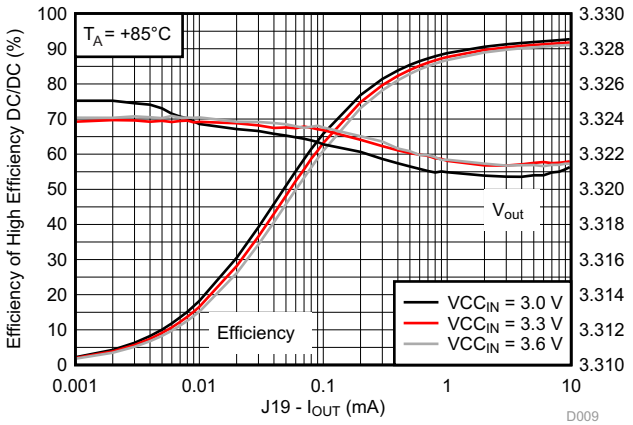


Figure 58. Efficiency and Output Voltage of High Efficiency DC/DC at T_A = 85°C

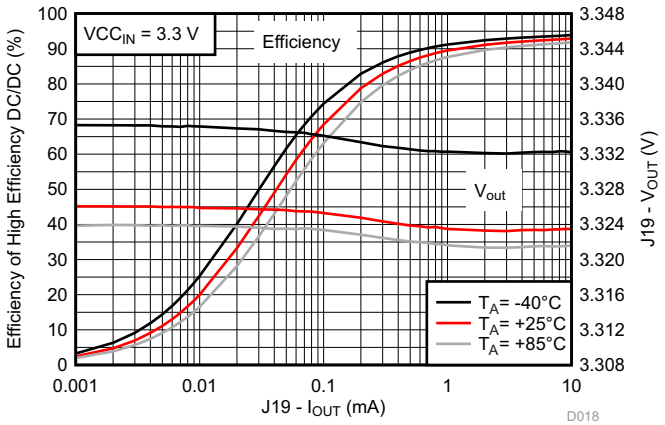


Figure 59. Efficiency and Output Voltage of High Efficiency DC/DC at VCC_{IN} = 3.3 V

7.1.5 Efficiency and Output Voltage of Low Iq LDO

Figure 60 to Figure 63 present the curves for the efficiency and for the output voltage of the low Iq LDO, based on the measurements of SMU 1, DMM 1, DMM 2, and SMU 2. The low Iq LDO was selected as post regulator by adequate J24 and J19 setup and configuration according to Table 13.

The SMU 1 sets the input voltage (VCC_{IN} of 3, 3.3, and 3.6 V) of the isolated DC/DC applied to pin 2 of J7. SMU 2 was used to sink a current from 1 µA up to 10 mA as a load current from the low Iq LDO. This load current (J19-IOUT) was used together with the output voltage (J19-VOUT) measured by SMU 2 to calculate the output power of the low Iq LDO.

The input power of the low Iq LDO have been derived by using the voltage drop measured with DMM1 across the external 1-Ω precision shunt resistor as input current. The input voltage of the low Iq LDO was measured with DMM 2 on the pin 1 of J24.

The measured values of SMU 1 of the input voltage and input current on J7 have not been used in this case to create the efficiency curves directly because they do not represent the input power of the low Iq LDO but the input power of the isolated DC/DC. Nevertheless, the three different values that SMU 1 was set up to provide as VCC_{IN} have been used to create for each chart three different efficiency and VOUT curves. Those three different curves can be used for kind of characterizing the input voltage dependency of the low Iq LDO. VCC_{IN} is the input voltage applied to the isolated DC/DC but not the real input voltage of the low Iq LDO. The input voltage of the low Iq LDO basically equals the output voltage of the isolated DC/DC, so it changes with loading of the isolated DC/DC as shown in Figure 52 to Figure 55. This restriction is based on the fact that all the performance evaluation and data collection had been done for the complete power path but not for the single power blocks separately.

Because the low Iq LDO was also selected as post regulator for the creation of the efficiency and output voltage curves of the isolated DC/DC (Figure 52 to Figure 55), approximating the real input voltage of the low Iq LDO is more straightforward compared to the method described before in Section 7.1.4. The needed steps are as follows:

1. Know the following parameters and conditions: ambient temperature T, input voltage VCC_{IN} applied to J7-pin 2, output load current J19-IOUT. See the following example:

   T = 25°C, VCC_{IN} = 3.3 V, J19-IOUT = 10 µA

2. Use the VOUT curves of the graphs provided in Section 7.1.3 to determine an approximated value for the input voltage of the low Iq LDO (J24-VIN). This input voltage is equal the J24-VOUT value at

   $$J24\_IOUT = J19\_IOUT + Iq_{U5} \approx J19\_IOUT + 3.2\ \mu A \quad (14)$$

   where Iq_{U5} is the quiescent current of the low Iq LDO U5. Iq is given with a typical value of 3.2 µA in the datasheet of the TPS715A33 [2]

   $J24\_IOUT \approx 10\ \mu A + 3.2\ \mu A = 13.2\ \mu A$

   $J24 - VIN \text{ at } 13.2\ \mu A \approx 6.25\ V$

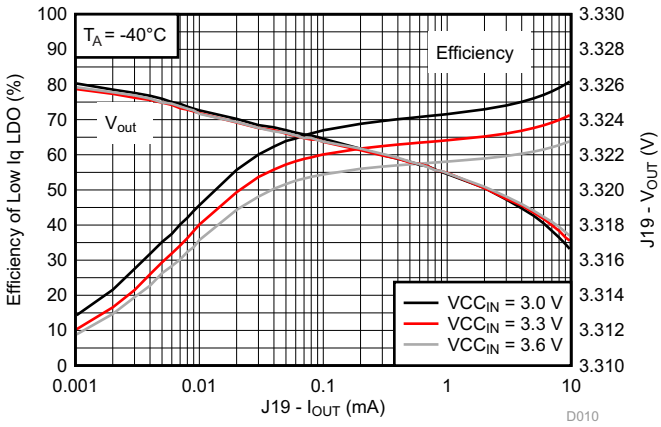


Figure 60. Efficiency and Output Voltage of Low Iq LDO at T_A = –40°C

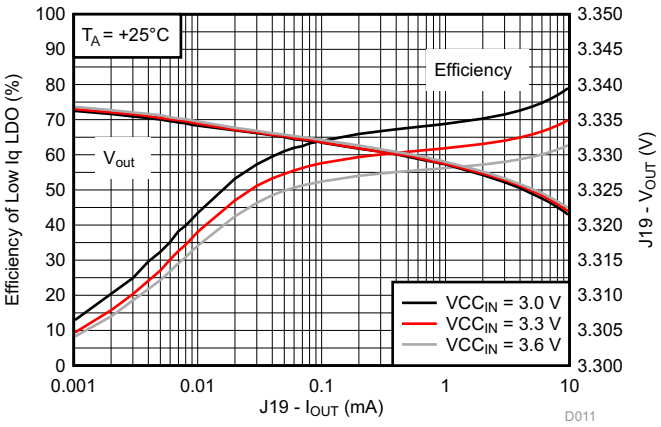


Figure 61. Efficiency and Output Voltage of Low Iq LDO at T_A = 25°C

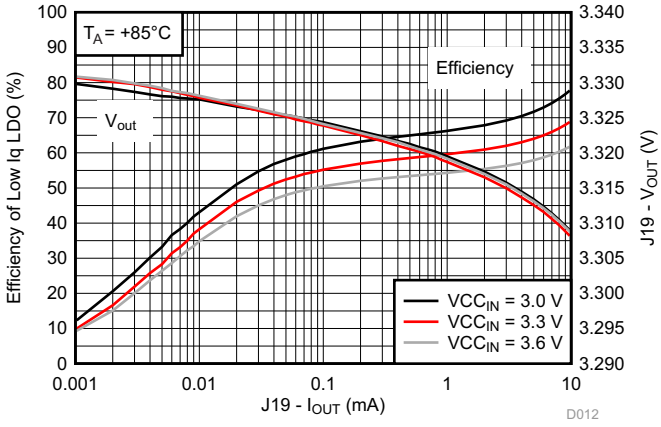


Figure 62. Efficiency and Output Voltage of Low Iq LDO at T_A = 85°C

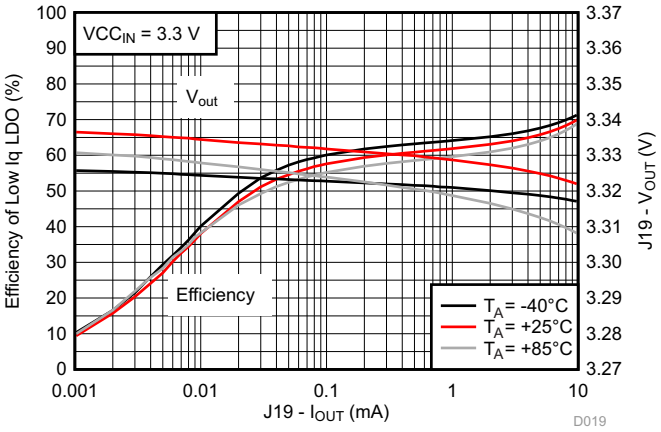


Figure 63. Efficiency and Output Voltage of Low Iq LDO at VCC_{IN} = 3.3 V

7.2 Isolated Data Transmission Testing

7.2.1 Functional Testing

The data transmission has been successfully tested from –40°C to 85°C. Random data has been transmitted in unidirectional mode and in half-duplex mode. For the half-duplex mode, the transmission direction was changed after every byte. The tested data rates were 9.6 kBaud, 31.25 kBaud, 62.5 kBaud, 125 kBaud, 250 kBaud, 500 kBaud, and 1 MBaud.

7.2.2 Current Consumption

Table 14 shows the results for the shutdown and the standby current.

Table 14. Standby and Shutdown Currents

PARAMETER	SPECIFICATION	CURRENT FOR NON-ISOLATED SIDE	CURRENT INTO ISOLATED SIDE	OVERALL SYSTEM CURRENT	UNIT
Standby current with LDO and LPM0	System standby and receive ready @ 3.0 V	175.0	417.5	592.5	µA
	System standby and receive ready @ 3.3 V	177.1	428.0	605.1	µA
	System standby and receive ready @ 3.6 V	179.3	438.5	617.8	µA
Standby current with LDO and LPM3	System standby and receive ready @ 3.0 V	22.5	141.0	163.5	µA
	System standby and receive ready @ 3.3 V	23.8	152.3	176.1	µA
	System standby and receive ready @ 3.6 V	25.0	163.3	188.3	µA
Shutdown current with LDO	System shutdown current @ 3.0 V	1.4	100.3	101.7	µA
	System shutdown current @ 3.3 V	1.5	111.0	112.5	µA
	System shutdown current @ 3.6 V	1.6	121.9	123.5	µA
Standby current with High Efficiency DC/DC and LPM0	System standby and receive ready @ 3.0 V	175.0	363.1	538.1	µA
	System standby and receive ready @ 3.3 V	177.1	353.2	530.3	µA
	System standby and receive ready @ 3.6 V	179.3	346.9	526.2	µA
Standby current with high efficiency DC/DC and LPM3	System standby and receive ready @ 3.0 V	22.5	163.4	185.9	µA
	System standby and receive ready @ 3.3 V	23.8	172.1	195.9	µA
	System standby and receive ready @ 3.6 V	25.0	181.7	206.7	µA
Shutdown current with high efficiency DC/DC	System shutdown current @ 3.0 V	1.4	136.6	138.0	µA
	System shutdown current @ 3.3 V	1.5	147.5	149.0	µA
	System shutdown current @ 3.6 V	1.6	159.5	161.1	µA

Figure 64 shows the current consumption of the complete system in half-duplex mode. Both MSP430FR5969s are active and the CPU is running with 8 MHz. The communication is continuously running in both directions. One byte is sent and then echoed back from the other side of the isolation.

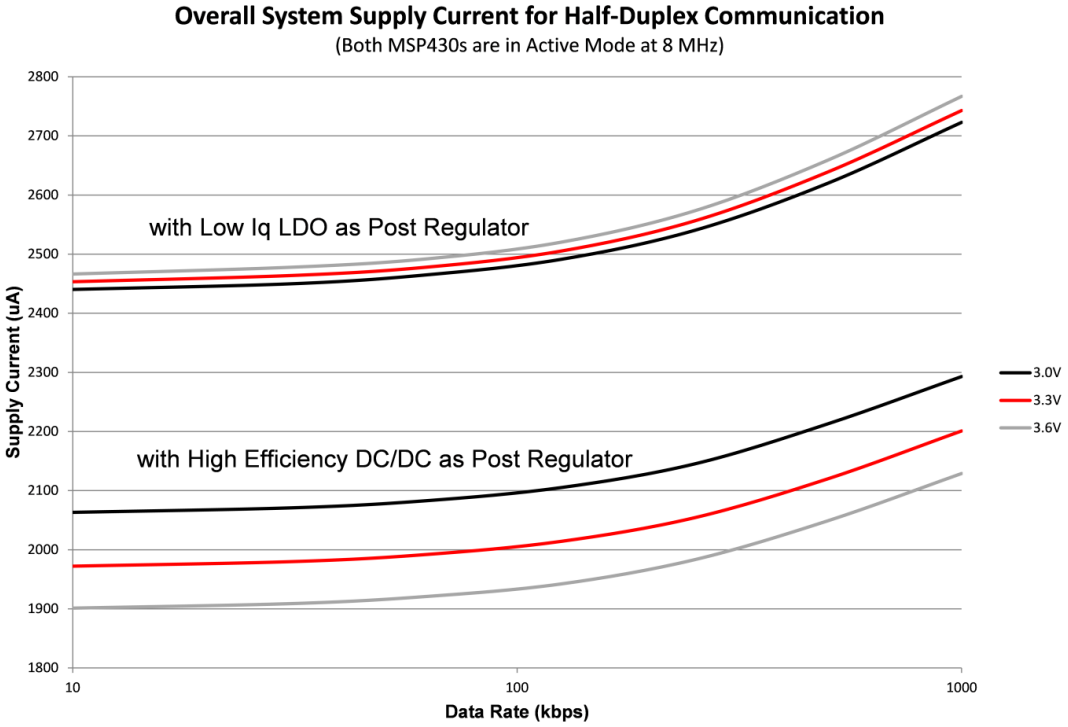


Figure 64. Overall System Supply Current

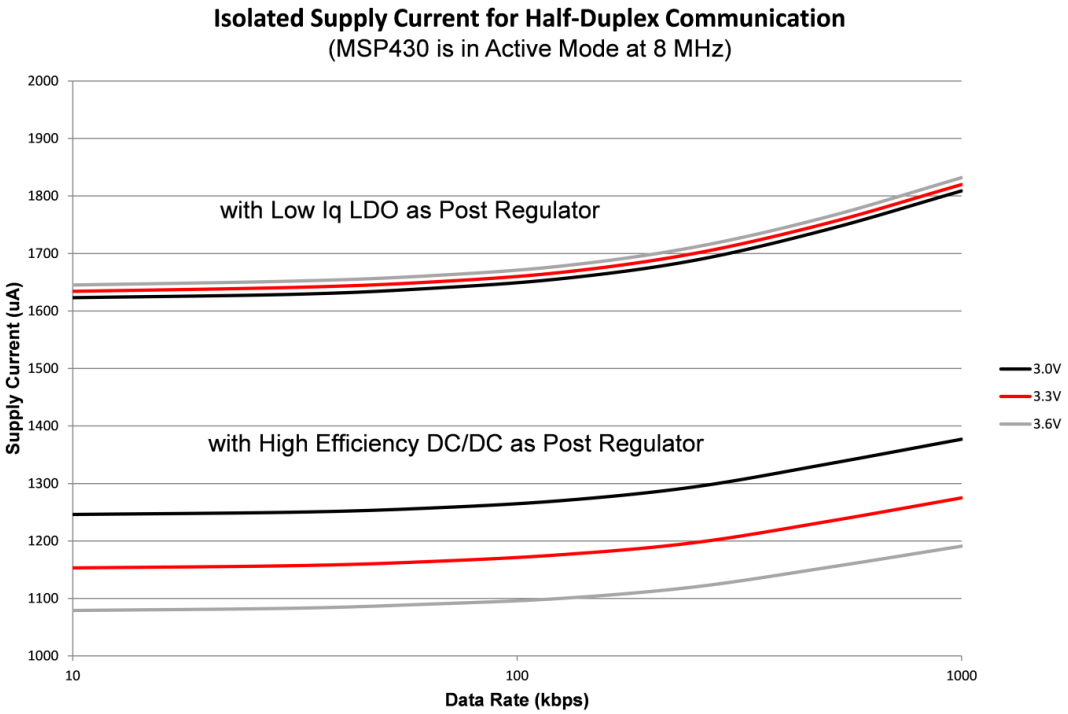


Figure 65. Isolated System Supply Current

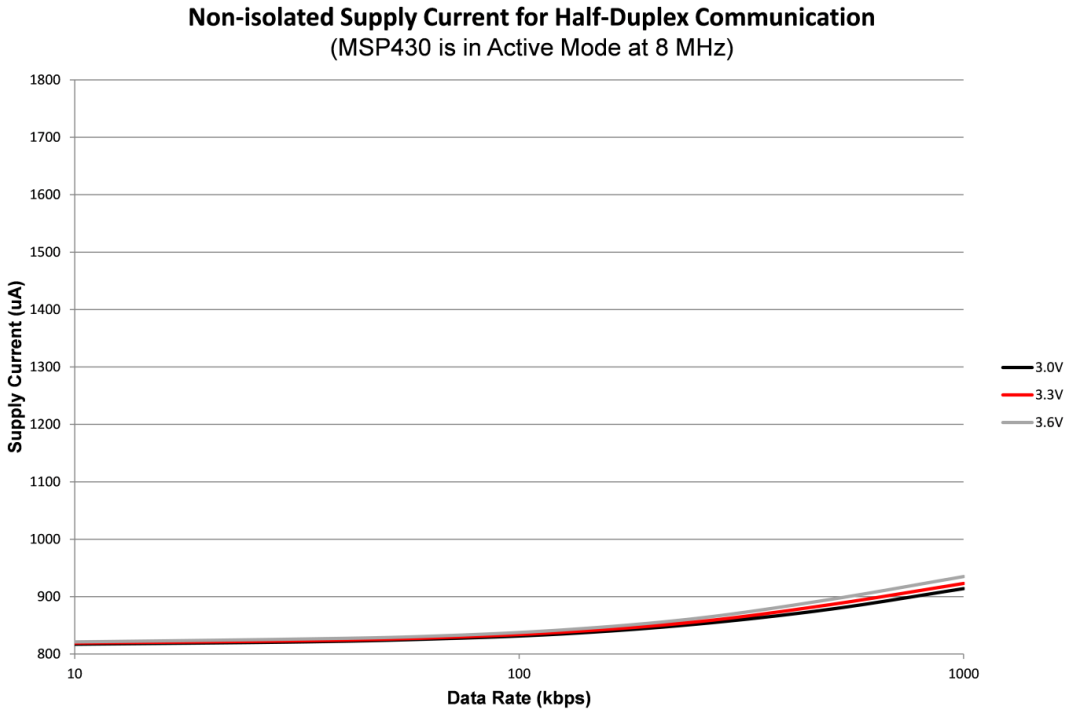


Figure 66. Non-Isolated System Supply Current

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00459.

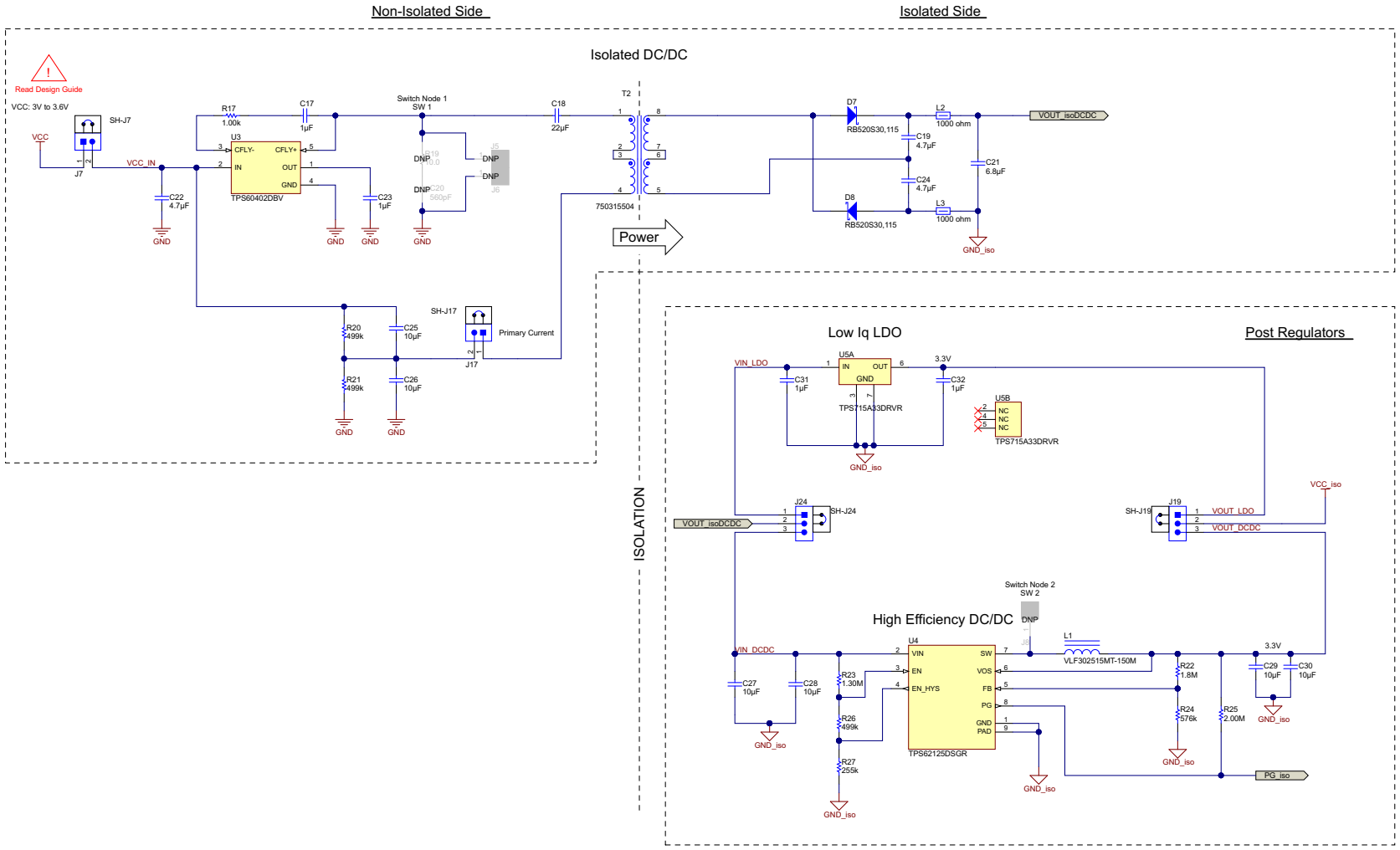


Figure 67. Isolated DC/DC Converter and Post Regulators Schematic

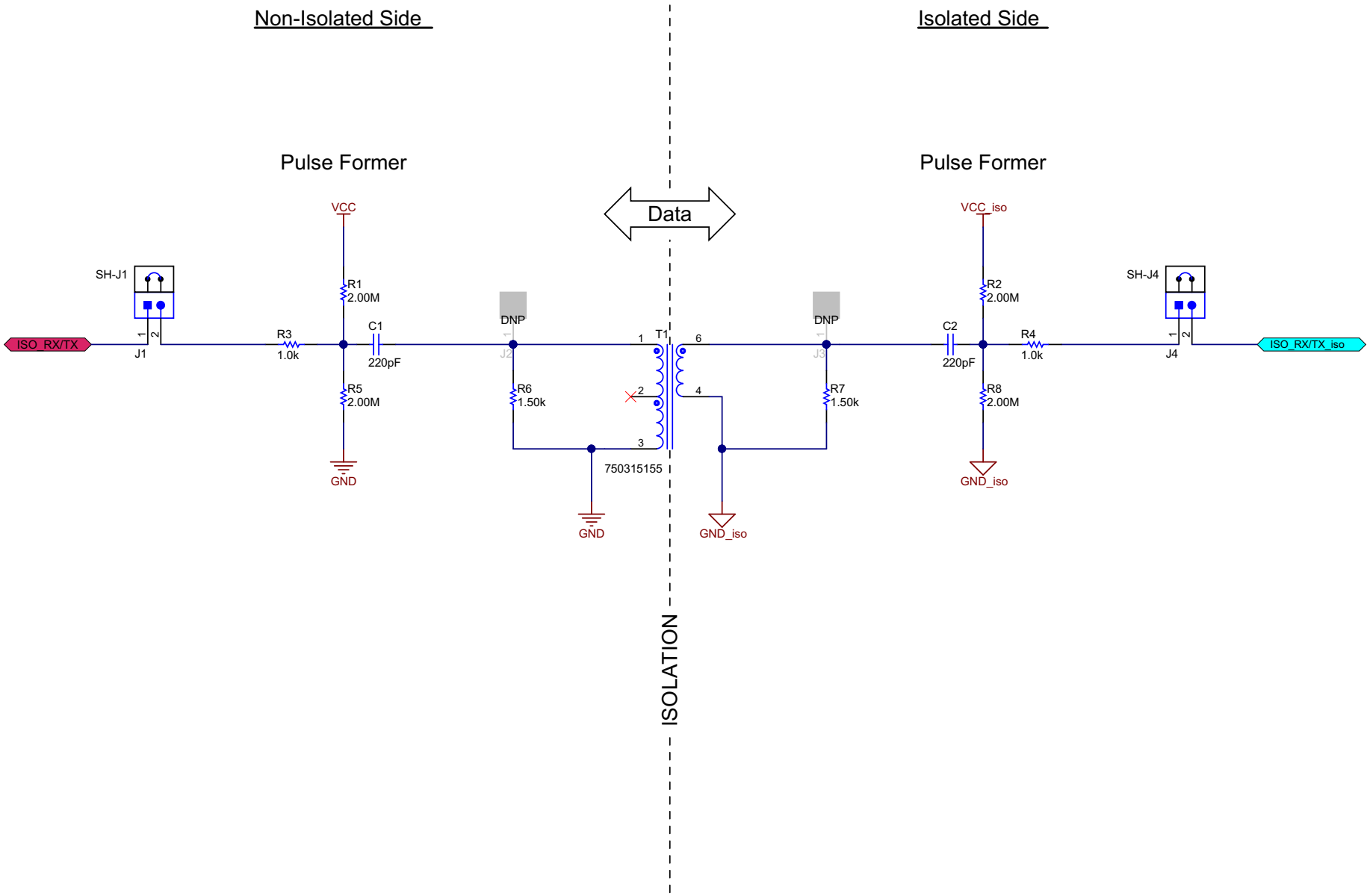


Figure 68. Isolation Schematic

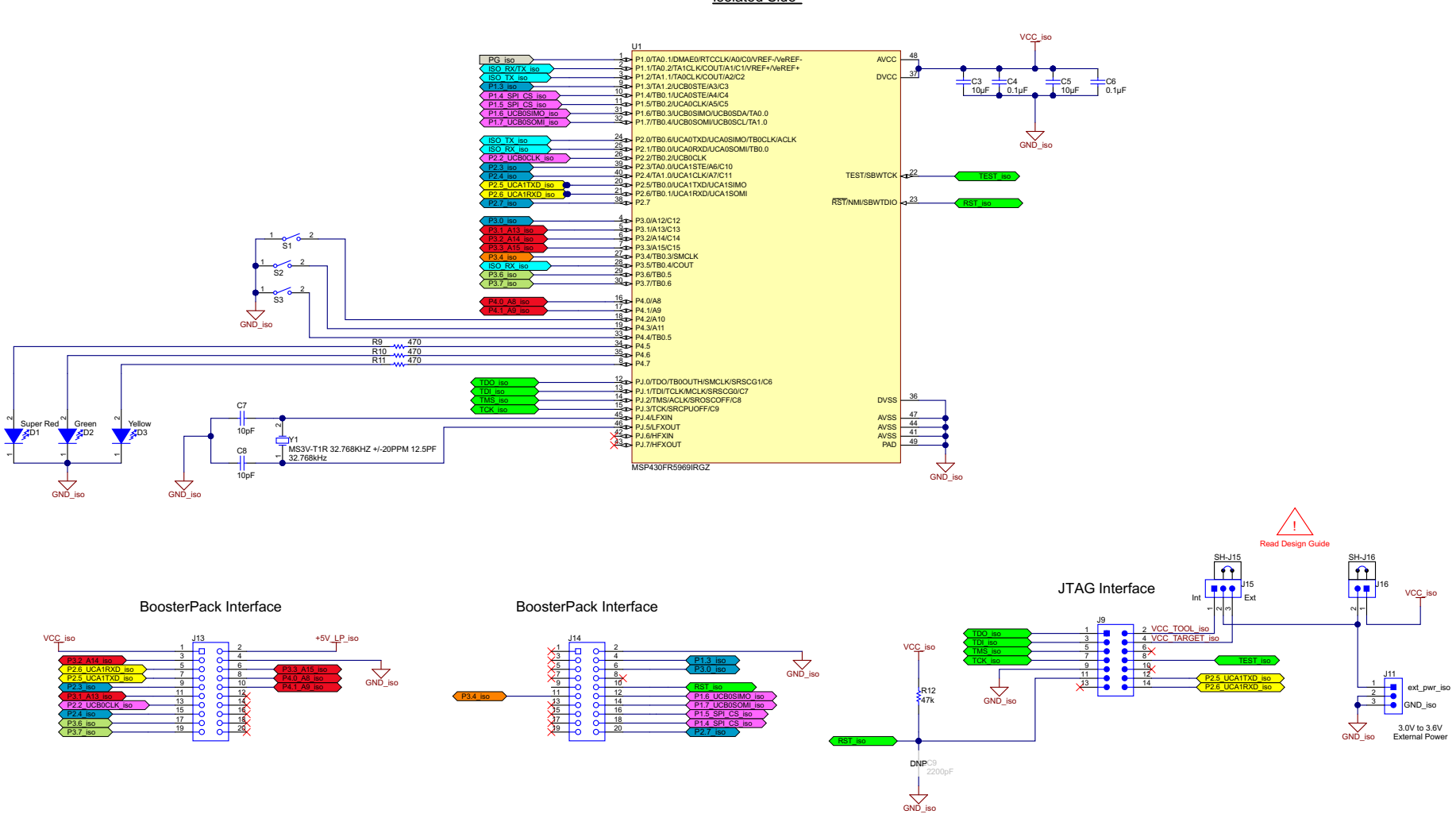


Figure 69. MCU 1—Isolated Side Schematic

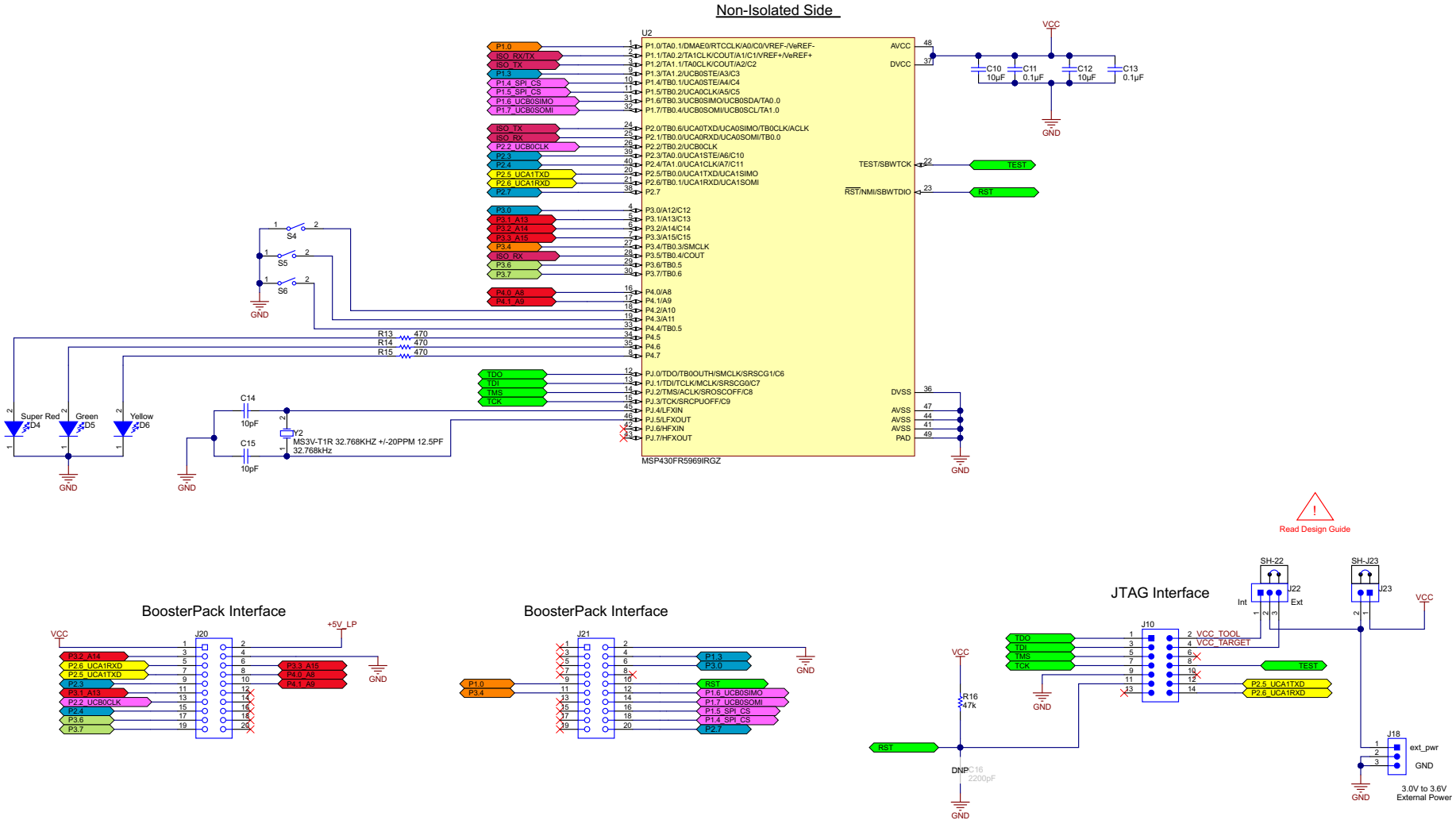


Figure 70. MCU 1—Non-Isolated Side Schematic

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00459.

Table 15. BOM

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	!PCB1	1		TIDA-00459	Any	Printed Circuit Board	
2	C1, C2	2	220pF	C1608C0G1H221J	TDK	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603
3	C3, C5, C10, C12, C27, C28, C29, C30	8	10uF	GRM21BR61C106KE15L	MuRata	CAP, CERM, 10 µF, 16 V, +/- 10%, X5R, 0805	0805
4	C4, C6, C11, C13	4	0.1uF	GRM155R71A104KA01D	MuRata	CAP, CERM, 0.1 µF, 10 V, +/- 10%, X7R, 0402	0402
5	C7, C8, C14, C15	4	10pF	GRM1555C1H100JA01D	MuRata	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402
6	C17	1	1uF	GRM155R61A105KE15D	MuRata	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0402	0402
7	C18	1	22uF	GRM31CR61A226KE19L	MuRata	CAP, CERM, 22uF, 10V, +/-10%, X5R, 1206	1206
8	C19, C24	2	4.7uF	CGB3B1X5R1A475K055AC	TDK	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X5R, 0603	0603
9	C21	1	6.8uF	C1608X5R1E685K080AC	TDK	CAP, CERM, 6.8 µF, 25 V, +/- 10%, X5R, 0603	0603
10	C22	1	4.7uF	C0603C475K8PACTU	Kemet	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603	0603
11	C23	1	1uF	GRM188R71A105KA61D	MuRata	CAP, CERM, 1uF, 10V, +/-10%, X7R, 0603	0603
12	C25, C26	2	10uF	GRM21BR71A106KE51L	MuRata	CAP, CERM, 10uF, 10V, +/-10%, X7R, 0805	0805
13	C31	1	1uF	GRM188R61C105KA93D	MuRata	CAP, CERM, 1 µF, 16 V, +/- 10%, X5R, 0603	0603
14	C32	1	1uF	GRM188R61A105KA61D	MuRata	CAP, CERM, 1 µF, 10 V, +/- 10%, X5R, 0603	0603
15	D1, D4	2	Super Red	150060SS75000	Wurth Elektronik eiSos	LED, Super Red, SMD	LED_0603
16	D2, D5	2	Green	150060VS75000	Wurth Elektronik eiSos	LED, Green, SMD	LED_0603
17	D3, D6	2	Yellow	150060YS75000	Wurth Elektronik eiSos	LED, Yellow, SMD	LED_0603
18	D7, D8	2	30V	RB520S30,115	NXP Semiconductor	Diode, Schottky, 30 V, 0.2 A, SOD-523	SOD-523
19	J1, J4, J7, J16, J17, J23	6		61300211121	Wurth Elektronik	Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH

Table 15. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
20	J9, J10	2		SBH11-PBPC-D07-RA-BK	Sullins Connector Solutions	Header (Shrouded), 2.54 mm, 7x2, Gold, R/A, TH	Header (Shrouded), 2.54 mm, 7x2, R/A, TH
21	J11, J18	2		TSW-103-08-G-S-RA	Samtec	Header, 100mil, 3x1, Gold, R/A, TH	3x1 R/A Header
22	J13, J14, J20, J21	4		SSW-110-23-F-D	Samtec	Connector, Receptacle, 100mil, 10x2, Gold plated, TH	10x2 Receptacle
23	J15, J19, J22, J24	4		61300311121	Wurth Elektronik	Header, 2.54 mm, 3x1, Gold, TH	Header, 2.54mm, 3x1, TH
24	L1	1	15uH	VLF302515MT-150M	TDK	Inductor, Shielded, Ferrite, 15 µH, 0.56 A, 0.275 ohm, SMD	IND_3x1.5x3mm
25	L2, L3	2	1000 ohm	742792662	Wurth Elektronik	Ferrite Bead, 1000 ohm @ 100 MHz, 0.6 A, 0603	0603
26	R1, R2, R5, R8, R25	5	2.00Meg	CRCW06032M00FKEA	Vishay-Dale	RES, 2.00 M, 1%, 0.1 W, 0603	0603
27	R3, R4	2	1.0k	CRCW06031K00JNEA	Vishay-Dale	RES, 1.0 k, 5%, 0.1 W, 0603	0603
28	R6, R7	2	1.50k	CRCW06031K50FKEA	Vishay-Dale	RES, 1.50 k, 1%, 0.1 W, 0603	0603
29	R9, R10, R11, R13, R14, R15	6	470	CRCW0402470RJNED	Vishay-Dale	RES, 470, 5%, 0.063 W, 0402	0402
30	R12, R16	2	47k	CRCW040247K0JNED	Vishay-Dale	RES, 47 k, 5%, 0.063 W, 0402	0402
31	R17	1	1.00k	CRCW04021K00FKED	Vishay-Dale	RES, 1.00k ohm, 1%, 0.063W, 0402	0402
32	R20, R21	2	499k	CRCW0402499KFKED	Vishay-Dale	RES, 499k ohm, 1%, 0.063W, 0402	0402
33	R22	1	1.8Meg	CRCW06031M80FKEA	Vishay-Dale	RES, 1.8 M, 1%, 0.1 W, 0603	0603
34	R23	1	1.30Meg	CRCW06031M30FKEA	Vishay-Dale	RES, 1.30 M, 1%, 0.1 W, 0603	0603
35	R24	1	576k	CRCW0603576KFKEA	Vishay-Dale	RES, 576 k, 1%, 0.1 W, 0603	0603
36	R26	1	499k	CRCW0603499KFKEA	Vishay-Dale	RES, 499 k, 1%, 0.1 W, 0603	0603
37	R27	1	255k	CRCW0603255KFKEA	Vishay-Dale	RES, 255 k, 1%, 0.1 W, 0603	0603
38	S1, S2, S3, S4, S5, S6	6		434121025816	Wurth Elektronik eiSos	Switch, Tactile, SPST, 12 V, SMD	SMD, 6x3.9mm
39	SH-22, SH-J1, SH-J4, SH-J7, SH-J15, SH-J16, SH-J17, SH-J19, SH-J23, SH-J24	10	1x2	969102-0000-DA	3M	Shunt, 100mil, Gold plated, Black	Shunt
40	T1	1	400 uH	750315155	Wurth Elektronik eiSos	Transformer, 400 uH, SMT	SMD, Body 8.26x6.6mm
41	T2	1	1.8 mH	750315504	Wurth Elektronik	Transformer, 1.8 mH, SMT	8.38x7.87mm
42	U1, U2	2		MSP430FR5969IRGZ	Texas Instruments	Mixed Signal Microcontroller, RGZ0048B	RGZ0048B

Table 15. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
43	U3	1		TPS60402DBV	Texas Instruments	UNREGULATED 60-mA CHARGE PUMP VOLTAGE INVERTER, DBV0005A	DBV0005A
44	U4	1		TPS62125DSGR	Texas Instruments	3V-17V, 300mA Step Down Converter With Adjustable Enable Threshold And Hysteresis, DSG0008A	DSG0008A
45	U5	1		TPS715A33DRVR	Texas Instruments	Single Output LDO, 80 mA, Fixed 3.3 V Output, 2.5 to 24 V Input, with Low IQ, 6-pin SON (DRV), -40 to 85 degC, Green (RoHS & no Sb/Br)	DRV0006A
46	Y1, Y2	2		MS3V-T1R 32.768KHZ +/- 20PPM 12.5PF	Micro Crystal AG	Crystal, 32.768kHz, 12.5pF, SMD	1.4x1.4x5.0mm SMD
47	C9, C16	0	2200pF	GRM155R70J222KA01D	MuRata	CAP, CERM, 2200 pF, 6.3 V, +/- 10%, X7R, 0402	0402
48	C20	0	560pF	GRM155R71H561KA01D	MuRata	CAP, CERM, 560pF, 50V, +/-10%, X7R, 0402	0402
49	FID1, FID2, FID3	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	N/A
50	H1, H2, H3, H4	0		NY PMS 440 0025 PH	B&F Fastener Supply	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw
51	H5, H6, H7, H8	0		1902C	Keystone	Standoff, Hex, 0.5"L #4-40 Nylon	Standoff
52	J2, J3, J5, J6, J8	0		61300111121	Wurth Elektronik	Header, 2.54 mm, 1x1, Gold, TH	Header, 2.54 mm, 1x1, TH
53	R19	0	10.0	CRCW040210R0FKED	Vishay-Dale	RES, 10.0 ohm, 1%, 0.063W, 0402	0402

8.3 PCB Layout Recommendations

The TIDA-00459 board has the form factor of a LaunchPad. A LaunchPad is an easy-to-use development tool intended for beginners and experienced users alike for creating microcontroller-based applications. For the LaunchPad, there are BoosterPack plug-in boards available to expand the LaunchPad's functionality. BoosterPack plug-in modules (www.ti.com/boosterpack) allow the user to add features like wireless connectivity, capacitive touch, temperature sensing, displays, and much more.

To create a BoosterPack for specific needs, use the resources found at http://www.ti.com/ww/en/launchpad/byob.html to create your BoosterPack design files, get support from our community, and take your idea from concept to PCB to product in a few easy steps.

8.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00459.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00459.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00459.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00459.

9 Software Files

To download the software files, see the design files at TIDA-00459.

10 References

1. Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies*, SN6501 Datasheet, (SLLSEA0)
2. Texas Instruments, *TPS715A, 24-V High Input Voltage, Micropower, 80-mA LDO Voltage Regulator*, TPS715A Datasheet; (SBVS047)
3. Texas Instruments, *TPS62125, 3-V to 17-V, 300-mA Step-Down Converter With Adjustable Enable Threshold and Hysteresis*, TPS62125 Datasheet; (SLVSAQ5)
4. Texas Instruments, *MSP430FR59xx Mixed-Signal Microcontrollers*, MSP430FR5969 Datasheet (SLAS704)
5. Texas Instruments, *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*, MSP430FR5969 User's Guide (SLAU367)
6. Texas Instruments, *TPS6040x Unregulated 60-mA Charge Pump Voltage Inverter*, TPS60402 Datasheet (SLVS324)
7. Texas Instruments, *Uniquely Efficient Isolated DC/DC Converter for Ultra-Low Power and Low-Power Applications*, TIDA-00349 Reference Design (TIDU813)
8. Texas Instruments, *Isolated, Ultra-Low Power Design for 4- to 20-mA Loop-Powered Transmitters*, TIDA-00167 Reference Guide (TIDU414)
9. Texas Instruments, *Magnetics Design for Switching Power Supplies*, Design Handbook (SLUP123)
10. Würth Elektronik, Power Transformer Spec Sheet 50315504 (PDF)

11 About the Author

THOMAS SCHNEIDER is a Systems Engineer at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Thomas brings to this role his wide experience in TI microcontrollers, especially MSP430. Thomas earned his Dipl.-Ing. (Univ.) degree in electrical engineering from the Technical University Munich (TUM) in Munich, Germany.

JÜERGEN SCHNEIDER is a Systems Engineer at Texas Instruments where he is responsible for developing TI Designs for the industrial automation segment. He holds a Dipl.-Ing. (FH) degree in industrial electronics and has worked 13 years as a design engineer for semiconductor manufacturing equipment, telemetry systems, and electro-medical devices before joining TI in 1999. Jüergen has worked with TI as an analog field specialist, FAE, and systems engineer for power solutions. He presents at technical conferences and seminars and has been one of the presenters of the industry-wide known TI Power Supply Design Seminar for multiple years. Jüergen also has the distinguishment of being elected as a Member, Group Technical Staff.

Revision History

Changes from Original (June 2015) to A Revision	Page
• Changed from preview page	1

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