TI Designs

Shunt-Based Ground Fault Protection for Inverters Powered from 100/110-V AC Supply

Design Overview

This TI design provides a reference solution for detecting ground fault in inverter-based drives. The inverter current is measured on both DC positive and DC negative bus using shunt resistors. The INA149 current sense amplifier with a common mode voltage range of 275 V is used to measure current on DC positive bus. Current on DC negative bus is sensed using precision op-amps. The difference between the two measured currents is compared against a fixed threshold to determine the ground fault condition using high-speed comparators.

Design Resources

TIDA-00439	Design Folder
INA149	Product Folder
OPA2376	Product Folder
TLC372	Product Folder
REF2033	Product Folder
TMDSHVMTRPFCKIT	Product Folder

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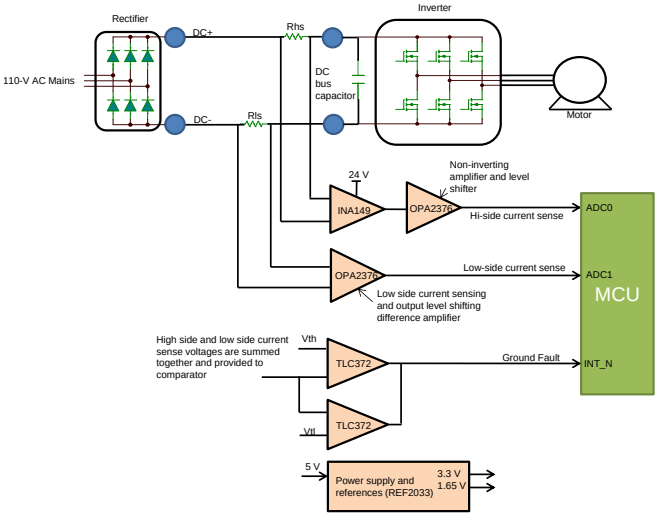
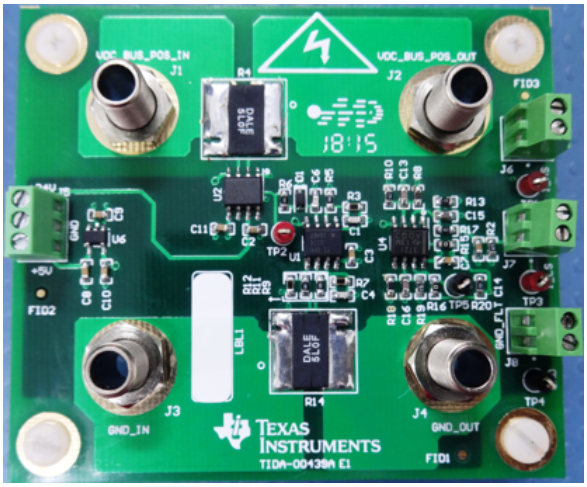
Design Features

- Shunt-Based Current Sensing for Inverter Control and Protection
- Rated to Measure DC Link Current of ±20 A_{pk} (Design Tested for ±5 A)
- High-Side Current Sense Circuit With High Common Mode Voltage of 275 V Supporting 100/110-V AC Mains Powered Drives
- Calibrated High-Side and Low-Side Measurement Error Over Operating Temperature Range of –10°C to 55°C < 1.5%
- Ground Fault:
  - Minimum Fault Current Detection of 300 mA
  - Detection Time of Less Than 50 µs
- Designed to be Interfaced With Built-in 3.3-V ADC of MCU

Featured Applications

- Variable Speed Drives
- Consumer Appliances
  - Washing Machine, Refrigerator, Air Conditioners, and so on





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1 Introduction

Ground faults are one of the major causes of drive failures. Early detection of ground faults can avoid major drive damage, electrocution of personnel, and fire hazards. This TI Design provides a reference solution to detect ground fault subsequently enabling shutdown of an inverter.

1.1 Ground fault in drives

A motor is considered to be a balanced 3-phase load; therefore, during the normal operating condition of a drive system, the sum of three phase currents drawn from the source should be zero. Due to faults in the motor winding or the cabling from the drive to the motor or in the drive itself, current can leak into the earth through the chassis of the motor or drive creating ground fault. This leak can cause hazardous situations and should be avoided.

An example ground fault condition is shown in Figure 1. In a power distribution system, the neutral wire is usually connected to the earth at the distribution transformer, and in the motor drive system, the chassis of the drive and motor are connected to the earth. Due to deterioration of the motor winding insulation, a resistance path is created between the winding and the chassis of the motor. This causes an earth leakage current to flow through the chassis into the earth and back into the neutral of the transformer as shown in Figure 1.

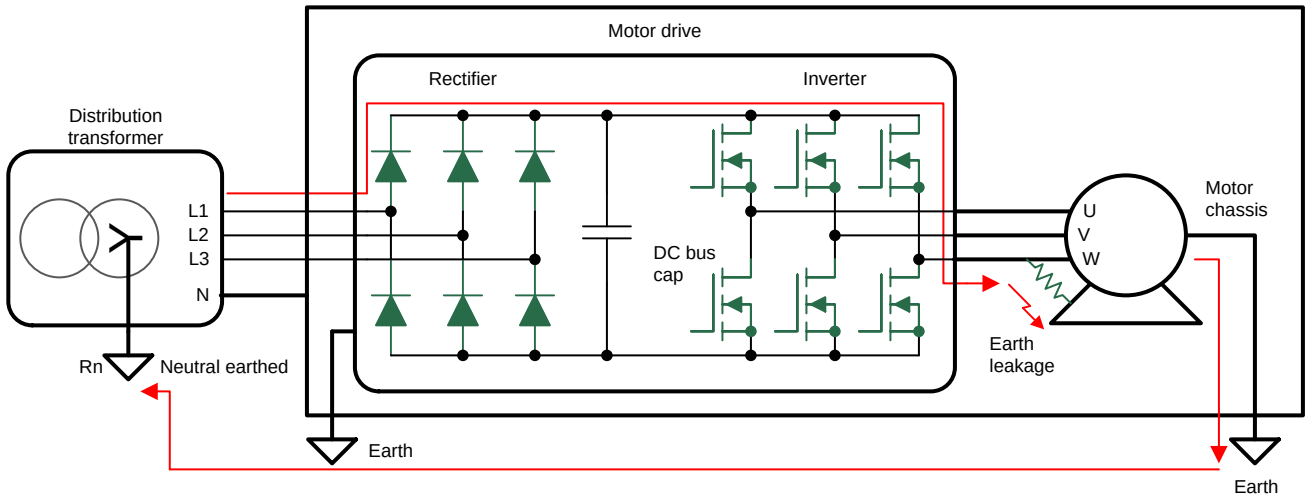

Figure 1. Ground Fault in Drive

1.2 Causes of Ground Fault

The main causes of ground fault are:

- **Faulty wiring**: During installation of a motor drive system, the phase wire may be wrongly connected to the earth terminal of the motor or there might be a cut in the winding insulation, which comes into contact with the motor chassis. This type of fault (dead short to earth) can result in a high current flow into the earth wire on starting the drive. This fault can be detected by fuses and circuit breakers in distribution systems where the transformer star point is connected to earth through low impedance. In case of high resistance earthing, where the fault current is limited, use ground fault detection devices to detect the leakage current.
- **Insulation degradation**: The insulation of a motor phase winding to chassis degrades over time due to heating and aging. Current may start leaking from the phase into the earth through the degraded insulation.
- **Moist environment**: Moisture may condense onto the motor windings during the down time. This provides a path to earth and is one of the major causes of ground fault currents. Due to this reason ground fault protection is usually provided in moist operating environments such as dirty and clean water treatment plants, wash down areas of industrial plants, pumping applications, and marine as well as mining applications.
- **Dust**: Dust may provide a high resistance path to earth. Ground fault protection is therefore usually provided in cement factories, mines, and gravel quarries.
- **Foreign object debris (FOD)**: During production, conductive metal parts may enter into the motor (for example, screws, metal pieces during metal cutting, grinding). Mechanical vibrations may also cause screws, bolts, nuts, and washers to be loosened and fall into the motor, which may cause a contact between phase winding and chassis.

1.3 Why is Ground Fault Protection Device Required?

Motor drive systems are usually protected by fuses and circuit breakers for overcurrents. The trip levels of these protection mechanisms are usually set higher than the maximum current required by the system by a certain margin. Apart from dead short between inverter output and earth, even a high resistance path to earth can cause current leakage into the earth. Earth leakage currents through high resistance paths are smaller in magnitude and cannot be detected by overcurrent protection mechanisms.

Some of the hazards of ground leakage current are electrocution arcing, which may cause fire hazards or damage to the wiring insulation due to continuous leakage of current through it. Ground currents also have an effect on the motor control algorithms if there is a current control loop involved. Ground currents are also an early indicator of insulation degradation. To avoid the possible hazards and to prevent downtime and loss due to stoppage in production, ground fault protection circuit is required.

1.4 Ground Fault Sensitivity Levels

Ground fault protection devices have different sensitivity levels. Sensitivity level means the ground fault current at which the device responds. The sensitivity is expressed as the rated difference current, denoted as IΔn. Based on this, they can be categorized into the following groups:

- High sensitivity (HS): 6 to 10 to 30 mA (for direct-contact, life injury, and protection from electrocution)
- Medium sensitivity (MS): 100 to 300 to 500 to 1000 mA (for fire protection)
- Low sensitivity (LS): 3 to 10 to 30 A (for machine and device protection)

Based on the application, protection level required and environment the devices with high, medium, or low sensitivity can be chosen.

2 System Description

A typical motor drive system powered from AC mains consists of an AC/DC converter and DC/AC inverter along with control circuit. The block diagram of the system is shown in Figure 2. The mains supply can be single phase or three phase, 110- V AC or 220-V AC depending on the drive, and the country in which the drive is to be used. The drive first converts the AC mains voltage into DC with the help of a power converter. The converter can be active PFC or may be a simple bridge rectifier depending on the drive.

For 110-V AC mains powered drives, the nominal DC bus voltage is approximately 170-V DC. The maximum DC bus voltage in this design is rated up to 275-V DC. This is to take into account variation in the mains voltage as well the increase in the DC bus voltage due to motor regeneration.

In normal operating conditions, the current flowing from the DC bus positive into the inverter and the current flowing back from the inverter into the DC bus negative are equal. This no longer holds true if earth leakage happens. The TIDA-00439 GND fault detection circuit detects this unbalanced current. The circuit is inserted between the rectifier stage and the DC bus capacitor as shown in Figure 2.

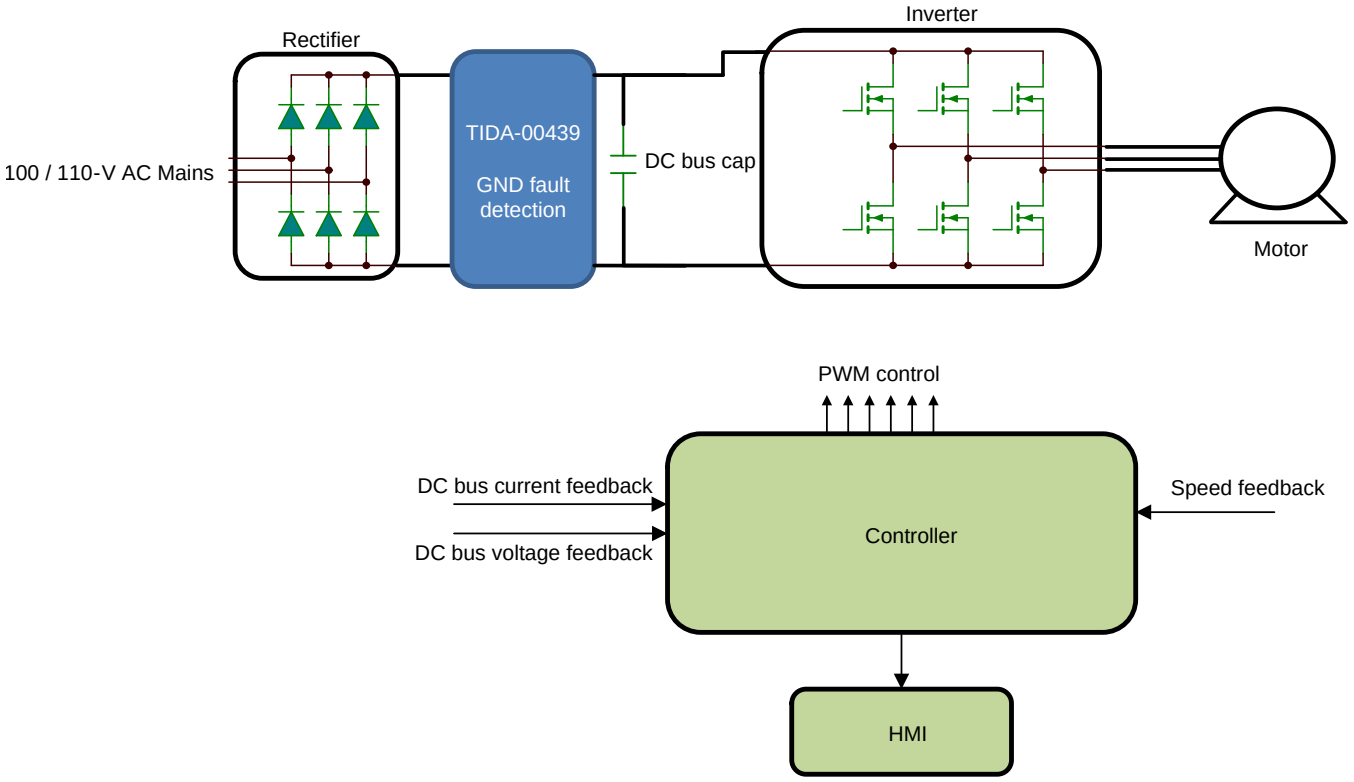

Figure 2. System Block Diagram

3 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
Drive AC input	110-V AC
DC bus voltage level maximum	275-V DC maximum
Maximum DC bus current	±20 A
Operating ambient temperature	–10°C to 55°C
Unbalanced current detection (GND fault current)	300 mA
Calibrated high-side and low-side current measurement error over temperature range	< 1.5%
Features	Low-side and high-side current sense outputs designed to be interfaced to 3.3-V inbuilt ADCs of MCUs

4 Block Diagram

The ground fault detection block shown in Figure 2 is expanded in detail in Figure 3. The main sections are the shunt resistors, the low-side current sensing circuit, the high-side current sensing circuit, and the GND fault detect comparator.

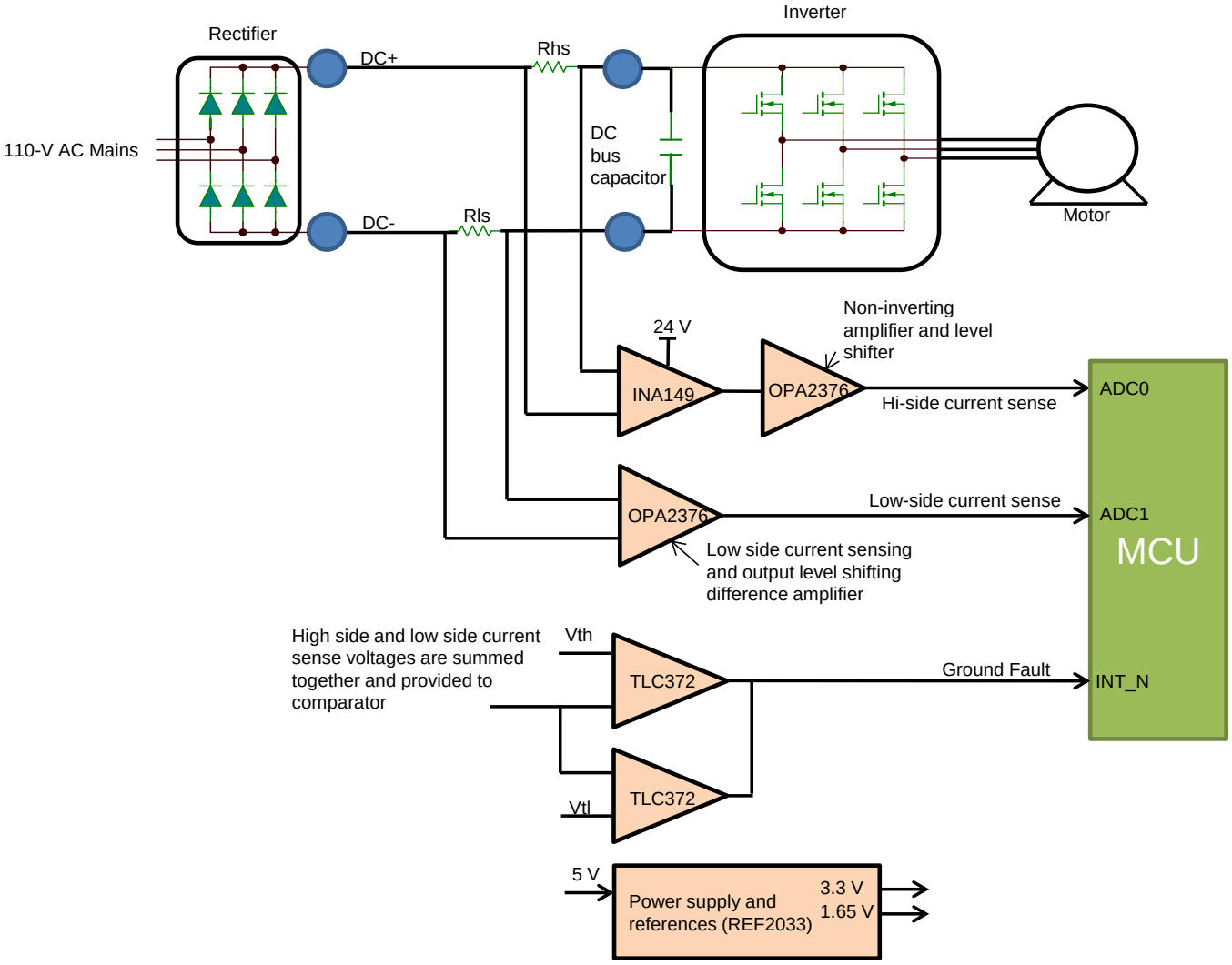

Figure 3. GND Fault Detection Circuit Block Diagram

The low-side current sensing circuit comprises of shunt resistor (Rls), the OPA2376 in difference amplifier topology with level shift of 1.65 V enabling to measure bidirectional current. The OPA2376 is powered from a 3.3-V supply making it compatible with integrated ADCs of MCU.

The high-side current sensing circuit comprises of shunt resistor (Rhs), the high common mode unity gain amplifier INA149 and OPA2376 as non-inverting amplifier with a gain of 14.7 and a 1.65-V level shift.

The circuit is powered from 24-V DC and 5-V DC, which are typically present in most of the industrial drives. The REF2033 is used to generate a 3.3-V supply and a 1.65-V reference for the circuit.

The TLC372-based window comparator is used to detect ground faults. For better accuracy, the high-side and low-side current sense voltages can be acquired by an MCU and calibrated. Then, the ground fault current can be calculated.

4.1 Highlighted Products

The TIDA-00439 reference design features the following devices, which were selected based on their specifications. The key features of the highlighted products are mentioned below.

For more information on each of these devices, see the respective product folders at www.ti.com or click on the links for the product folders on the first page of this reference design.

4.1.1 INA149

The INA149 is a precision unity-gain difference amplifier with a very high input common-mode voltage range. It is a single, monolithic device that consists of a precision op-amp and an integrated thin film resistor network. The INA149 can accurately measure small differential voltages in the presence of common-mode signals up to ±275-V DC. The INA149 inputs are protected from momentary common-mode or differential overloads of up to 500 V.

In this non-isolated current measurement application, the INA149 can replace isolation amplifiers. This ability can eliminate costly isolated input side power supplies and the associated ripple, noise and quiescent current. The excellent 0.0005% non-linearity and 500-kHz bandwidth of the INA149 are superior to those of conventional isolation amplifiers. The operating temperature range is from –40°C to 125°C.

The INA149 is chosen in the design for its high common-mode input voltage range of 275-V DC, low gain, and non-linearity errors.

4.1.2 OPA2376

The OPA2376 is a low-noise dual operational amplifier with e-trim™, offering outstanding DC precision and AC performance. The device's rail-to-rail input and output, low offset (25 µV max), low noise (7.5 nV/√Hz), quiescent current (950 µA max), and a 5.5-MHz bandwidth make this part very suitable for precision applications. The IC is specified for operation from –40°C to 125°C.

The OPA2376 was chosen for its rail-to-rail input and output voltage ranges, very low input offset voltage, low offset voltage drift with temperature, low bias currents due to e-trim and high bandwidth at a relatively low cost.

4.1.3 TLC372 – LinCMOS™ Dual Differential Comparator

The TLC372 is fabricated using LinCMOS technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Each device features an extremely high input impedance (typically greater than 10^{12}), allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The TLC372I is characterized for operation from −40°C to 85°C.

The TLC372 is chosen for the dual package, fast response time, and the open drain output so that the outputs can be logic ANDED with just a single pull-up resistor.

4.1.4 REF2033

Applications with only a positive supply voltage often require additional stable voltage in the middle of the ADC input range to bias input bipolar signals. The REF2033 provides a reference voltage for the ADC and a second highly accurate voltage that can be used to bias the input bipolar signals.

The REF2033 offers excellent temperature drift (8 ppm/°C, max) and initial accuracy (0.05%) on both the V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430 µA. In addition, the V_{REF} and V_{BIAS} outputs track each other with a precision of 6 ppm/°C (max) across the temperature range of –40°C to 85°C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete solution. Both the V_{REF} and V_{BIAS} have the same excellent specifications and can sink and source current equally well. Very long-term stability and low noise levels make these devices ideally-suited for high-precision industrial applications.

This device is chosen for its dual outputs in very small package, very low drift in output with temperature, and for its V_{REF} and V_{BIAS} tracking for higher accuracy.

5 System Design Theory

The detailed design procedure for each of the circuit sections is described below:

5.1 High-Side Current Measurement Solution

5.1.1 Design

The high-side current sense measurement circuit is designed to measure current on DC positive bus, which can go up to 275-V DC. 110-V AC powered drives have a nominal DC bus voltage of approximately 170-V DC. An extra margin of 100-V DC has to be provided to accommodate the rise in DC bus voltage during the motor regeneration mode and the variations in the mains voltage.

The INA149 suits this operating condition perfectly as it is a precision unity-gain difference amplifier with an input common mode voltage range of ±275-V DC. It has the ability to measure small differential voltages in the presence of very high common-mode voltage, which is common when measuring high-side current without isolated power supplies. The ability to measure small voltages in the range of millivolts in high CMV is because of its best in class CMRR of 100 dB enhancing overall system performance.

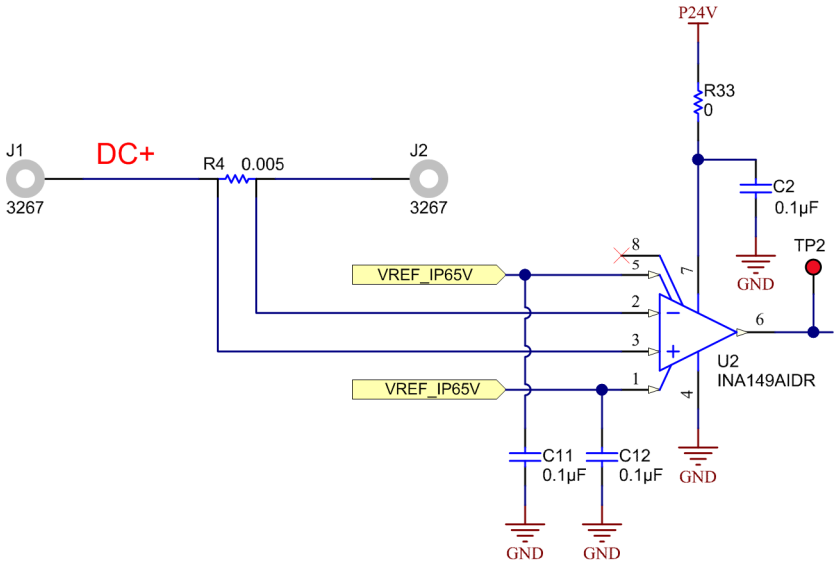

Figure 4. INA149 High-Side Current Sense Circuit

The high-side current sensing circuit is shown in Figure 4. The input common mode voltage range of INA149 is dependent on its power supply voltage. To measure current at the rated nominal DC bus voltage of 170-V DC with 100-dB CMRR, take care while selecting the supply voltage for INA149. The relationship between supply voltage and input common mode voltage range can be found out from Figure 5, which shows the internal structure of INA149. Performing a nodal analysis at the non-inverting input V_{oa_i} leads to Equation 1.

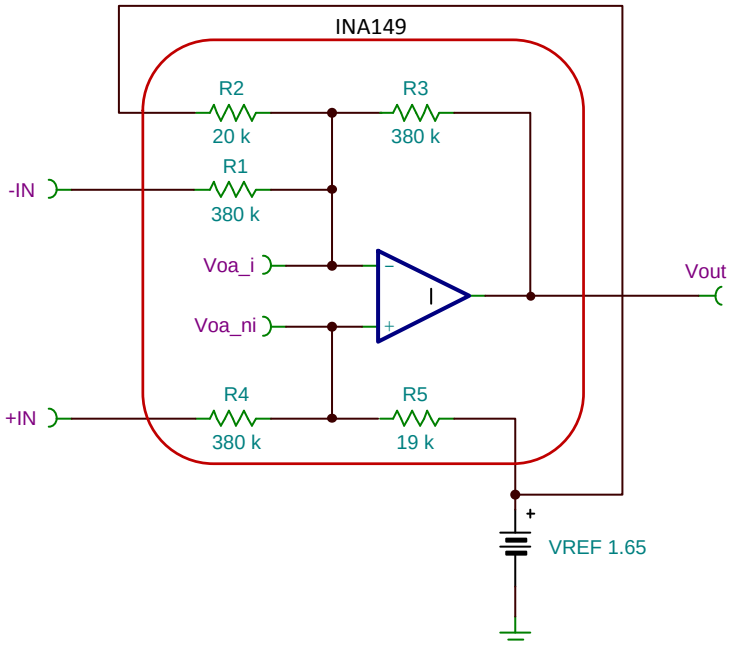

Figure 5. Internal Structure of INA149

$$V_{oa\_i} = 0.952351 \times V_{REF} + 0.047917 \times V_{CM} \quad (1)$$

The op-amp inputs must be approximately 1.5 V from either of the power supply rails V_- and V_+ to operate linearly and $V_{oa\_ni} = V_{oa\_i}$ for an op-amp with negative feedback. This condition allows the user to modify Equation 1 to estimate the common mode voltage limits:

$$V_{CM(LOW)} = \frac{(V_- + 1.5) - (0.952381 \times V_{REF})}{0.047917} \quad (2)$$

$$V_{CM(HIGH)} = \frac{(V_+ - 1.5) - (0.952381 \times V_{REF})}{0.047917} \quad (3)$$

Where $V_{CM(LOW)}$ is the lower limit for the input common mode voltage range and $V_{CM(HIGH)}$ is the upper limit for the input common mode voltage range

24-V DC is a standard DC power supply on industrial drive boards. For this power supply and reference voltage of 1.65 V, the CMV limits can be calculated from Equation 2 and Equation 3 to be $V_{CM(low)}$ = -1.49 V and $V_{CM(HIGH)}$ = 436.76 V. This is easily above the design requirement of 275-V DC. Note that the INA149 has a limit of 275-V input CMV maximum, which should not be exceeded.

RC filter (R33, C2) on the 24 V supply rail is provided for filtering in case of a noisy 24-V supply. The cut off frequency for the filter can be chosen based on noise spectrum.

The maximum DC link current specification for the design is ±20 Ap. The current shunt (R4) inserted on DC positive bus is chosen such that ±20 A generates a voltage of ±100 mV across it.

$$R_{HS\_sh} = \frac{V_{HS\_sh\_max}}{I_{DClink\_max}} = \frac{100\ m}{20} = 5\ m\Omega \quad (4)$$

Where R_{HS_sh} is the high side shunt resistance,
$V_{HS\_sh\_max}$ is the maximum voltage drop across the shunt,
I_{DClink_max} is the maximum current through the shunt

The maximum power dissipated in the shunt is calculated in Equation 5:

$$P_{dissipated\_HS\_sh\_max} = I_{DClink\_max}^{2} \times R_{HS\_sh} = 20^{2} \times 5\ m = 2\ W \quad (5)$$

$P_{dissipated\_HS\_sh\_max}$ is the maximum power dissipated across the shunt resistor.

A 5-mΩ shunt resistor is selected with a wattage rating of 3 W.

The transfer function of INA149 is given in Equation 6:

$$V_{out} = \left(V_{+IN}\right) - \left(V_{-IN}\right) + \left(20 \times REF_{A}\right) - \left(19 \times REF_{B}\right) \quad (6)$$

Where $V_{+IN} - V_{-IN}$ is the voltage across the shunt resistor, V_{HS_sh}
And $REF_A = REF_B = V_{REF}$

Therefore, Equation 6 can be simplified as:

$$V_{out} = V_{HS\_sh} + V_{REF} \quad (7)$$

$V_{out} = V_{HS\_sh} + V_{REF}$

$$V_{out} = \left(I_{HS\_sh} \times R_{HS\_sh}\right) + V_{REF} \quad (8)$$

Where I_{HS_sh} is the current through the shunt resistor
R_{HS_sh} is 5 mΩ,
V_{REF} = 1.65 V.

Using these values in Equation 8, it can be simplified to

$$V_{out} = \left(I_{HS\_sh} \times 5\ m\right) + 1.65 \quad (9)$$

For DC link currents changing from 20 A to –20 A, the output of INA149 changes from 1.75 V to 1.55 V, giving an output swing of 0.2 V. This output voltage swing can be increased by increasing the value of the high-side shunt resistor, but the tradeoff for this is increased power dissipation across the shunt resistor.

The output offset voltage of INA149 is dependant on the CMRR and the input common-mode voltage. This offset voltage can be calculated with Equation 10:

$$\Delta V_{os} = \Delta V_{CMV} \times 10^{\frac{-CMRR(dB)}{20}} \quad (10)$$

From Figure 6, the minimum CMRR of INA149 is taken as 100 dB. With 170-V DC link voltage as the common mode voltage, the output offset of INA149 is calculated as

$$\Delta V_{os} = 170 \times 10^{\frac{-100}{20}} = 1.7 \text{ mV} \quad (11)$$

This offset error can be calibrated after taking the initial measurement and comparing with the ideal value with the help of software inside the MCU.

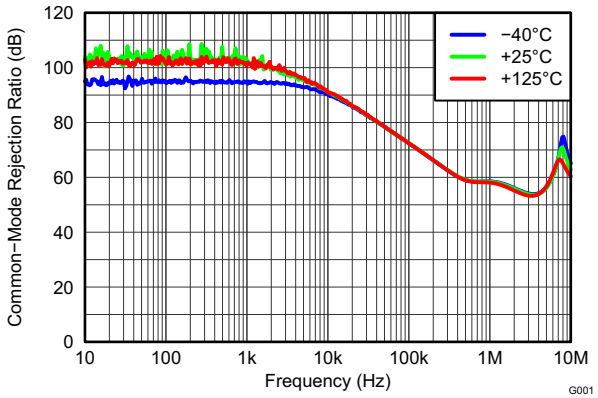

Figure 6. CMRR versus Frequency at Various Temperatures

In order to use the complete 3.3-V dynamic input range of the inbuilt ADC of MCUs, the 0.2-V output swing of INA149 is amplified to approximately 0 to 3.3 V. This is accomplished by the non-inverting amplifier stage shown in Figure 7. The OPA2376 has been chosen for its high precision, very low input offset voltage, low noise, low quiescent power, wide bandwidth and single supply operation. It is very important that the amplifier has a very low input offset voltage because of the high gain of the amplifier stage; any input offset voltage is amplified along with the input signal.

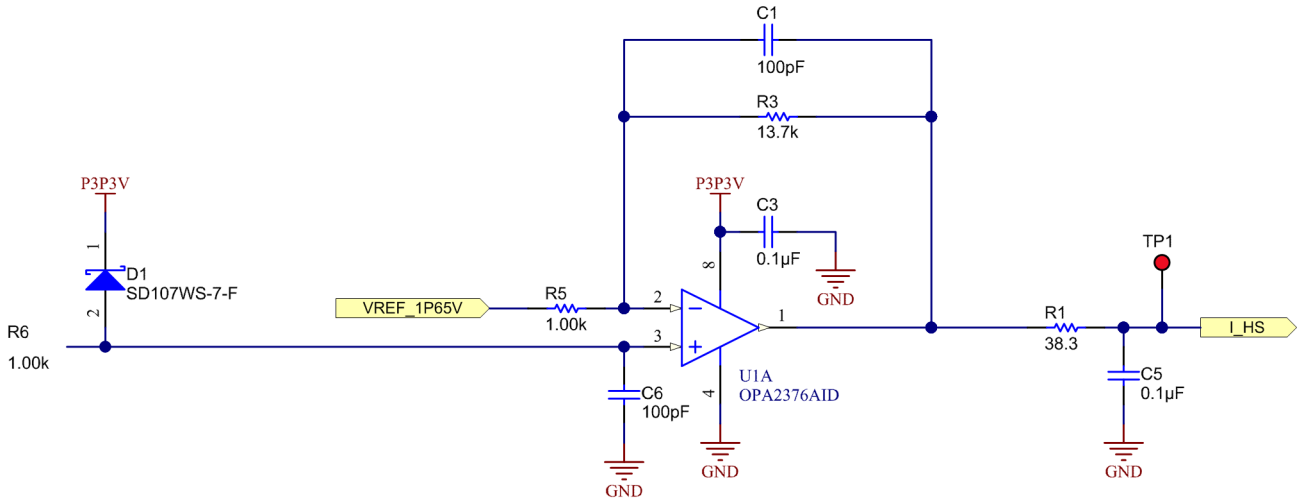

Figure 7. High-Side Current Sense Gain Stage

The input stage of this amplifier has to be protected, as the INA149 output of the preceding stage can saturate to 24 V in case of any faults in the circuit. A schottky diode D1 is connected to 3.3 V for protection along with R6 to limit the current through D1 during forward bias. R6 should be selected such that it is large enough to limit the current through D1 in case it gets forward biased and should not be too large so that the input bias current of the op-amp and the reverse leakage current of D1 create a large voltage drop across it. Any voltage drop across the resistor R6 adds additional input offset to the op-amp.

The transfer function of the non-inverting amplifier stage is given by Equation 12:

$$V_{out} = V_{in}\left(1+\frac{R3}{R5}\right) - V_{REF}\left(\frac{R3}{R5}\right) \quad (12)$$

V_{REF} is 1.65 V, 20 A through a 5-mΩ current sense resistor creates a voltage drop of 100 mV. This has to be amplified to near 3.3 V. Therefore, a gain of 14.7 V/V is chosen with R3 = 13.7 KΩ and R5 = 1 KΩ. Select 0.1% resistors for good accuracy. Equation 12 simplifies to

$$V_{out} = 14.7\ V_{in} - 22.605 \quad (13)$$

When the output of the INA149 swings from 1.55 to 1.75 V, the output of the gain section swings from 0.18 to 3.12 V, which corresponds to a –20 to 20-A change in the DC link current. The OPA2376 output voltage swing is limited up to 20 mV from the rails and 40 mV over temperature. Due to this reason, the output voltage should be limited to 50 mV from the rails.

5.1.2 Simulation Results Using TINA-TI

The design is simulated in TINA-TI to verify the functionality. All TINA-TI models can be found on the respective device product folders. The current through the shunt resistor R4 in Figure 8 is varied from –20 A to 20 A. This is done by keeping V_DC_BUS constant at 170 V and varying VG2 from 0 to 340 V. By doing this, the common mode to INA149 can be maintained constant at 170 V and the current through R4 can be varied from –20 A to 20 A if RL is selected to be 8.5 Ω. The output of INA149 and OPA2376 are monitored.

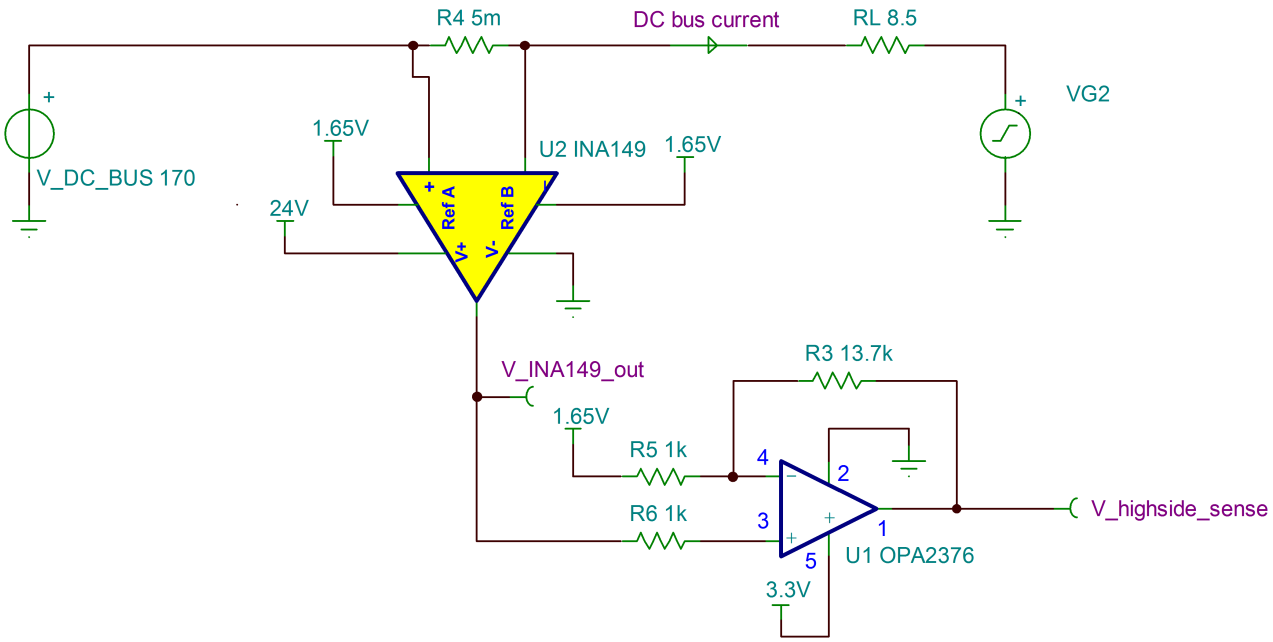

Figure 8. INA149 High-Side Current Sensing Simulation Model

The DC bus current is varied from –20 A to 20 A linearly from 5 ms to 15 ms. The variation of INA149 and OPA2376 outputs is shown in Figure 9.

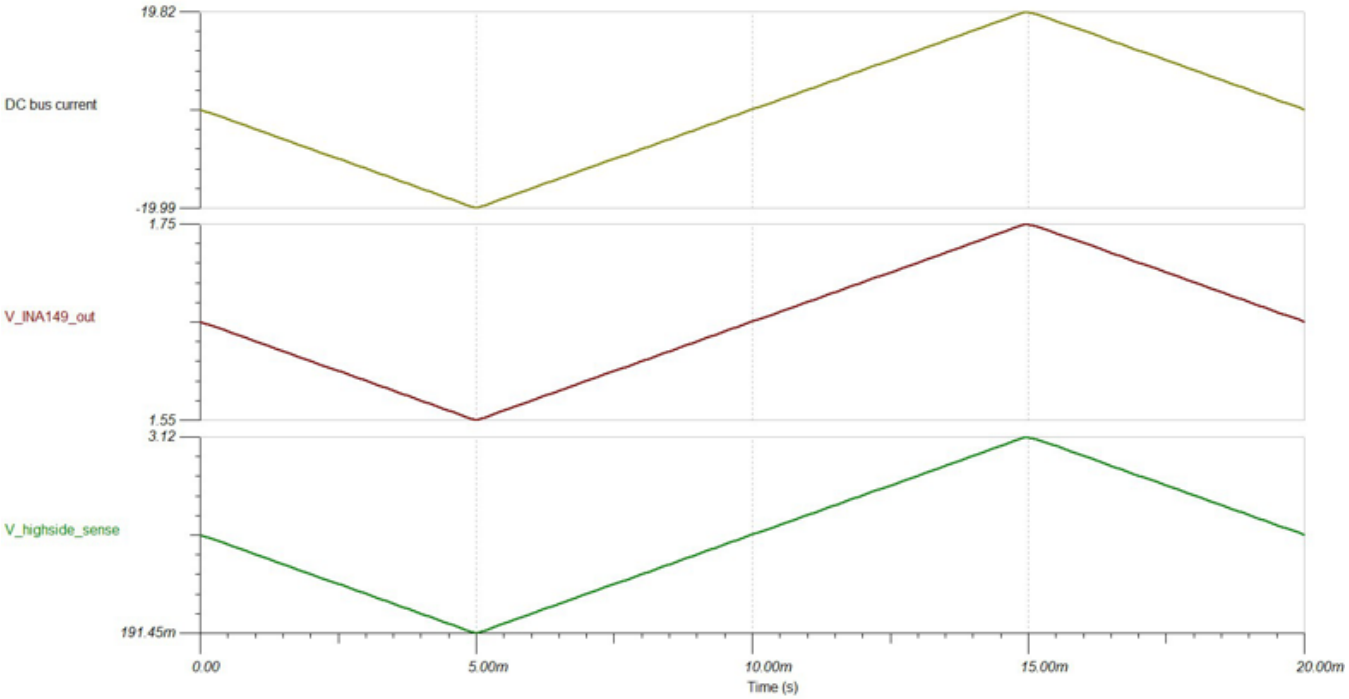

Figure 9. Simulation Results for INA149 High-Side Current Sense

5.2 Low-Side Current Measurement Solution

5.2.1 Design

The low-side current sensing circuit is shown in Figure 10. The difference amplifier topology is used for measuring the voltage drop across the low-side shunt resistor R14.

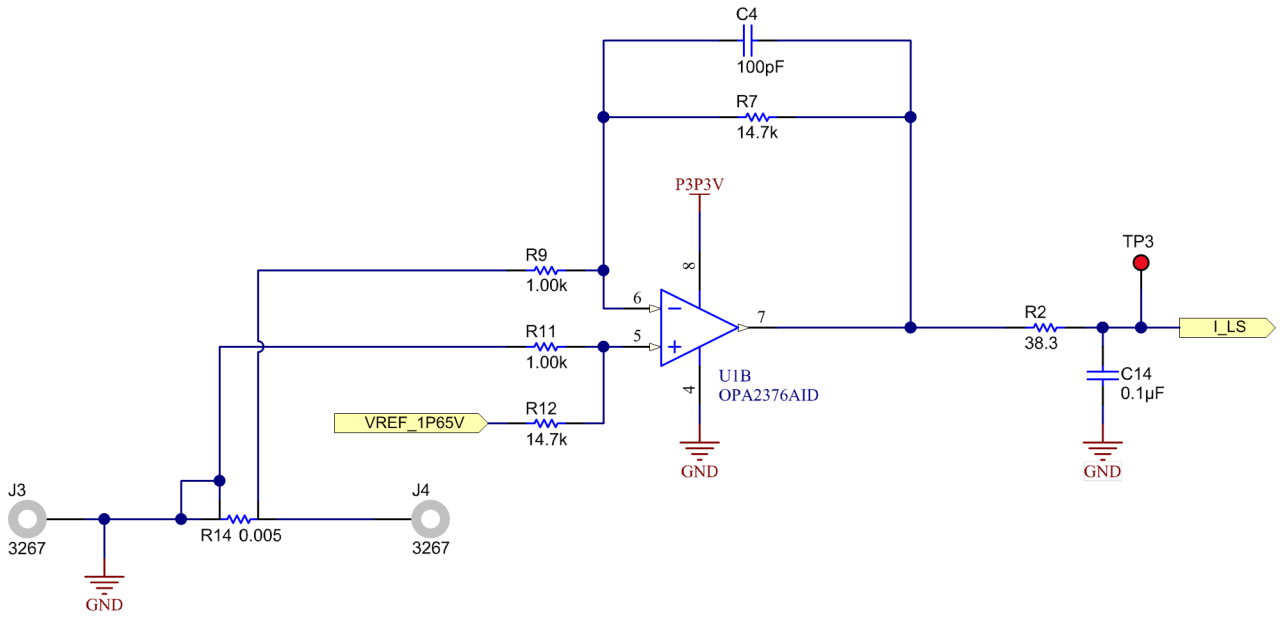

Figure 10. Low-Side Current Measurement Circuit

The selection of the low-side current sense resistor R14 is same as that of high-side current sense resistor selection and is 5 mΩ with 3 W.

The transfer function of the difference amplifier is given by Equation 14. Refer to Figure 10 for the reference designators.

$$V_{out} = \left(\frac{R_{11}(R_9 + R_7)}{R_9(R_{11} + R_{12})} \right) V_{ref} + \left(\frac{R_{12}(R_9 + R_7)}{(R_{11} + R_{12})R_9} \right) V_{in\_p} - \left(\frac{R_7}{R_9} \right) V_{in\_n} \quad (14)$$

If V_{REF} is 1.65 V, R11 = R9, and R12 = R7, Equation 14 becomes

$$V_{out} = V_{REF} + \left(\frac{R_7}{R_9} \right) V_{in\_p} - \left(\frac{R_7}{R_9} \right) V_{in\_n} \quad (15)$$

Where V_{in_p} and V_{in_n} are the non-inverting input and inverting inputs of difference amplifier respectively. $V_{in\_p} – V_{in\_n} = VR14$ is the voltage drop across the low-side shunt resistor R14. V_{in_p} is connected to GND, and V_{in_n} is connected across R14 with respect to GND to get inverted output. The reason for inverted output is explained in Section 5.3. Equation 15 becomes

$$V_{out} = V_{REF} - V_{R14} \left(\frac{R_7}{R_9} \right) \quad (16)$$

A ±20-A current through the shunt resistor R14 creates a voltage drop of ±100 mV across it. This range has to be converted into a 0 to 3.3-V dynamic input range of the ADC. 0 A is level shifted to 1.65 V with the help of V_{REF} and a gain of 14.7 V/V is selected to map ±100 mV to ±1.47 V around 1.65 V. Equation 16 becomes

$$V_{out} = 1.65 - \left(14.7 \times I_{DClink} \times R_{14} \right) \quad (17)$$

Where I_{DClink} is the DC bus current. When it changes from –20 A to 20 A the output changes from 3.12 V to 180 mV. The OPA2376 output voltage swing is limited up to 20 mV from the rails and 40 mV over temperature. Due to this reason, the output voltage should be limited to 50 mV from the rails.

0.1% resistors should be selected for R7, R9, R11, and R12 for good accuracy. If still a higher accuracy is required, then expensive ratio tracking resistors can be used. The advantage of the discrete counterpart is that the gain can be adjusted to exactly the value required.

5.2.2 Simulation Results Using TINA-TI

The DC bus current is simulated with the help of a current source I_DC_BUS. Current through the shunt resistor R14 in Figure 11 is varied linearly and the output V_lowside_sense is monitored.

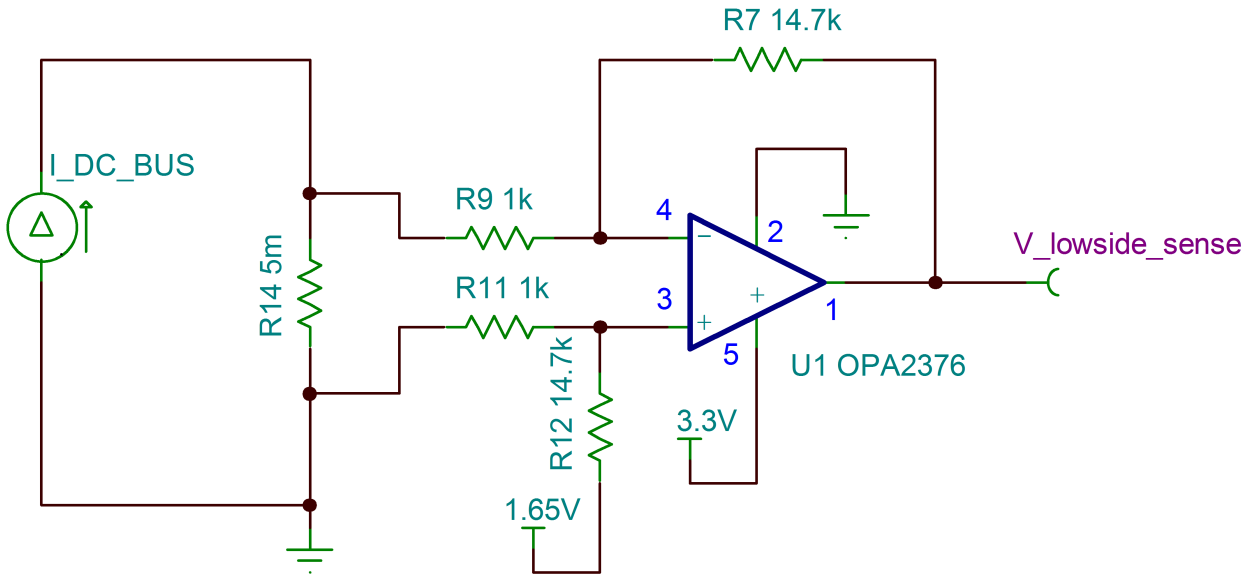

Figure 11. Low-Side Current Sense Amplifier

The DC bus current is varied from 20 A to –20 A linearly from 5 ms to 15 ms. The variation of the low-side sense voltage is shown in Figure 12.

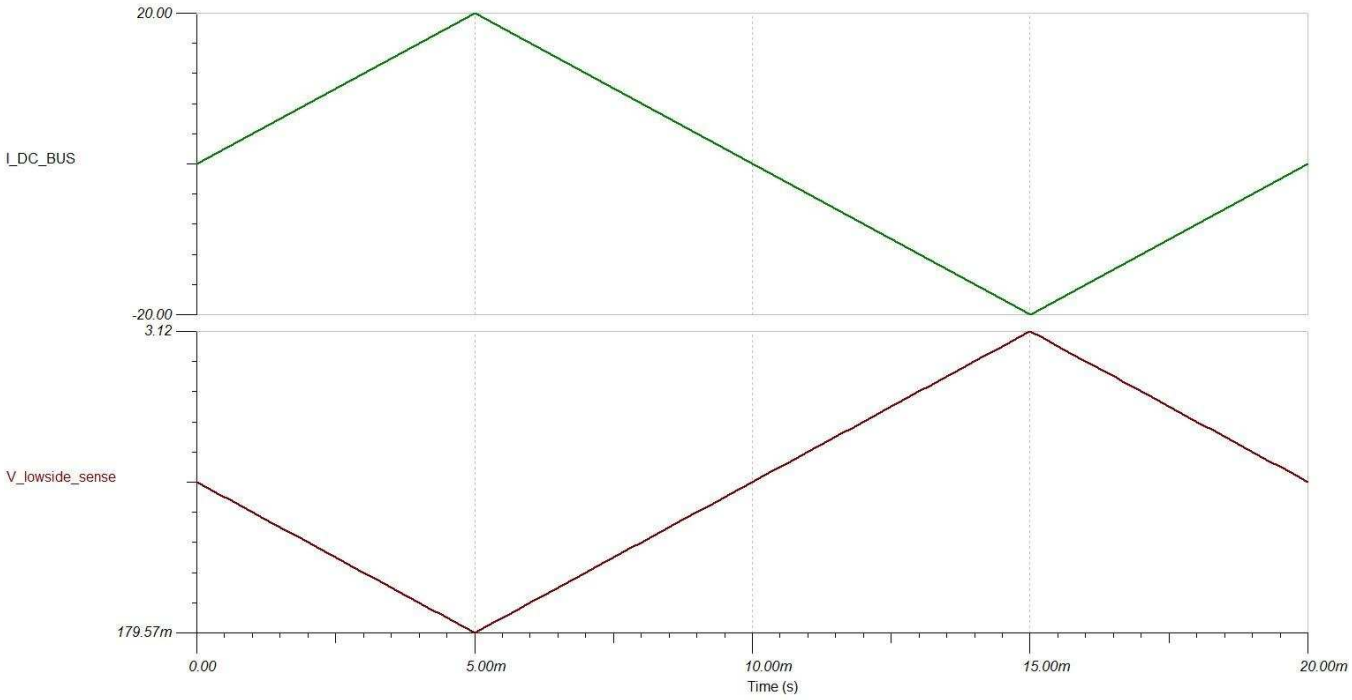

Figure 12. Low-Side Current Sense Amplifier Simulation Results

5.3 Ground Fault Detect Comparator

Comparator circuit used to detect the ground fault is shown in Figure 13. The comparator triggers when the difference between the high-side current and the low-side current is more the set threshold (±300 mA in this case). Window comparators are used for this functionality with the upper comparator detecting when the high-side current exceeds the low-side current by 300 mA and the lower comparator detects if the high-side current is less than the low-side current by 300 mA. The TLC372 is chosen for this design, which contains dual comparators in a single package, fast response time, and an open drain output, which helps to logic AND the outputs of the two comparators with the help of a single pull-up resistor R20.

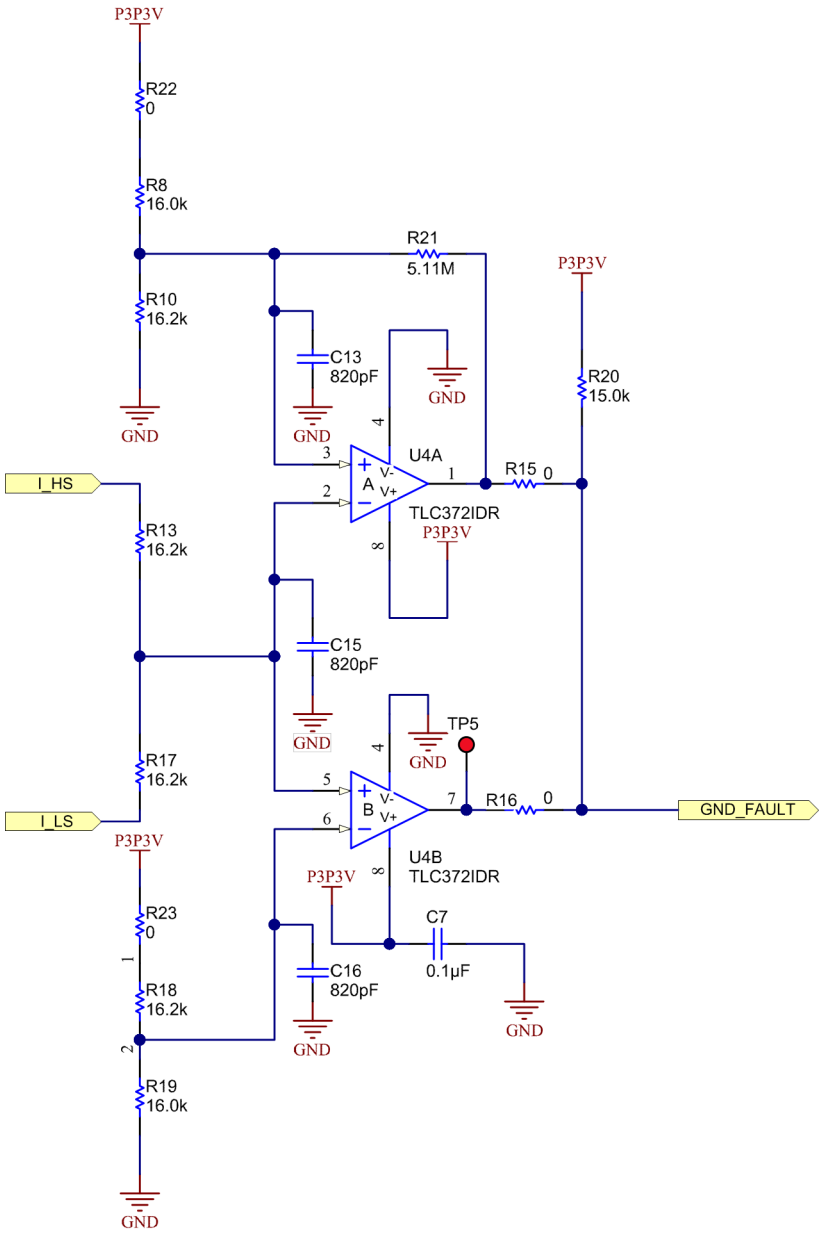

Figure 13. GND Fault Comparator Circuit

The average of the high-side and low-side current sense voltages (Vmid) is compared with the upper threshold voltage and lower threshold voltage. The threshold voltage is selected using Equation 18 to Equation 21:

$$\text{Threshold voltage} = \frac{\text{Ground fault current to be detected} \times \text{Shunt resistor} \times \text{Gain}}{2} \quad (18)$$

For the 300-mA ground fault limit, Equation 18 becomes

$$\text{Threshold voltage} = \frac{300\ \text{mA} \times 5\ \text{m}\Omega \times 14.7}{2} = 0.011025\ \text{V} \quad (19)$$

$$\text{Upper threshold} = \text{Vref} + \text{Threshold voltage} = 1.65 + 0.011025 = 1.661\ \text{V} \quad (20)$$

$$\text{Lower threshold} = \text{Vref} - \text{Threshold voltage} = 1.65 + 0.011025 = 1.6389\ \text{V} \quad (21)$$

Resistor divider networks are used to generate the upper and lower threshold voltages from a 3.3-V supply. R8 and R10 are used for the upper threshold and R18 and R19 are used for the lower threshold. R22 and R23 are used to finely calibrate the threshold voltage manually. R21 is the hysteresis setting resistor. The transfer functions of the high-side current sense circuit and the low-side current sense circuit have the same slope but different signs. This is done so that the average of both remain the same for any value of current flowing through them in the normal operating condition as shown in Equation 25. Ideally, the average of the high-side and low-side current sense outputs should be exactly 1.65 V but due to offset and gain errors in both the signal paths there will be deviations from this. The threshold resistor values have to be calibrated during the board testing. The comparator output provides indication of the earth fault, which can be connected to the interrupt of the microcontroller. On interrupt, the MCU can acquire both the high-side and low-side current sense voltages, calibrate the sensed values and estimate the accurate value of ground fault current.

The upper threshold voltage can be calculated by Equation 22:

$$V_{uth} = 3.3 \times \left(\frac{R_{10}}{R_{10} + R_{18}} \right) = 3.3 \times \left(\frac{16.2\ \text{k}}{16\ \text{k} + 16.2\ \text{k}} \right) = 1.6602\ \text{V} \quad (22)$$

The lower threshold voltage can be calculated by Equation 23:

$$V_{uth} = 3.3 \times \left(\frac{R_{19}}{R_{19} + R_{18}} \right) = 3.3 \times \left(\frac{16\ \text{k}}{16\ \text{k} + 16.2\ \text{k}} \right) = 1.6398\ \text{V} \quad (23)$$

V_{mid} is the voltage at the junction of R13 and R17,

$$V_{mid} = \frac{(I\_HS \times R_{17}) + (I\_LS \times R_{13})}{(R_{13} + R_{17})} \quad (24)$$

If R13 = R17, then V_{mid} becomes the average of I_HS and I_LS which is ideally 1.65 V,

$$V_{mid} = \frac{(I\_HS) + (I\_LS)}{2} \quad (25)$$

The TLC372 has an open drain output. In the normal operating condition, Vmid is between the upper and lower thresholds. In this case, both the comparators are in the open drain output condition, the outputs are tied together and pulled up to 3.3 V through R20. If the Vmid signal goes either above the upper threshold or below the lower threshold, the output of the respective comparator is pulled down to zero. Select R20 to be large enough to limit the power dissipation during this state.

5.4 Power Supply and Reference Section

In this application, a bipolar signal (bidirectional DC link current) has to be sensed using a unipolar power supply, to achieve this it is required to level shift the output of the signal conditioning stages to midpoint of the power supply rail. A voltage reference is required to bias the signal conditioning stage outputs to the middle of the ADC dynamic range. The REF2033 IC provides both the 3.3-V supply to the op-amps as well as the 1.65-V reference voltage for biasing the signal to the middle of the ADC range. Both the outputs of the REF2033 IC can sink/source 20 mA. Also, there is excellent tracking between the 3.3-V and 1.65-V supplies and both the supplies are available in a single extremely small SOT23-5 package thus reducing BOM count and board size.

The power supply section is shown in Figure 14.

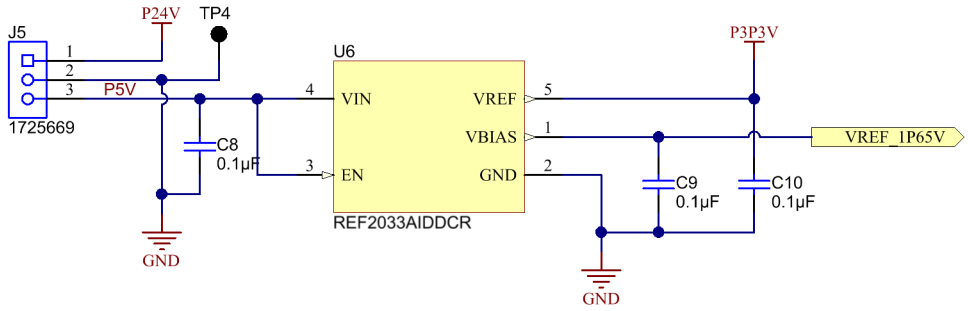

Figure 14. Power Supply and Reference Circuit

The IC is supplied with a 5-V power supply. The outputs are 3.3 V and 1.65 V. Place 0.1-uF noise decoupling capacitors close to the IC pins for clean power input and output rails.

The load on both the 3.3-V supply as well as the 1.65-V bias source is shown in Table 2.

Table 2. Power Supply Load Calculation for TIDA-00439

SI NO	NAME OF IC OR COMPONENT	POWER SUPPLY OR REFERENCE USED (V)	MAX CURRENT TAKEN BY THE IC (mA)	MAXIMUM POWER CONSUMPTION (mW)	MAXIMUM TOTAL OUTPUT CURRENT (mA)
1	OPA2376	3.3	2.55	8.415	3.375
2	TLC372	3.3	0.4	1.32	
3	Comparator output pullup resistor R20	3.3	0.22	0.726	
4	Comparator input threshold reference circuit	3.3	0.205	0.6765	
5	OPA2376	1.65	1.747	2.88	1.747
6	INA149	24	1	24	1

The maximum load on the 3.3-V supply is 3.375 mA and the total load on the 1.65-V supply is 1.747 mA. REF2033 IC with sink/source capability of 20 mA is used.

6 Test Results

The following tests are carried out on the design:

- High-side and low-side current measurement error
- Measurement error across different DC link voltages
- Measurement error across operating temperature from –10°C to 55°C
- Detection of ground fault scenario and response time
- Testing on C2000 motor control kit for ground fault operation

6.1 High-Side and Low-Side Current Measurement Error

The test setup for measuring error of the high-side and low-side current measurement circuit is shown in Figure 15. A variable load is connected to a high-voltage DC power supply through the TIDA-00439 board. The board is powered up with 5 V and 24 V supplied by an external DC power supply. The high-voltage DC power supply (simulates DC bus voltage in actual drive) is set to 170-V DC. The load is varied from –5 A to 5 A with the help of the variable electronic load and the high-side and low-side current measurement outputs are recorded.

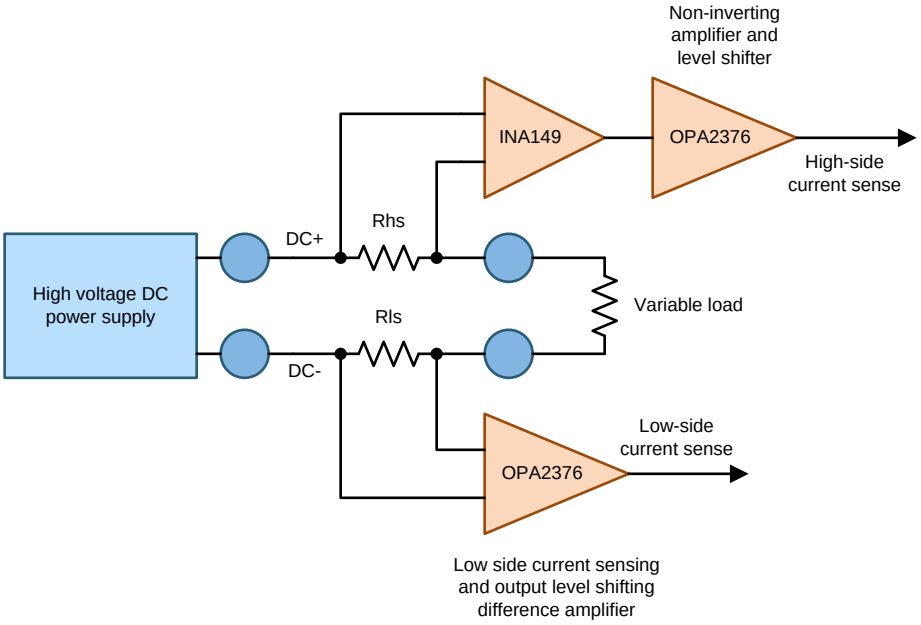

Figure 15. Test Setup for TIDA-00439 High-Side and Low-Side Current Measurement Error

Figure 16 shows the graph of variation of current measurement error of the signal conditioning circuit versus the DC bus current, and Figure 17 shows the calibrated result. Table 3 shows the corresponding readings.

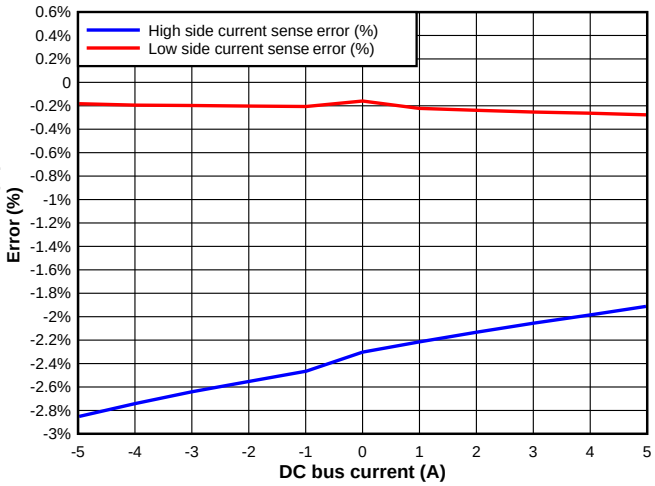

Figure 16. Current Sense Error versus DC Bus Current (Non-Calibrated)

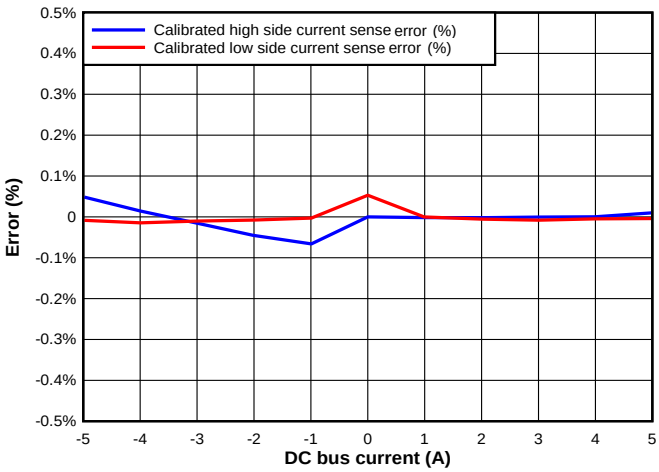

Figure 17. Current Sense Error Versus DC Bus Current (Calibrated)

Table 3. Current Sense Output and Error versus DC Bus Current

DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE (V)	CALIBRATED HIGH-SIDE CURRENT SENSE VOLTAGE (V)	HIGH-SIDE CURRENT SENSE ERROR (%)	CALIBRATED HIGH-SIDE CURRENT SENSE ERROR (%)	LOW-SIDE CURRENT SENSE VOLTAGE (V)	CALIBRATED LOW-SIDE CURRENT SENSE VOLTAGE (V)	LOW-SIDE CURRENT SENSE ERROR (%)	CALIBRATED LOW-SIDE CURRENT SENSE ERROR (%)
–5.0119	1.2453	1.2825	–2.85	0.05	2.0172	2.0207	–0.18	–0.01
–3.9922	1.3195	1.3569	–2.74	0.01	1.9417	1.9452	–0.19	–0.01
–3.0036	1.3916	1.4291	–2.64	–0.02	1.8686	1.8721	–0.20	–0.01
–2.0131	1.4638	1.5015	–2.55	–0.05	1.7953	1.7988	–0.20	–0.01
–0.9913	1.5384	1.5762	–2.46	–0.07	1.7197	1.7232	–0.21	0.00
0.0003	1.6121	1.6501	–2.30	0.00	1.6473	1.6508	–0.16	0.05
0.9909	1.6847	1.7228	–2.22	0.00	1.5731	1.5766	–0.22	0.00
2.013	1.7597	1.798	–2.13	0.00	1.4973	1.5008	–0.24	–0.01
3.003	1.8324	1.8708	–2.06	0.00	1.4239	1.4274	–0.25	–0.01
3.9925	1.905	1.9436	–1.99	0.00	1.3507	1.3542	–0.26	0.00
5.0125	1.98	2.0187	–1.91	0.01	1.2752	1.2787	–0.28	0.00

6.2 High-Side Current Measurement Error Across Different DC Bus Voltages

The variation of high-side current measurement error with DC bus voltage is shown in Figure 18 and the test results tabulated in Table 4.

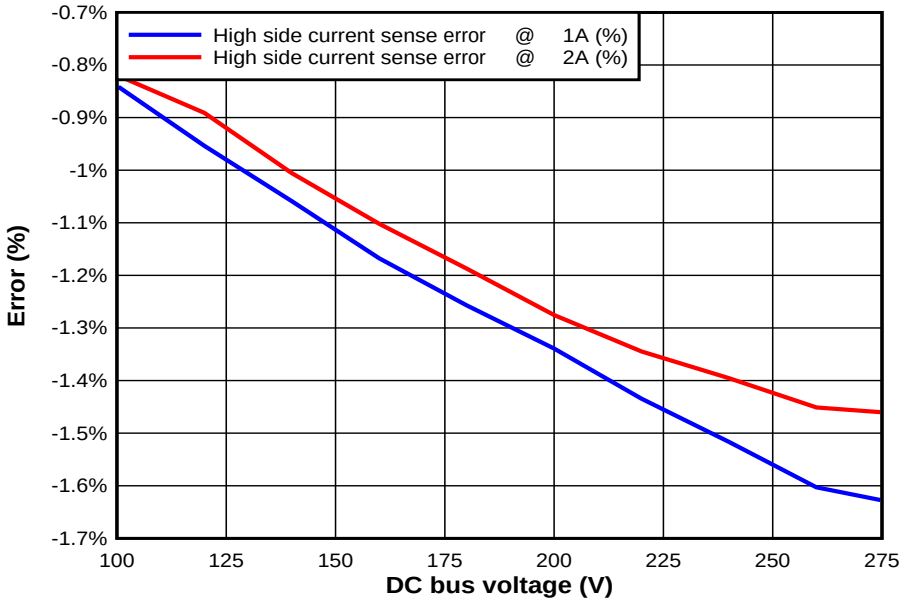

Figure 18. High-Side Current Measurement Error versus DC Bus Voltage (Non-Calibrated)

Table 4. High-Side Current Sense Voltage and Measurement Error versus DC Bus Voltage

DC BUS VOLTAGE (V)	HIGH-SIDE CURRENT SENSE VOLTAGE @ 1 A (V)	HIGH-SIDE CURRENT SENSE ERROR @ 1 A (%)	HIGH-SIDE CURRENT SENSE VOLTAGE @ 2 A (V)	HIGH-SIDE CURRENT SENSE ERROR @ 2 A (%)
100	1.7089	–0.84	1.782	–0.82
120	1.7068	–0.95	1.7802	–0.89
140	1.7049	–1.06	1.7782	–1.01
160	1.7031	–1.17	1.7765	–1.10
180	1.7015	–1.26	1.7751	–1.19
200	1.7001	–1.34	1.7735	–1.28
220	1.6985	–1.43	1.7724	–1.34
240	1.6971	–1.52	1.7713	–1.40
260	1.6957	–1.60	1.7702	–1.45
275	1.6953	–1.63	1.7698	–1.46

The reduction in percentage accuracy from 1 A to 2 A is because the offset is now a smaller part of the larger output value at 2 A compared to 1 A.

6.3 Measurement Error versus Temperature

The variation of the signal conditioning circuit output over temperature is found in this test. The board is kept inside a temperature chamber and tested at –10°C, 25°C, and 55°C. The variation of high-side measurement error is shown in Figure 19 and results in Table 5. The variation of low-side measurement error is shown in Figure 20 and results in Table 6.

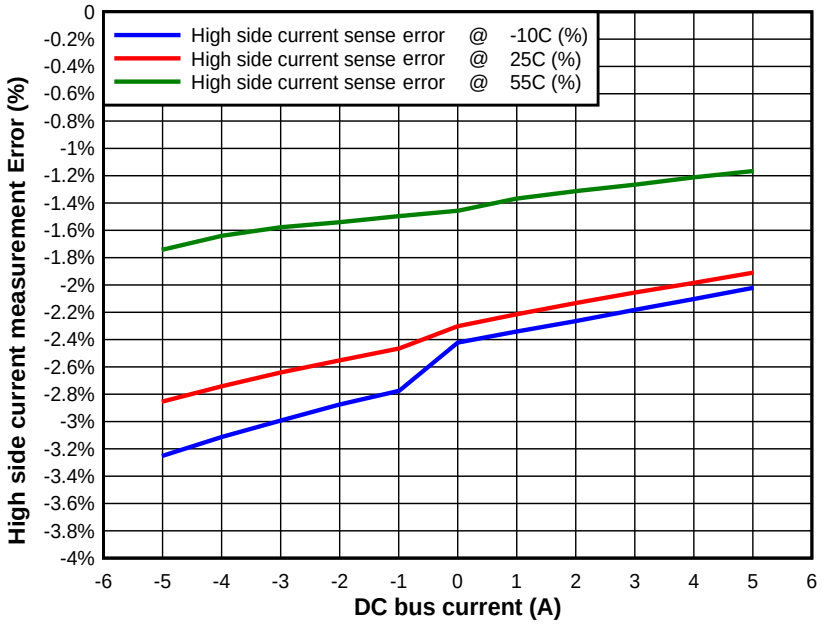

Figure 19. High-Side Current Measurement Error versus Current at –10°C, 25°C, and 55°C (Non-Calibrated)

Table 5. High-Side Current Sense Voltage and Measurement Error versus DC Bus Current at –10°C, 25°C, and 55°C

–10°C			25°C			55°C		
DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE (V)	HIGH-SIDE CURRENT SENSE ERROR (%)	DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE (V)	HIGH-SIDE CURRENT SENSE ERROR (%)	DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE (V)	HIGH-SIDE CURRENT SENSE ERROR (%)
–5.0124	1.2399	–3.25	–5.0119	1.2453	–2.85	–5.016	1.2593	–1.74
–3.9929	1.3143	–3.11	–3.9922	1.3195	–2.74	–3.9933	1.3345	–1.64
–3.0043	1.3864	–2.99	–3.0036	1.3916	–2.64	–3.0034	1.4069	–1.58
–2.0135	1.4588	–2.88	–2.0131	1.4638	–2.55	–2.0126	1.4791	–1.54
–0.991	1.5334	–2.77	–0.9913	1.5384	–2.46	–0.9906	1.5537	–1.50
0.0008	1.6101	–2.42	0.0003	1.6121	–2.30	0.008	1.6261	–1.46
0.9911	1.6825	–2.34	0.9909	1.6847	–2.22	0.9911	1.6993	–1.37
2.0136	1.7573	–2.26	2.013	1.7597	–2.13	2.0135	1.7744	–1.31
3.0044	1.83	–2.18	3.003	1.8324	–2.06	3.0042	1.8471	–1.27
3.993	1.9026	–2.10	3.9925	1.905	–1.99	3.9931	1.9197	–1.21
5.012	1.9776	–2.02	5.0125	1.98	–1.91	5.0127	1.9947	–1.17

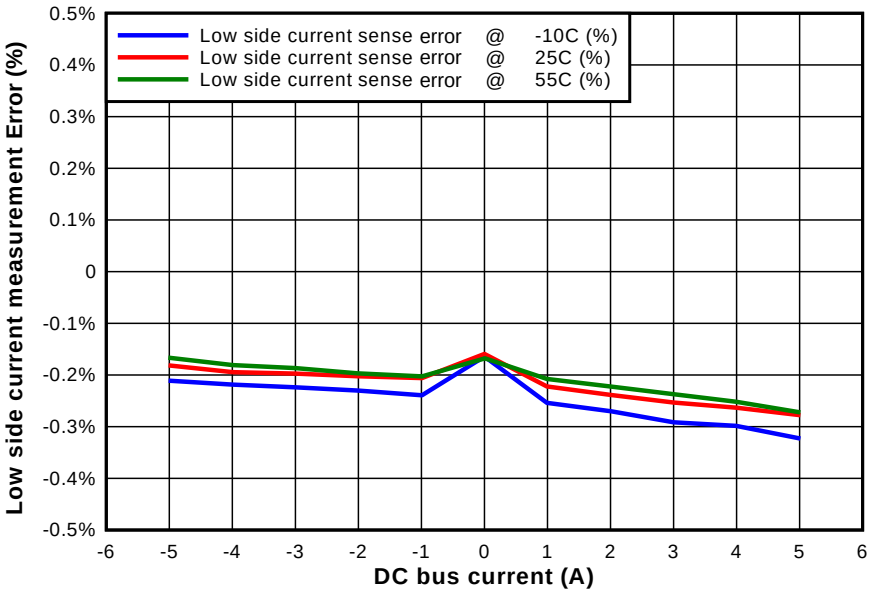

Figure 20. Low-Side Measurement Error versus Current at –10°C, 25°C, and 55°C (Non-Calibrated)

Table 6. Low-Side Current Sense Voltage and Measurement Error versus DC Current at –10°C, 25°C, and 55°C

–10°C			25°C			55°C		
DC BUS CURRENT (A)	LOW-SIDE CURRENT SENSE VOLTAGE (V)	LOW-SIDE CURRENT SENSE ERROR (%)	DC BUS CURRENT (A)	LOW-SIDE CURRENT SENSE VOLTAGE (V)	LOW-SIDE CURRENT SENSE ERROR (%)	DC BUS CURRENT (A)	LOW-SIDE CURRENT SENSE VOLTAGE (V)	LOW-SIDE CURRENT SENSE ERROR (%)
–5.0124	2.0165	–0.21	–5.0119	2.0172	–0.18	–5.016	2.0179	–0.17
–3.9929	1.9411	–0.22	–3.9922	1.9417	–0.19	–3.9933	1.9421	–0.18
–3.0043	1.868	–0.22	–3.0036	1.8686	–0.20	–3.0034	1.8688	–0.19
–2.0135	1.7948	–0.23	–2.0131	1.7953	–0.20	–2.0126	1.7954	–0.20
–0.991	1.7192	–0.24	–0.9913	1.7197	–0.21	–0.9906	1.7198	–0.20
0.0008	1.6472	–0.16	0.0003	1.6473	–0.16	0.008	1.6471	–0.17
0.9911	1.5726	–0.25	0.9909	1.5731	–0.22	0.9911	1.5733	–0.21
2.0136	1.4969	–0.27	2.013	1.4973	–0.24	2.0135	1.4975	–0.22
3.0044	1.4235	–0.29	3.003	1.4239	–0.25	3.0042	1.4241	–0.24
3.993	1.3504	–0.30	3.9925	1.3507	–0.26	3.9931	1.3509	–0.25
5.012	1.2749	–0.32	5.0125	1.2752	–0.28	5.0127	1.2754	–0.27

6.4 Detection of GND Fault Scenario and Response Time

This section shows the detection of the GND fault scenario. The GND fault is simulated using the setup shown in Figure 21. A constant electrical load is connected on the output of the TIDA-00439. One side of a variable electronic load is connected to the constant load and the other side is connected to DC– so that it bypasses the TIDA-00439. The variable electronic load is used to simulate the earth leakage fault current. In the test setup, the constant load is set to 86 mA. The variable electronic load is a square wave of 100 Hz and a 350-mA peak.

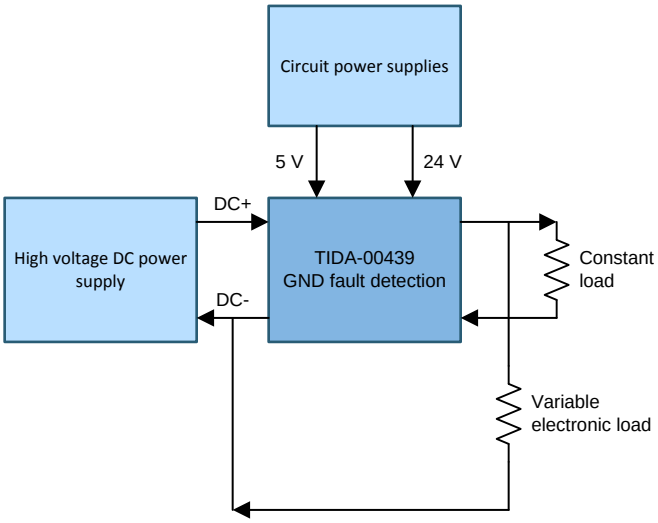

Figure 21. Setup for Creation of GND Fault Scenario

In Figure 22, the waveform in green is the earth leakage current, which is a square wave varying from 100 mA to 350 mA. This pulsed waveform is generated from the variable electronic load. The yellow waveform is the output of the GND fault detect comparator. The pink waveform is the average of the high-side and low-side current sense outputs. The blue waveform is the upper leakage detection threshold with hysteresis. It can be seen that as the earth leakage current crosses 300 mA, the pink waveform crosses the upper threshold and the GND fault comparator output is pulled low.

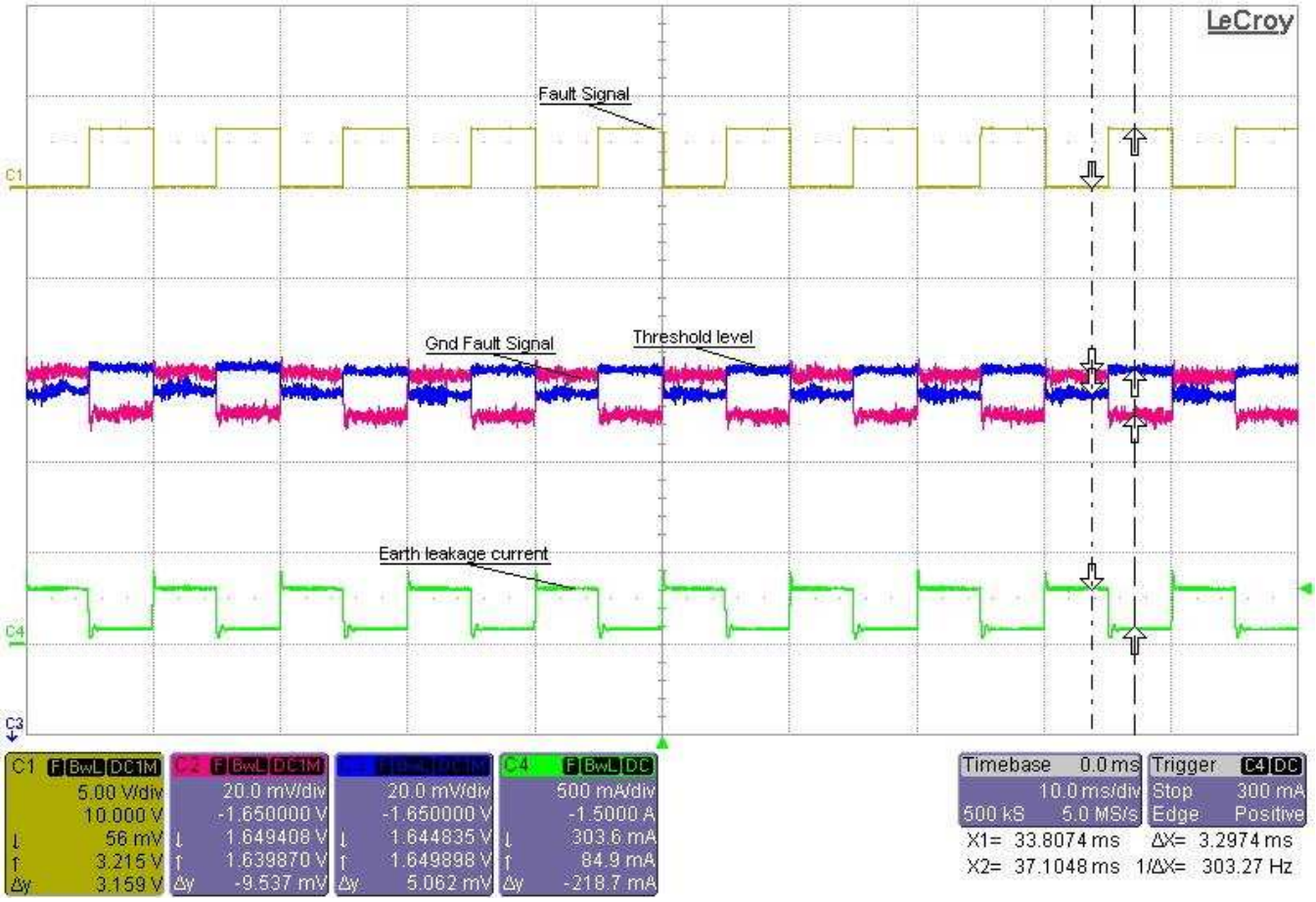

Figure 22. Detection of GND Fault

Figure 23 shows the response time to GND fault. The yellow waveform is the output of the GND fault detect comparator. When the output is pulled down low, it indicates a GND fault. The green waveform is the earth leakage current, which has a frequency of 100 Hz and varies from 100 to 350 mA. A zoomed-in version also shown to find out the response time. The response times is found out to be 40 µs.

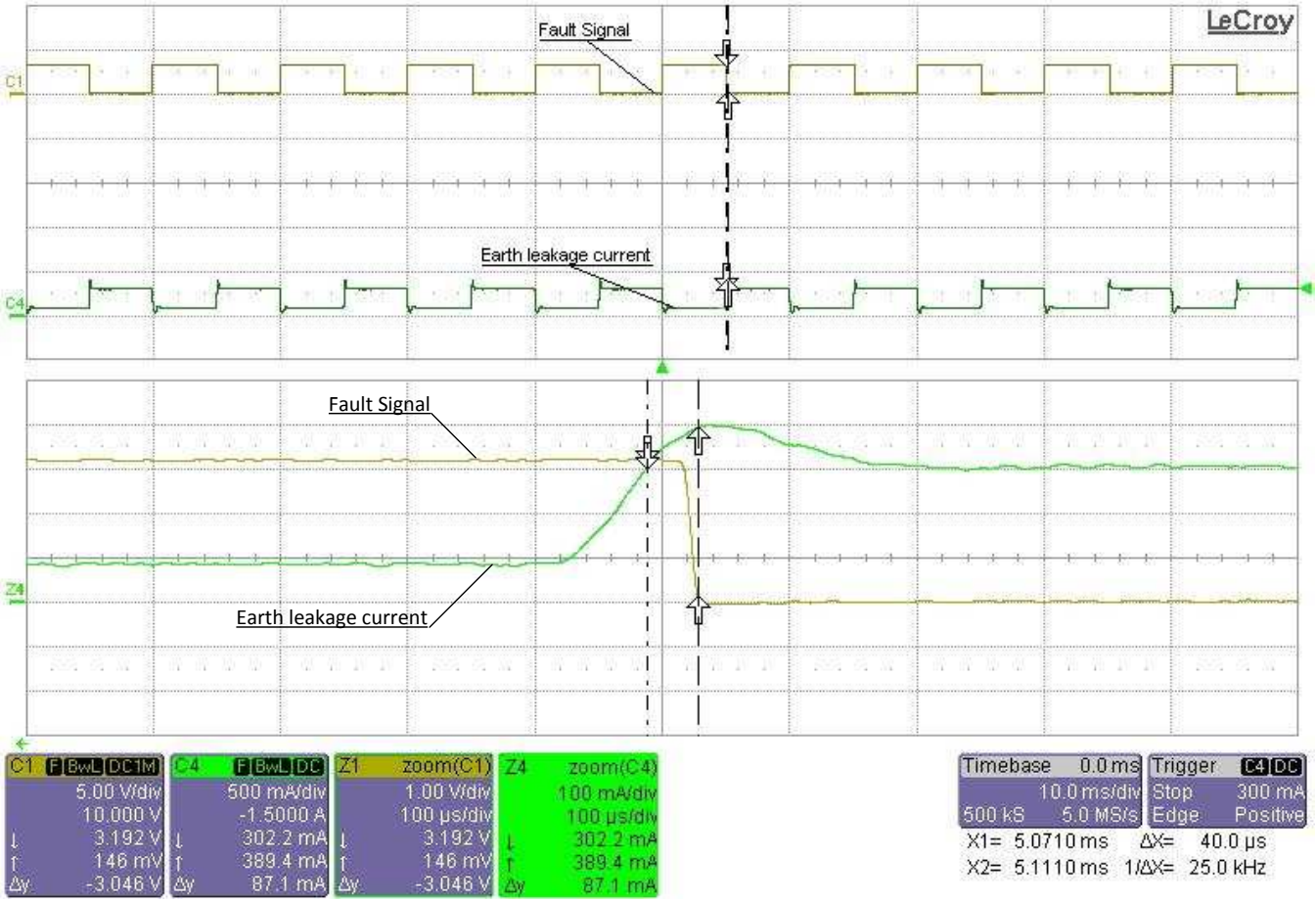

Figure 23. Response Time to GND Fault

6.5 Testing With C2000 High-Voltage Motor Control Kit to Detect GND Fault

In this test, the TIDA-00439 is used to detect GND fault on an actual motor drive. The C2000 high-voltage motor control application kit is used as the motor driver. A three-phase AC induction motor is connected to the drive. The block diagram of the setup is shown in Figure 24, and the actual setup shown in Figure 25 and Figure 26. The DC power supply is connected to the drive through the TIDA-00439 board. The motor is controlled by a GUI, which is shown in Figure 27. Connect the PC to the motor control kit through USB, power on the DC supply to the drive, select the motor type (either PMSM or ACIM), and enable the motor if none of the faults are flagged off. Detailed information about the high-voltage motor control application kit and the GUI are available by downloading the TI controlSUITE software.

The test result is shown in Figure 28. The yellow waveform is the earth leakage current with a frequency of 100 Hz and varying from a 100-mA to 350-mA peak. The response time is found to be 34.4 µs. The motor is run at 1000 rpm from a DC bus voltage of 170 V.

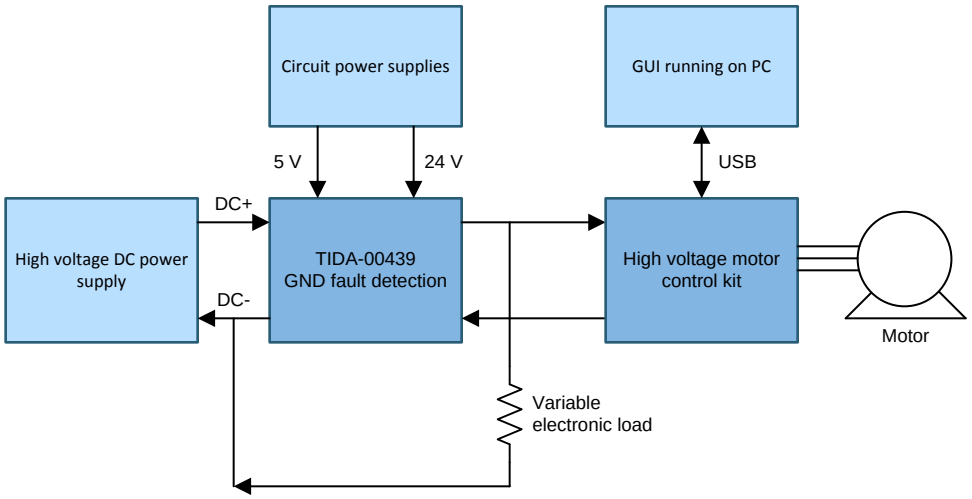

Figure 24. Block Diagram of C2000 High-Voltage Motor Drive Setup

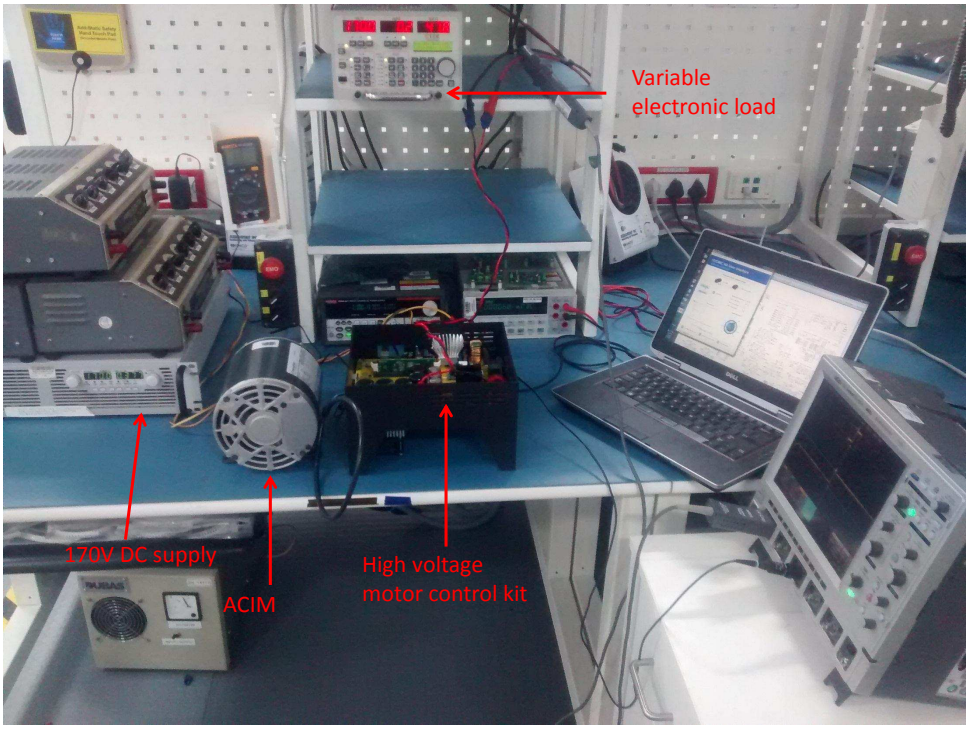

Figure 25. C2000 High-Voltage Motor Drive Setup

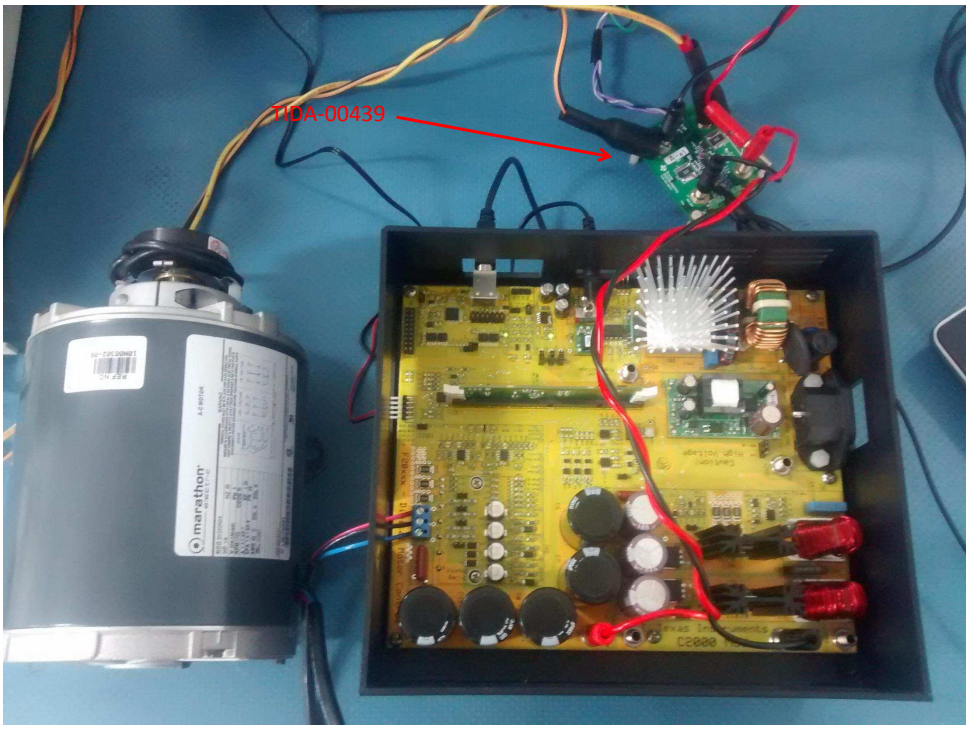

Figure 26. TIDA-00439 Connected to C2000 Motor Control Kit

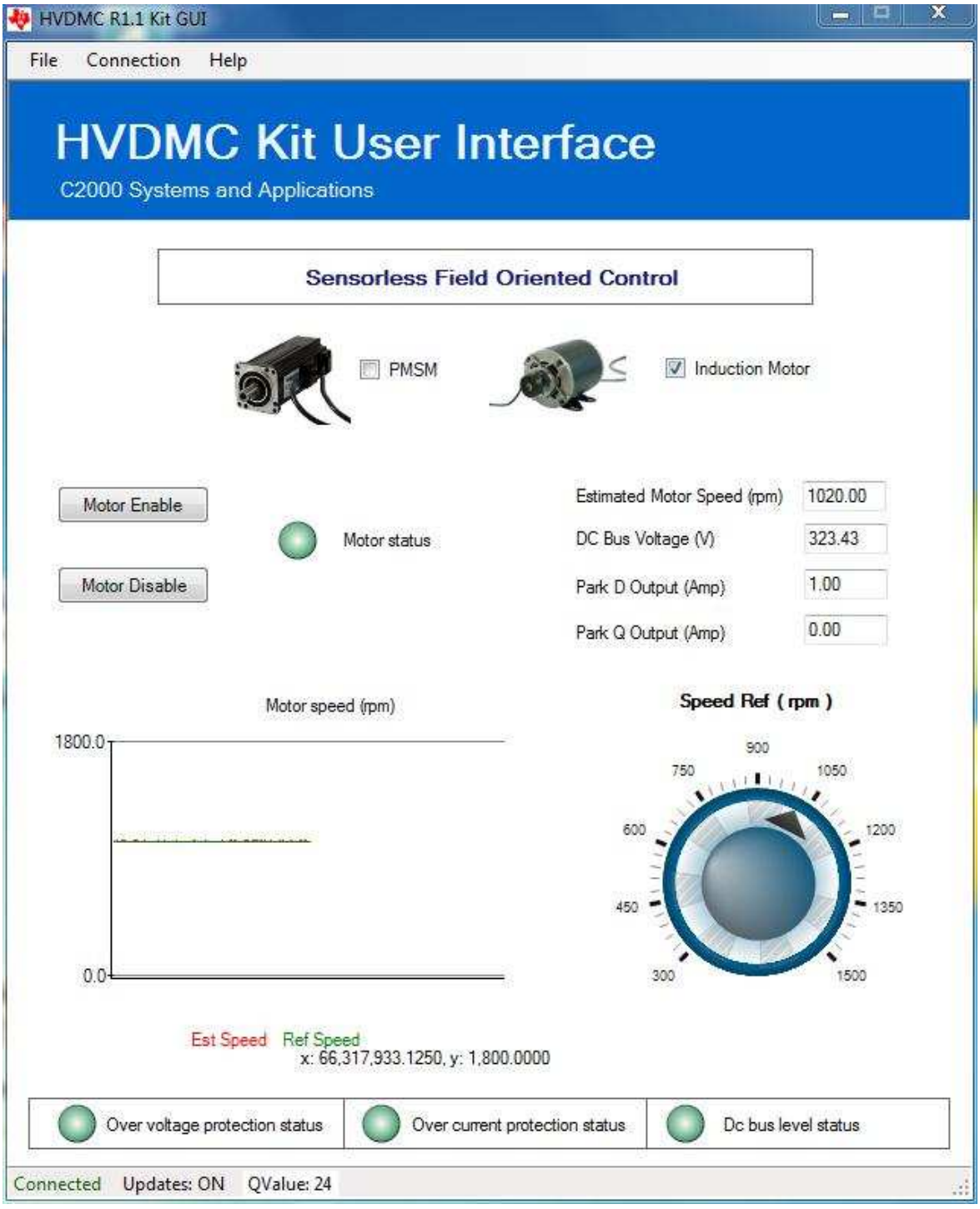

Figure 27. GUI to Control AC Motor

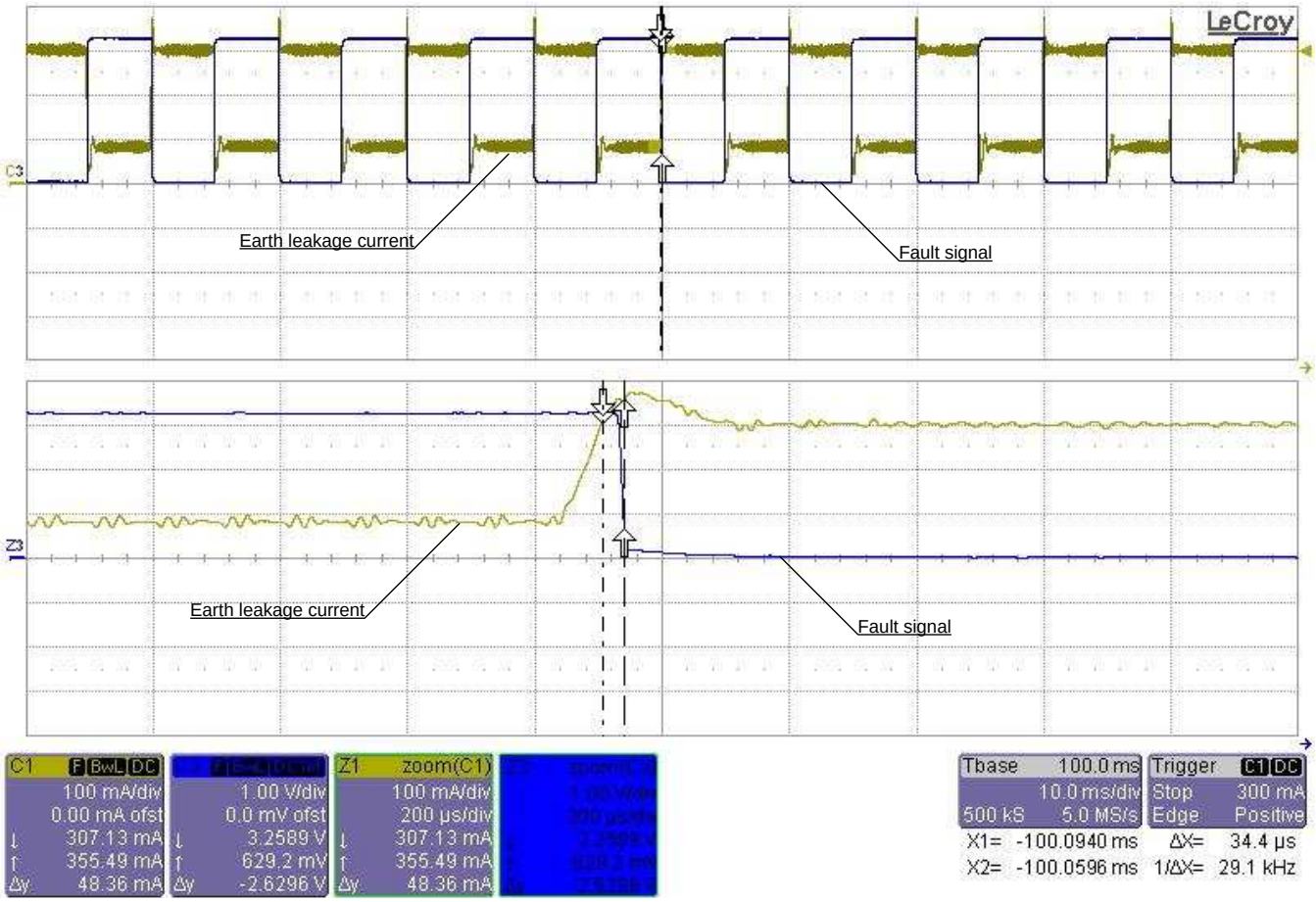

Figure 28. GND Fault Response Time

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00439.

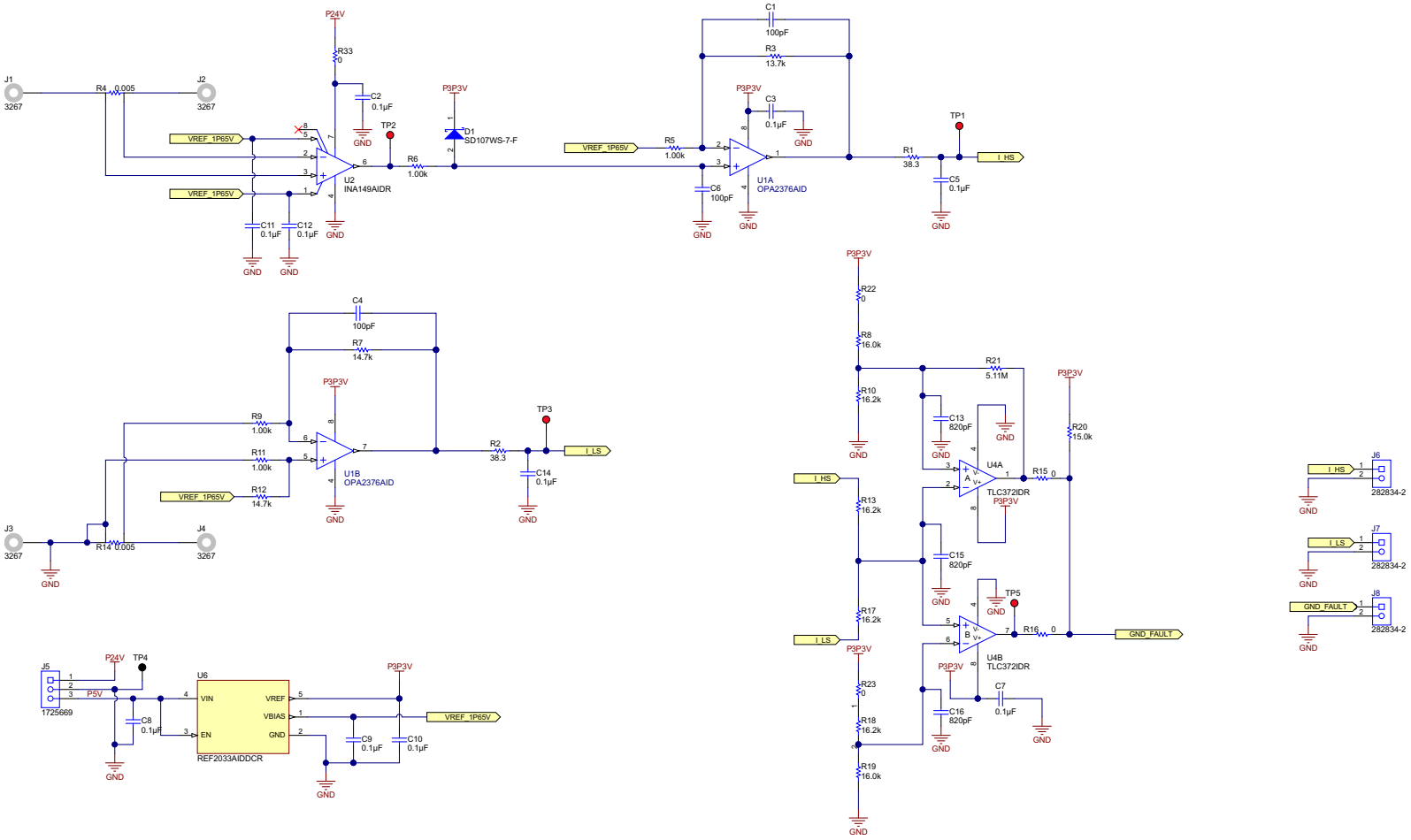

Figure 29. Sensing and Signal Conditioning

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00439.

7.3 PCB Layout Recommendations

The component placement and layout is very important to get the specified performance from the device as mentioned in the datasheet. This board contains high voltage nets. Take special care to provide sufficient spacing between high-voltage nets and low-voltage nets.

7.3.1 Layout Recommendations for High-Side Current Measurement Signal Chain

Figure 30 shows the layout for the INA149 difference amplifier IC:

- Use kelvin connections for current sense resistor. Place the +IN and –IN pins of the amplifier as close to the current sense resistor as possible. Make sure the traces from the current shunt resistor to the pins are symmetrical and short.
- Place the power supply noise decoupling capacitor C2 very close to the power supply pin of the IC. The function of this capacitor is to decouple the noise from the rest of the circuit from entering the IC. Therefore, during layout take care that the power supply first enters the capacitor and then into the IC power pin. If this is not done, the decoupling capacitor does not decouple the noise effectively. Also trace length from the decoupling capacitor to the IC power pin should be kept very short to minimize the trace stray parasitic inductance.
- Similarly C11 and C12 (placed on bottom layer connected through a via) should be kept close to pins 5 and 1, respectively. Make sure the reference signal first enters the capacitor and then into the pin in order to shunt the noise into the GND effectively.

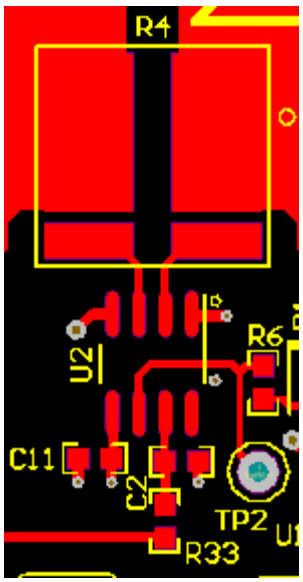

Figure 30. Layout Recommendations for INA149 Current Sense Circuit

- The output signal from INA149 to the next amplifier stage can be long because it is a low impedance net.
- For the succeeding non-inverting amplifier stage, make sure that the inverting and non-inverting nodes of the amplifier are as small as possible. Any noise that is picked up into these nodes gets amplified into the output signal. The output trace (low impedance) can be long but the input traces (high impedance) should be as small as possible.
- Place the decoupling capacitor as close as possible to the power pin as described before.

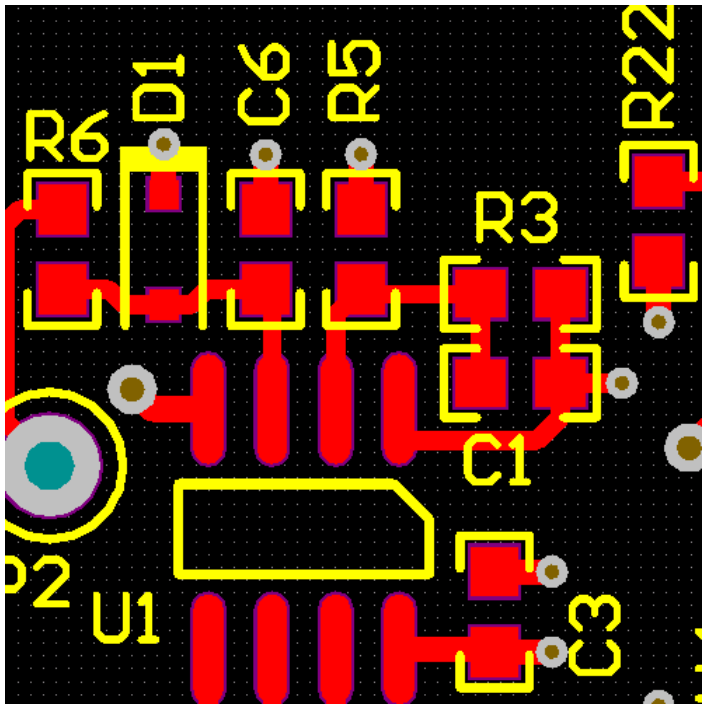

Figure 31. Layout Recommendations for OPA2376 High-Side Non-Inverting Amplifier

7.3.2 Layout Recommendations for Low-Side Current Monitor

- Use kelvin connections from the low-side current shunt resistor. Place the difference amplifier close to the shunt resistor and join it with short balanced traces to avoid offset voltages created due to input bias current of the op-amp and the trace parasitics.
- Keep all traces at the inverting and non-inverting nodes of the op-amp to be very short. Any noise coupled into these pins will be amplified and appear on the output.
- Place the power supply noise decoupling capacitor C6 very close to the power supply pin of the IC. The function of this capacitor is to decouple the noise from the rest of the circuit from entering the IC. Therefore, during layout take care that the power supply first enters the capacitor and then into the IC power pin, if this is not done the decoupling capacitor does not decouple the noise effectively. Also trace length from the decoupling capacitor to the IC power pin should be kept very short to minimize the trace stray parasitic inductance.

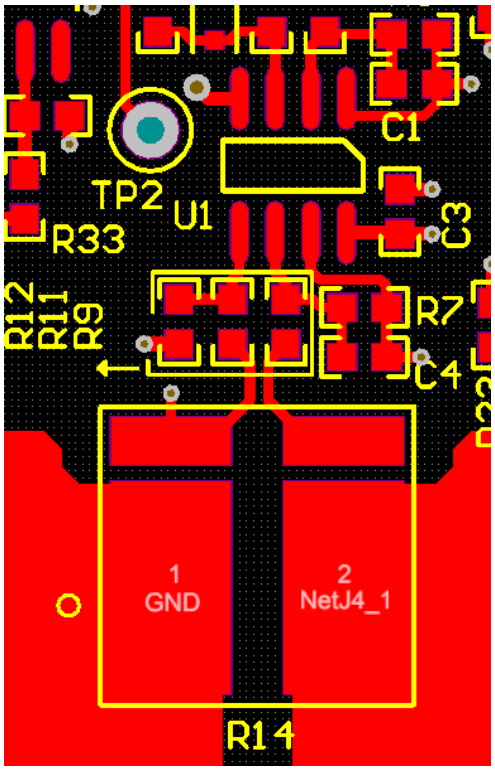

Figure 32. Layout Recommendations for OPA2376 Low-Side Difference Amplifier

7.3.3 Low-Side and High-Side Sense Resistor Wiring (Kelvin Connections)

- Current can be most precisely measured with the help of current shunt resistors. In order to make the power dissipation in these resistors negligible, very small values of current shunt resistors are used which are usually in the range of mΩ. At this range of resistance values the contact resistance and the termination resistance may be larger than the value of the resistor itself or may be a significant percentage in comparison to the value of the resistor. Therefore, if the voltage drop is measured across the resistor terminals like in Figure 33, what is actually measured is the sum of the voltage drops across the resistor and the resistor contacts as well as a part of the high current carrying trace. This adds a significant error to the actual voltage drop across the resistor, which is needed.
- This error can be avoided by using kelvin sense connections (connected on the inner side of the resistor pads) as shown in the lower picture of Figure 33. Now the actual current carrying path and the solder joint is no longer a part of the sense connection and the voltage measured is the actual voltage drop across the shunt resistor.
- For very low values of shunt resistors, a four-terminal resistor along with kelvin connection has to be used to get good accuracy.

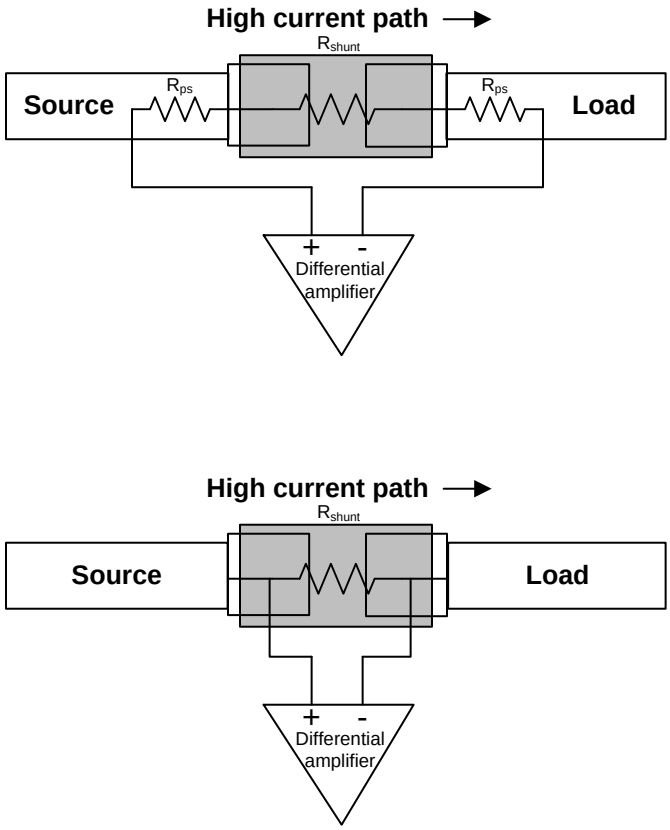

Figure 33. Non-Kelvin Connection versus Kelvin Connection

7.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-00439.

The size of the PCB is 71.12 × 62.23 mm.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00439.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00439.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00439.

8 References

1. Texas Instruments, *High Voltage Digital Motor Control Kit (R1.1) Quick Start Guide* (PDF)
2. Texas Instruments, *High Voltage Motor Control and PFC (R1.1) Kit Hardware Reference Guide* (PDF)
3. EE Times, *A Current Sensing Tutorial — Part IV: Layout and Troubleshooting Guidelines* (PDF)

9 About the Authors

PAWAN NAYAK is a systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the Motor Drive segment within Industrial Systems. Pawan brings to this role his experience in analog system design, mixed signal design and power supplies. Pawan earned his Bachelor of Engineering in Electronics and Communication Engineering from Visvesvaraya Technological University, India.

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Revision History

Changes from Original (June 2015) to A Revision	Page
• Changed from preview page	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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