TI Designs

Two-Wire Interface to a HIPERFACE DSL® Encoder

TI Designs

This reference design is an EMC-compliant industrial interface to a two-wire HIPERFACE DSL encoder. Applications include industrial servo drives. The design features a 3.3-V supply RS-485 transceiver and line termination and coupling for encoder power over RS-485 as per HIPERFACE DSL specification.

The design has been tested up to 100-m cable length with an integrated cable, where the encoder's two-wire twisted pair was integrated in the same motor cable. The encoder connector output is protected against over-voltage and short circuit to prevent damage to an encoder or during a cable short. The design features an industrial compliant 24-V input with a wide range from 18 to 36 V. A 3.3-V I/O connector with logic signals for easy interface to a host processor with HIPERFACE DSL Master IP Core is made available.

Design Resources

TIDA-00177	Design Folder
SN65HVD78	Product Folder
TPS5401	Product Folder
TPS24750	Product Folder
LM2903	Product Folder
CSD15571Q2	Product Folder
CSD25402Q3A	Product Folder
LMZ14201	Product Folder

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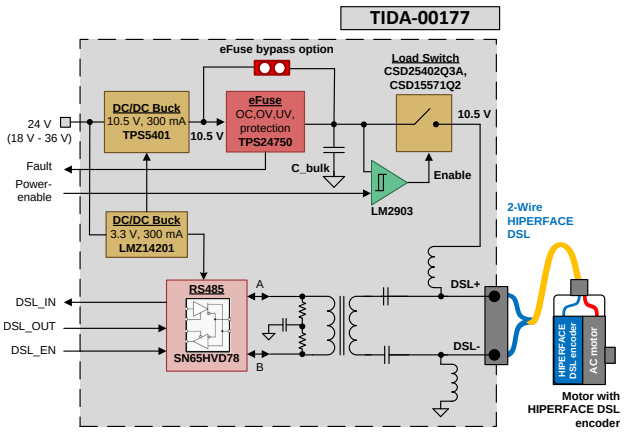
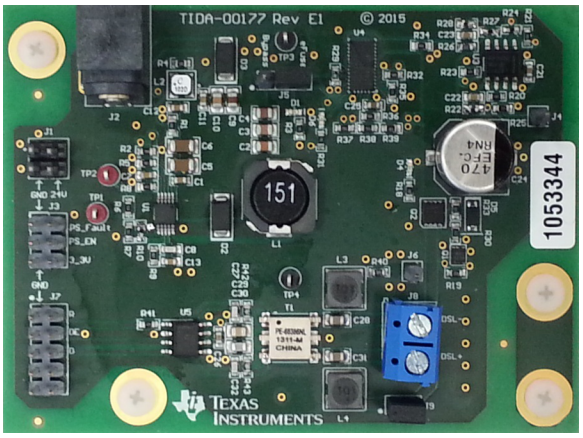
Design Features

- Two-Wire Interface to HIPERFACE DSL Encoder. Supports HIPERFACE DSL 9.375-MBaud Transfer Rate With Power Over RS-485, Cable Length up to 100 m
- 3.3-V Supply Half-Duplex RS-485 Transceiver With 12-kV IEC-ESD and 4-kV EFT
- Wide Input (18 to 36 V) Non-Isolated Power Supply With Configurable Output Voltage 7 to 12 V, Default 10.5 V, 250 mA (3.5-A Peak) Compliant to HIPERFACE DSL Specification
- OV, UV, and Precise Overcurrent Limit With Short-Circuit Protection Leveraging TI eFuse Technology With Fault Indicator
- Logic Interface (3.3-V I/O) to Host Processor Like Sitara™ for the HIPERFACE DSL Master
- Designed to Meet EMC Immunity for ESD, Fast Transient Burst, and Surge With Levels According to IEC61800-3

Featured Applications

- Servo Drives
- Industrial Drives
- Factory Automation and Control





1 System Description

1.1 TI Design Overview

This TI design implements an industrial temperature and EMC-compliant two-wire interface to a HIPERFACE DSL position encoder. The major building blocks of this TI design are the two-wire bidirectional RS-485 physical interface with power over RS-485 and the HIPERFACE DSL-compliant encoder power supply with overvoltage, overcurrent, and short-circuit protection. A simplified system block of a servo drive with a master interface to a HIPERFACE DSL encoder is shown in Figure 1, with the TI design represented by the box in light green. The host running the HIPERFACE DSL Master is not part of this design.

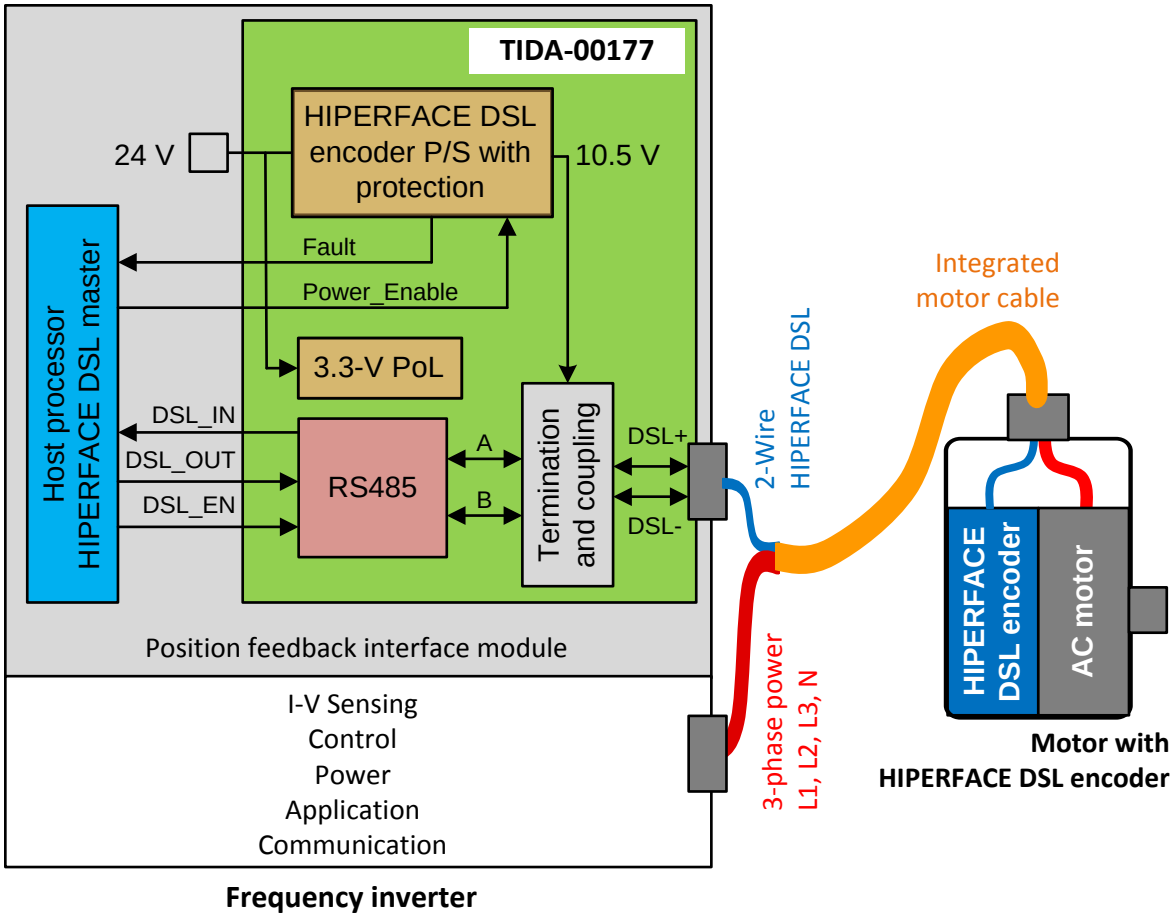


Figure 1. TIDA-00177 System Overview

The reference design connects to the HIPERFACE DSL encoder through a two-wire connector with DSL+/US and DSL–/GND. This design supports cable lengths up to 100 m. For cable specifications, refer to the HIPERFACE DSL standard.

The reference design is powered through a standard 24-V DC rail as typically used in drives. DC/DC buck converters each generate the 3.3-V supply rail for the RS-485 transceiver as well as the adjustable 10.5-V rail to supply the HIPERFACE DSL encoder. An eFuse is added to protect the encoder supply output for overvoltage, overcurrent, and short circuit. The eFuse can be bypassed if these features are not required. An additional load switch in combination with a bulk capacitor ensures the power supply provides enough inrush current during the power up cycle of the HIPERFACE DSL encoder.

The RS-485 line termination leverages a transformer as well as decoupling capacitors and inductors to modulate the RS-485 differential signal onto the power supply rail, as specified for the integrated cable with two core wires per HIPERFACE DSL specification.

A 3.3-V interface is provided to connect to a host processor like Sitara or FPGA to run the HIPERFACE DSL master protocol. The interface provides the DSL_IN, DSL_OUT, and DSL_EN signals to the host processor, which runs the HIPERFACE DSL Master protocol.

A fault signal is provided to the host processor for overvoltage and overcurrent indication and an Enable signal for the HIPERFACE DSL supply voltage if desired. The complete feature list of the design is described in Section 2.

1.2 Introduction to HIPERFACE DSL

HIPERFACE DSL is a digital protocol specified and owned by Sick. HIPERFACE DSL is derived from **HI**gh **PER**formance Inter**FACE D**igital **S**ervo **L**ink. The robustness of the protocol enables the connection to the motor feedback system through the motor connection cable and simplifies the installation of an encoder system in the drive.

Key features of HIPERFACE DSL two-wire physical interface are:

- Digital interface compliant to RS-485 standard with a transfer rate of 9.375 MBaud
- Half-duplex communication with the encoder through dual wires
- Power supply and communication with the encoder carried out using the same dual wires. The connection cables to the encoder are routed as a shielded, twisted pair cable in the power supply cable to the motor. Therefore, no separate cable for the encoder plug connector is required
- Cable length between the frequency inverter and the encoder up to 100 m, without degradation of the operating performance

The digital HIPERFACE DSL protocol can be used for a variety of frequency inverter applications with following features:

- For the feedback cycle of the frequency inverter's synchronous cyclic data that enables synchronous processing of position and rotation speed of the encoder (shortest possible cycle time: 12.1 µs)
- Transmission of the safe position of the motor feedback system with a maximum cycle time of 192 µs
- Redundant transmission of the safe position of the motor feedback system with a maximum cycle time of 192 µs so that suitable motor feedback systems can be used in SIL2 applications (in accordance with IEC 61508).
- Transmission of the safe position of the motor feedback system on a second channel with a maximum cycle time of 192 µs so that suitable motor feedback systems can be used in SIL3 applications (in accordance with IEC 61508)
- Parameter data channel for bi-directional general data transfer with a band width of up to 340 kBaud. Includes an electronic type label for designation of the motor feedback system and for storage of frequency inverter data in the motor feedback system
- Sensor Hub channel through which motor data from external sensors is transmitted and are connected by the HIPERFACE DSL Sensor Hub protocol to the motor feedback system

1.2.1 HIPERFACE DSL Protocol Overview

HIPERFACE DSL is a fast digital protocol for motor feedback systems for the connection between servo drive and motor feedback systems. The protocol is typically implemented in the transport layer in the frequency inverter using a digital logic circuit (DSL Master IP Core). The position data are generated in two different ways in HIPERFACE DSL: either in free running mode, in which the position values are sampled and transmitted as fast as possible, or in SYNC mode, in which the position data are sampled and transmitted synchronously with a defined clock signal. With a frequency inverter application, this clock signal is normally the clock feedback of the frequency inverter.

In SYNC mode, the protocol matches the time points for the sampling of the data without time fluctuations with the clock coming from the frequency inverter. For each frequency inverter cycle, at least one position value is sampled and transmitted with constant latency to the DSL master. As the protocol matches the internal data transfer speed to the frequency inverter cycle, the overall transfer rate of the HIPERFACE DSL depends on the frequency inverter clock.

The protocol package is matched to the various lengths. Provided the frequency inverter cycle is long enough, additional sampling points can be positioned in the frequency inverter cycle, known as "extra" packages. The number of additional packages is programmed by the user with a distribution value. The number of packages transmitted per frequency inverter cycle cannot be selected at random, as the lower and upper range length of a protocol package must be adhered to. This must be taken into account when setting the distribution value. In free running mode, the frequency inverter cycle is not taken into account for sampling and transmission and the protocol uses the minimum package length. It must be noted that the minimum package length in free running mode is shorter than the minimum package length in SYNC mode.

Table 1. Frequency Inverter Cycle and Length of Protocol Packages

INVERTER CYCLE FREQUENCY (kHz)	CYCLE TIME (µs)	PROTOCOL PACKET LENGTH (µs)	PROTOCOL PACKETS PER INVERTER CYCLE
2	500	12.5	40
4	250	12.5	20
6.25	160	13.33	12
8	125	12.5	10
16	62.5	12.5	5
40	25	12.5	2
37 to 84	27 to 12.1	27 to 12.1	1
Free running	—	11.52	—

For details on the protocol, refer to HIPERFACE DSL protocol specification.

1.2.2 HIPERFACE DSL Physical Layer

As a physical layer, HIPERFACE DSL uses a transfer in accordance with EIA-485 (RS-485). Valid RS-485 interface drivers must comply with the conditions in Table 2.

Table 2. RS-485 Transceiver Specifications

CHARACTERISTIC	VALUE
Transfer rate	> 20 MBaud
Permitted common mode voltage	–7 to 12 V
Minimum differential input voltage detected	< 200 mV
Minimum load resistance	< 55 Ω
Receiver propagation delay	< 60 ns
Transmitter propagation delay	< 60 ns
Transmitter power-up delay	< 80 ns
Transmitter power-down delay	< 80 ns
Transmitter rise time	< 10 ns
Transmitter fall time	< 10 ns

1.2.3 HIPERFACE DSL Encoder Supply Voltage

Motor feedback systems with HIPERFACE DSL have been developed for operation with a supply voltage of 7 to 12 V. The voltage supply is measured at the encoder plug connector. The specification for the HIPERFACE DSL power supply is listed in Table 3.

Table 3 describes the specification for the power supply.

Table 3. Power Supply Specification

PARAMETER	VALUE
Operating supply voltage	7 to 12 V
Supply voltage power-up ramp time (0 to 7 V)	< 180 ms
Inrush current (0 to 100 µs)	≤ 3.5 A
Inrush current (0 to 100 µs)	≤ 1 A
Operating current	≤ 250 mA at 7 V

A more detailed diagram of the inrush current versus the supply voltage is shown in Figure 2.

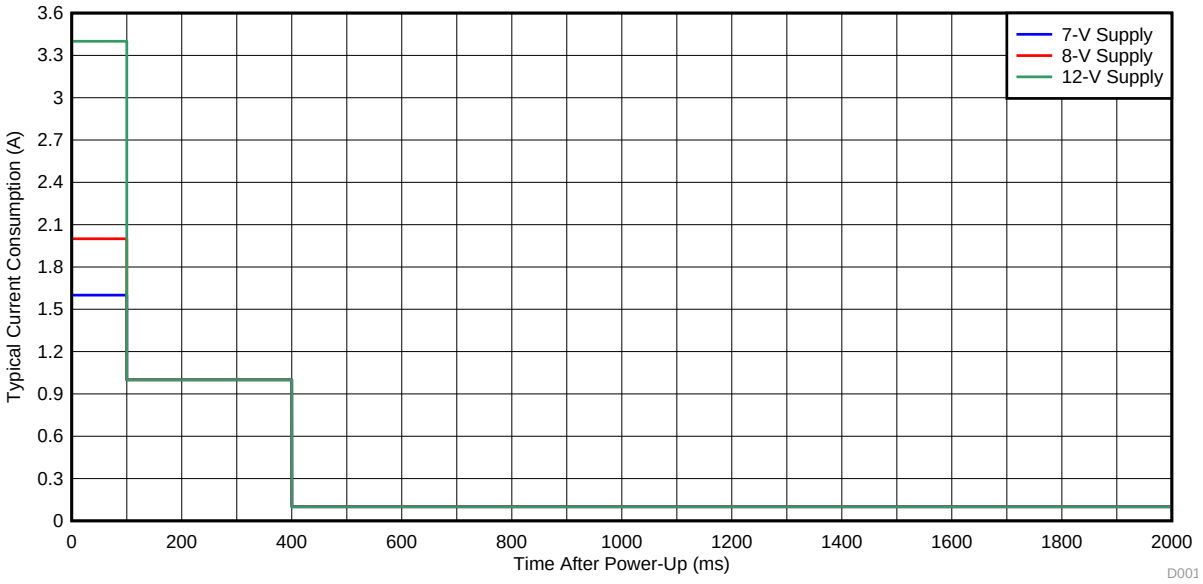


Figure 2. Maximum Inrush Current versus Supply Voltage

1.2.4 Encoder Interface Circuit

HIPERFACE DSL can be used in two different interface circuit configurations. Each configuration requires a different kind of connection cable.

1.2.4.1 Separate Encoder Cable—Four-Wire Interface

When using a separate encoder cable, the four-wire interface is used. The corresponding block diagram is shown in Figure 3.

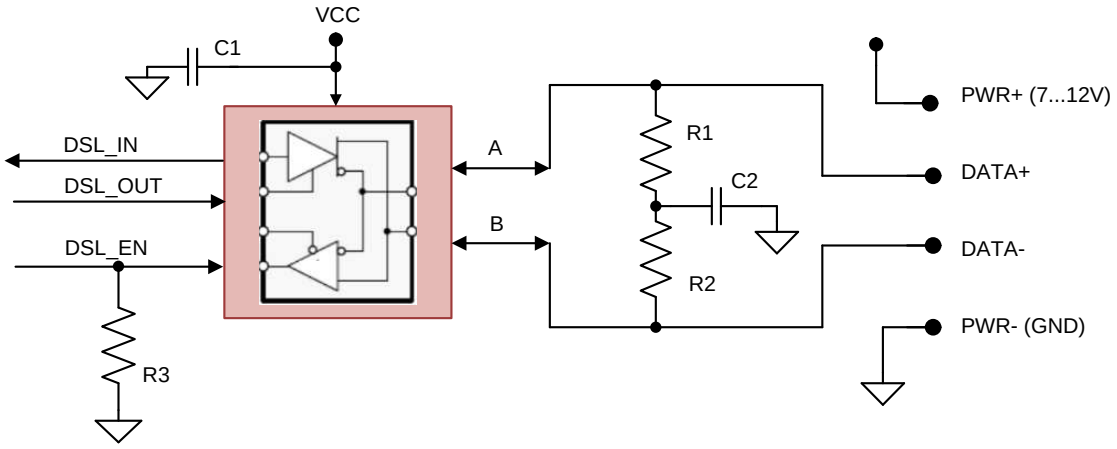


Figure 3. Four-Wire Interface Circuit With Separate Encoder Cable

The corresponding values of the passive components for line termination are provided in the HIPERFACE DSL specification. R1 = R2 = 56 Ω, C1 = 100 ns, C2 = 2.2 µF.

1.2.4.2 Integrated Motor Cable—Two-Wire Interface

For use with a two-wire cable integrated in the motor cable, a transformer is required to increase common mode rejection ratio. The supply voltage and GND are coupled onto the RS-485 differential signals through an inductor L1 and L2, and DC decoupled to the transformer through capacitors C3 and C4, respectively. The differential RS-485 signals after the transformer are AC coupled into the two wires through wires. The corresponding values of the passive components for line termination are provided in the HIPERFACE DSL specification. R1 = R2 = 56 Ω, C1 = 100 ns, C2 = 2.2 µF/16 V, C3 = C4 = 470 nF/50 V. L1 = L2 = 100 µH.

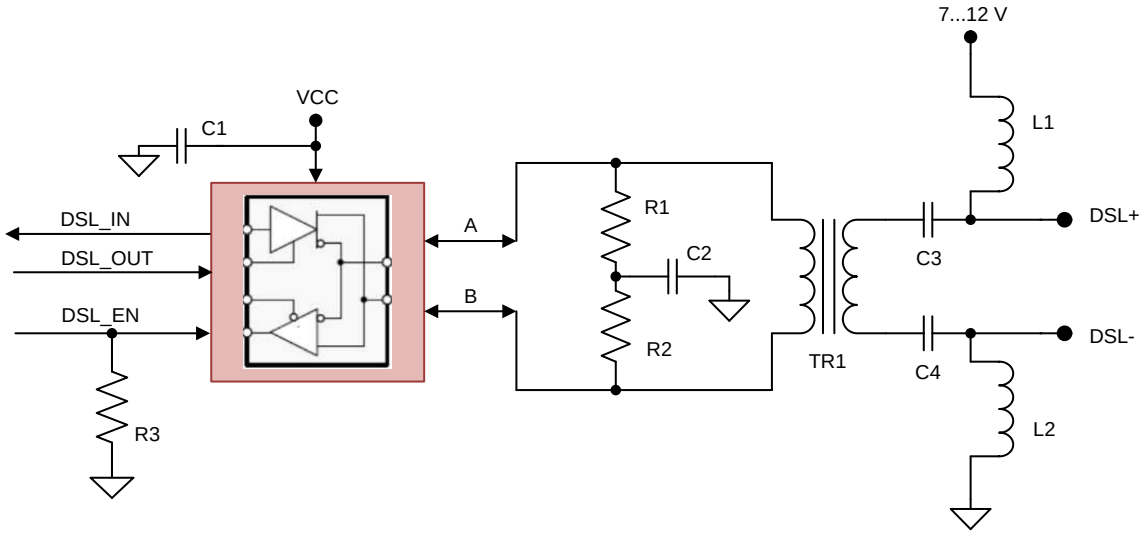


Figure 4. Two-Wire Interface Circuit With Integrated Motor Cable

1.2.5 Cable Specification

The cable recommended for connecting the frequency inverter to the HIPERFACE DSL motor feedback system is shown in Table 4. These technical data apply to all configurations.

Table 4. HIPERFACE DSL Cable Technical Information

CHARACTERISTICS	MINIMUM	TYPICAL	MAXIMUM	UNIT
Length			100	m
Impedance at 10 MHz	100	110	120	Ω
DC loop resistance			0.1	Ω/m
Velocity ratio	0.66			°C
Propagation delay		5		ns/m
Limit frequency	25			MHz
Maximum current per cable	250			mA
Operating temperature	–40		125	ºC

For more information on cable specifications, refer to the white paper *Cable and Connector for HIPERFACE DSL Motor and Drive Applications* (http://www.sick.com/group/EN/home/products/technologies/hiperfacedsl/Pages/hiperfacedsl_documentation.aspx).

2 Design Features

As outlined in Section 1, this TI design realizes an industrial temperature range, EMC-compliant two-wire interface to HIPERFACE DSL position encoders. A 3.3-V I/O logic interface is provided to connect to a HIPERFACE DSL Master IP Core. The HIPERFACE DSL Master (IP Core) is not part of this TI design.

The design key features are:

- 24-V input voltage with wide input range (18 to 36 V) and reverse polarity protection
- EMC-compliant two-wire hardware interface to a HIPERFACE DSL encoder (power over RS-485). Supports HIPERFACE DSL 9.375 MBaud transfer rater with power over RS-485, cable length up to 100 m
- 3.3-V supply half-duplex RS-485 transceiver with 12-kV IEC-ESD and 4-kV EFT with direct interface to host processor
- HIPERFACE DSL compliant power supply with 10.5-V output (adjustable) with high-efficiency, 200-mA nominal output current and minimum 3.5-A inrush current (100 µs)
- Optional overvoltage, undervoltage, and precise overcurrent limit with short-circuit protection leveraging TI eFuse technology
- Fault indicators and enable signal to enable or disable the power supply for HIPERFACE DSL through host processor
- Logic interface (3.3-V I/O) to connect to host processor like Sitara for the HIPERFACE DSL master
- Designed to meet EMC immunity for ESD, Fast Transient Burst, and Surge with levels according to IEC61800-3
- Industrial temperature range of –40ºC to 85ºC

2.1 Input Supply Voltage With Reverse Polarity Protection

Table 5. Input Power Supply Specification

CHARACTERISTICS	VALUE
Input voltage	18 to 36 V, 24 V (nominal)
Max. input current	500 mA
Reverse polarity protection	Yes
Input EMI filter	Yes
Connector	DC Jack (3.5 mm)

2.2 Two-Wire HIPERFACE DSL Encoder Connector

Table 6. HIPERFACE DSL Encoder Connector Features

FEATURE	SPECIFICATION
Type	Two-wire HIPERFACE DSL
PHY	Single RS-485 half-duplex transceiver with 3.3-V supply and IEC-ESD
Supply voltage	10.5 V (over RS-485)
Interface circuit	Two-wire (incl. transformer and power over RS-485)
Isolation	No
Connector or signals	Two-terminal connector for DSL+ and DSL– signals
Cable length	Up to 100 m

2.3 HIPERFACE DSL Power Supply With Protection

Motor feedback systems with HIPERFACE DSL have been developed for operation with a supply voltage of 7 to 12 V. The voltage supply is measured at the encoder plug connector. A certain inrush current has to be provided during power-up as outlined in the previous section. The features of this TI design are listed in the following subsections.

An eFuse was added as part of the entire encoder power supply to electronically disconnect power from the encoder in case of a fault. Fault conditions are overvoltage and undervoltage and continuous overcurrent. A fault flag is made available on the logic I/O connector to allow a host controller to recognize the fault condition and react accordingly. The advantage of an eFuse is that is can be re-enabled by power-cycling and provides a precise current limit also versus temperature and aging.

2.3.1 Supply Voltage and Current

Table 7. HIPERFACE DSL Supply Voltage and Current Specification

CHARACTERISTICS	VALUE
Output voltage	10.5 A (±5%)
Supply voltage power-up ramp time (0 to 7 V)	< 1 ms
Inrush current (0 to 100 µs)	3.5 A (min), 7 A (max)
Inrush current (100 to 400 µs)	≥ 1 A
Output current (nominal)	250 mA (±10%)

2.3.2 Protection

Table 8. HIPERFACE DSL Supply Output Protection Features

CHARACTERISTICS	VALUE
Overvoltage	12 V
Undervoltage	7 V
Overcurrent (continuous)	< 250 mA (±10%)
Short-circuit protection	Yes
Short-circuit shutdown (output voltage off)	30 ms (eFuse)
Overcurrent, overvoltage, and undervoltage fault flag	Yes
Bypass option for eFuse (if desired)	Yes
Option to disable HIPERFACE DSL output	Yes

2.4 Logic I/O Connector Interface to Host Processor for HIPERFACE DSL IP Core

The design features a 3.3-V I/O interface to a host processor for the HIPERFACE DSL Master IP Core. Additional signals are provided for control and monitoring the encoder supply if desired.

Table 9. TIDA-00177 Logic Interface

PARAMETER	VALUE
DSL_IN (O)	3.3-V I/O
DSL_OUT (I)	3.3-V I/O
DSL_EN (I)	3.3-V I/O (default pulldown)
Overcurrent, overvoltage, and undervoltage fault flag (O)	3.3-V I/O

2.5 EMC Immunity Requirements According to IEC61800-3

This TI design has been developed to meet ESD, EFT, and Surge (IEC61000-4-2, 4-4, 4-5) with levels specified in IEC618000-3. IEC618000-3 specifies the EMC requirements for adjustable speed electrical power drive systems. The intention of this TI design has been for use in such drives. Table 10 specifies the minimum requirements, as applicable for example cases or cabinets and connectors.

The design is part of a servo drive and only the shielded connector for the HIPERFACE DSL encoder can be accessed. It is assumed the connecter's shield is tied to Earth.

According to IEC61800-3, the connector would then fall under "Ports for process measurement and control lines, DC auxiliary supplies lower than 60V". Since the encoder cable can be up to 100 m, fast transient burst, surge, and conducted RF common mode applies for use in Environment 2.

Table 10. Extract of IEC61800-3 EMC Requirements for Environment 2

PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION
Enclosure ports	ESD	IEC61000-4-2	±4-kV CD or 8-kV AD, if CD not possible	B
	Radiated RF	IEC61000-4-3	80 to 1000 MHz, 10 V/m, 80% AM (1 kHz) 1.4 to 2 GHz, 3 V/m, 80% AM (1 kHz) 2 to 2.7 GHz, 3 V/m, 80% AM (1 kHz)	A
Ports for control lines and DC auxiliary supplies < 60 V	Fast transient burst	IEC61000-4-4	±2-kV/5 kHz, capacitive clamp	B
	Surge 1.2/50 µs, 8/20 µs	IEC61000-4-5	±1 kV. Since shielded cable > 20 m, direct coupling to shield (2 Ω/500 A)	B
	Conducted RF	IEC61000-4-6	0.15 to 80 MHz, 10 V/m, 80% AM (1 kHz)	A

The performance (acceptance) criterion is defined, as follows:

Table 11. EMC Compliance Acceptance Criterions

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module must continue to operate as intended with no loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module must continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module must continue to operate as intended automatically, after manual restart, power off, or power on.

3 System Block Diagram

The major building blocks are the protected encoder power supply and the RS-485 transceivers including line termination and coupling for power over RS-485. The block diagram is shown in Figure 5.

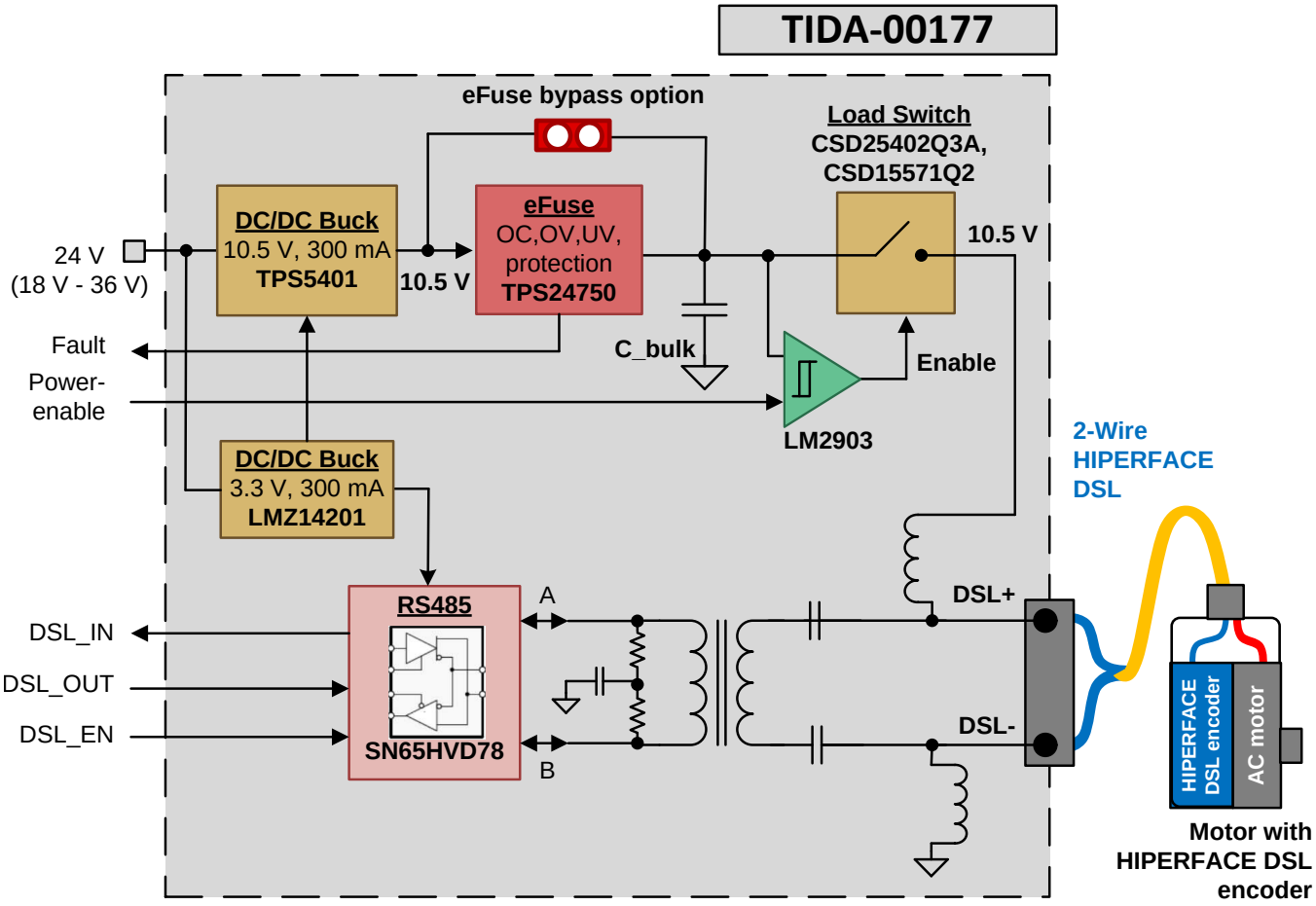


Figure 5. TIDA-00177 System Block Diagram

4 Circuit Design and Component Selection

Due to the challenging current profile at the start-up required by the HIPERFACE DSL encoders (in brief no soft-start has to be provided), the current peak at the start-up is very high, as can be seen in Figure 2.

This can be achieved mainly in two ways:

1. Oversize the SMPS to be able to provide a minimum of a 3.5-A peak without soft-start: this results in a too big, too expensive solution, for a system whose current requirement is 250 mA max after the start-up.
2. Charge a bulk capacitor and then, driven by a proper comparator with hysteresis, connect the fully charged cap to the output.

Smaller and cheaper when compared to the first one, the second option has been implemented here.

4.1 RS-485 Communication and Logic Interface

4.1.1 RS-485 Transceiver

The installation of HIPERFACE DSL in a drive system requires an interface circuit with special components as well as a FPGA or host processor for the HIPERFACE DSL Master IP Core.

The interface circuit is described thoroughly in this section. The chapter also contains recommendations for the selection of components.

The digital logic core (IP Core) is supplied by SICK for prescribed FPGA types. In addition, the type of cable recommended for the connection between the frequency inverter and the motor feedback system is described thoroughly in this chapter. It may also be possible to use other sorts of cable. However, these must be tested before use.

As a physical layer, HIPERFACE DSL uses a transfer in accordance with EIA-485 (RS-485). Valid RS-485 interface drivers must comply with the conditions in Table 12.

Table 12. RS-485 Driver Interface Specifications

CHARACTERISTIC	VALUE	TIDA-00177 SOLUTION BASED ON SN65HVD78D
Transfer rate	>20 MBaud	Up to 50 MBaud
Permitted common mode voltage	–7 to 12 V	–7 to 12 V
Minimum differential input voltage detected	< 200 mV	80 mV (typ)
Load resistance	< 55 Ω	54 Ω
Receiver propagation delay	< 60 ns	< 35 ns
Transmitter propagation delay	< 60 ns	< 15 ns
Transmitter power-up delay	< 80 ns	< 30 ns
Transmitter power-down delay	< 80 ns	< 30 ns
Transmitter rise time	< 10 ns	< 6 ns
Transmitter fall time	< 10 ns	< 6 ns
ESD	NA	12-kV CD
EFT	NA	4 kV

4.1.2 RS-485 Termination and Transient Protection

To minimize voltage rails, a 3.3-V supply RS-485 transceiver with a 5-V tolerant I/O and low quiescence power has been selected. Due to the 3.3-V I/O, it can typically directly connected to a processor.

Integrated Cable—Two-Wire Interface
For a connection through a two-wire cable integrated in the motor cable, the data cables must be provided with a transformer to raise the common mode rejection ratio. To feed the supply voltage into the data cables, choke coils are also required.

With reference to Figure 4, the following values have been used:

Table 13. Interface Circuit With Two-Wire Cables (Integrated in Cable)

COMPONENT	DESCRIPTION	PART
C1	Ceramic capacitor	2.2 µF, 16 V
C2, C3	Ceramic capacitor	470 nF, 50 V
L1, L2	Inductors	Würth Elektronik 744043101, 100 µH or Panasonic ELL6SH101M, 100 µH
R1, R2	Resistors	56R
R3	Resistors	1k to 100k
U1	RS-485 transceiver	Texas Instruments SN65HVD78D
TR1	Transformer	Pulse Engineering PE-68386NL or Murata 78602/1C or Epcos B78304B1030A003

4.1.3 TIDA-00177 Interface Solution

In order to meet the previous requirement, the SN65HVD78D has been selected to implement the RS-485 transceiver.

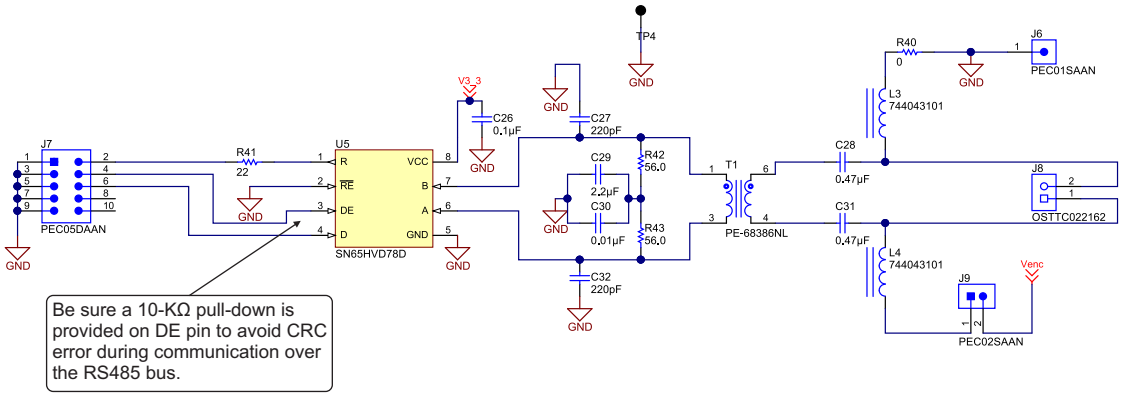


Figure 6. TIDA-00177 HIPERFACE DSL Two-Wire Interface

In the solution, the transceiver topology is half-duplex with the receiver always active, and the transmitter is enabled from the MPU GPIO. Data are collected by the CPU across the R and D pin (RX and TX, respectively).

4.1.4 Logic Power Supply

The communication interface needs a 3.3-V rail for the RS-485 transceivers. This is achieved by a simple switcher module, the LMZ14201.

3.3-V PoL

The voltage rail for the RS-485 is 3.3 V at 300 mA, coming from the 24-V bus (the voltage can be between 17 and 36 V). As this power supply does not need to be isolated, a buck (step-down) topology is optimal. The specifications for this power supply are:

- Input: 17 to 36 V, 24 V nominal
- V_{OUT}: 3.3 V @ 300 mA
- Target switching frequency ~ 700 kHz
- Non-isolated

Assuming that on the end application the 3.3-V rail will also be used to power other parts of the system (µC, FPGA, and so on), a good performance as well as high integration and easiness of use power module has been chosen.

In particular, the Texas Instruments LMZ142001 power module presents several advantages:

- Really easy to design with, saving time to market and development cost
- Already tested for EMI and EMC
- Allows size and parts count effective solutions

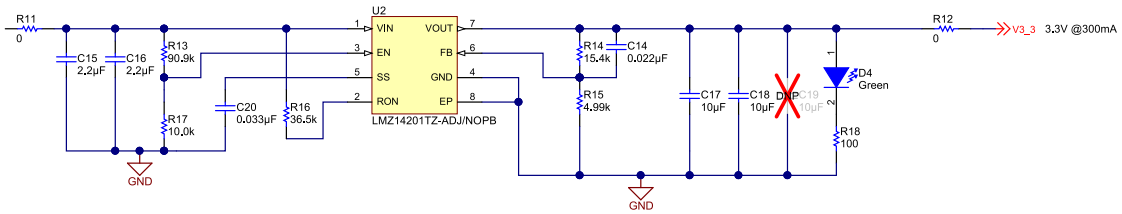


Figure 7. 3.3-V Logic Power Supply

For more details on the part, how to calculate the external components, and layout guidelines, refer to its TI product page folder.

4.2 Protected Encoder Power Supply

The encoder requires a voltage between 7 and 12 V at 250 mA, coming from the 24-V bus (the voltage can be between 17 and 36 V): as this voltage conversion does not needs to be isolated, a buck (step-down) topology is optimal. This voltage rail also requires some protections like overvoltage protection (OVP), undervoltage protection (UVP), over-temperature protection (OTP), overcurrent protection (OCP), and short-circuit protection (SCP). These features are handled by an eFuse.

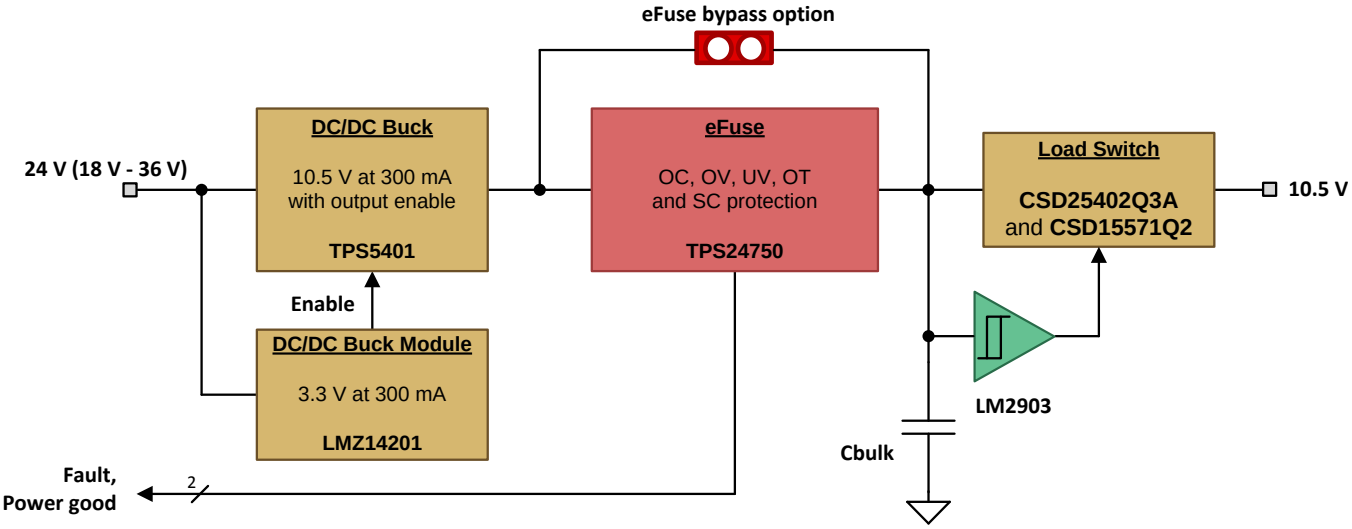


Figure 8. TIDA-00177 Power Management Solution

The whole system will work in the following way:

- During power-up, the load switch is open and the TPS5401 will charge the bulk capacitor to 10.5 V.
- When the bulk capacitor voltage exceeds 10 V, the load switch is turned on and the bulk capacitor provides the 3.5-A peak current for 100 us to the HIPERFACE DSL encoder (if already connected). The solution behaves the same even when the encoder is connected after the start-up.
- The advantage of the eFuse in the middle between the DC-DC converter and the bulk capacitor is that it still limits the current to, for example, 250 mA in case of a short circuit and turn-off P/S after 25 ms.
- A comparator with hysteresis is selected to change the switching threshold after the load is applied (that is, using a normal comparator will cause bouncing, since the cap will be discharged by the big current inrush); the bulk capacity is calculated in order to ensure voltage does not drop below 7 V during the first 500 µs.

In particular, the amount of charge at the start-up is calculated as:
$Q_{start\text{-}up} = 3.5\ A \times 100\ \mu s + 1\ A \times 300\ \mu s < C_{bulk} \times (10\ V - 8\ V)$

From which the minimum value of C_{bulk} can be calculated as $C_{bulk} > 325\ \mu F$. Therefore, a value of 470 µF has been chosen for C_{bulk} to compensate tolerances, temperature, and aging effects on the real capacitor value.

4.2.1 Load Switch Control and Protection With eFuse

This block performs two main features:

- Protect the encoder by using the eFuse TPS24750 (OVP, OTP, UVP, and OCP)
- Provide the correct current profile to the encoder as for its own specification (the real challenge of the design)

For the latter feature, a big capacitor is charged and, once the voltage on it is around 10 V then the power switch (CSD25402) is turned on, providing to the encoder all the current it needs (in particular the inrush one, stated to be 3.5 A for the first 100 µs).

The purpose of the big bulking cap is then to maintain the voltage above the minimum working voltage of the encoder (7 V).

This is why a comparator with hysteresis based on the LM2903 is used (U3A); the other op-amp (U3B) is used to override the automatic control (by using a GPIO on the J4 input) performed by U3A and whose thresholds are designed to be 7 V and 10 V (rising and falling, respectively).

The selection is made at the BOM level through the 0-Ω shunt R21 and R23.

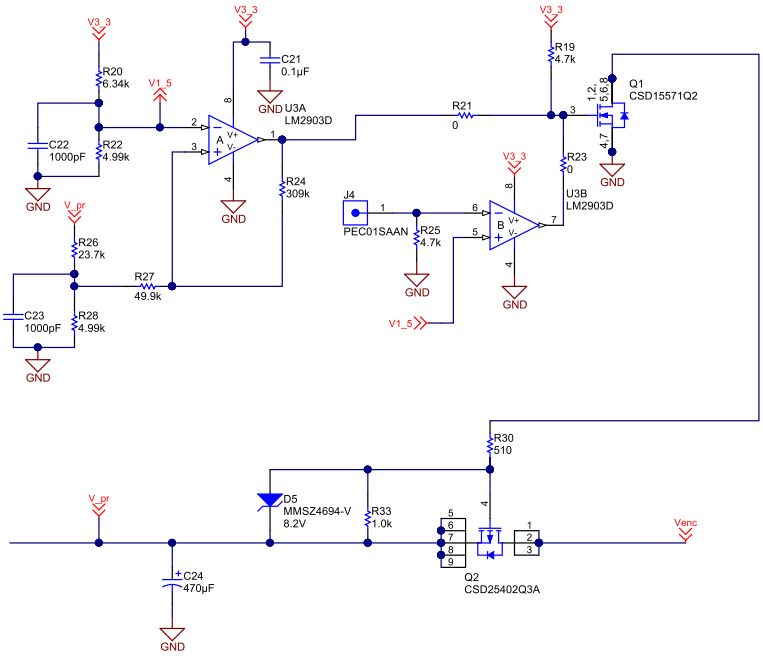


Figure 9. Load Switch Control Circuit

Since the LM2903 is an open-drain output op-amp, the calculation is a bit more complex than usual. A reference for the comparator is set to 1.512 V by Equation 1:

$$3.3\ V \times \frac{R_{22}}{R_{20} + R_{22}} = 1.512\ V \tag{1}$$

While the two thresholds for the $V_{\_pr}$ are set by

$$V_{pr} \times K_1 \times K_2 = 1.512\ V \tag{2}$$

In which

$$K_1 = \frac{R_{28}}{R_{26} + R_{28}} = 0.174 \tag{3}$$

resulting in $V_{\_pr} \approx 10.1$ V (the rising threshold), and

$$K_2 = \frac{R_{24}}{R_{24} + R_{27}} = 0.861 \tag{4}$$

In which

$$V_{pr} \times K_1 + \left(3.3\ V - V_{pr} \times K_1\right) \times K_3 = 1.512\ V \tag{5}$$

resulting in $V_{\_pr} \approx 7.06$ V (the falling threshold).

The equations before look complex at first sight, but when it is assumed to be R27 + R24 >> R26 + R28, then the full comparator with hysteresis could be seen as:

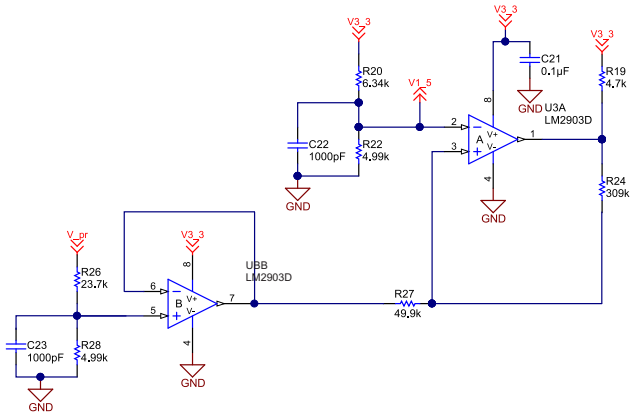


Figure 10. Simplified Circuit for Thresholds Calculation

This makes life easier when designing the load switch commutation thresholds.

To ensure all the assembled boards perform properly, a worst case analysis has to be leaded on the calculation of the comparator's thresholds.

Also note that the divider R20/R22 has a double purpose:

- Give the ability to override the load switch control through GPIO (by acting on the O-ring, R21/R23, and, in particular, removing the R21).
- Help to prevent the maximum voltage on the non-inverting pin of the comparator (pin U3.3) being higher than the max allowed rating for the pin (since the supply is 3.3 V as well).

4.2.2 Protection With eFuse

About the eFuse, the BOM has been designed in according to the following:

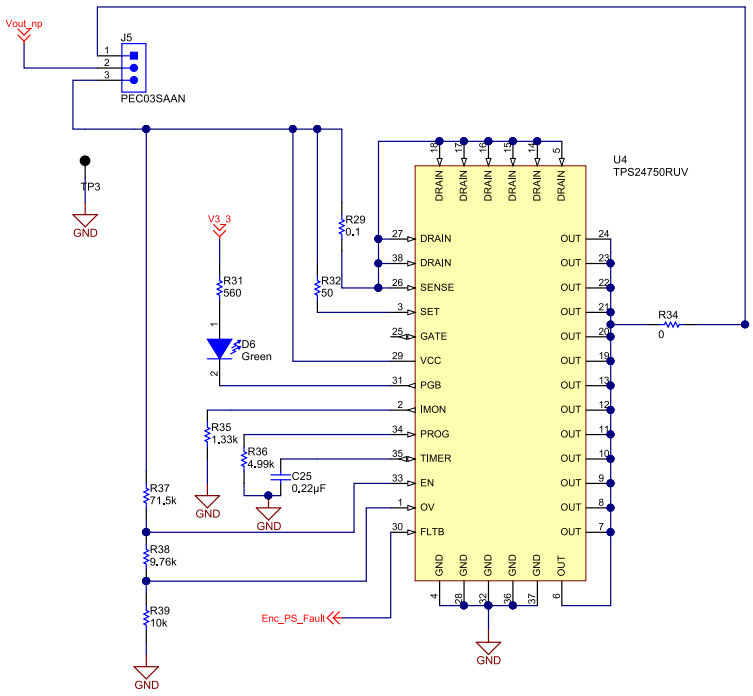


Figure 11. eFuse TPS24750

UVP is triggered by the V_{ENABLE} (pin EN) when lower than 1.3 V. This occurs for an input voltage (to the eFuse, named V_{OUT_NP}) of

$$K_3 = \frac{R_{27}}{R_{19} + R_{24} + R_{27}} = 0.137 \quad (6)$$

The divider has been chosen in order to enable the device when the input voltage is (nominal or typical value) above 6 V. Therefore, the undervoltage threshold is 6 V.

OVP is triggered by V_{OVP} (pin OV) when higher than 1.35 V. This occurs for an input voltage V_{OUT_NP}) of

$$V_{out\_np} \times \frac{R_{38} + R_{39}}{R_{37} + R_{38} + R_{39}} = 1.3\ V \quad (7)$$

The divider has been chosen in order to have the device triggering OVP when the input voltage is above 12.3 V. Therefore, OV is set to 12.3 V.

Overcurrent limit: The current limit I_{LIM} is set by Equation 8:

$$V_{out\_np} \times \frac{R_{39}}{R_{37} + R_{38} + R_{39}} = 1.35\ V \quad (8)$$

I_{LIM} provides a means of sensing the voltage across this resistor, as well as a way to monitor the drain-to-source voltage across the internal FET. R_{SENSE} is set to 0.1 Ω.

A fast-trip shutdown occurs when the voltage across the R_{SENSE} resistor exceeds 60 mV.

Since the TPS5401 is set to work at 300 mA maximum, best practice leads to the setting of OCP (fast trip) at around double the nominal maximum load, so 600 mA = 60 mV / R_{SENSE}, from which the 100-mΩ value has been calculated. R_{SET} = 50 Ω

The R_{SET} resistor scales the current limit and power limit settings. It coordinates with R_{IMON} and R_{SENSE} to determine the current limit value. R_{IMON} = 1.33 kΩ

The R_{IMON} resistor scales the current-limit and power-limit settings. The voltage present at this pin is proportional to the current flowing through sense resistor, R_{SENSE}. This voltage can be used as a means of monitoring current flow through the system. The value of R_{IMON} can be calculated in combination with R_{SENSE} and R_{SET}.

An overload protection is triggered when the voltage on IMON pin is above 675 mV; that means, with the used values, a current limitation set to 250 mA ±10%.

CAUTION

This pin should not have a bypass capacitor or any other load except for R_{IMON}.

The R_{PROG} resistor sets the maximum power permitted in the internal MOSFET during inrush. *Do not apply a voltage to this pin.* If the constant power limit is not desired, like in this design, use a PROG resistor of 4.99 kΩ, otherwise set the power limit accordingly to the specific needs.

The overcurrent timer limit is set by the TIMER pin (C25) to 220 nF.

The timer pin source is a 10-µA constant current. This means that adding a cap from the TIMER pin to GND generates a voltage ramp on the same pin. Like the SS pin in the DC/DC converters, it represents an easy way to program times (a comparator triggers an event when the voltage on the timer cap reaches a predefined value, like 1.35 V in the TPS24750).

So the equation to calculate the C_{timer} is

$$I_{LIM} = 675\ mV \times \frac{R_{SET}}{R_{IMON} + R_{SENSE}} \quad (9)$$

When a fault triggering delay of 30 ms is wanted, the C_{timer} should be 220 nF. This allows the bulk capacitor to be properly charged at the start-up without triggering the eFuse fault.

A capacitor (CT) connected from the TIMER pin to GND determines the overload fault timing. The TIMER pin sources 10 µA when an overload is present, and discharges CT at 10 µA otherwise. Internal FET is turned off when V_{timer} reaches 1.35 V. In an application implementing auto-retry after a fault, this capacitor also determines the period before the internal FET is re-enabled. A minimum timing capacitance of 1 nF is recommended to ensure proper operation of the fault timer. The value of CT can be calculated from the desired fault time tilts, using the Equation above.

Either latch mode (TPS24750, TPS24752) or retry mode (TPS24751, TPS24753) occurs if the load current exceeds the current limit threshold or the fast trip shutdown threshold. While in latch mode, the TIMER pin continues to periodically charge and discharge the attached capacitor. In retry mode, the internal MOSFET is disabled for sixteen cycles of TIMER charging and discharging. The TIMER pin is pulled to GND by a 2-mA current source at the end of the 16^{th} cycle of charging and discharging. The internal MOSFET is then re-enabled.

The TIMER pin capacitor, CT, can also be discharged to GND during latch mode or retry mode whenever any of the following occurs:

- Enable pin voltage is below its falling threshold
- V_{CC} pin voltage drops below the UVLO threshold
- OV pin voltage is above its rising threshold

The TIMER feature does not interact with the die OTP.

C_{timer} has been set big to avoid false tripping of OCP at the start-up, since the TPS5401 has to charge the big bulk capacitor.

Summarizing, the TPS5401 has been designed to provide up to a 300-mA output current, since the encoder is specified to consume 250 mA max.

So the eFuse intervenes at 250 mA ±10% (see the R_{IMON}, R_{SET}, and R_{SENSE} settings).

Act on R_{IMON} (R35 in the schematic) to change the OCP threshold of the eFuse. In particular, the bigger the R35 the lower the current threshold, and vice versa.

Note that the TPS2492 has a similar function and support voltages between 9 and 80 V and is available in a TSSOP package.

4.2.3 HIPERFACE DSL Encoder Inrush Current Profile Emulator

In order to check if the system is able to meet the HIPERFACE DSL encoder current requirement at start-up (see Figure 2), an Encoder Current Profile Emulator has been designed.

The biggest challenge of this design is to emulate the load (the real encoder) with passive components.

Recalling the current profile at the start-up specified for the encoder Figure 2, some calculation or simulation could be performed to evaluate the best values for the passive network that will be used to emulate the inrush current and operating current:

- Maximum 3.5 A (0 to 100 µs)
- Maximum 1 A (100 to 400 µs)
- Operating current maximum 250 mA at 7 V

The network used to emulate the load is shown in Figure 12.

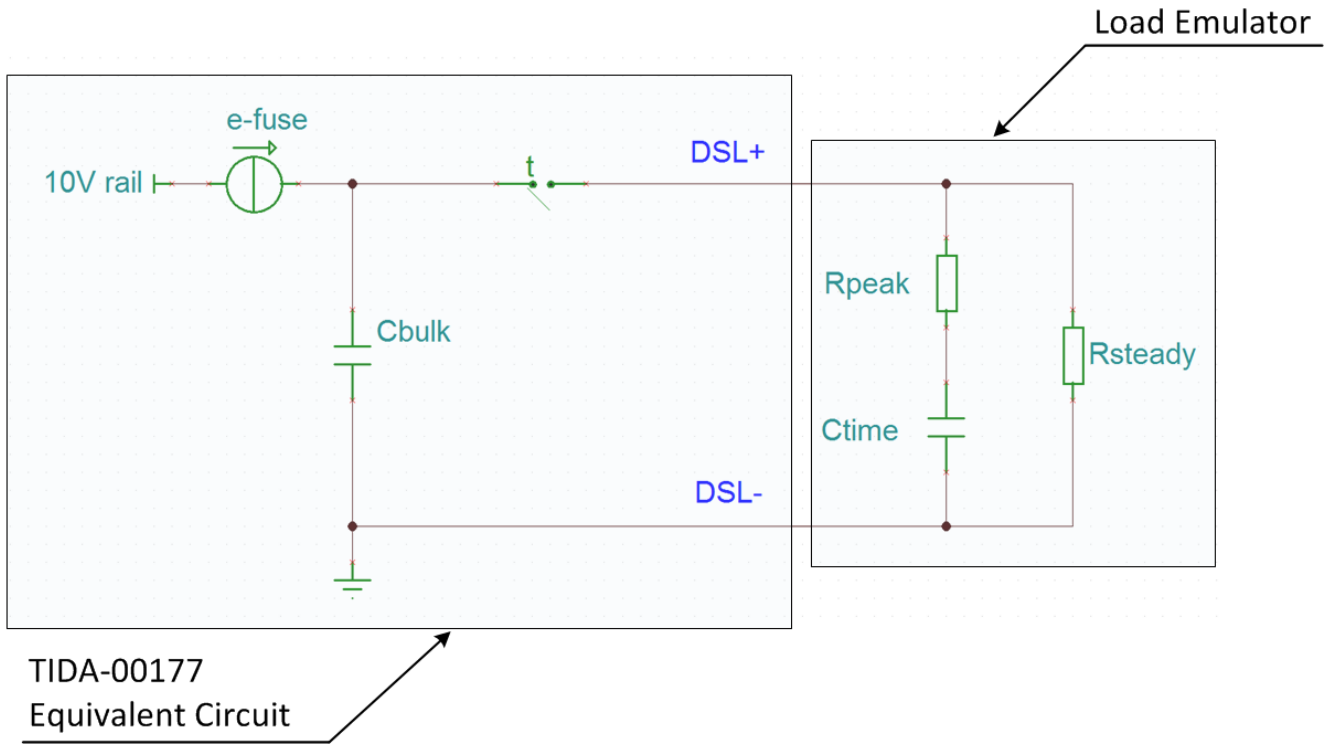


Figure 12. Encoder Current Profile Emulator Test Circuit

In which:

- The ideal 10-V rail generator represents the TPS5401.
- The current generator is 250 mA and represents the eFuse that limits the current to that value (so the combination of TPS + eFuse can be assumed to behave like a current generator).
- C_{bulk} is the big capacitor used to hold the charge and maintains and guarantees a 7-V minimum for the encoder supply (refer to C24 in the schematic).
- The switch corresponds to the power NexFET Q2 and closes when the charge on C24 is 10 V with a tolerance of ±5%. This depends on the tolerances of the selected resistors and the 3.3-V supply rail.
- R_{peak}, C_{timer}, and R_{steady} represent the encoder emulator and, in particular:
  - After the switch Q2 has closed, after a long time or in a steady state, or anyway after 400 us, as for the load current profile, the output current is 250 mA max at the minimum voltage (7 V). This is why eFuse and TPS have been designed for such current level. So C_{timer} is fully charged and the only load is represented by R_{steady}, which is then calculated as 10 V / 250 mA = 40 Ω.
  - Before the switch Q2 closes, C_{timer} is empty, so the actual load is R_{peak} // R_{steady}. Since a peak of 3.5 to 4 A is wanted, most of this current will flow into R_{peak} (R_{steady} has already been calculated). A value for R_{peak} of 3 to 3.3 Ω has been calculated.
  - C_{timer} defines the duration of the current peak and in how much time it settles down to the static value of 250 mA max.

Solving the little circuit shown in Figure 12 leads to (depending on the settled constrain) a maximum value for C_{timer} of 100 to 120 µF (to avoid the voltage on C24 dropping below 7 V and have the load switch to open).

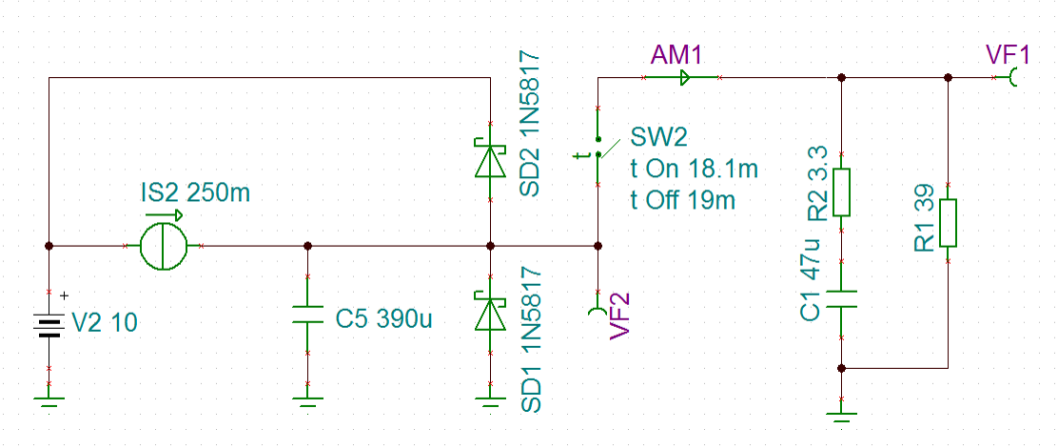


Figure 13. System Level Simulation Circuit of Encoder Current Profile Emulator

A system level equivalent circuit has been then simulated. The achieved results have been:

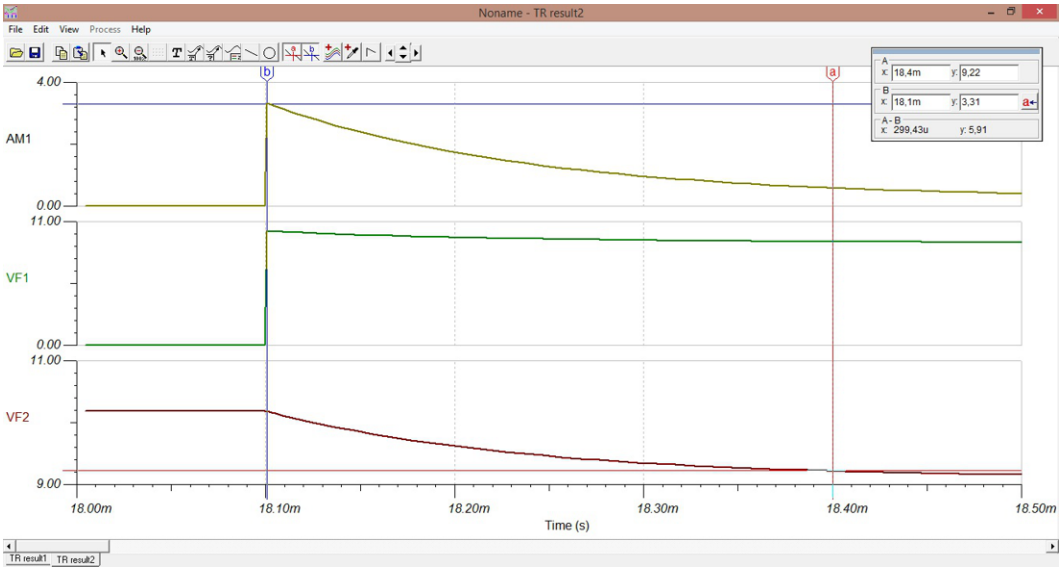


Figure 14. System Level Simulation Results

The peak current is 3.3 A and the voltage drops of less than 1 V in or after 400 µs.

The physical implementation of the circuit and load-emulator described so far is achieved by combining the electronic load Chroma (that implements the 39-Ω or 250-mA constant current load) and an RC network for the rest.

In particular, the 3-Ω resistor has to sustain the 3- to 4-A peak for 100 µs, so the design uses three 10-× resistors with a big package/power rating (1206 or 2510) in parallel.

4.2.4 Input Filter

Conducted EMI are generated by the normal operation of switching circuits. Large discontinuous currents are generated by the power switches turning ON and OFF. In a buck topology, those large discontinuous currents are present at the input side. The voltage ripple, created by those discontinuous currents, can be conducted to the rest of the system through physical contact of the conductor. Excessive input voltage ripples can disturb the normal operation of other part of the system (source, load, others). To prevent this, the input filter can be used to reduce the input voltage ripple and thus prevent to compromise the operation of the complete system.

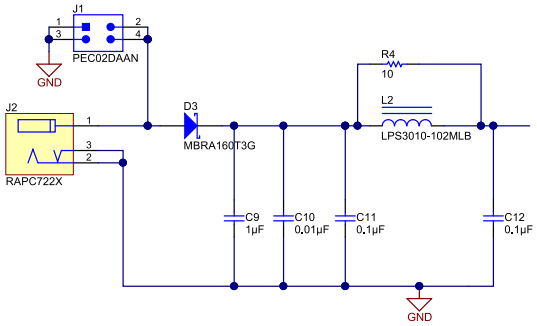


Figure 15. TIDA-00177 Input Stage (Connector, Reverse Polarity Protection, and EMI Filter)

4.2.5 DC/DC Buck (TPS5401)

The TPS5401 is a 3.5 to 42-V input, 0.8 to 39-V at 0.5-A output buck converter with integrated FET. Its frequency can be adjusted from 100 kHz to 2.5 MHz or can be synchronized with an external clock. It can also be enabled or disabled. All of these features make the TPS5401 a good fit for the TIDA-00177.

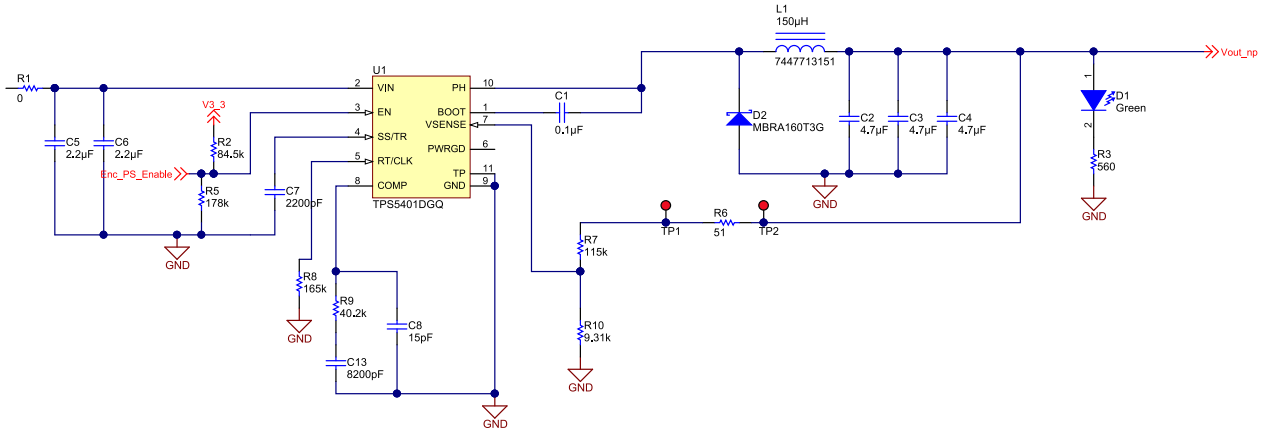


Figure 16. Protected Encoder Power Supply Schematic Based on TPS5401

Setting Output Voltage and Changing Parameters

The output voltage is set through the resistor divider R7/R10 according to Equation 10:

$$C_{timer} = \frac{10\ \mu A}{1.35\ V} \times timer\_fault\_delay \tag{10}$$

Note that the TPS5401 is pin-to-pin compatible with the TPS54040A, TPS54140A, TPS54240, TPS54340, and TPS54540, which have different current capabilities and accuracy.

4.3 Connector to HIPERFACE DSL Encoder

A two-pin connector (J8) is provided to connect a HIPERFACE DSL encoder to the TIDA-00177. For more details, look at the J8 description in Section 5.2.

4.4 Design Upgrades

It is recommended to add a pulldown resistor at the logic input DSL_EN in case the host processor connected to it does not have an internal pulldown. The pulldown value could be 4.7 to 10 kΩ.

5 Getting Started

5.1 PCB Overview

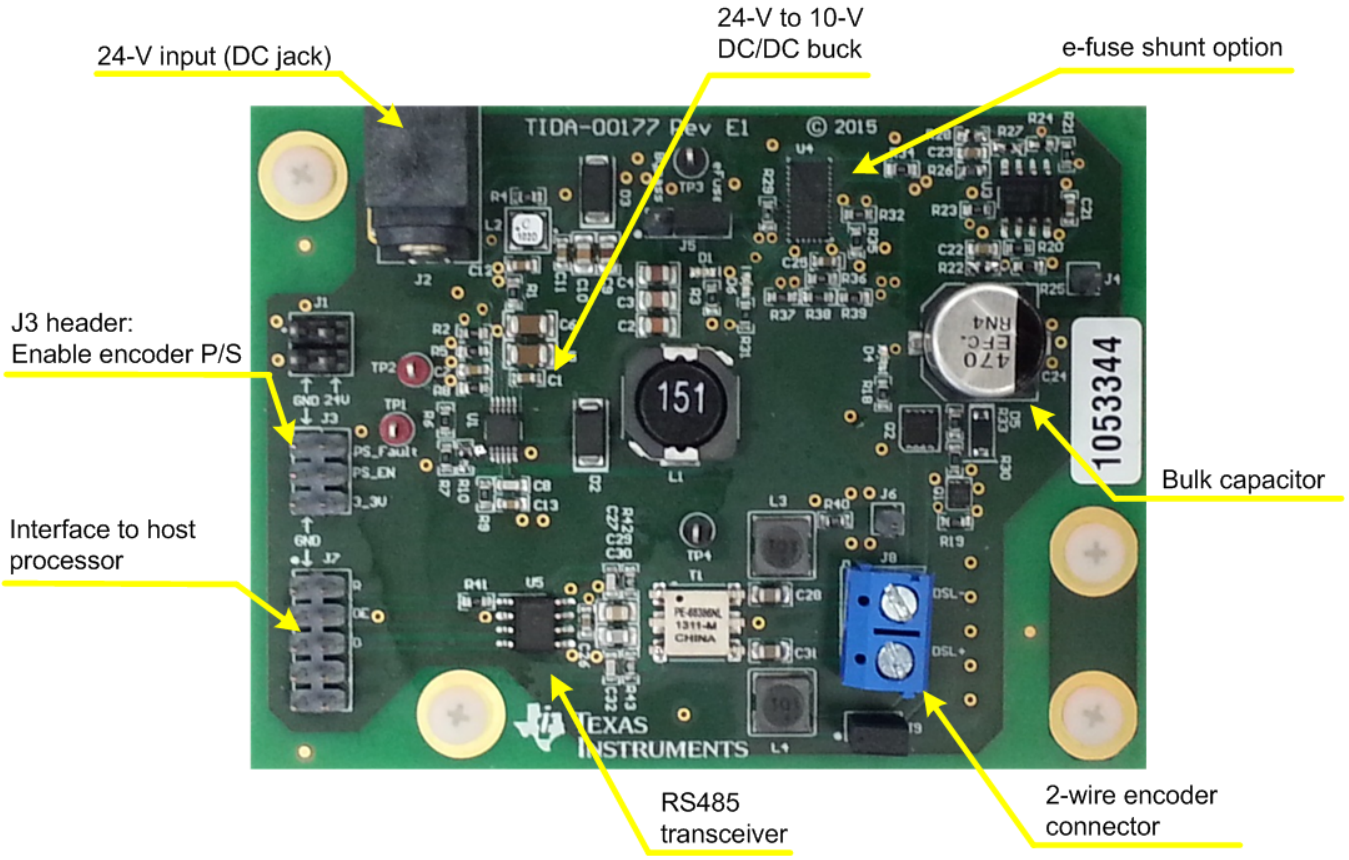


Figure 17. TIDA-00177 Board Picture

The headers and default jumper settings are explained in Section 5.2.

5.2 Connectors and Jumper Settings

5.2.1 Connector and Jumpers Overview

The connector assignment and jumper settings are outlined in Table 14 through Table 18.

The 24-V nominal input voltage can be supplied through either connector J1 or J2.

Table 14. 24-V Input (Terminal; J1)

PIN	DESCRIPTION
1	GND
2	24-V input voltage (18 to 36 V)
3	GND
4	24-V input voltage (18 to 36 V)

Table 15. 24-V Input (DC Jack; J2)

PIN	DESCRIPTION
Internal	24-V input voltage (18 to 36 V)
External	GND

If desired, an external supply voltage other than the 5.25-V encoder supply voltage can be applied through connector J5.

Table 16. Power Supply Monitor and Enable Connector (J3)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	GND	2	PS_Fault (from the eFuse)
3	GND	4	PS_Enable
5	GND	6	3.3 V

Table 17. Host Processor Interface (J7)

PIN	DESCRIPTION	PIN	DESCRIPTION (3.3-V I/O)
1	GND	2	R (RS-485 transceiver)
3	GND	4	DE (RS-485 transceiver)
5	GND	6	D (RS-485 transceiver)
7	GND	8	Not used
9	GND	10	Not used

For detailed signal descriptions on the host processor interface, refer to Section 4.3.

Table 18. DSL Connector (J8)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	DSL+	2	DSL–

5.2.2 Default Jumper Configuration

Prior to working with the TIDA-00177 board, ensure the following default jumper settings are applied. Refer to the board picture in Figure 17 for details.

Table 19. Default Jumpers Settings

HEADER	JUMPER SETTING
J3	Insert a jumper between J3 pins 4-6 to enable the 10.5-V nominal supply for the encoder (optional, not required due to onboard pullup)
J5	Insert a jumper between J5 pins 1-2 to bypass the eFuse; insert a jumper between J5 pins 2-3 otherwise
J9	Insert a jumper between J9 pins 1-2 to enable the two-wire RS-485 configuration, accordingly to HIPERFACE DSL specification.

5.3 Design Evaluation

5.3.1 Prerequisites

The following hardware equipment and software is required to evaluate the TIDA-00177 TI design.

Table 20. Prerequisites

EQUIPMENT	COMMENT
24-V power supply	24-V output power brick with at least a 250-mA output current Output connector 2.1-mm I.D. × 5.5-mm O.D. × 9.5-mm Female
TIDA-00177 hardware	For default jumper settings per Section 6.2
Jumpers for board settings	2 pins, 100 mil
Arbitrary digital pattern generator or any host processor	Use any function generator or a processor that can manage a baud rate of 10 Mbps at least
Two-wire HIPERFACE DSL encoder	

5.3.2 Hardware Setup

Follow these steps:

1. Solder a 10-kΩ pulldown resistor from /DE to GND, like in Figure 18:

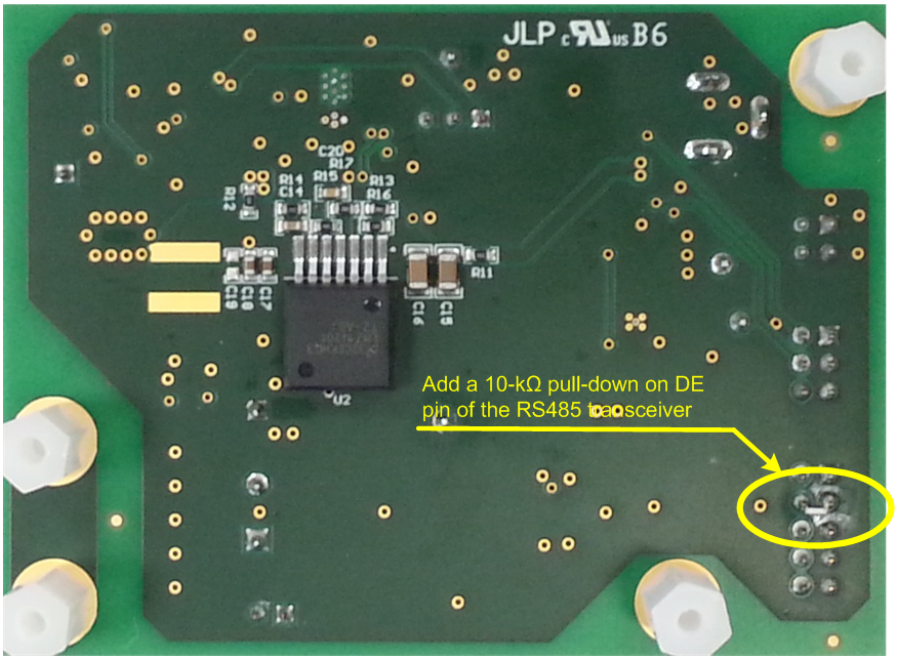


Figure 18. Pulldown Resistor on the DE Pin of the RS-485 Transceiver

2. Verify the TIDA-00177 is configured with the default settings as per Section 5.2.2.
3. Connect a two-wire HIPERFACE DSL encoder to the board by using the connector J8.
4. Connect the TIDA-00177 board to the arbitrary pattern generator (or a processor) by using the connector J7, as per Table 21:

Table 21. TIDA-00177 Host Processor Interface (J7)

J7 PIN	DESCRIPTION	CONNECT TO
1	GND	GND
2	DSL_IN	Data RX
3	GND	GND
4	DSL_EN	Data TX enable
5	GND	GND
6	DSL_OUT	Data TX
7	GND	GND
8	Not used	—
9	GND	GND
10	Not used	—

6 Test Results

As the whole system has been divided in functional blocks, the tests are also divided in the same way to characterize each block performance.

In particular, the following tests have been planned:

- HIPERFACE DSL interface (including 3.3-V PoL)
- HDSL Encoder P/S with protection (eFuse and load/power switch)
- Full system evaluation (tests with the real encoder)

The following equipment has been used for the TIDA-00177 testing session:

Table 22. Test Equipment for TIDA-00177

TEST EQUIPMENT	PART #
Programmable 16-bit waveform generator	Keysight (Agilent) 33600A
Low speed oscilloscope (suitable for power mgt tests)	Tektronix TDS2024B
High speed oscilloscope (suitable for analog signal tests)	Tektronix TDS784C
Adjustable SMPS	Knuerr-Heinzinger Polaris 125-5
24 V @ 2.5-A SMPS (power brick)	V-infinity 3A-621DN24
True RMS multimeter	Fluke 179
Differential probes	Tektronix P6630
Single ended probes	Tektronix P6139A
Programmable thermal chamber	Voetsch VT 4002
Programmable electronic load module	Chroma 63103
Control module for electronic load module	Chroma 6314
Thermal camera	Fluke TI40
Control system loop analyzer	V_{ENABLE} 3120
HIPERFACE DSL encoder	EKM36-0KF0A018A (http://www.sick.com/group/EN/home/Pages/homepage1.aspx)
HIPERFACE DSL integrated motor cable (20 m, 50 m, 80 m, 100 m)	TOPSERV Hybrid PUR 708545 LI9YC11Y 4G2,5 +(2x1,0)C+(2x22AWG)C (http://www.helukabel.de/en/en/home.html)
HIPERFACE DSL Programming Tool and Analyzer PGT-09-S	PGT-09-S (http://www.sick.com/group/EN/home/Pages/homepage1.aspx)

NOTE: Whenever not mentioned, the tests have been performed at ambient temperature around 22ºC.

6.1 Two-Wire HIPERFACE DSL Interface

To test the communication interface, a dual output signal or function generator could be used.

One channel is configured as a clock at 9.375 MHz, while the other channel as arbitrary digital sequence generator, at the same bit/rate (9.375 Mbps).

Rise and fall times are set at 4 ns (max).

6.1.1 Eye Diagram versus Cable Length With Two-Wire Interface (Including Power)

Eye diagrams are measured at the cable far end at the differential input of the RS-485 transceiver. For that purpose, another TIDA-00177 (on that board with 10.5 V disabled) was used to terminate the line at the cable far end.

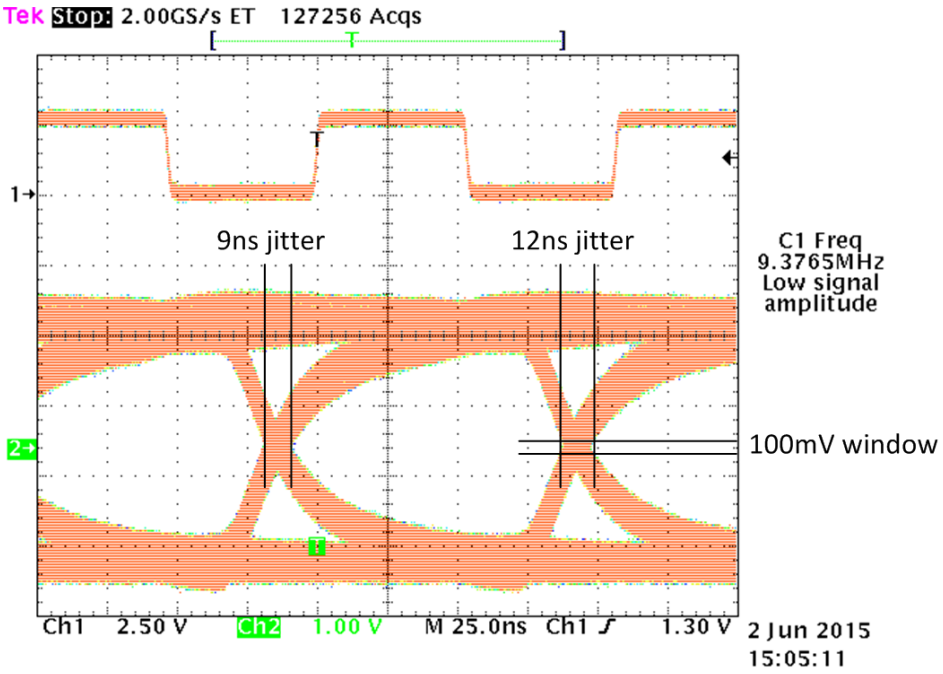


Figure 19. Eye Diagram Far End RS485 Receiver With 100-m Cable

Measured jitter is 9 ns at worst case, while the eye diagram aperture (considering a worst case detection window of 100 mV) is 12 ns, which is equivalent to 11.3% (88.7% UI-open worst case).

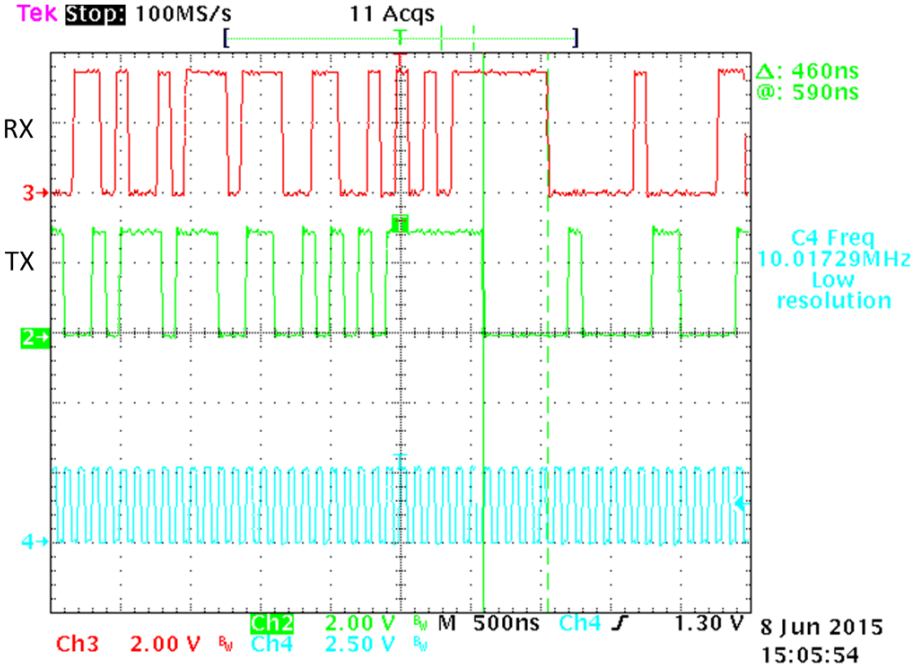


Figure 20. Eye Diagram Far End RS-485 Receiver With 80-m Cable

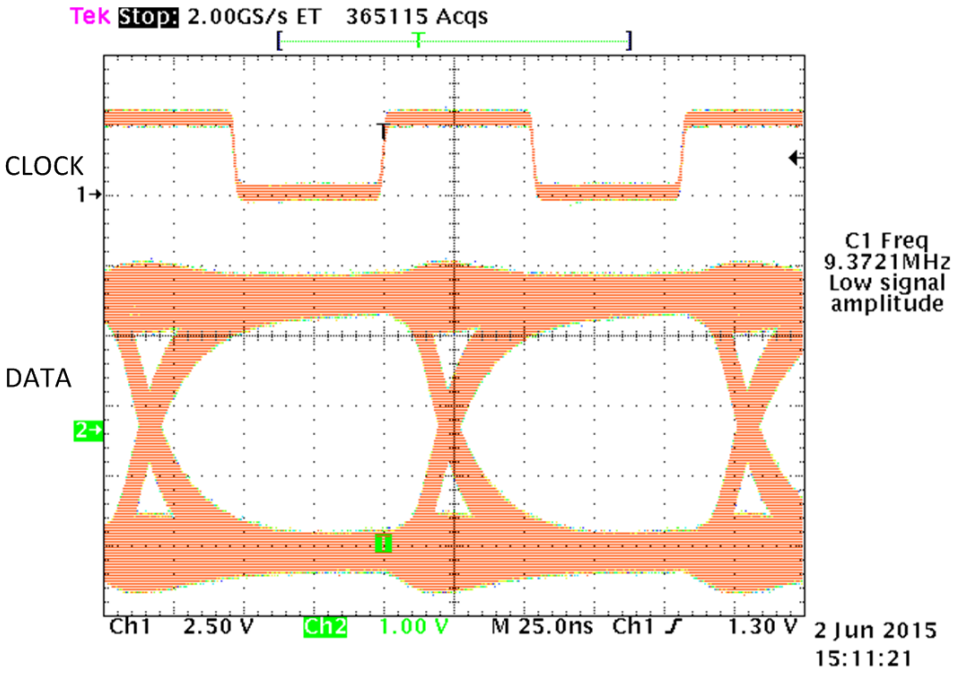


Figure 21. Eye Diagram Far End RS-485 Receiver With 50-m Cable

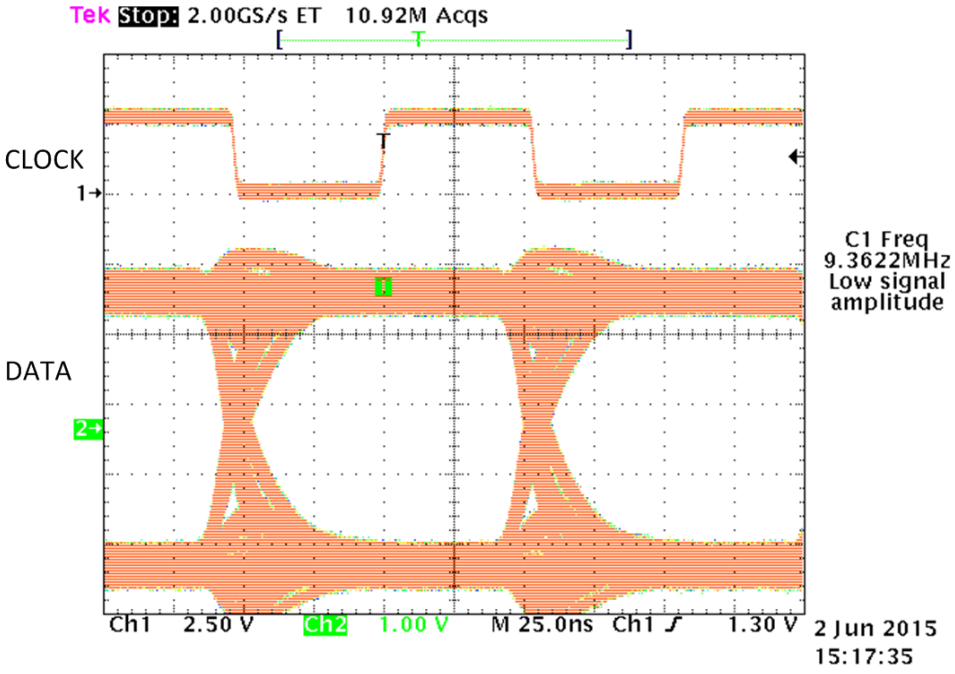


Figure 22. Eye Diagram Far End RS-485 Receiver With 20-m Cable

The jitter of the received differential-NRZ random data at the cable far end with 120-Ω termination at the baud rate of 9.375 MHz is typically less than 10% (0.90 UI-open).

6.1.2 Signal Integrity

Tests were done with 20 m with line termination (as in Section 6.1.1).

Receive

Figure 23 clearly shows how the data are modulated on the supply line of the encoder at the receiver side. Indeed, the DC levels of the data stream are respectively 0 V (DSL–) and 10.5 V (DSL+).

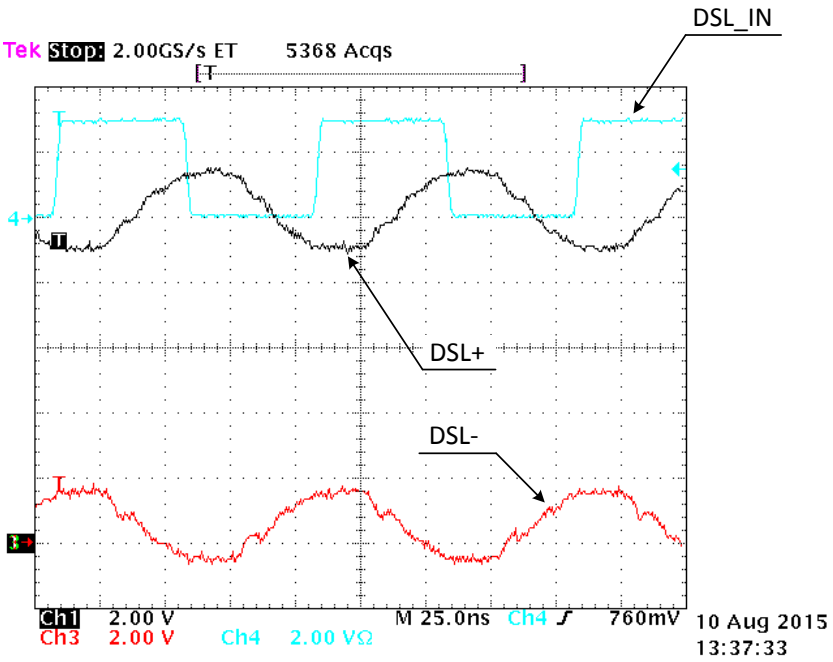


Figure 23. Receive Mode With 20-m Cable—Propagation Delay DSL_IN versus DSL+ and DSL–

Figure 24 shows the AC coupled signal on the secondary side of the transformer used to decouple the power rail from the TTL level signals.

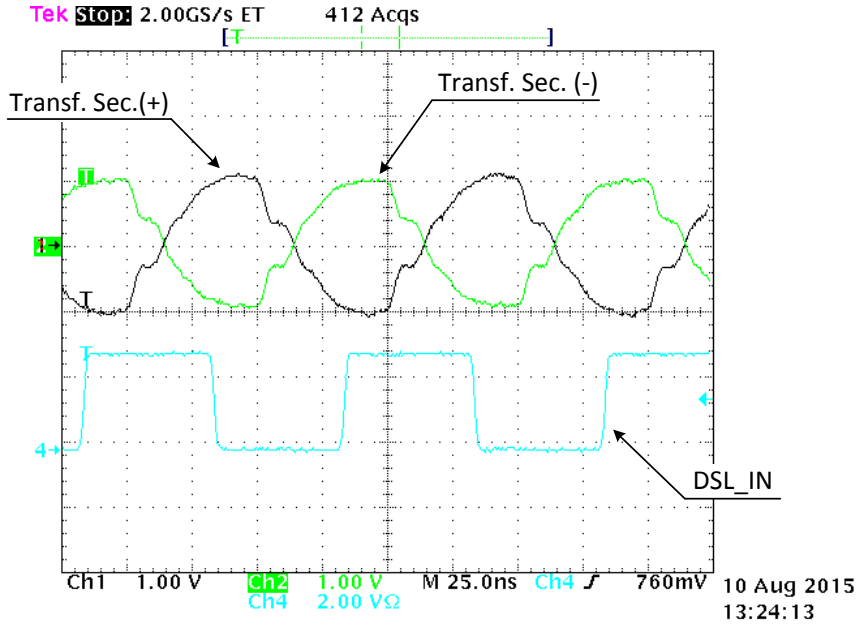


Figure 24. Receive Mode With 20-m Cable—Propagation Delay DSL_IN versus Transformer Secondary

Figure 25 shows the output signal of the RS-485 transceiver (A and B) at the receiver side.

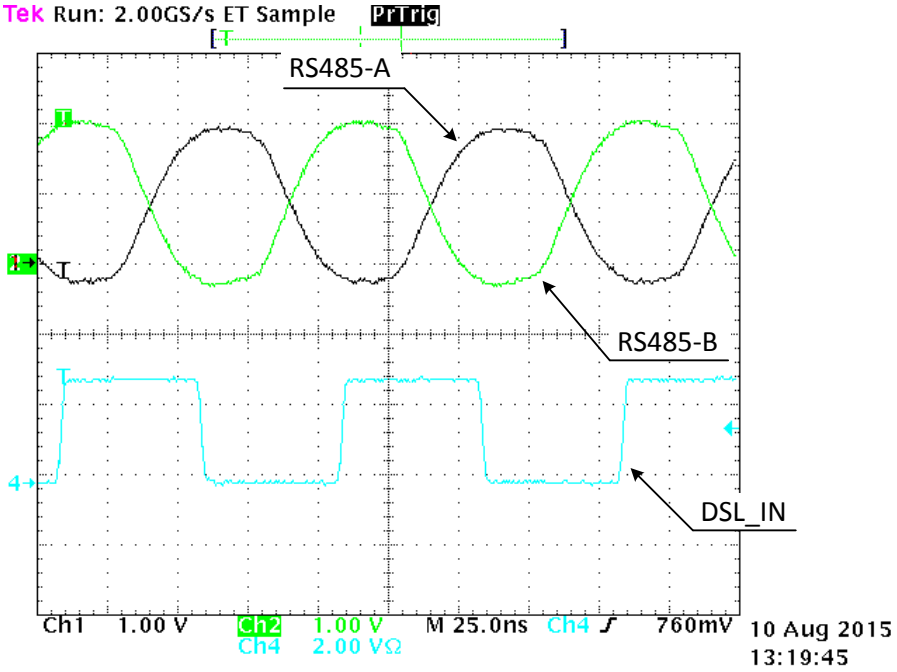


Figure 25. Receive Mode With 20-m Cable—Propagation Delay DSL_IN versus RS485 A-B

Transmit

Figure 26 shows the A and B output signal of the RS-485 transceiver at the transmitter side, while DSL_OUT is the transmitted pattern. The previous one is also possible to measure the propagation delay of the SN65HVD78 in the range of 7 to 8 ns.

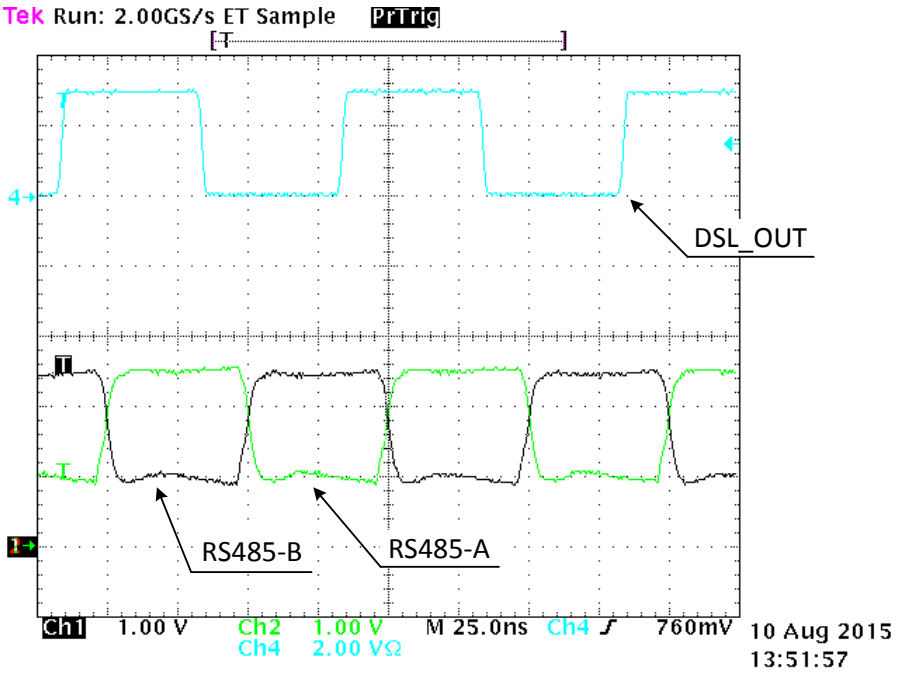


Figure 26. Transmit Mode With 20-m Cable—Propagation Delay DSL_OUT versus RS485 A-B

Figure 27 shows the AC coupled signal on the secondary side of the transformer used to decouple the power rail from the TTL level signals at the transmitter side.

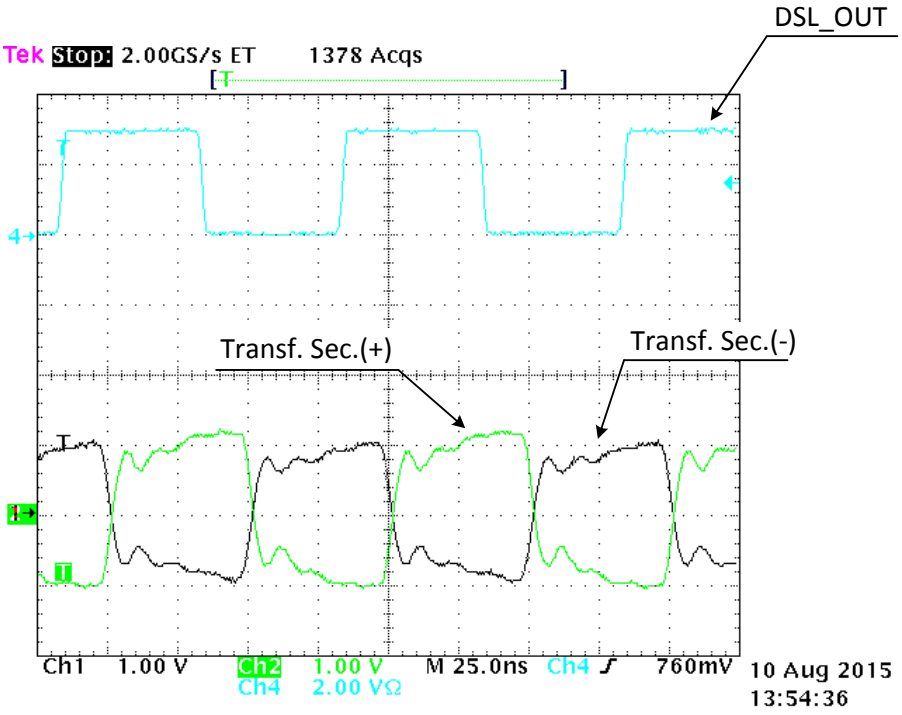


Figure 27. Transmit Mode With 20-m Cable—Propagation Delay DSL_OUT versus Transformer Secondary

Figure 28 clearly shows how the data are modulated on the supply line of the encoder at the transmitter side. Indeed, the DC levels of the data stream are respectively 0 V (DSL–) and 10.5 V (DSL+).

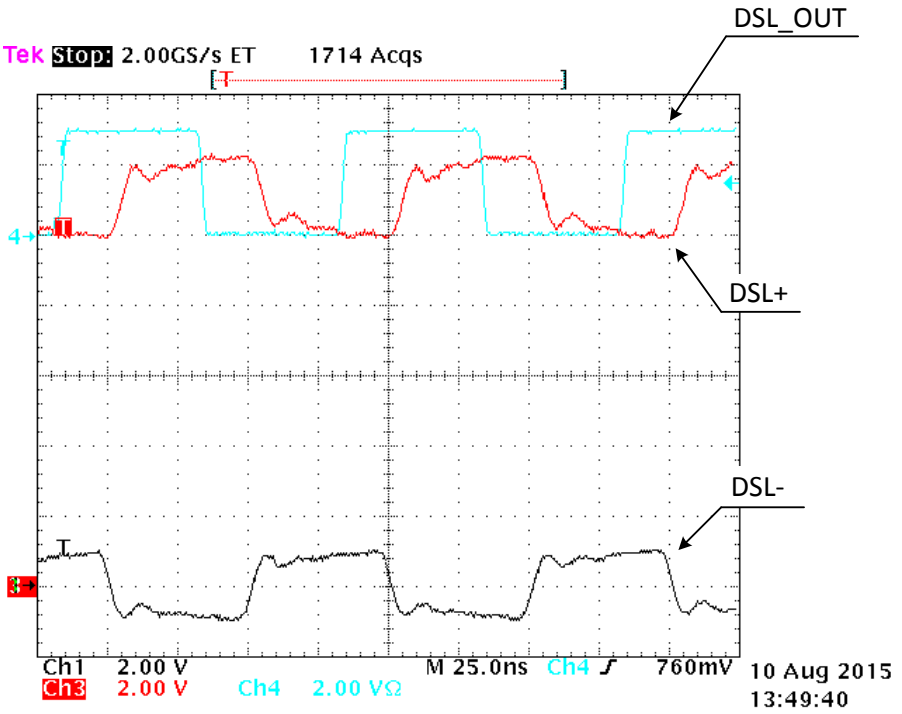


Figure 28. Transmit Mode With 20-m Cable—Propagation Delay DSL_OUT versus DSL+ and DSL–

6.1.3 Signal Integrity Test—Communication Among Two TIDA-00177 Boards

These tests consist in using two TIDA-00177 boards, one transmitting data and the other receiving. The data pattern at TX and RX are compared to check no data transmission occurs. The two boards have been connected through the DSL interface with a cable.

The TX master board is used as it is while the RX one is configured in a way to avoid conflicts on the power bus. In particular, J9 is left open and the resistor R40 has been removed at the receiver side (refer to Section 7.1 for details).

Transmission occurs at 9.375 MHz. A random pattern has been generated with a programmable signal generator; the same patter has been recognized at the receiver side.

NOTE: The clock is used only for baud rate check.

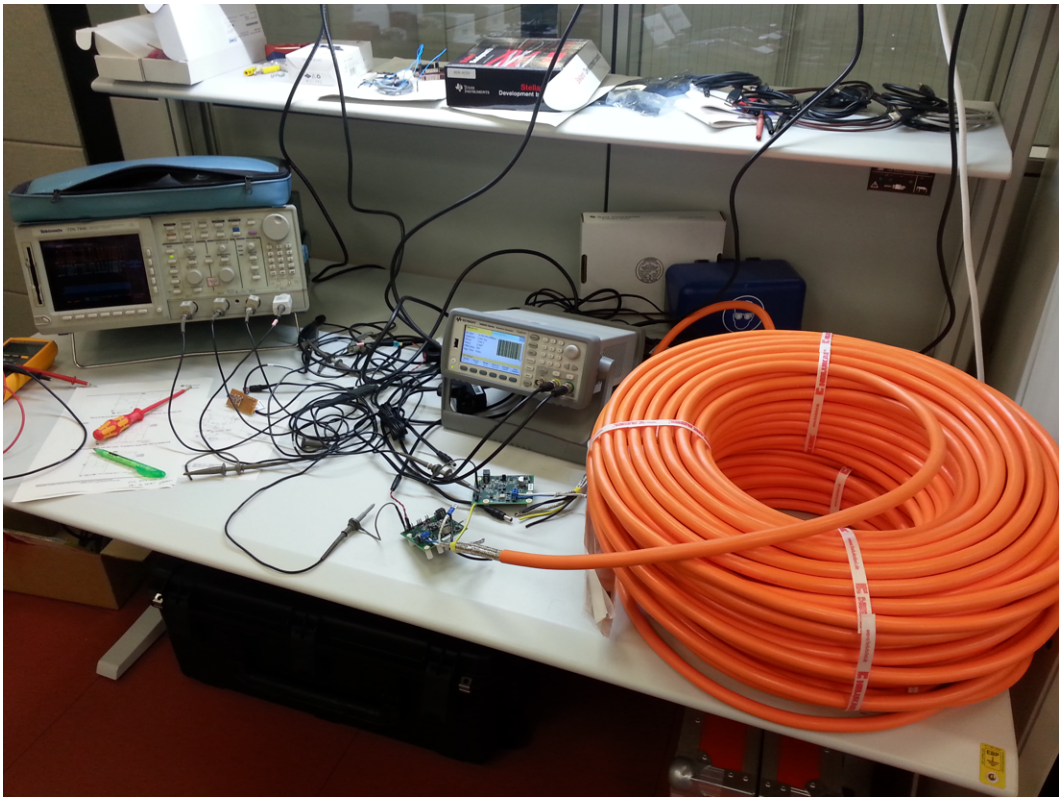


Figure 29. Signal Integrity and Communication Test Setup

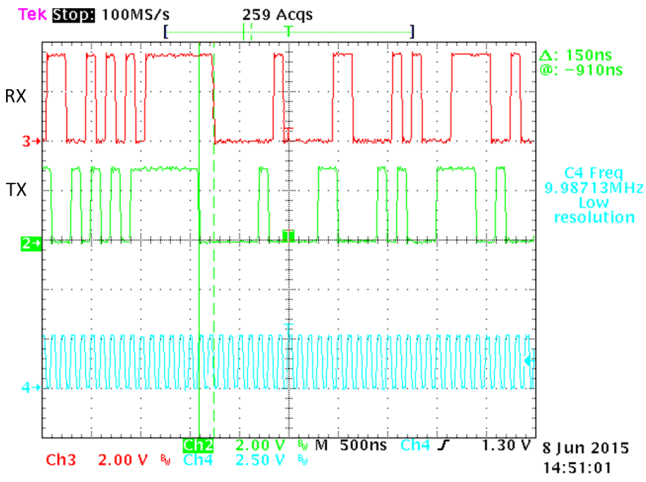


Figure 30. Propagation Delay Over 20-m Cable

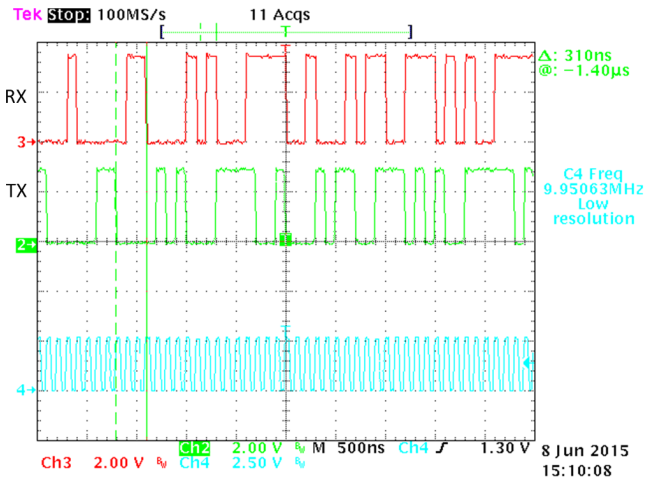


Figure 31. Propagation Delay Over 50-m Cable

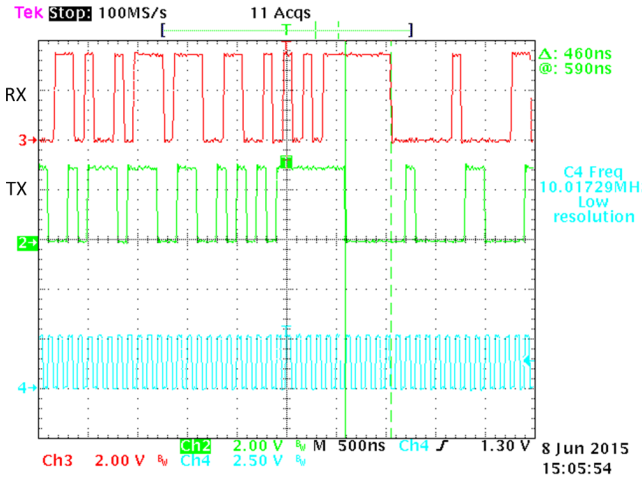


Figure 32. Propagation Delay Over 80-m Cable

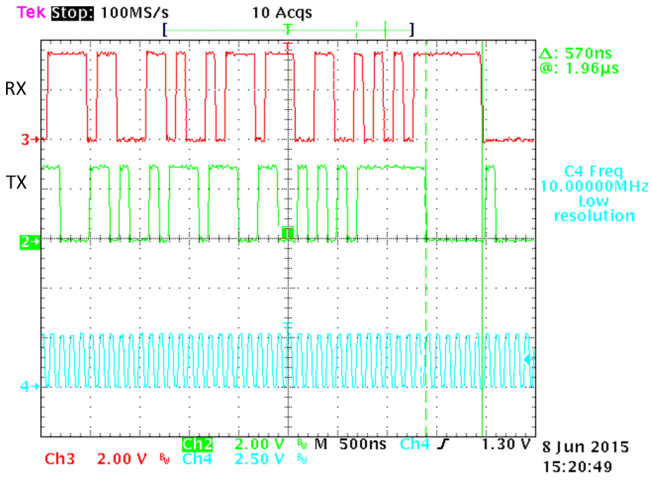


Figure 33. Propagation Delay Over 100-m Cable

The delay introduced by the electronic could be separated by the one due to the cable:

Table 23. Contributions of Various Parts to Total Propagation Delay

CABLE LENGTH	TOTAL DELAY	CABLE DELAY	TX BOARDS DELAY	RX BOARDS DELAY
20 m	150 ns	5.22 ns/m	≈ 33 ns	≈ 13 ns
50 m	310 ns	5.22 ns/m	≈ 33 ns	≈ 13 ns
80 m	460 ns	5.22 ns/m	≈ 33 ns	≈ 13 ns
100 m	570 ns	5.22 ns/m	≈ 33 ns	≈ 13 ns

The communication has been tested in both directions (half-duplex). Previously, the master was the transmitter and providing the power over the DSL bus. Now the slave is transmitting and using the power bus provided by the master (set in receiving mode).

Figure 34 through Figure 36 provide the results of the tests with a 20-m long cable:

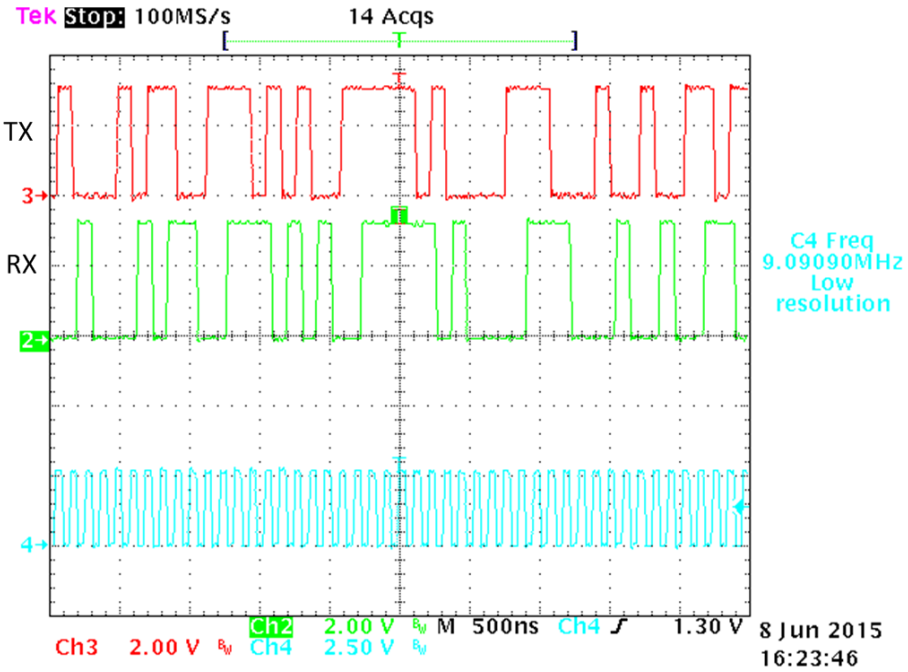


Figure 34. Random Data Pattern Transmission Test Results #1

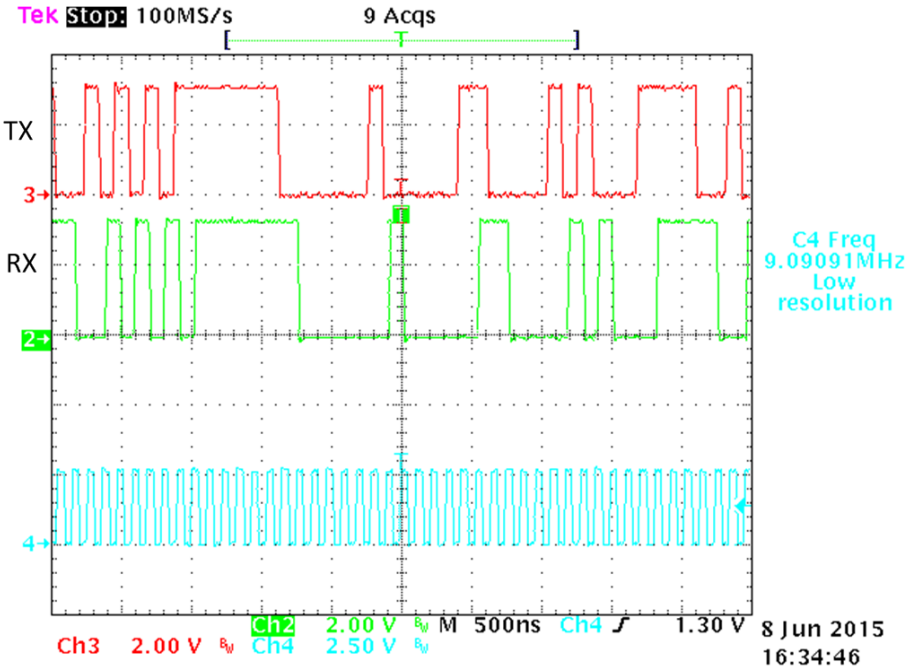


Figure 35. Random Data Pattern Transmission Test Results #2

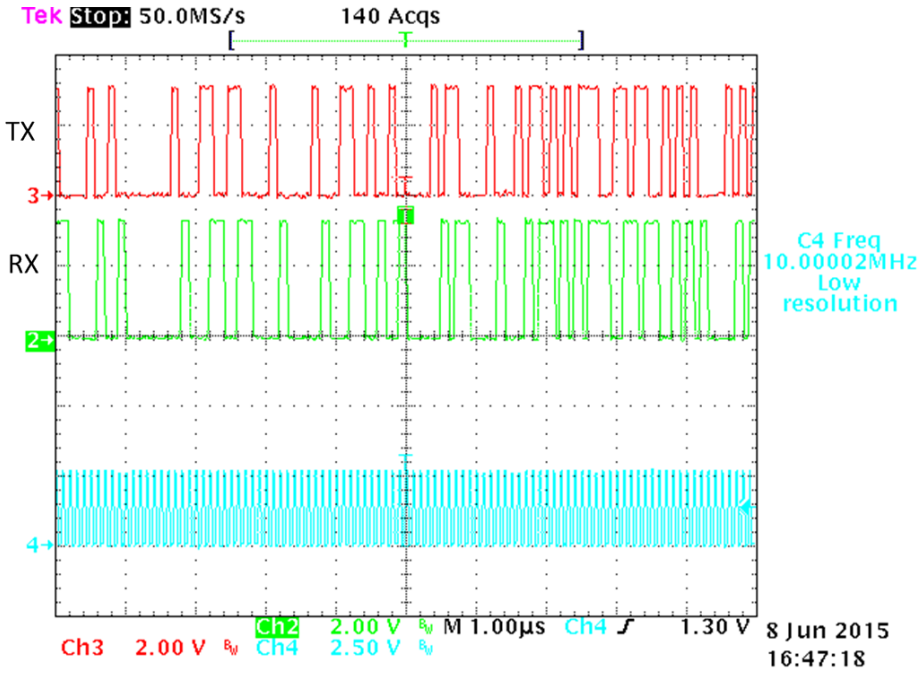


Figure 36. Random Data Pattern Transmission Test Results #3

NOTE: Not providing proper termination on the DE line cause transmission errors.

6.2 DC/DC Buck and Load Switch

This section verifies the subsystems DC/DC power supply (24 to 10.5 V) and the switching threshold of the load switch. The entire HIPERFACE DSL power supply including protection is tested in Section 6.3.1.

6.2.1 TPS5401 (24 to 10.5 V) DC/DC Buck

The main tests performed related to:

- Start-up
- Ripple and regulation
- Stability
- System efficiency

For the purpose of power management section tests, the jumper J5 is left unpopulated so the eFuse and the other circuits are not engaged.

Note that by changing setting on the jumper, J5 is possible to bypass the eFuse TPS24750.

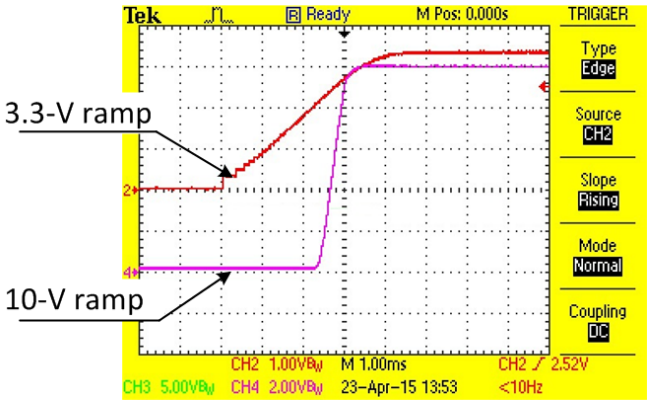


Figure 37. 10.5-V and 3.3-V Start-up at 24-V Input

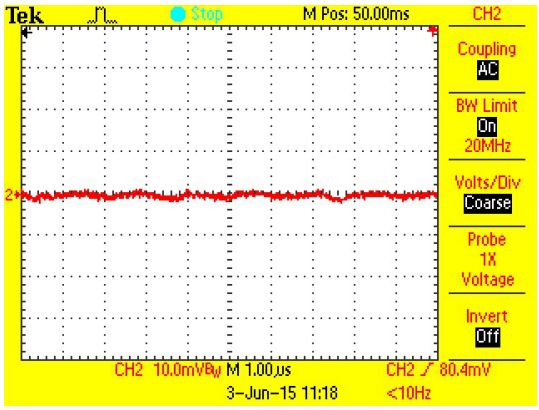


Figure 38. Output Voltage Ripple at 10.5 V With 24-Vin No Load

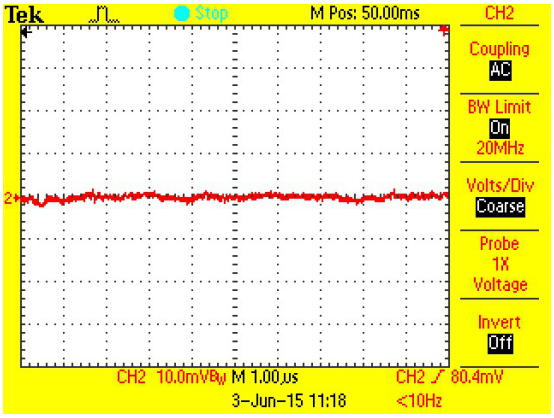


Figure 39. Output Voltage Ripple at 10.5 V With 24-V_{IN} Full Load

In any working condition, the voltage ripple of the 10.5-V rail is lower than 10 mV_{PP}.

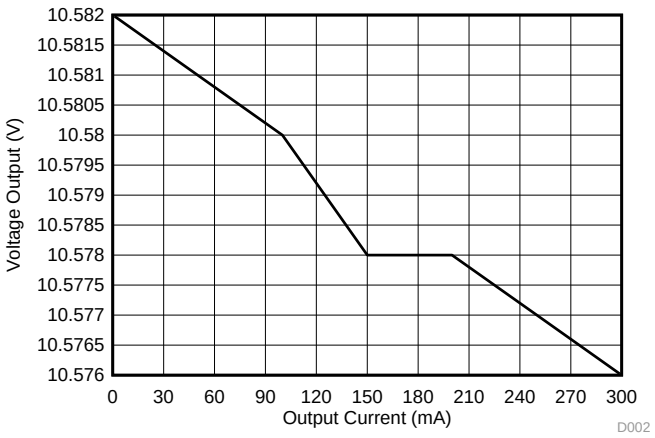


Figure 40. Load Regulation for 10.5-V Rail

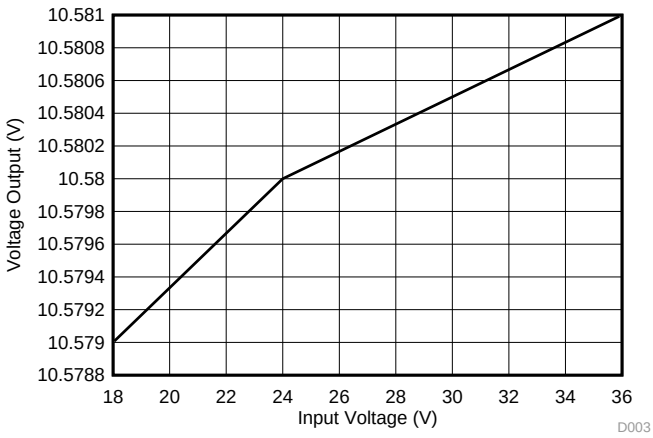


Figure 41. Line Regulation for 10.5-V Rail

The DC level of the 10.5-V rail is into the range of ±2% in any working conditions.

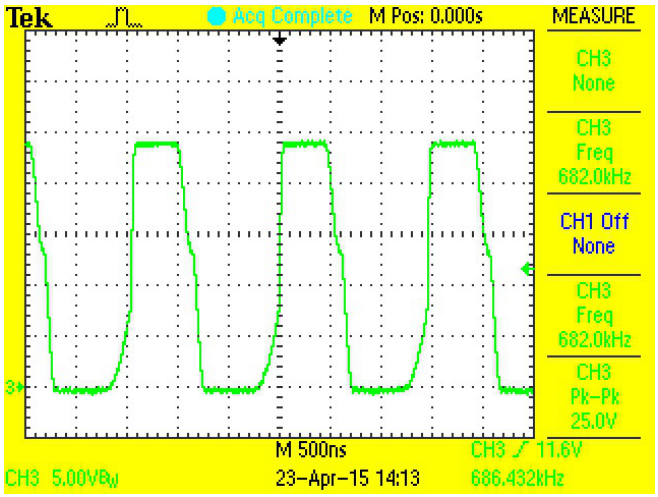


Figure 42. Switching Frequency of TPS5401 at 24-V Input, No Load

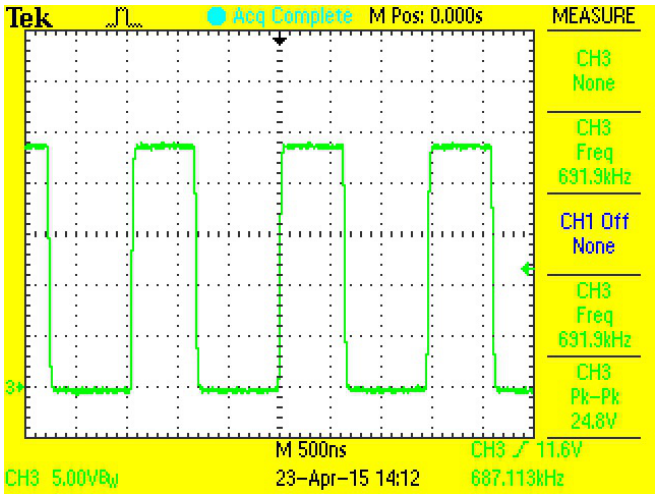


Figure 43. Switching Frequency of TPS5401 at 24-V Input, Full Load

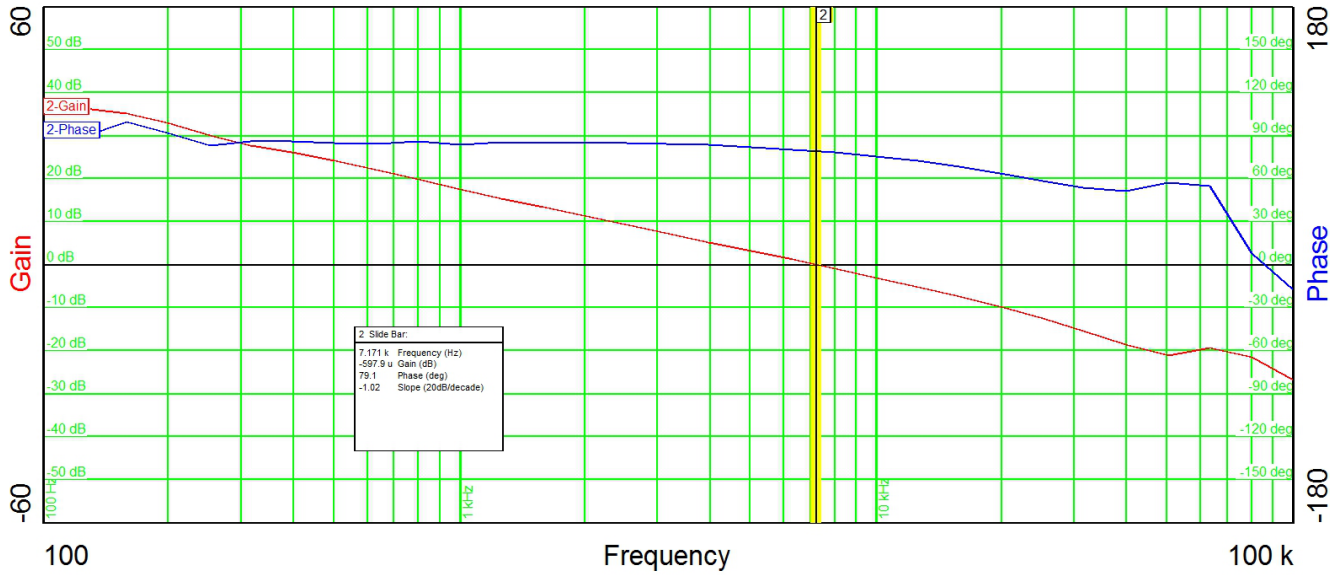


Figure 44. Gain Loop of TPS5401, 24-V Input, Full Load

The system is well designed with a crossover frequency of ≈ 7 KHz and a good phase margin (> 60 degrees) in all the working conditions:

Table 24. Summary of Gain Loop Response for 10.5-V Rail

INPUT VOLTAGE (V)	CROSS-OVER FREQUENCY (KHz)	PHASE MARGIN (DEGREES)
18	6.8	75
24	7.2	79
36	7.5	81

Because of the very low output current, thermal tests have not been leaded (there is no reason to expect any thermal stress for any part at 85 degrees).

From an efficiency point of view, the full system losses have been measured (without transmission) because it makes no sense to split the contribution of the various parts:

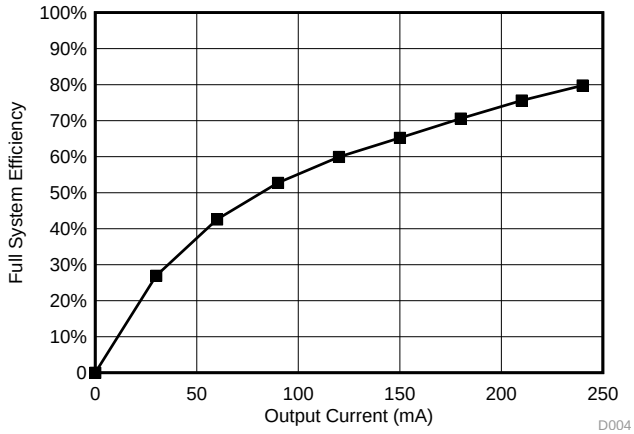


Figure 45. Total System Efficiency versus Output Current

6.2.2 3.3-V PoL

The quality of the regulation for the 3.3-V PoL, performed by the LMZ14201 module has been tested as well:

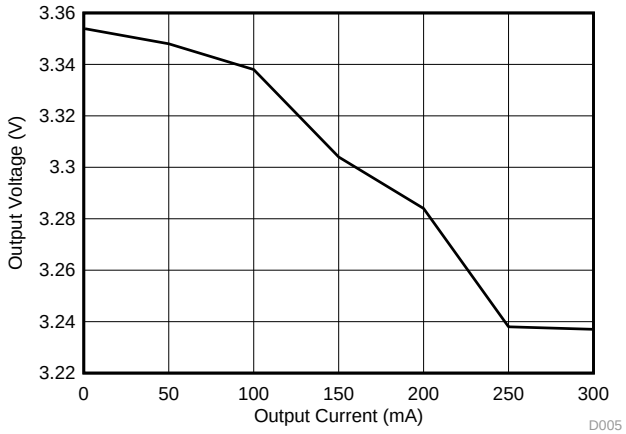


Figure 46. 3.3-V PoL Load Regulation

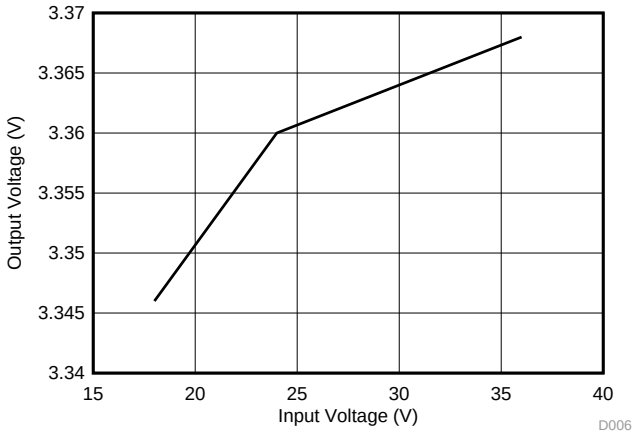


Figure 47. 3.3-V PoL Line Regulation

The typical current consumption for a continuous 9.375-MHz data transfer is around 45 mA.

6.2.3 Switching Threshold of Load Switch

In this section, the behavior of eFuse and power switch are evaluated. First of all, the accuracy of the thresholds of the comparator with hysteresis are verified. For this purpose, the resistor R34 is removed and a slowly variable signal is applied to J5.1. A dummy load of 1 kΩ is applied on the output after the switch Q2 (between J6 and J9.2), where the voltage is monitored. In this way, the two thresholds at which the comparator swings are detected. In particular:

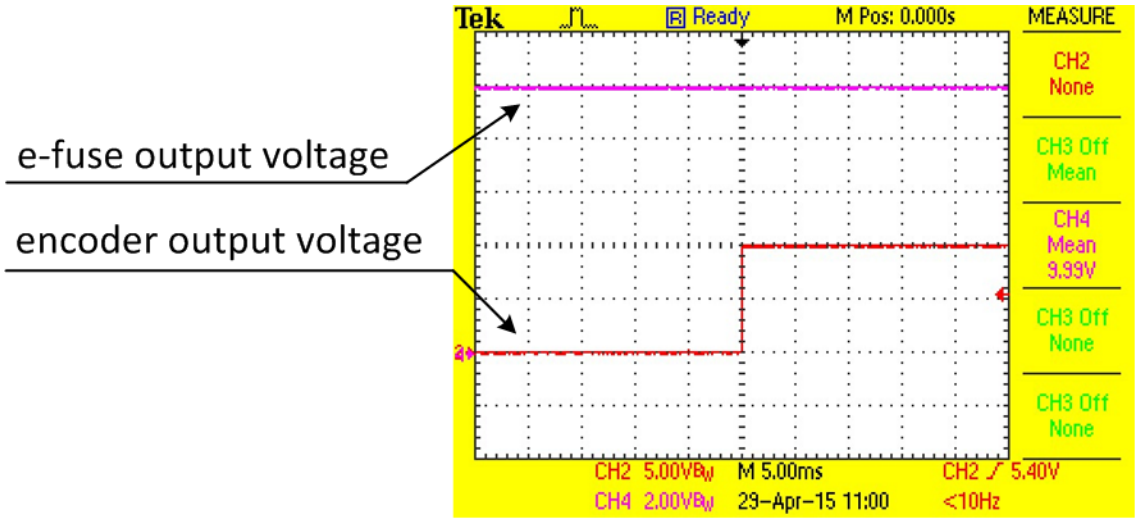


Figure 48. Comparator Rising Threshold at 10.0 V

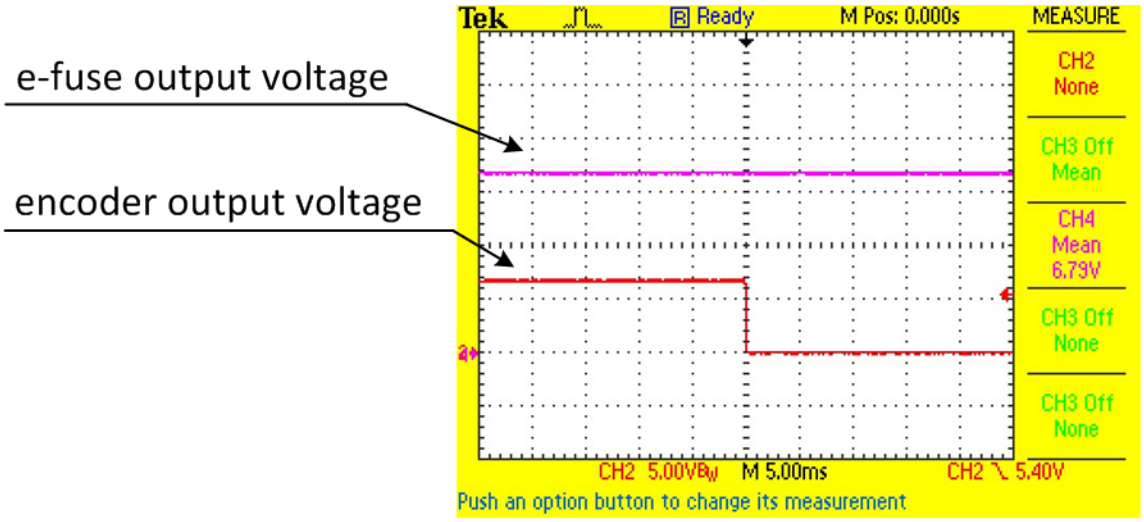


Figure 49. Comparator Falling Threshold at 6.8 V

At this point, the resistor R34 could be set back and the jumper J5 configured to apply the 10.5-V nominal power rail to the eFuse (J5.1-J5.2 in short).

6.3 System Level Tests

6.3.1 HIPERFACE DSL Encoder P/S Tests With Load Emulation

The system is then tested under the described setup:

- Jumper J5 shorting pins 2 and 3
- 24-V input is applied

The following waveforms are grabbed:

- V_{OUT_NP} CH4 in the scope plots
- $V_{\_pr}$ CH3 in the scope plots
- V_{enc} CH2 in the scope plots
- I_{OUT} (from V_{enc} pin, or on top of R_{peak}) CH1 in the scope plots

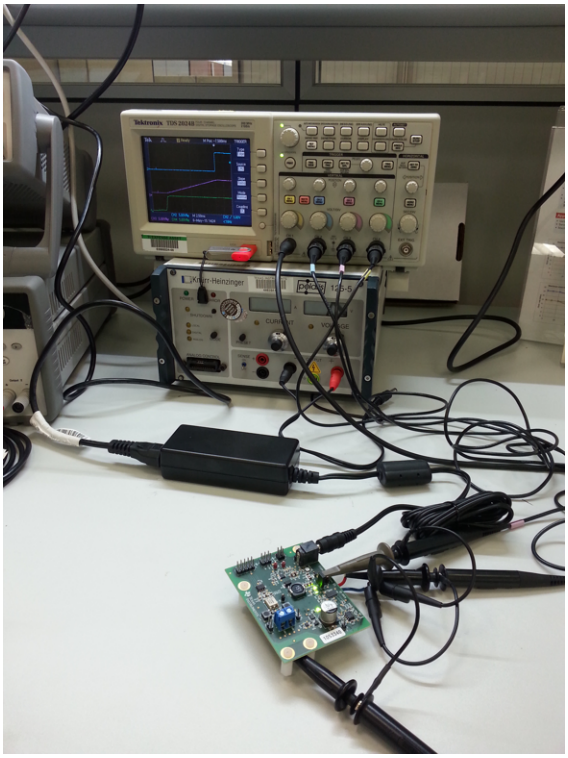


Figure 50. System Level Test Setup

The first test performed is the "normal operation mode", or the start-up with little load. Results have been:

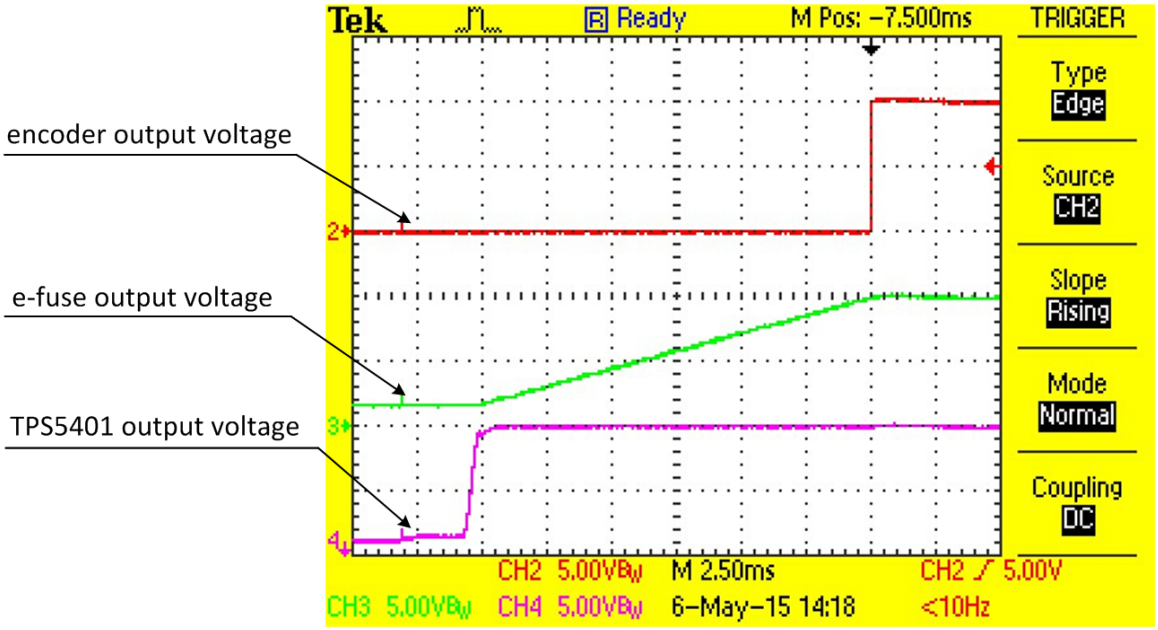


Figure 51. Start-up With Light Load Output (< 10 mA)

Then the start-up tests with current profile emulator, as explained in Section 4, were performed.

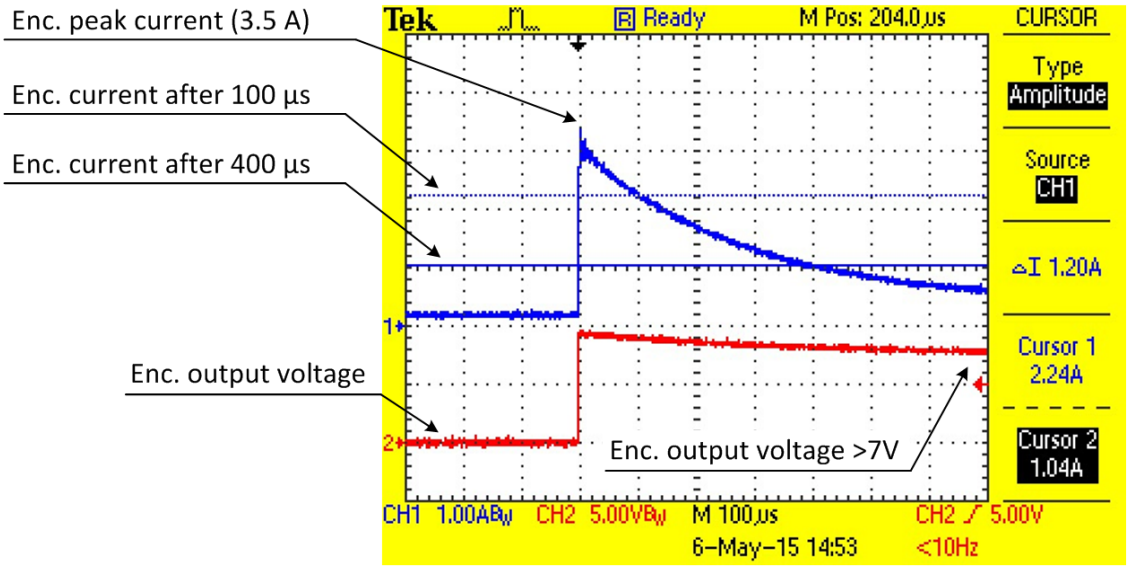


Figure 52. Output Current Profile With Encoder Current Profile Emulator

From the previous waveforms, it can be seen how:

- The peak current specification is fully met (3.44 A)
- The steady-state output voltage (after the inrush current has finished) is above the minimum required voltage (7.6 V > 7 V)
- The current delivered after 100 µs is higher than 2 A (2.24 A)
- The current delivered after 400 µs is higher than 1 A (1.04 A)

This means the TIDA-00177 fully met the required specifications.

A different load emulator has then been tested; in particular, with reference to Figure 12, where the values R_{peak} = 0, R_{steady} = 70 Ω, and C_{timer} = 3 × 22-µF ceramic capacitors are used.

The purpose of this test is to check the worst case peak current (R_{peak} = 0) when a real encoder load is applied (R_{steady} ≈ 70 Ω // 50 µF).

The following results have been achieved:

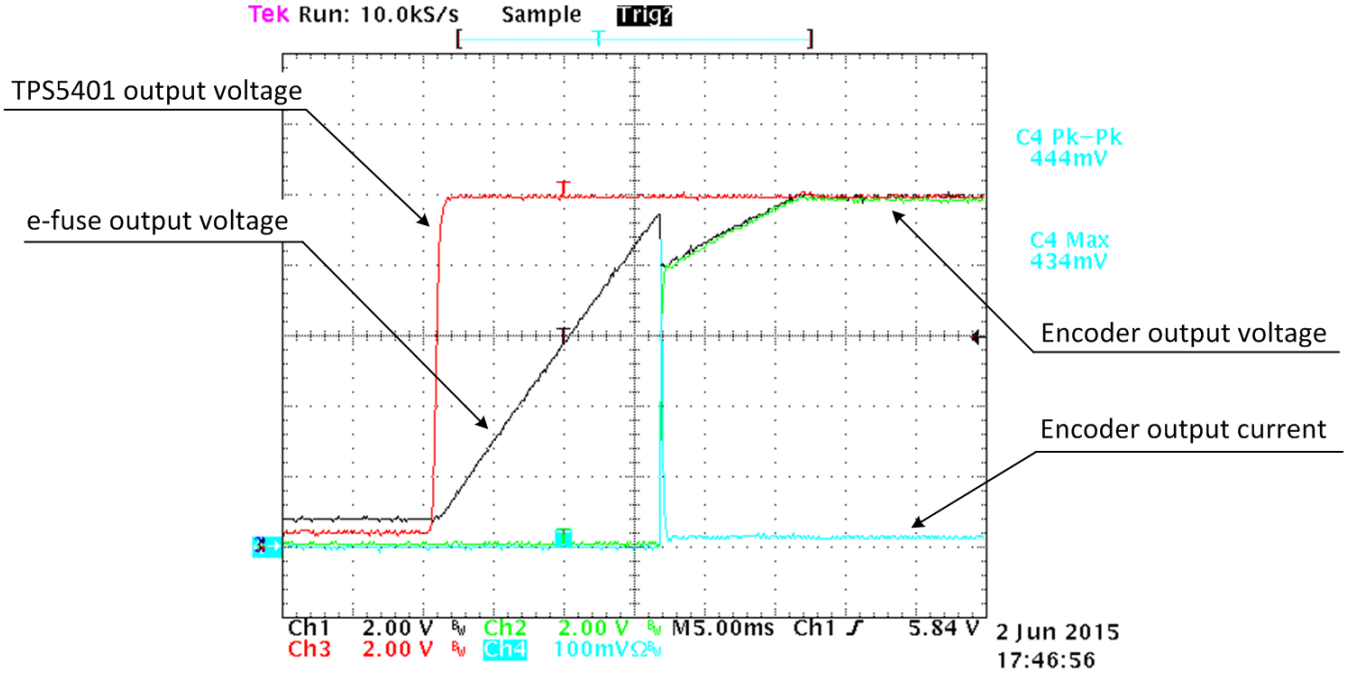


Figure 53. Start-up Current Profile With Load Emulator (70 Ω // 68 µF)

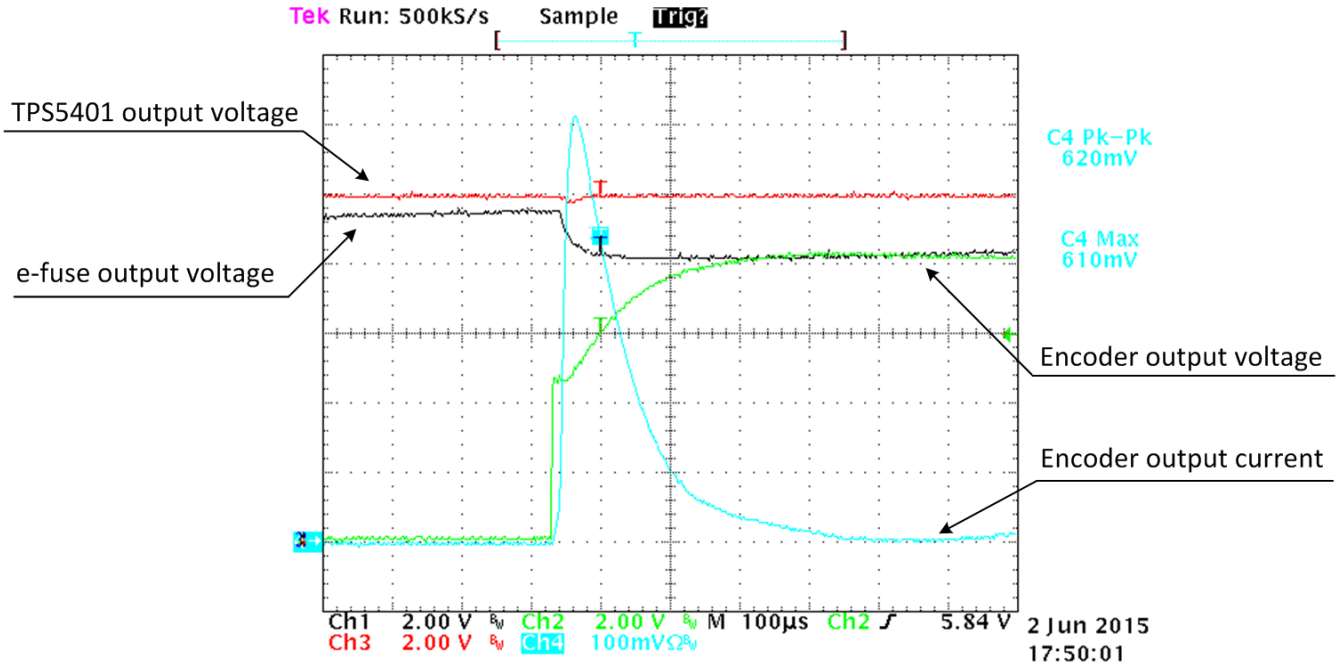


Figure 54. Start-up Current Profile With Load Emulator (Zoom)

NOTE: Note that the current probe has now an attenuation of 10:1, meaning the detected peak current is around 6 to 6.5 A.

The following types of protection:

- UVP: This is performed by both the eFuse and the TPS5401 (UVLO/enable threshold). This is not tested here because these are IC featuring, not system level features.
- OVP: Similar to UVP, but this time only the eFuse performs the protection.
- OCP: This is also performed by the eFuse that has been set in the system to limit the current at 250 mA nominal. This test could be easily performed by reducing the resistance of the load emulator to trigger the OCP level of the TPS27450.
- SCP: This is the main feature of the system protection (in case of system failure, no current is provided to the encoder or output). This is also performed by the eFuse through its fast-trip shutdown feature (that is, when the voltage across the R_{SENSE} resistor exceeds 60 mV, meaning a 600-mA current).
- OTP: This feature also, being IC related, is not tested at system level.

OCP Test Results

The overcurrent protection has been simply tested applying an electronic load on the system output and slowly increasing the output current until the OCP of the eFuse is triggered.

This occurs at around a 235-mA current load (= 250 mA nominal ±10% on the I_{LIM} comparator):

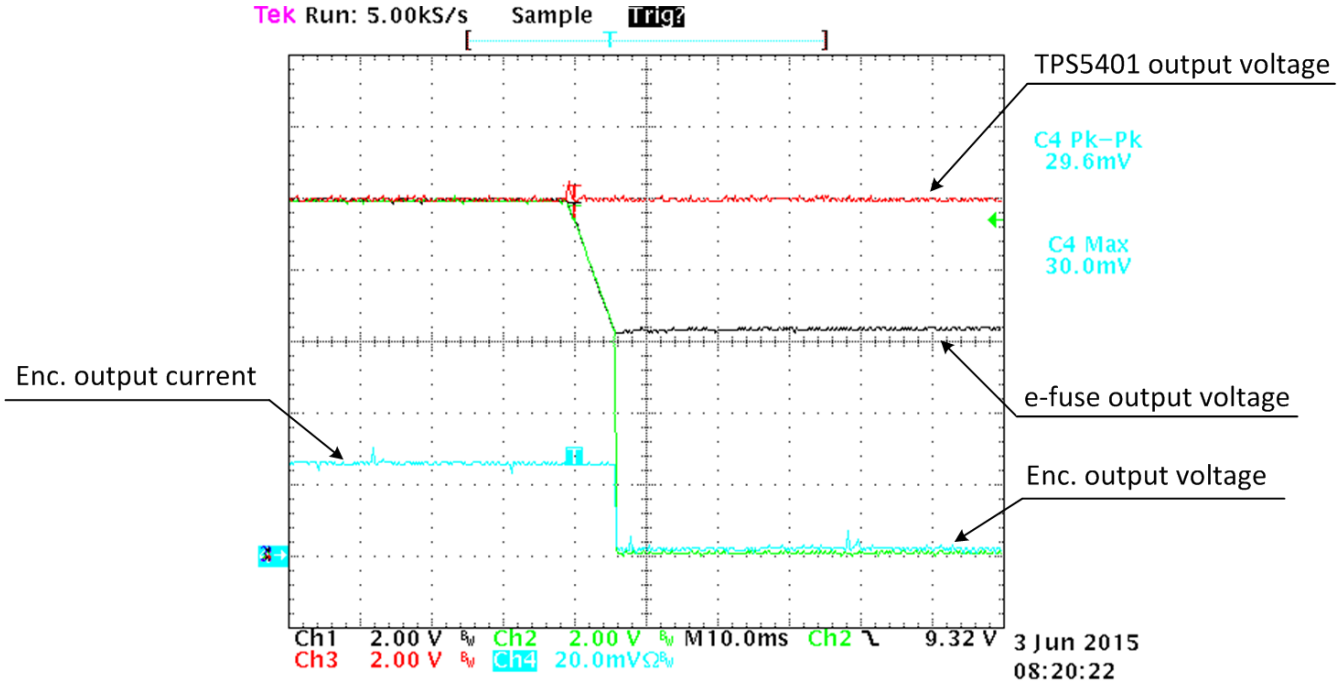


Figure 55. Main Voltages Profile When Output Current Slowly Increases up to 250 mA

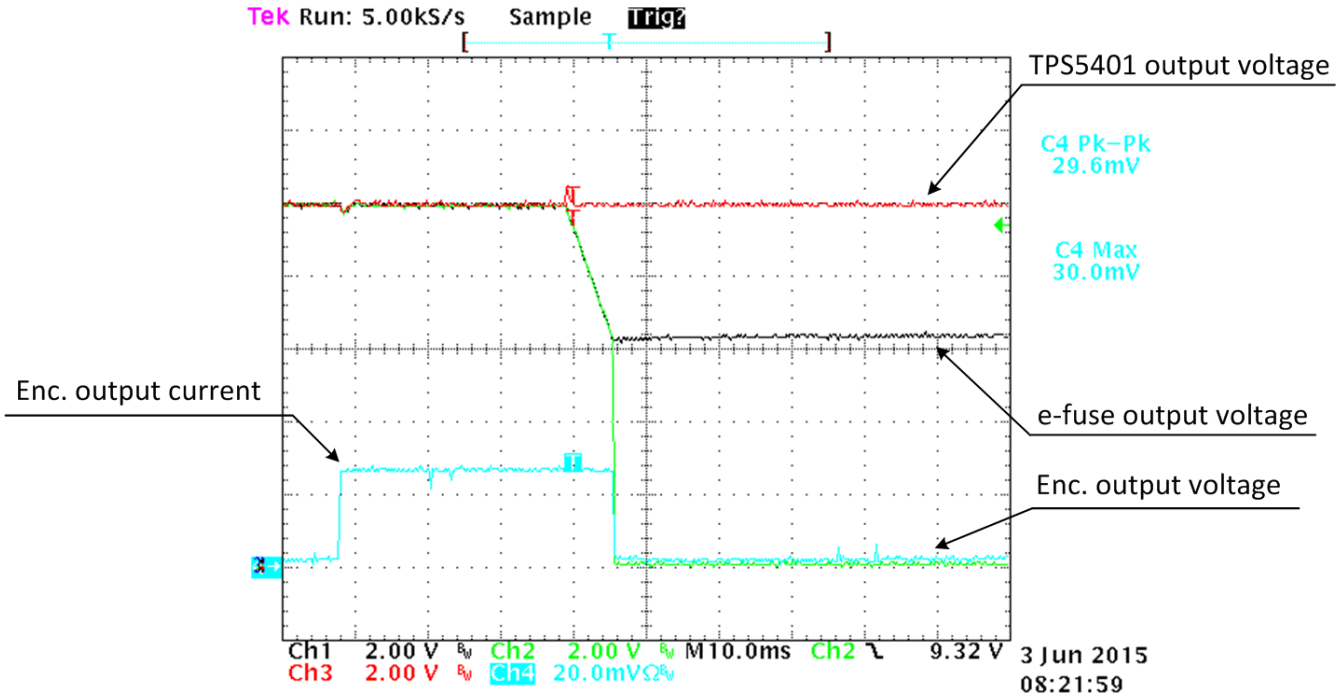


Figure 56. Main Voltages Profile After 250-mA Current Load is Suddenly Applied

The observed behavior is that when the output current exceeds the limit sets by the eFuse the output voltage (that is held by the big bulk capacitor) drops down until the lower threshold of the load switch comparator turns it off. Again, the eFuse triggers the OCP event 30 ms, in according to C_{timer} settings.

NOTE: Act on R35 to increase the OCP threshold, accordingly to the equation R35 = 330 V / I_{LIM}, so that 1K could be used to set ILim = 330 mA.

Short-Circuit Protection Test Results

The short-circuit protection could be tested in two ways: applying a real short circuit on the output, or still using the electronic load with a 1-A current (>0.6-A fast trip threshold) directly on the output and then let the system to start up with a 1-A load.

Again, the SCP is triggered by the eFuse that latches and opens the input-to-output connection:

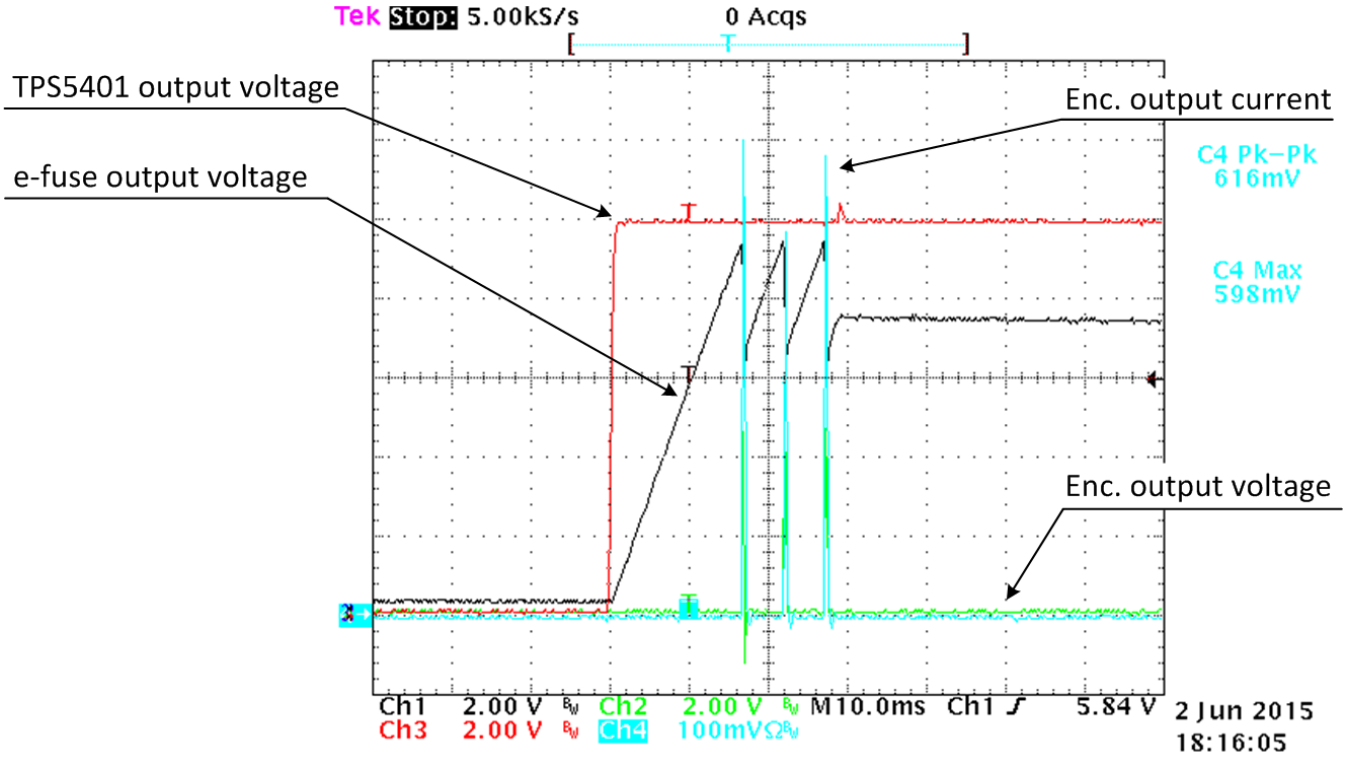


Figure 57. Start-up With Short Circuited Output With eFuse

In the previous figures, after 10.5 V has ramped up and the eFuse has been enabled, the output bulk capacitor is charged. At this point, the load switch turns on shunting the previous cap.

At this point, the voltage drops below 7 V and the load switch turns off. Since less than 30 ms have been passed, the output cap charges again and process repeats. After 30 ms, the eFuse latches the OCP (fast trip) /SCP and keeps permanently off the system. At this point, a power cycle is required to clear the fault.

If the eFuse is bypassed, then the behavior of the system is the following:

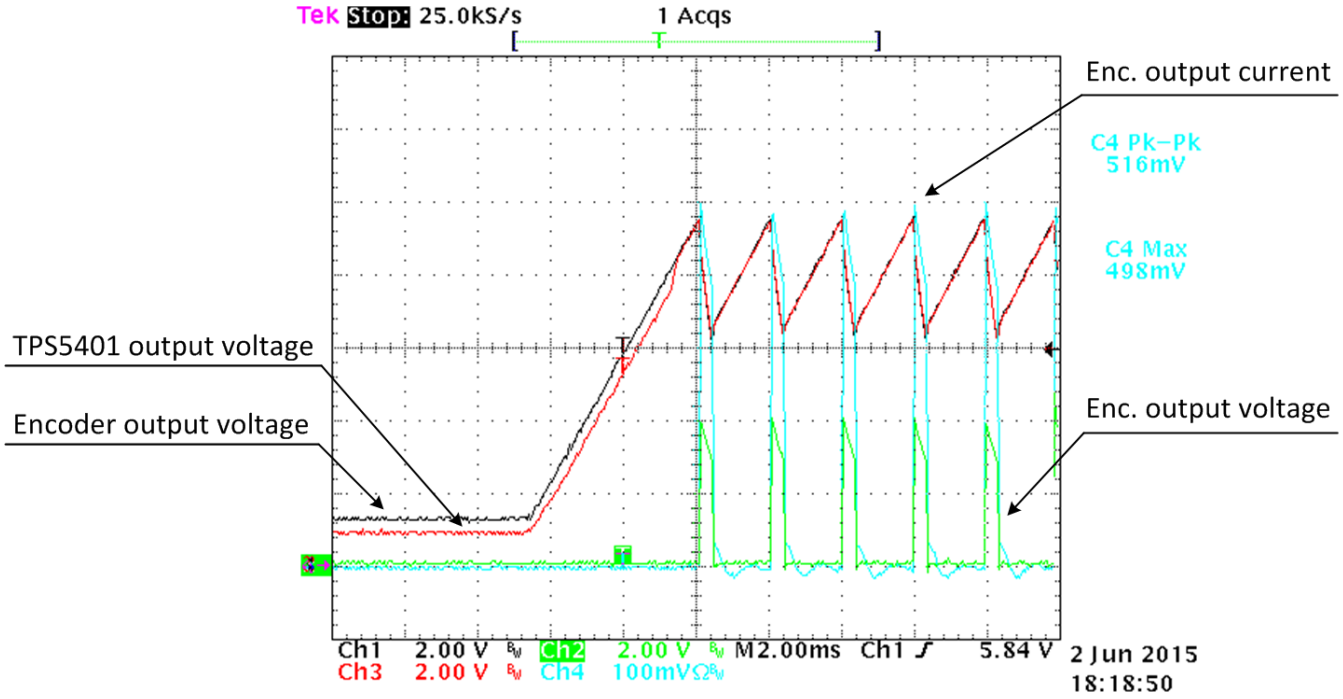


Figure 58. Start-up With Short-Circuited Output Without eFuse

Here it is possible to observe the advantage of using the eFuse: without the latching protection, the output bulk capacitor will be keep toggling between charge and discharge and the only protection level is achieved by the load switch (that has no latching condition).

Under these conditions, the current is limited only by the TPS5401 embedded current limiter.

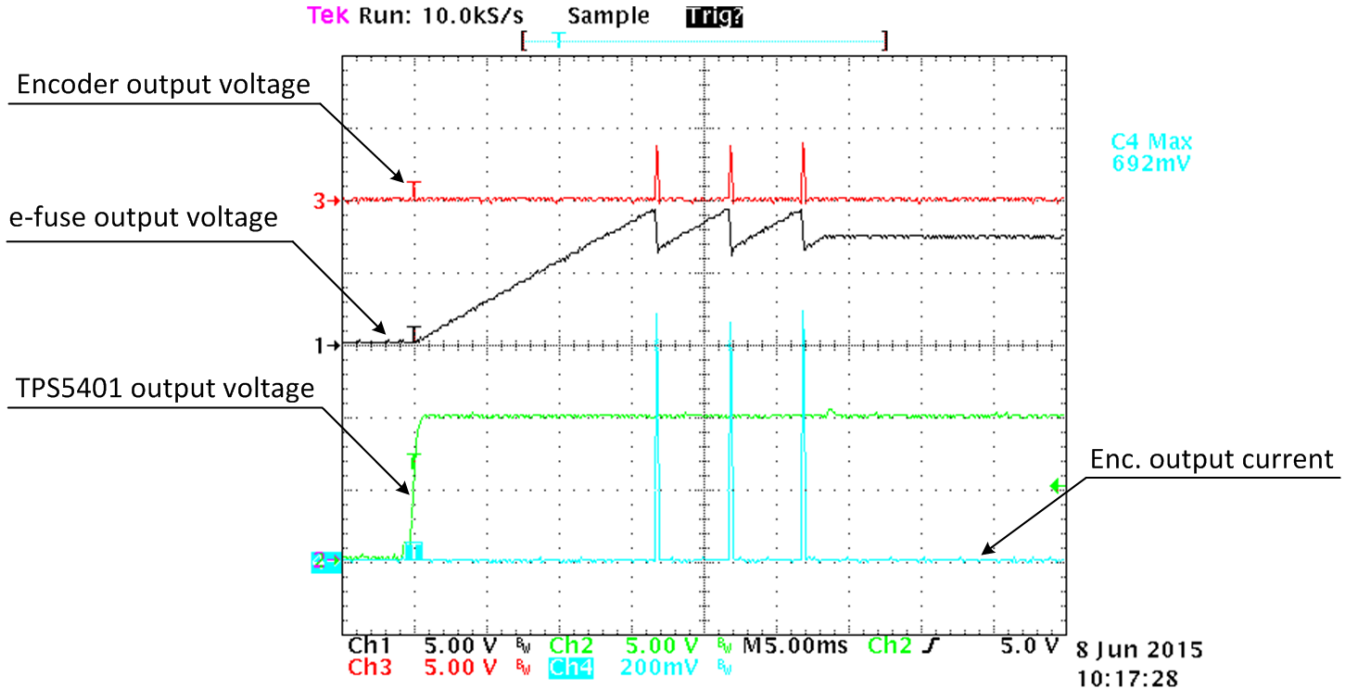


Figure 59. Start-up With Short-Circuited Output

If the eFuse fault pin is triggered, then it is possible to observe the eFuse latching event occurs after roughly 25 to 30 ms from the start-up:

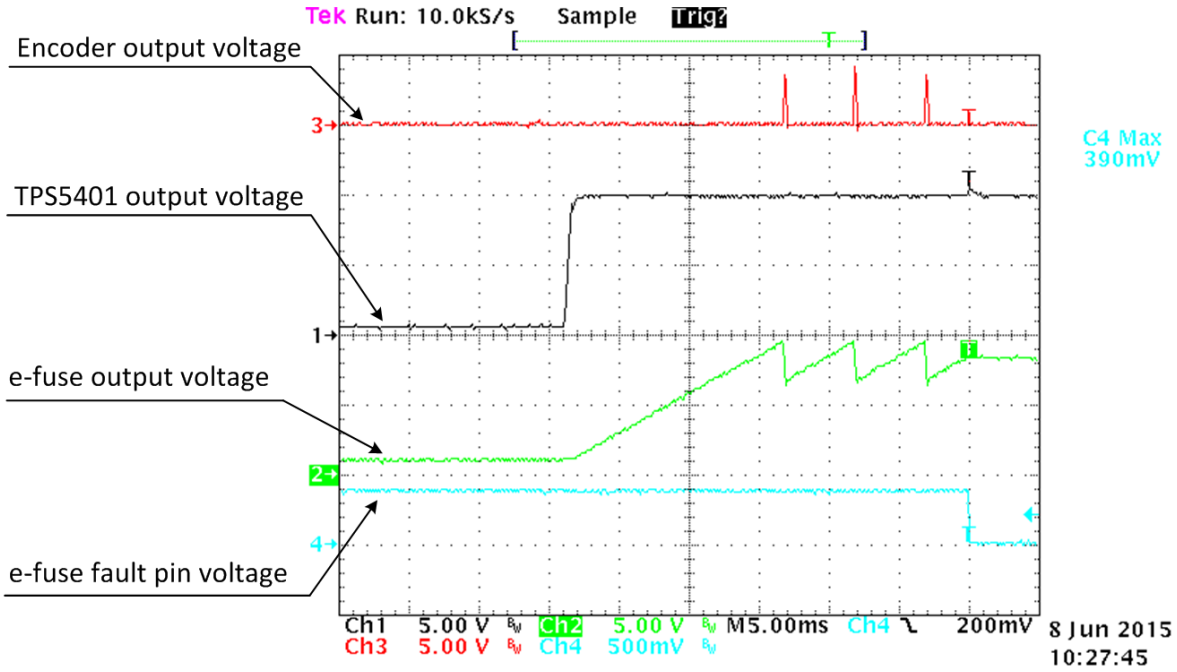


Figure 60. Fault Detection Performed by eFuse

After eFuse latches, the bulk capacitor slowly discharges over time:

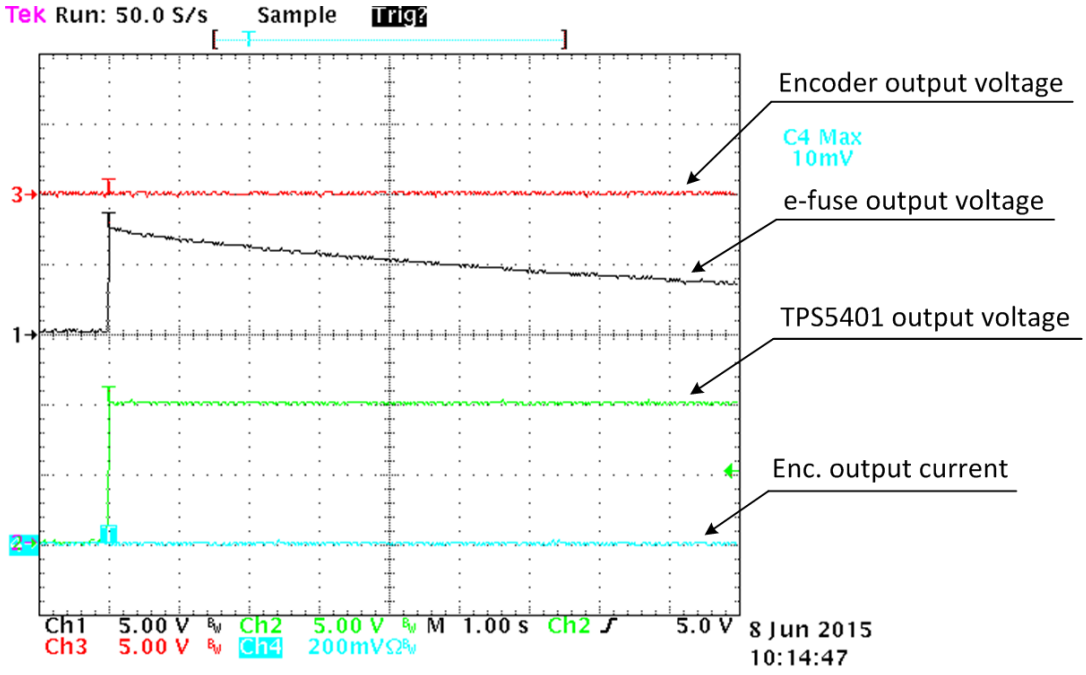


Figure 61. Start-up With Short-Circuited Output (Steady State)

6.4 HIPERFACE DSL Encoder Test

6.4.1 Startup (Power)

When the real encoder is used, the following behaviors have been observed:

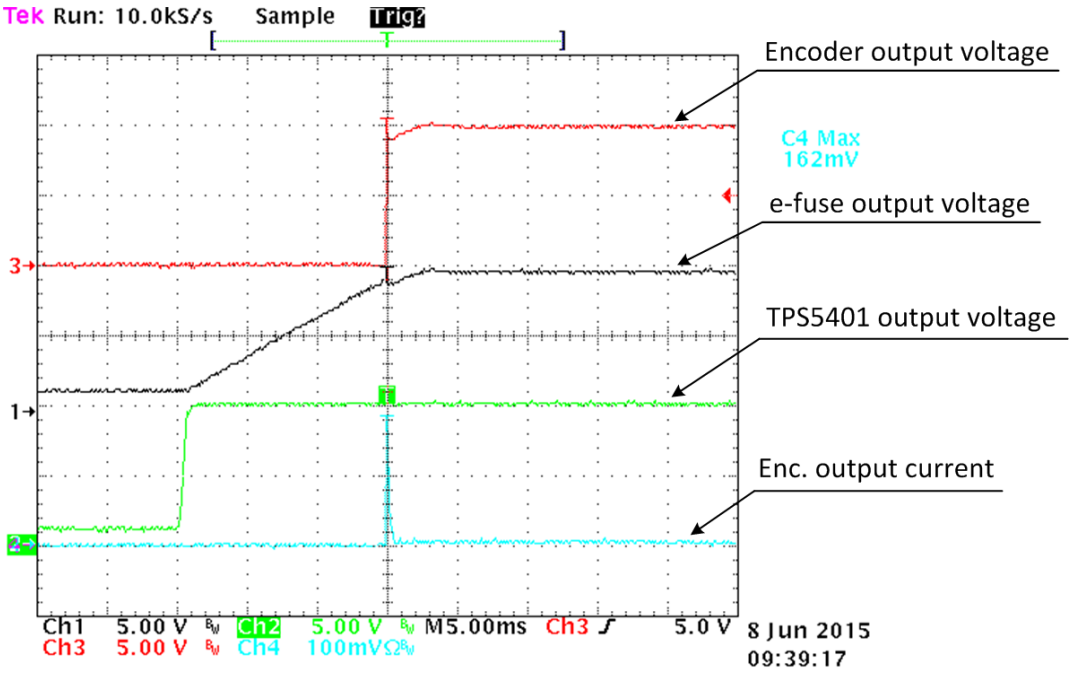


Figure 62. Start-up With Encoder

Zooming in, it is then possible to observe the encoder supply and input current profile.

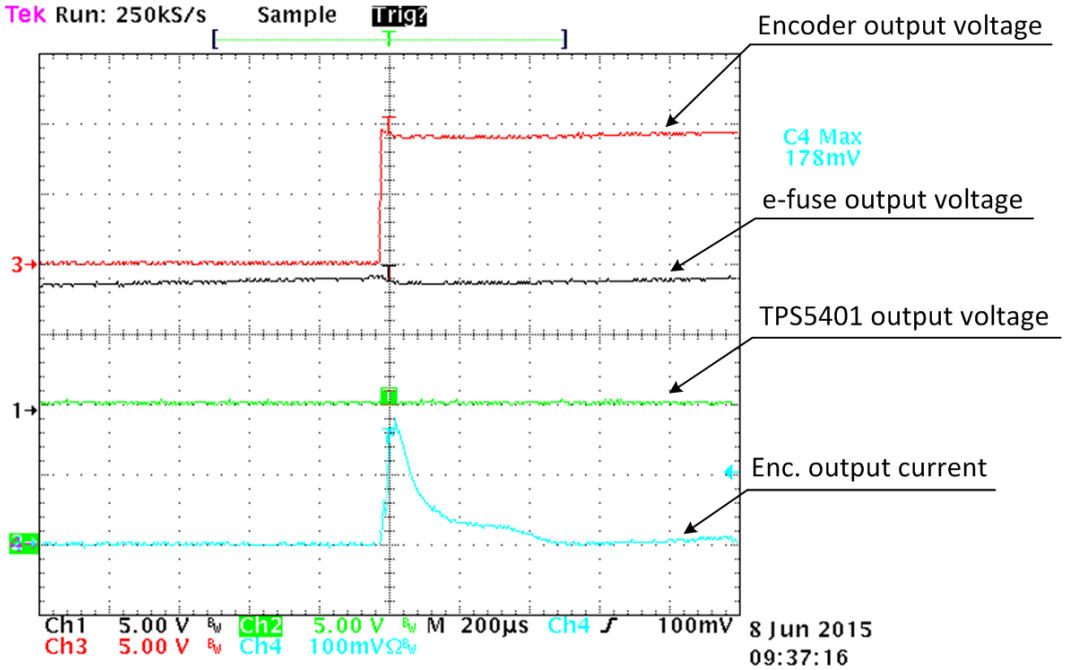


Figure 63. Start-up With Encoder (Zoom on Current Load Profile)

Note that Channel 4 (encoder output current) has always a set probe attenuation of 10:1, meaning that the input peak current (referring to the previous picture) is about 1.8 A.

Also note the encoder current supply shape versus time, as per Figure 2.

The turn-off mode (soft-stop) has been tested. It shows a normal behavior during the turn-off with nothing to notice:

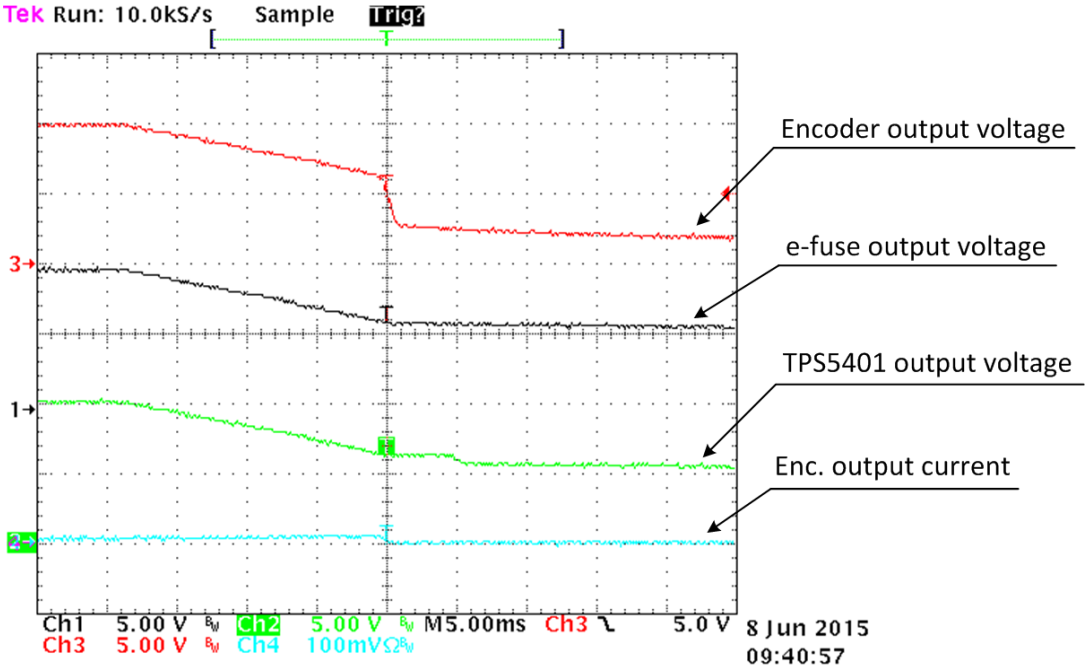


Figure 64. System Turn-off

6.4.2 System Performance Tests up to 100-m Cable Length

The tests were conducted with a modified HIPERFACE DSL Programming and Analyzer Tool PGT-09-S, where the physical interface was replaced by the TIDA-00177. The onboard RS-485 transceiver was removed and four wires were connected to the logic signals DSL_IN, DSL_OUT, DSL_EN, and GND. These were then connected to the TIDA-00177, connector J7. The HIPERFACE DSL wires DSL+ and DSL– were connected to the TI design J8. Figure 66 shows the setup. The test equipment is listed in Table 25.

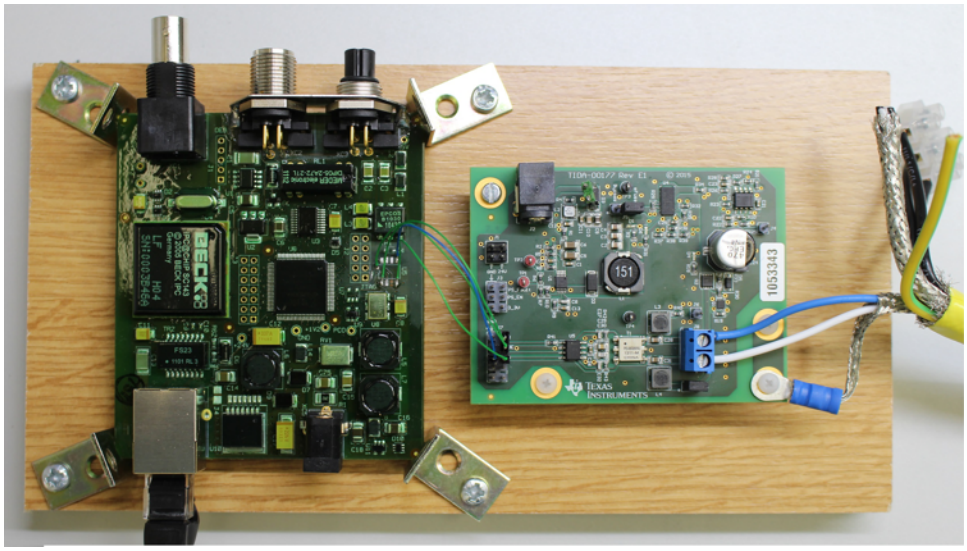


Figure 65. Modified PGT-09-S Connected to TIDA-00177 Two-Wire HIPEFACE DSL Interface

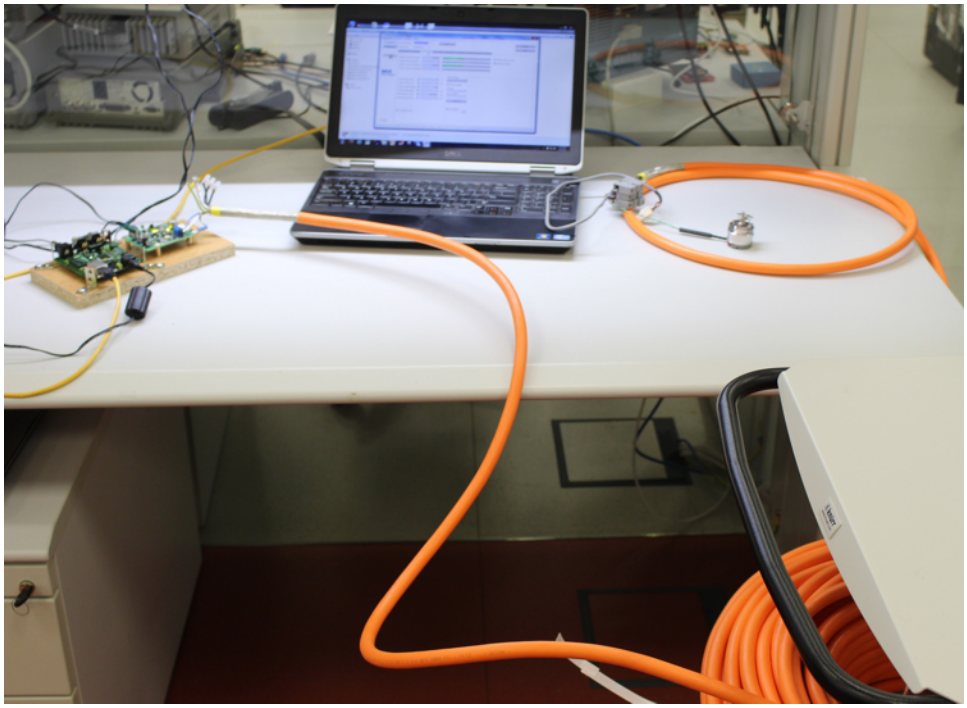


Figure 66. Picture of Test Setup With Modified PGT-09-S Connected to TIDA-00177 and HIPERFACE DSL Encoder EKM36

The tests were done without a motor powered through the same integrated cable. No communication errors where observed at any length up a 100-m cable length during the test. The duration was around three minutes.

Table 25. Test Results

CABLE LENGTH (m)	RESULTS
20	No errors observed
50	No errors observed
80	No errors observed
100	No errors observed

Figure 67 shows the screen log of the PGT-09-S GUI, after around 2.5 min.

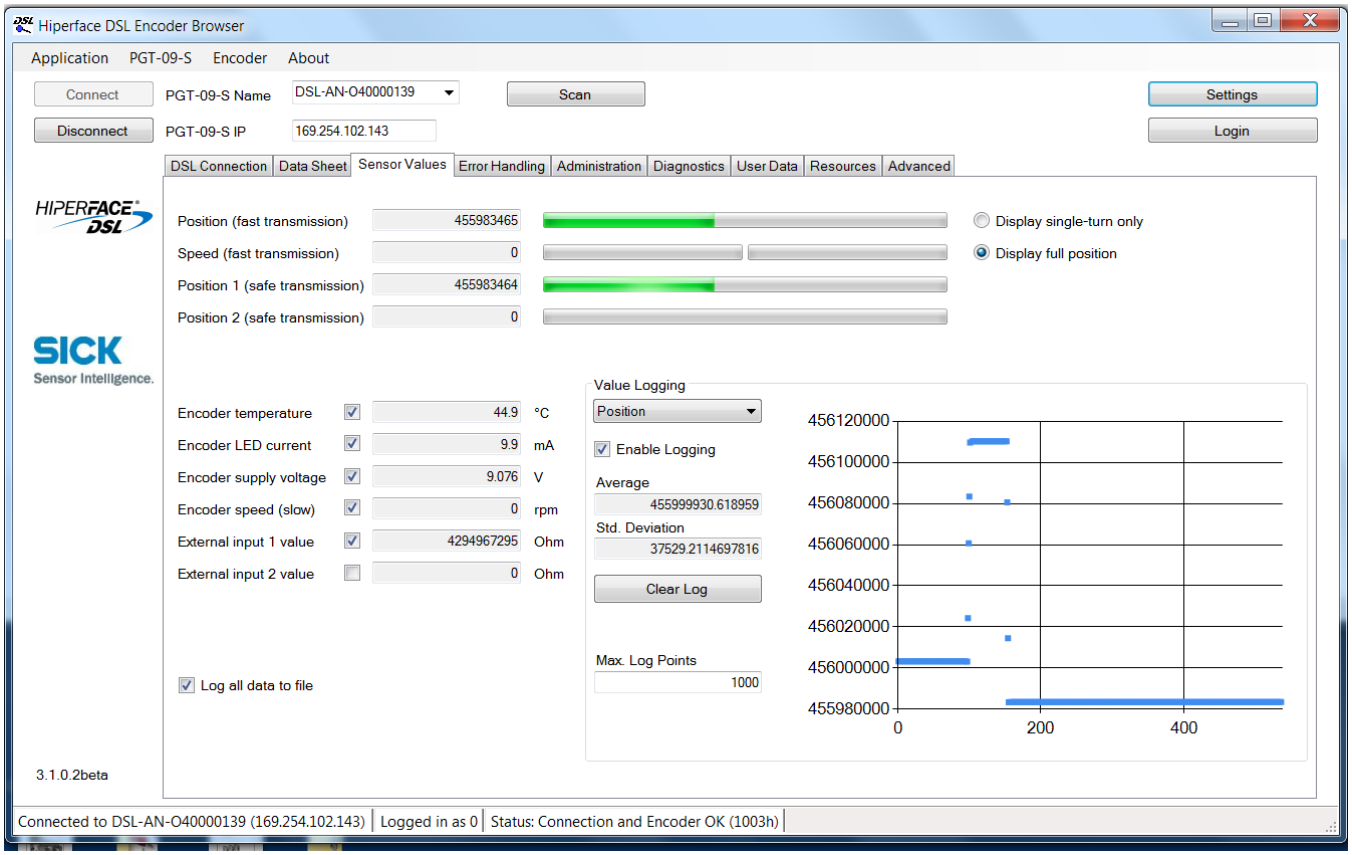


Figure 67. PGT-09-S With TIDA-00177 at 100-m Cable

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00177.

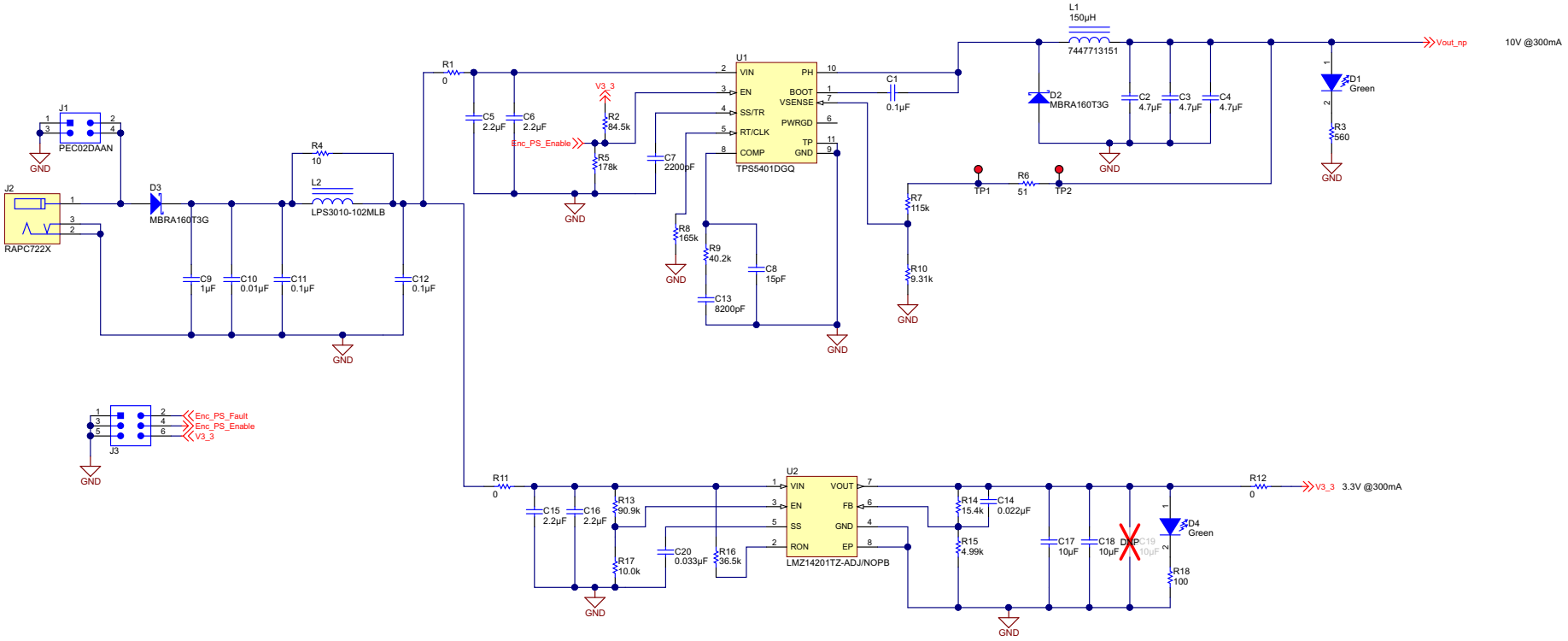


Figure 68. Power Management Solution

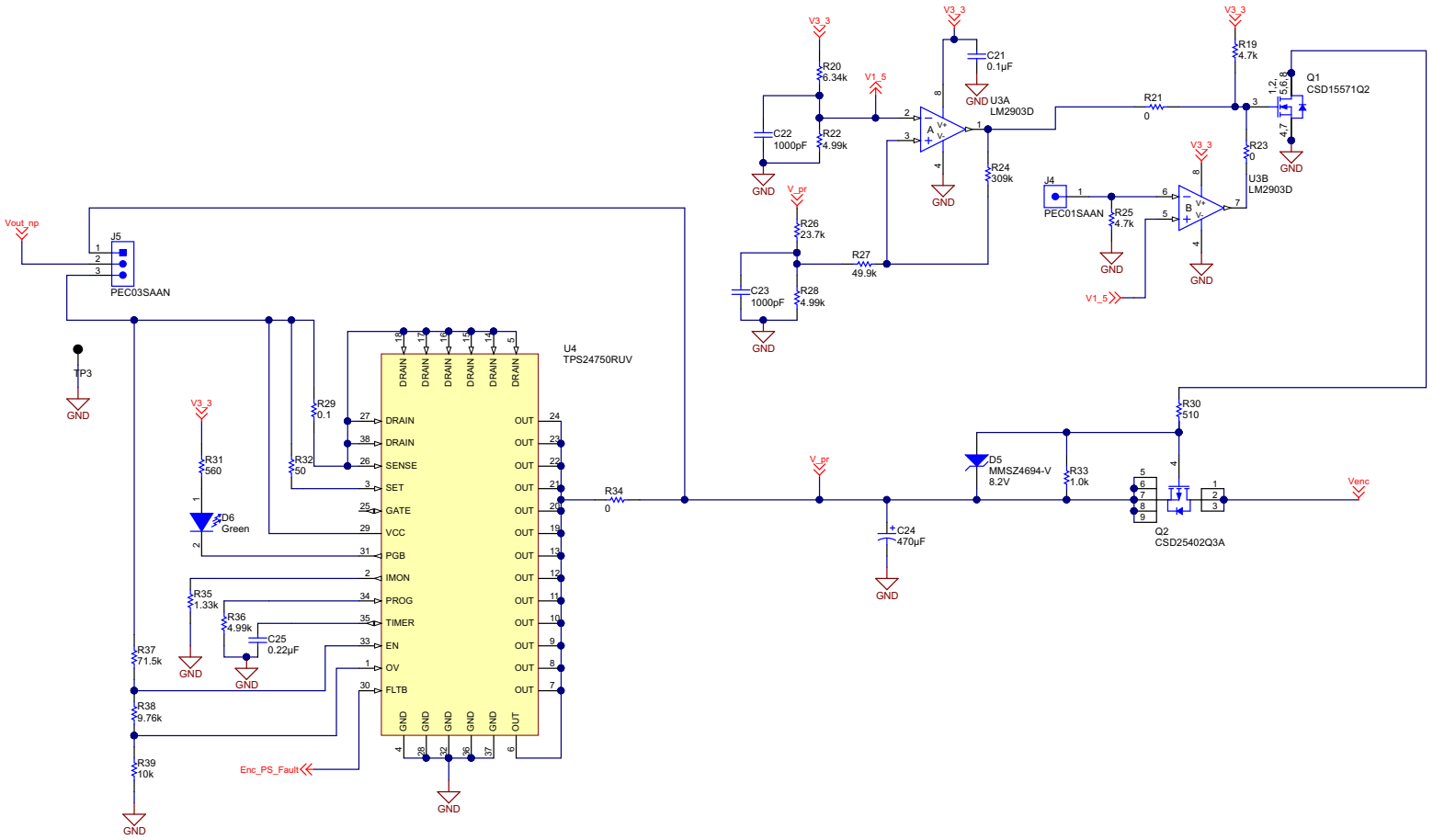


Figure 69. Protection Solution

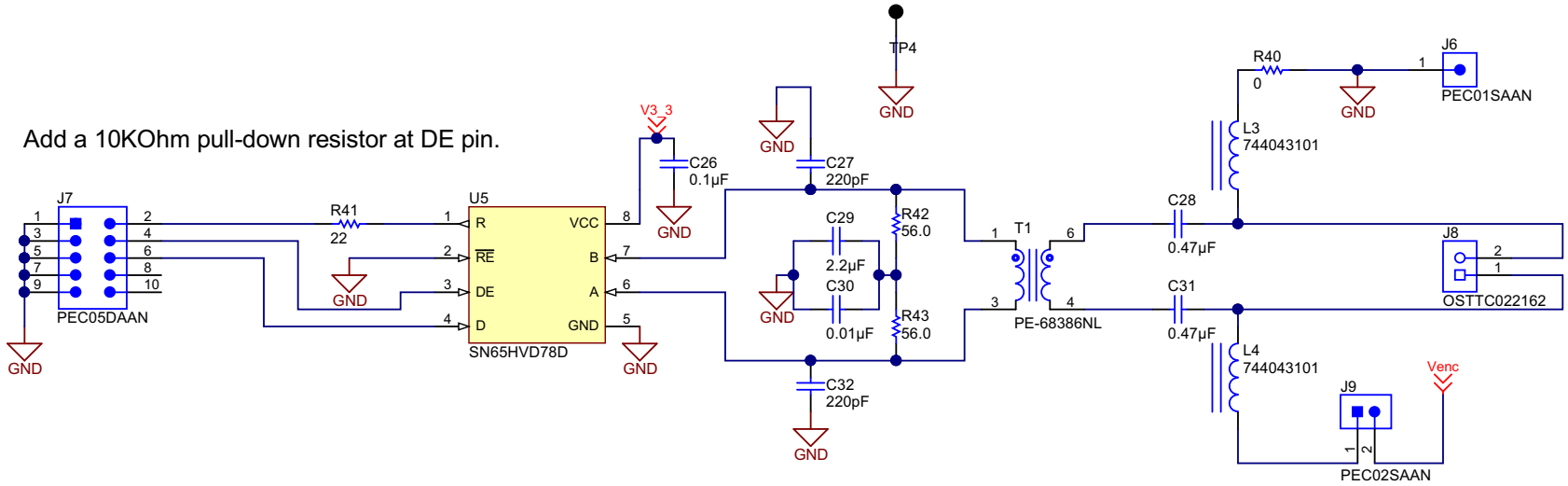


Figure 70. HIPERFACE DSL Interface Solution

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00177.

Table 26. BOM

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGEREFERENCE	FITTED
1	!PCB1	Printed Circuit Board	Any	TIDA-00177		Fitted
3	C1, C11, C12	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	MuRata	GRM188R71H104KA93D	0603	Fitted
3	C2, C3, C4	CAP, CERM, 4.7 µF, 50 V, +/- 10%, X5R, 0805	TDK	C2012X5R1H475K125AB	0805	Fitted
2	C5, C6	CAP, CERM, 2.2 µF, 50 V, +/- 10%, X7R, 1206	MuRata	GRM31CR71H225KA88L	1206	Fitted
1	C7	CAP, CERM, 2200pF, 16V, +/- 10%, X7R, 0603	MuRata	GRM188R71C222KA01D	0603	Fitted
1	C8	CAP, CERM, 15 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H150JA01D	0603	Fitted
1	C9	CAP, CERM, 1 µF, 50 V, +/- 10%, X7R, 0805	MuRata	GRM21BR71H105KA12L	0805	Fitted
1	C10	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0805	MuRata	GRM216R71H103KA01D	0805	Fitted
1	C13	CAP, CERM, 8200 pF, 25 V, +/- 10%, X7R, 0603	MuRata	GRM188R71E822KA01D	0603	Fitted
1	C14	CAP, CERM, 0.022uF, 16V, +/- 10%, X7R, 0603	MuRata	GRM188R71C223KA01D	0603	Fitted
2	C15, C16	CAP, CERM, 2.2uF, 50V, +/-10%, X5R, 1206	MuRata	GRM31CR61H225KA88L	1206	Fitted
2	C17, C18	CAP, CERM, 10uF, 10V, +/-20%, X5R, 0603	TDK	C1608X5R1A106M	0603	Fitted
1	C20	CAP, CERM, 0.033uF, 16V, +/- 10%, X7R, 0603	MuRata	GRM188R71C333KA01D	0603	Fitted
2	C21, C26	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	MuRata	GRM188R71C104KA01D	0603	Fitted
2	C22, C23	CAP, CERM, 1000 pF, 25 V, +/- 10%, X7R, 0603	MuRata	GRM188R71E102KA01D	0603	Fitted
1	C24	CAP, AL, 470 µF, 25 V, +/- 20%, 0.15 ohm, SMD	Panasonic	EEE-FC1E471P	SMT Radial G	Fitted
1	C25	CAP, CERM, 0.22 µF, 16 V, +/- 10%, X7R, 0603	MuRata	GRM188R71C224KA01D	0603	Fitted
2	C27, C32	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H221JA01D	0603	Fitted
2	C28, C31	CAP, CERM, 0.47 µF, 50 V, +/- 10%, X7R, 0805	MuRata	GRM21BR71H474KA88L	0805	Fitted

Table 26. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGEREFERENCE	FITTED
1	C29	CAP, CERM, 2.2 µF, 25 V, +/- 10%, X7R, 0805	MuRata	GRM21BR71E225KA73L	0805	Fitted
1	C30	CAP, CERM, 0.01 µF, 50 V, +/- 5%, C0G/NP0, 0805	MuRata	GRM2195C1H103JA01D	0805	Fitted
3	D1, D4, D6	LED, Green, SMD	OSRAM	LG L29K-G2J1-24-Z	1.7x0.65x0.8mm	Fitted
2	D2, D3	Diode, Schottky, 60V, 1A, SMA	ON Semiconductor	MBRA160T3G	SMA	Fitted
1	D5	Diode, Zener, 8.2 V, 500 mW, SOD-123	Vishay-Semiconductor	MMSZ4694-V	SOD-123	Fitted
6	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial	Fitted
4	H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	Screw	Fitted
4	H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	Standoff	Fitted
1	J1	Header, 100mil, 2x2, Tin, TH	Sullins Connector Solutions	PEC02DAAN	Header, 2x2, 2.54mm, TH	Fitted
1	J2	Power Jack, mini, 2.1mm OD, R/A, TH	Switchcraft	RAPC722X	Jack, 14.5x11x9mm	Fitted
1	J3	Header, 100mil, 3x2, Tin, TH	Sullins Connector Solutions	PEC03DAAN	3x2 Header	Fitted
2	J4, J6	Header, 1x1, Tin, TH	Sullins Connector Solutions	PEC01SAAN	Header, 1x1	Fitted
1	J5	Header, 100mil, 3x1, Tin, TH	Sullins Connector Solutions	PEC03SAAN	Header, 3 PIN, 100mil, Tin	Fitted
1	J7	Header, 100mil, 5x2, Tin, TH	Sullins Connector Solutions	PEC05DAAN	Header, 5x2, 100mil, Tin	Fitted
1	J8	Terminal Block, 2-pole, 200mil, TH	On-Shore Technology	OSTTC022162	THD, 2-Leads, Body 10.16x7.6mm, Pitch 5.08mm	Fitted
1	J9	Header, 100mil, 2x1, Tin, TH	Sullins Connector Solutions	PEC02SAAN	Header, 2 PIN, 100mil, Tin	Fitted
1	L1	Inductor, Shielded Drum Core, Ferrite, 150uH, 0.7A, 0.57 ohm, SMD	Wurth Elektronik eiSos	7447713151	10x3x10mm	Fitted
1	L2	Inductor, Shielded Drum Core, Ferrite, 1 µH, 1.5 A, 0.09 ohm, SMD	Coilcraft	LPS3010-102MLB	LPS3010	Fitted
2	L3, L4	Inductor, Shielded Drum Core, Ferrite, 100 µH, 0.3 A, 0.52 ohm, SMD	Wurth Elektronik eiSos	744043101	WE-TPC-M2	Fitted
1	Q1	MOSFET, N-CH, 20 V, 10 A, SON 2x2mm	Texas Instruments	CSD15571Q2	SON 2x2mm	Fitted
1	Q2	MOSFET, P-CH, -20 V, -15 A, SON 3.3x3.3mm	Texas Instruments	CSD25402Q3A	SON 3.3x3.3mm	Fitted
7	R1, R11, R12, R21, R23, R34, R40	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Fitted
1	R2	RES, 84.5 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060384K5FKEA	0603	Fitted

Table 26. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGEREFERENCE	FITTED
2	R3, R31	RES, 560, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603560RJNEA	0603	Fitted
1	R4	RES, 10 ohm, 5%, 0.25W, 0603	Vishay-Dale	CRCW060310R0JNEAHP	0603	Fitted
1	R5	RES, 178 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603178KFKEA	0603	Fitted
1	R6	RES, 51 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060351R0JNEA	0603	Fitted
1	R7	RES, 115 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603115KFKEA	0603	Fitted
1	R8	RES, 165k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603165KFKEA	0603	Fitted
1	R9	RES, 40.2 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060340K2FKEA	0603	Fitted
1	R10	RES, 9.31 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-079K31L	0603	Fitted
1	R13	RES, 90.9k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060390K9FKEA	0603	Fitted
1	R14	RES, 15.4k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060315K4FKEA	0603	Fitted
4	R15, R22, R28, R36	RES, 4.99k ohm, 1%, 0.1W, 0603, RES, 4.99 k, 1%, 0.1 W, 0603, RES, 4.99 k, 1%, 0.1 W, 0603, RES, 4.99k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K99FKEA	0603	Fitted
1	R16	RES, 36.5k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060336K5FKEA	0603	Fitted
1	R17	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	0603	Fitted
1	R18	RES, 100, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603100RJNEA	0603	Fitted
2	R19, R25	RES, 4.7 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06034K70JNEA	0603	Fitted
1	R20	RES, 6.34 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-076K34L	0603	Fitted
1	R24	RES, 309 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603309KFKEA	0603	Fitted
1	R26	RES, 23.7 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060323K7FKEA	0603	Fitted
1	R27	RES, 49.9 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060349K9FKEA	0603	Fitted
1	R29	RES, 0.1, 1%, 0.1 W, 0603	Panasonic	ERJ-3RSFR10V	0603	Fitted
1	R30	RES, 510, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603510RJNEA	0603	Fitted
1	R32	RES, 50, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060350R0FKEA	0603	Fitted
1	R33	RES, 1.0 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00JNEA	0603	Fitted
1	R35	RES, 1.33 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K33FKEA	0603	Fitted
1	R37	RES, 71.5 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060371K5FKEA	0603	Fitted
1	R38	RES, 9.76 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06039K76FKEA	0603	Fitted
1	R39	RES, 10 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	0603	Fitted
1	R41	RES, 22, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060322R0JNEA	0603	Fitted
2	R42, R43	RES, 56.0, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0756RL	0603	Fitted
1	T1	Transformers, Gate Drive , 785uH, SMT	Pulse Engineering	PE-68386NL	8.6x2.5x6.7 mm	Fitted
2	TP1, TP2	Test Point, Miniature, Red, TH	Keystone	5000	Red Miniature Testpoint	Fitted

Table 26. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGEREFERENCE	FITTED
2	TP3, TP4	Test Point, Miniature, Black, TH	Keystone	5001	Black Miniature Testpoint	Fitted
1	U1	Buck Step Down Regulator with 3.5 to 42 V Input and 0.8 to 39 V Output, -40 to 150 degC, 10-Pin MSOP-PowerPAD (DGQ), Green (RoHS & no Sb/Br)	Texas Instruments	TPS5401DGQ	DGQ0010D	Fitted
1	U2	1A SIMPLE SWITCHER® Power Module with 42V Maximum Input, 7 pin TO-PMOD	National Semiconductor	LMZ14201TZ-ADJ/NOPB	TZA07A	Fitted
1	U3	Dual Comparator, D0008A	Texas Instruments	LM2903D	D0008A	Fitted
1	U4	2.5 to 18 V Positive Voltage 10A Integrated Hot-Swap Controller, RUV0036A	Texas Instruments	TPS24750RUV	RUV0036A	Fitted
1	U5	3.3V-Supply RS-485 with IEC ESD Protection, D0008A	Texas Instruments	SN65HVD78D	D0008A	Fitted
0	C19	CAP, CERM, 10uF, 10V, +/-20%, X5R, 0603	TDK	C1608X5R1A106M	0603	Not Fitted

7.3 PCB Layout Guidelines

Since there are no noise-sensitive circuits in this design, no particular attentions are required in the layout design, except for the power management section for the purpose of the EMI/EMC compliance.

This is actually minor because on one side the design with the TPS5401 has been already proved in the TIDA-00177 while on the other side the LMZ14201, being a module with an embedded shielded inductor, is already EMI/EMC compliant.

The design of a four-layer PCB with at least one complete ground plane has then been performed.

Layout guidelines can be also found in the datasheets of the TI parts used in the TIDA-00177.

7.3.1 TPS5401

Bypass the VIN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.

Take care to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The GND pin should be tied directly to the thermal pad under the IC.

Connect the thermal pad to any internal PCB ground planes using multiple vias directly under the IC.

Route the PH pin to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor should be located close to the PH pins, and the area of the PCB conductor should be minimized to prevent excessive capacitive coupling.

The RT/CLK pin is sensitive to noise, so locate the RT resistor as close as possible to the IC and routed with minimal lengths of trace.

7.3.2 TPS24750

Decoupling capacitors on VCC pin should have minimal trace lengths to the pin and to GND.

Traces to SET and SENSE must be short and run side-by-side to maximize common-mode rejection. Use Kelvin connections at the points of contact with R_{SENSE}.

High current carrying power path connections should be as short as possible and sized to carry at least twice the full-load current, more if possible.

Minimize connections to IMON pin after the previously described connections have been placed.

To operate at rated power, solder the PowerPAD™ directly to the PC board GND plane directly under the device. The PowerPAD is at GND potential and can be connected using multiple vias to inner layer GND.

7.3.3 SN65HVD78

Use V_{CC} and ground planes to provide low-inductance. Apply 100- to 220-nF bypass capacitors as close as possible to the V_{CC} pins of the transceiver, UART, and controller ICs on the board. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.

Use 1k to 10k pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.

Insert pulse-proof resistors into the A and B bus lines.

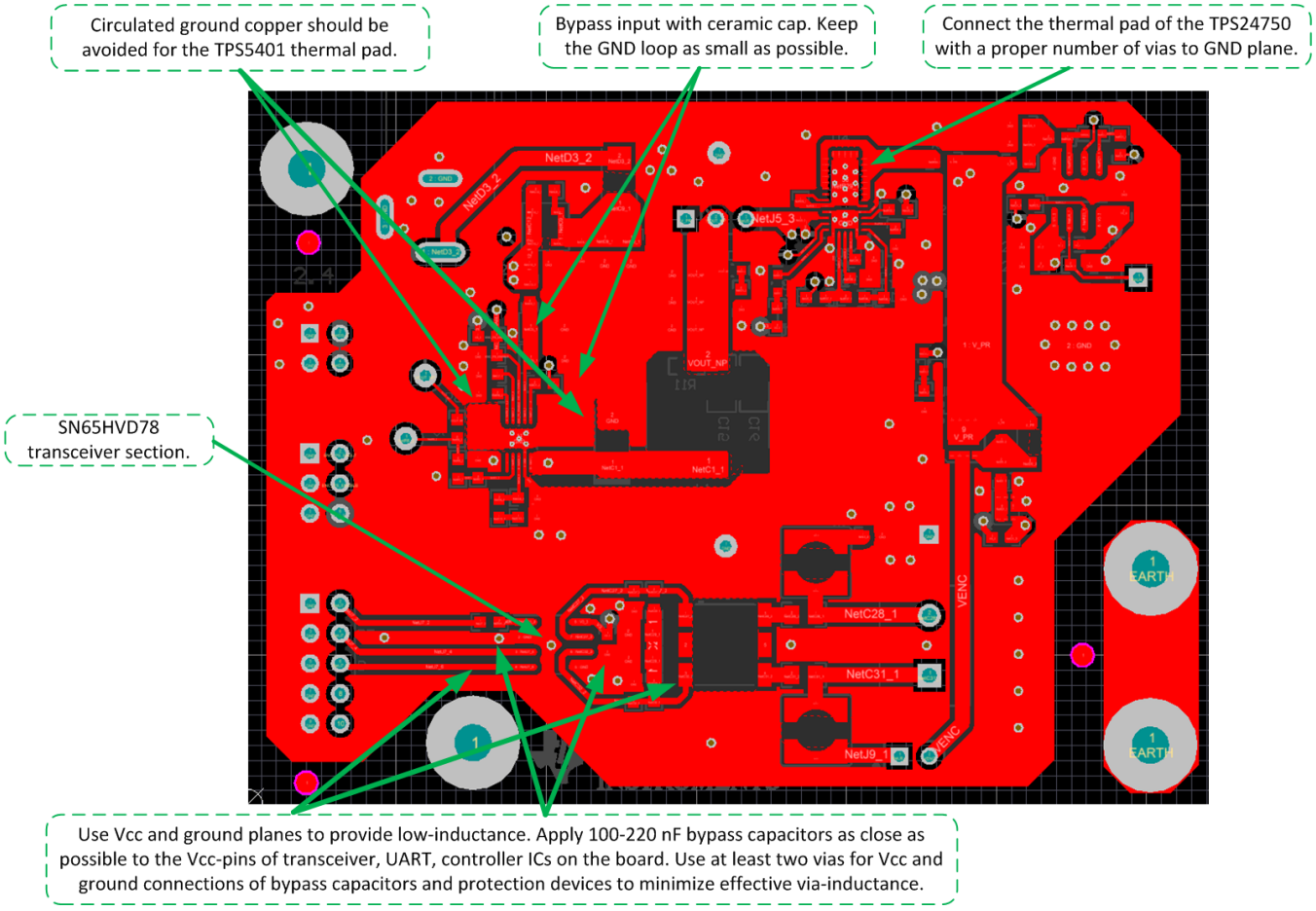


Figure 71. Top Layer (1/2)

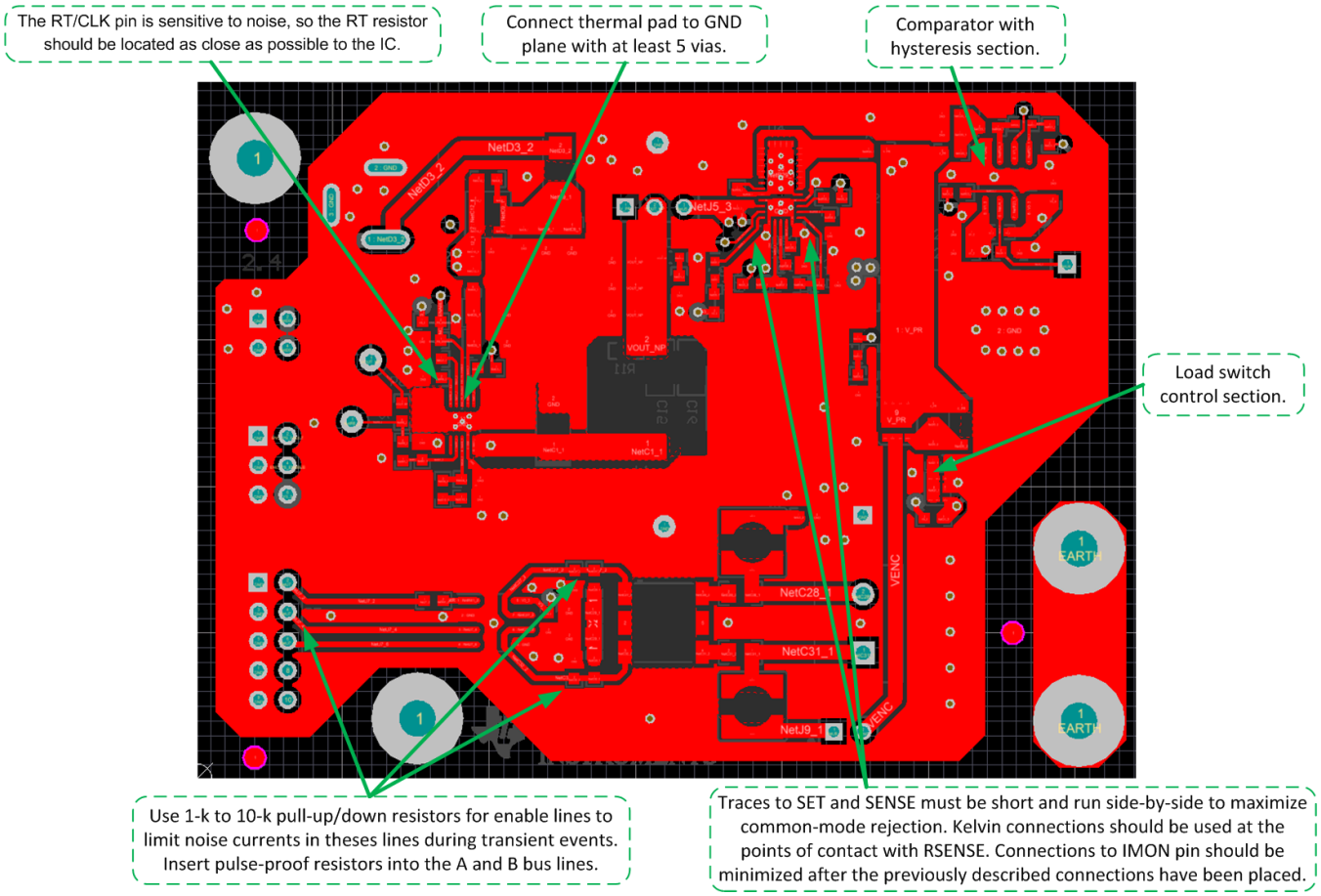


Figure 72. Top Layer (2/2)

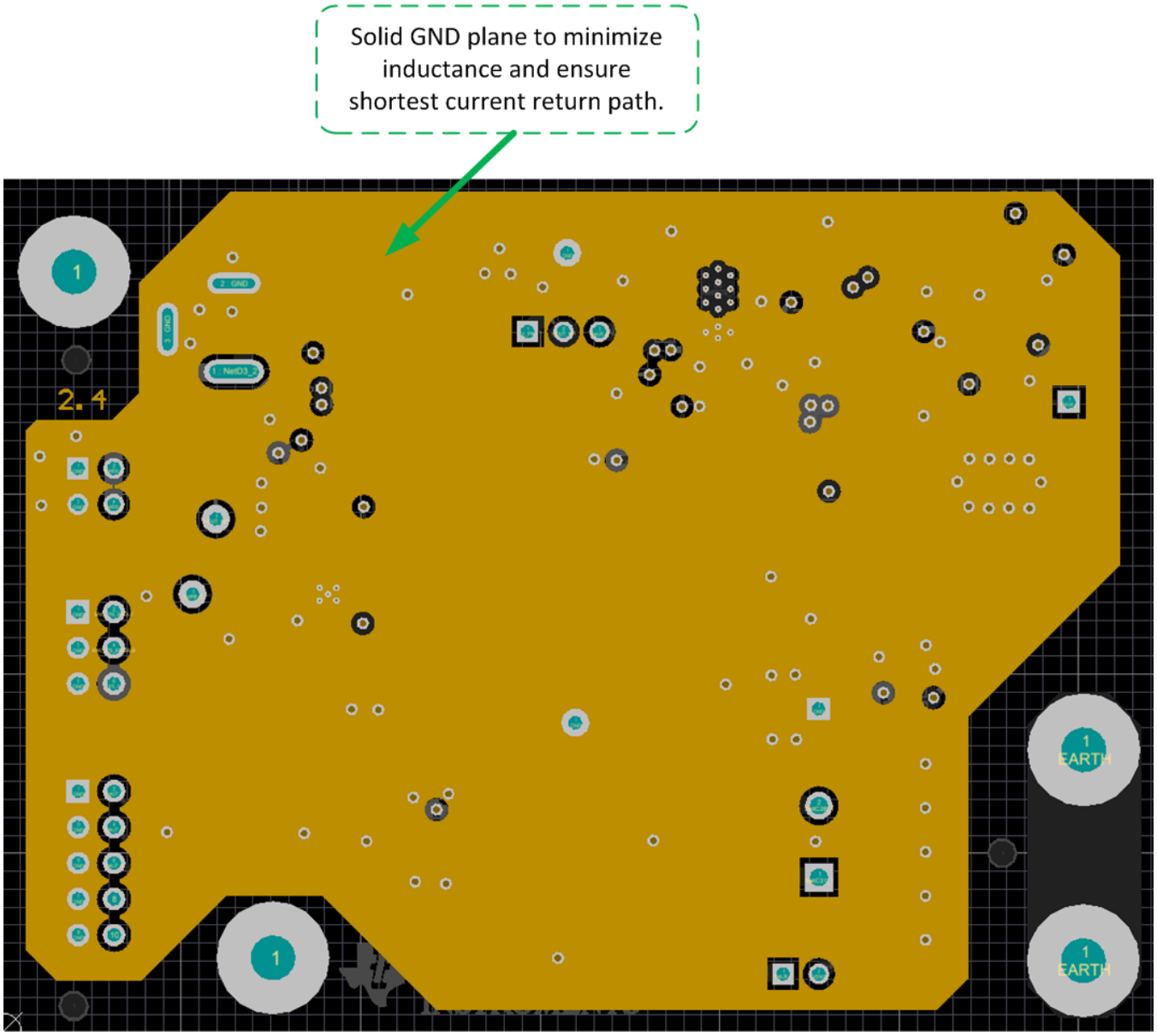


Figure 73. Power Plane (GND)

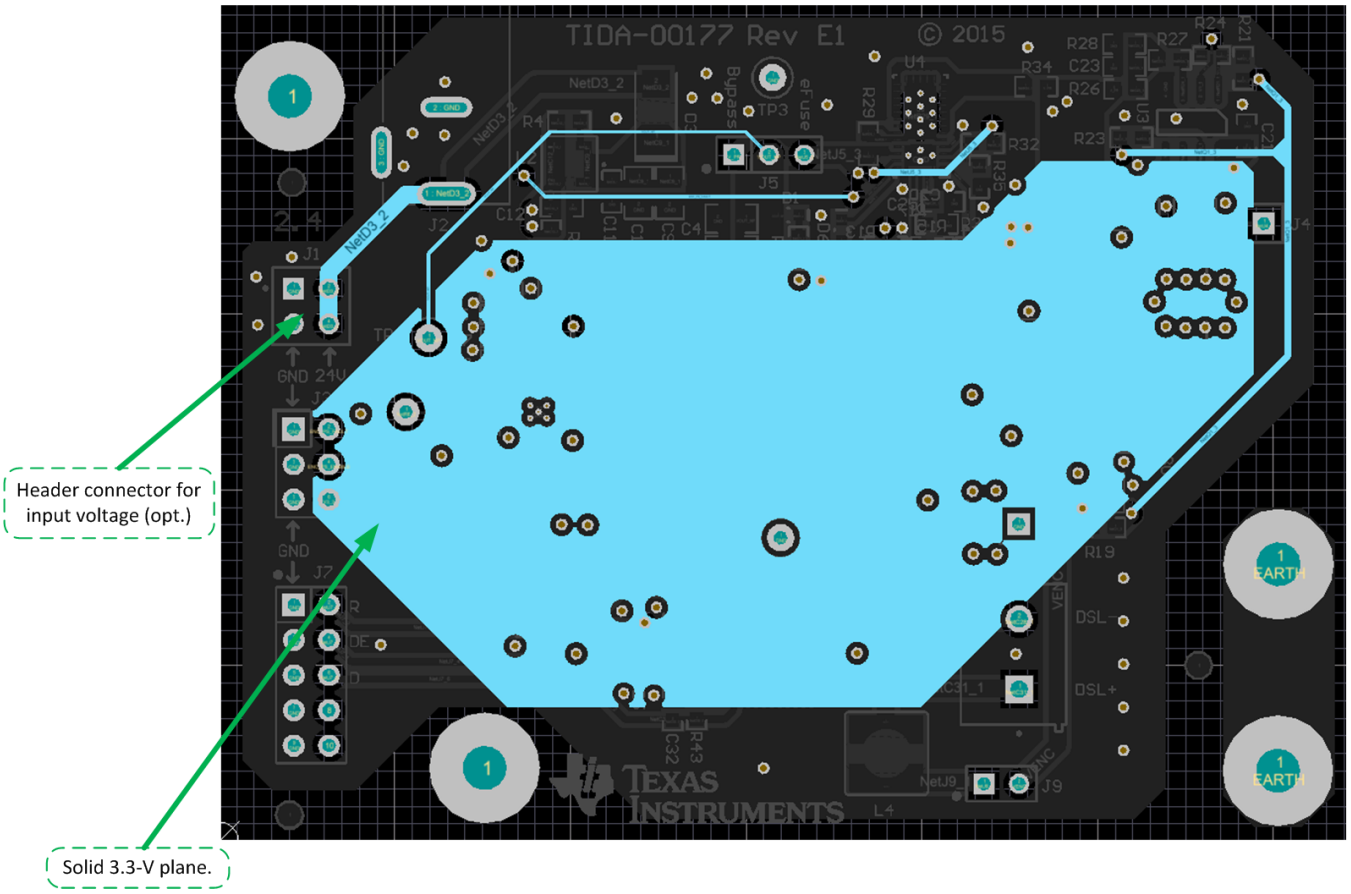


Figure 74. Power Plane (VCC)

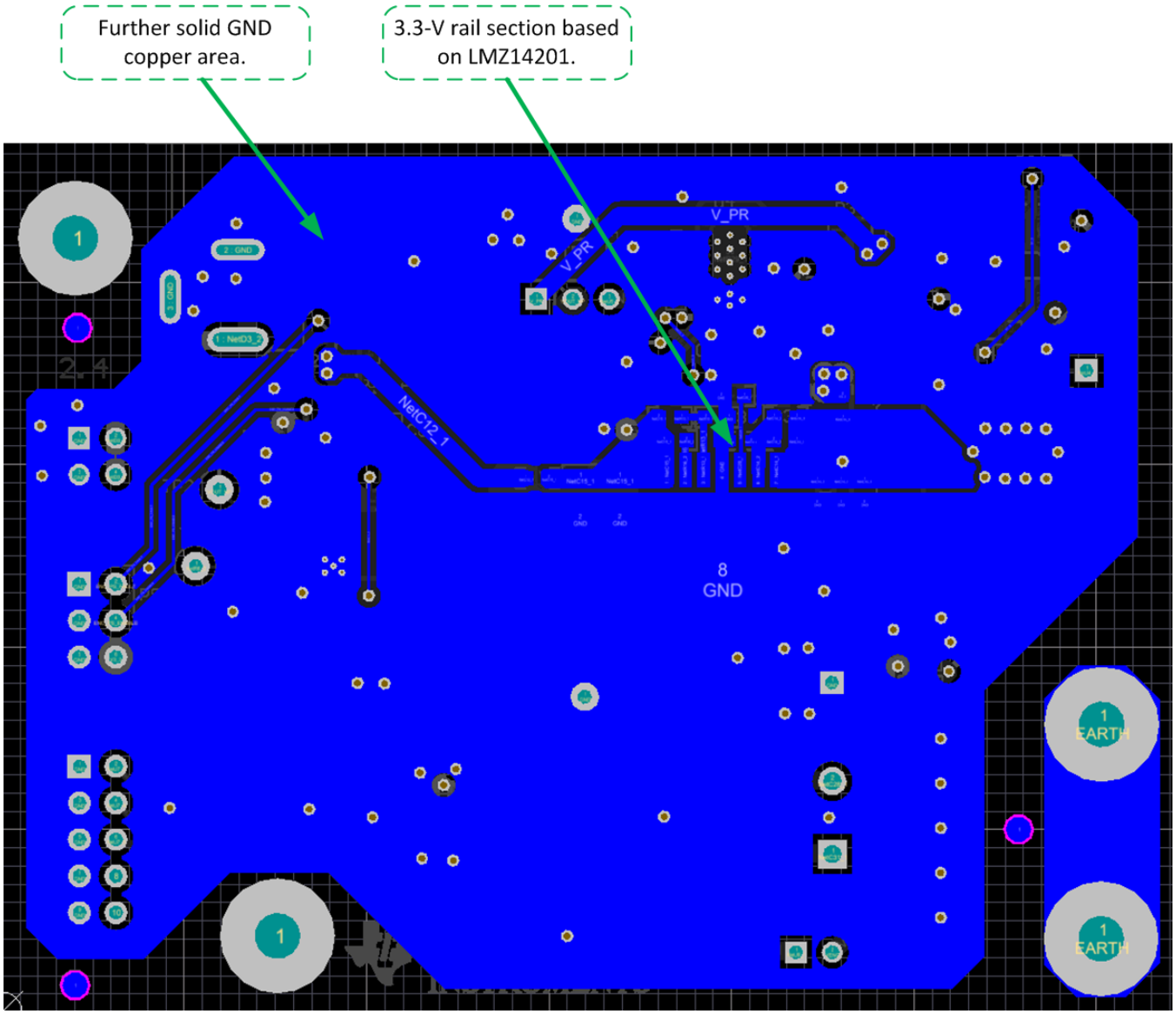


Figure 75. Bottom Layer

7.4 Layer Plots

To download the layer plots, see the design files at TIDA-00177.

7.5 Altium Project

To download the Altium project files, see the design files at TIDA-00177.

7.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00177.

7.7 Assembly Drawings

To download the Gerber files, see the design files at TIDA-00177.

8 References

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9 About the Authors

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Revision History

Changes from Original (June 2015) to A Revision	Page
• Changed from preview page	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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