TI Designs

Generating the AVS SmartReflex Core Voltage for the K2E SoC Using the TPS544C25 and PMBus

Design Overview

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Design Resources

TIDEP0042	Tool Folder Containing Design File
K2EEVM	K2E EVM Information
66AK2E05	Product Folder
66AK2E02	Product Folder
AM5K2E04	Product Folder
AM5K2E02	Product Folder
TPS544C25	Product Folder
PCA9306	Product Folder

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Design Features

- Provides the AVS SmartReflex™ Core voltage required by the K2E SoC
- Meets the 5% voltage requirement for CVDD
- Uses the PMBus interface on the TPS544C25 for control
- Uses software to send the V_{OUT} command
- Complete system reference with schematics, BOM, design files, and HW Design Guide implemented on the K2E SoC platform for testing and evaluation.

Featured Applications

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- Communications Equipment
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1 Overview

This TI Design is based on the power supply circuit for the core voltage of the 66AK2Ex and AM5K2E0x SoCs implemented on the K2E SoC. TI designed the circuit to support the use of either the PMBus or the LM10011 to command the proper AVS voltage. This TI Design discusses the circuit required for control using the PMBus.

2 Circuit Description

The 66AK2Ex and AM5K2E0x SoCs requires automatic voltage scaling (AVS) for the core voltage. Software operating on the SoC to read the required voltage from the SmartReflex™ subsystem in the SoC. An I^2C interface is connected to the PMBus interface on the device. The software generates PMBus commands to direct the TPS544C25 to adjust the voltage generated by that device.

3 Design Summary

The 66AK2E0x and AM5K2E0x SoCs use SmartReflex™ technology to decrease both static and dynamic power consumption, while maintaining the performance of the device. To acheive this, the SmartReflex™ controller provides an optimized core voltage level based on the process corner of the device. This requires a separate core power supply for each SoC that can be configured by the SmartReflex ™controller. This design uses software running on the SoC to communicate with the TPS544C25 PMBus interface to generate the core voltage CVDD.

3.1 Introduction to the TPS544C25 Using PMBus

The TPS544C25 device is a synchronous buck converter with integrated FETs capable of a 30-A current output. Two methods are available to set the output voltage of the converter as shown in Figure 1 and Figure 2.

- The use of an LM10011 device connected to the feedback pin. This approach is discussed in a separate design.
- The use of the PMBus interface connected to an I^2C on the K2E SoC.

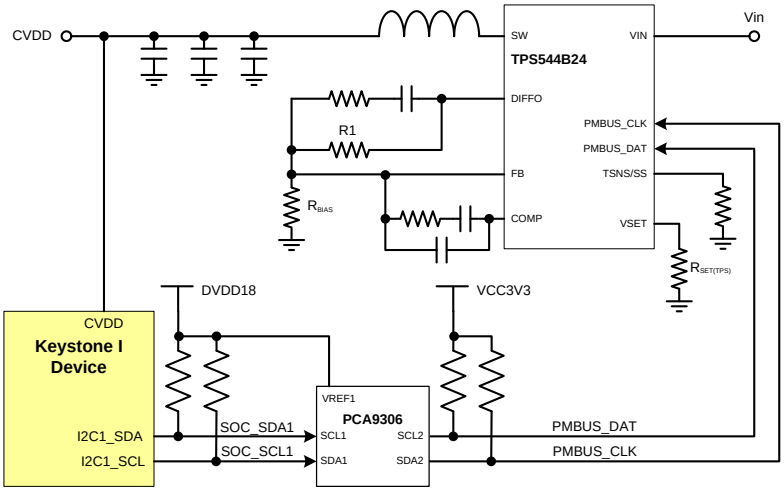

Figure 1. CVDD Power Circuit Using the TPS544C25 Controlled by PMBus

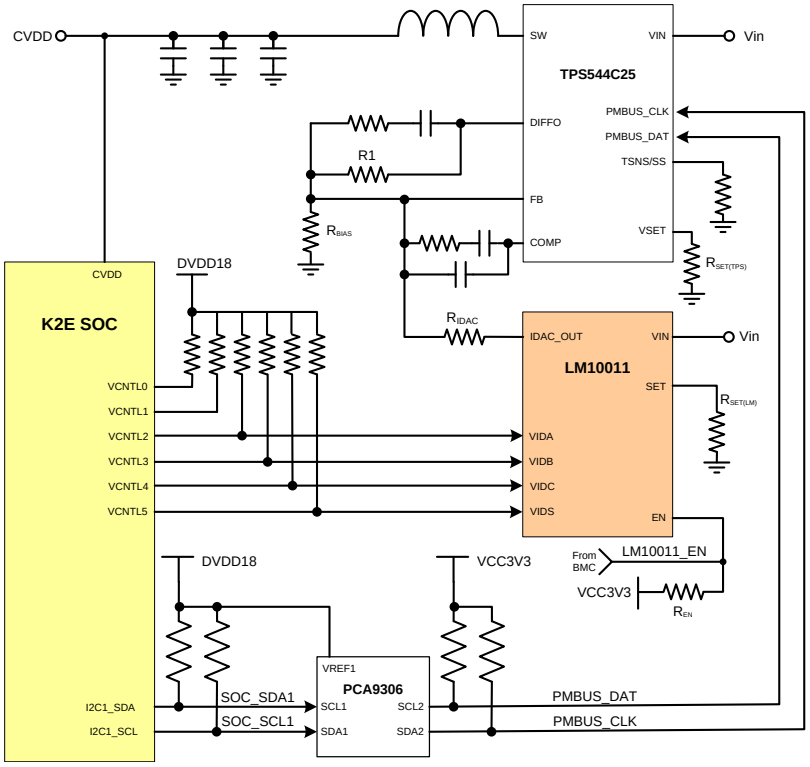

Figure 2. Circuit Supporting Both LM10011 and PMBus Control

The circuit on the K2E SoC can be configured for three different methods of operation.

- **Mode 1 –** LM10011 only: As delivered, the K2E SoC is configured to control the AVS voltage using only the LM10011. For more details on this mode see the TI Design *Generating AVS SmartReflex Core Voltage for K2E Using TPS544C25 & LM10011* (TIDEP0041).
- **Mode 2 –** Selectable between LM10011 and PMBus: A small modification made to the default K2E SoC allows AVS support from either the LM10011 or from the PMBus interface. In mode 1, the REN resistor value is 0-Ω, ensuring that the LM10011 is enabled at all times. Replacing the 0-Ω resistor with a 10-KΩ resistor lets the board management controller (BMC) to control whether the LM10011 is enabled. In this mode, the LM10011 is enabled at boot and sets the initial voltage output level of the TPS544C25 using the $R_{SET(LM)}$ resistor. More details on setting the initial voltage level with the LM10011 can be found in the TI Design *Generating AVS SmartReflex ™Core Voltage for K2E Using TPS544C25 & LM10011* (TIDEP0041).
- **Mode 3 –** PMBus only: The K2E SoC circuit can be modified to remove the functionality of the LM10011 from the circuit. In this mode, the AVS voltage level must be set with software using the PMBus connection to the TPS544C25. Removing RIDAC from the circuit isolates the current provided by the LM10011. The value of $R_{SET\ (TPS)}$ must be changed from a 121 KΩ to 78.7 KΩ to set the initial output voltage of the TPS544C25. Some KeyStone™ II devices require an initial voltage of 1.10 V. Check the data manual for the part to ensure the proper initial voltage is present. These changes are represented in the schematics provided with this TI Design.

3.2 TPS544C25 Basics

To understand how the TPS544C25 operates, study the data manual and the associated design collateral. This document provides a brief discussion of the basic operation of the device. The TPS544C25 provides the DC-DC converter for the CVDD core voltage of the K2E SoC. A functional block diagram of the TPS544C25 device is in Figure 3.The K2E SoC requires the use of an AVS power supply that configures the output voltage based on the requirement of the SoC. The TPS544C25 is implemented on the K2E SoC to provide that capability. The TPS544C25 supports two methods of setting the AVS voltage. Both methods can be supported by the K2E SoC by installing different components. The first uses the LM10011 and the VCNTL interface to control the AVS voltage level. The first method of setting the AVS voltage is the default mode, and the component values in the EVM schematic will enable this method. The first method uses the PMBus interface to modify the output voltage. Changes to the components installed and software running on the SoC are required to support this second method. This TI Design only describes only the PMBus™ mode.

To understand the interaction between the PMBus commands and the TPS544C25, requires some basic information about setting the output voltage for the part. Buck converters use an error amplifier to compare a reference voltage to feedback voltage based on V_{OUT}. The reference voltage is fixed and the feedback voltage is created using a resistor divider. In Figure 2, the resistors used to generate the feedback voltage are called R1 and Rbias. The values of these resistors are selected to ensure that the voltage at the FB pin will equal the reference voltage for the desired V_{OUT}.

The TPS544C25 uses a reference digital-to-analog converter (DAC) to modify the reference voltage. By changing the reference voltage, the output voltage can be modified without replacing the resistors on the board. The reference DAC has a range of 0 V to 1.5 V. If the value of V_{OUT} is within this range, a voltage divider at the FB pin is unnecessary and Rbias can be removed. The TPS544C25 only uses Rbias to scale V_{OUT} for higher voltage ranges than are supported by the 0 V to 1.5 V range reference of the DAC. Because the required AVS voltage for the K2E SoC fall within this range, the scaling resistor is not necessary for this design. The current at the FB pins, Ifb, is less than 75 nA. Because the FB pin is connected to V_{OUT} through R1, the voltage drop between V_{OUT} and the FB pin is less than 1 mV. The voltage at the FB pin is equal to V_{OUT} – (R1 × 75 nA).

The output voltage is defined by the V_{OUT}_COMMAND register and supports a 1-V swing from 0.5-V to 1.5-V using the values 256 to 768. The output voltage is set to the value of V_{OUT}_COMMAND x 1.953 mV and the default value of V_{OUT}_COMMAND is 486, which produces a V_{OUT} of 0.95 V.

The initial voltage of the device is based on the default value of the V_{OUT}_COMMAND unless a Rset (TPS) resistor is connected to the VSET pin of the device. The table in section 7.3.6.3 of the TPS544C25 data manual provides a correlation between the value of the resistor connected from the VSET pin and ground to the initial V_{OUT} voltage generated by the part. In this design a 78.7-K resistor generates a V_{OUT}_COMMAND value for 1.05 V. This value is generated as an initial voltage to the reference leg of the error amplifier. Figure 3 shows the functional block diagram of theTPS544C25.

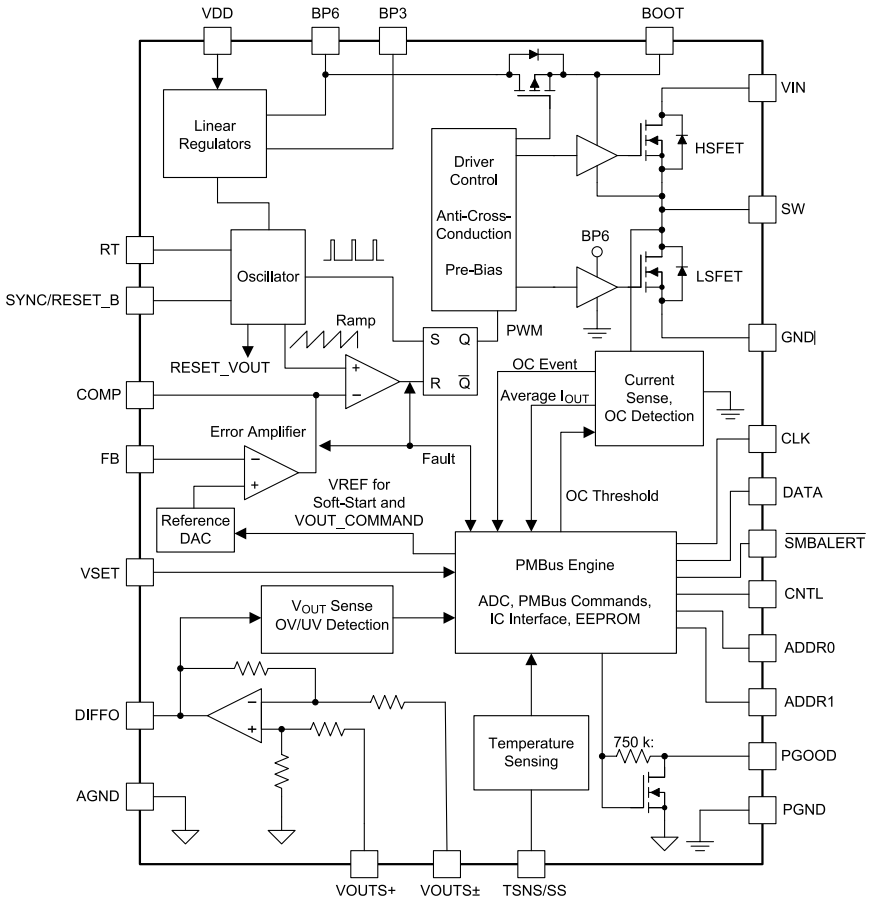

Figure 3. TPS544C25 Functional Block Diagram

3.3 Implementation

Although this TI Design follows the example and is similar to the PMBus control in the data manual, the difference is the value selected for R1. The output voltage control diagram for the device is in Figure 4. In the data manual, the example uses a 10-K resistor and the value in the TI Design is 6.81 K. The value of 6.81 K is required when using the LM10011 to generate the proper voltage at the output of the TPS544C25. The current flow through this resistor is minimal so the difference in the voltage drop between the two values does not have a significant effect on the output voltage of the supply. In PMBus mode, the voltage is changed by altering the reference voltage to the error amplifier rather than by monitoring the voltage drop across R1. Therefore, the 6.81-K resistor value has not been altered in this TI Design.

3.3.1 Output Voltage Control

The CVDD voltage range for the K2E SoC is within the 0.5-V to 1.5-V range of the V_{REF} DAC using the V_{OUT}_SCALE_LOOP value of 1. The SmartReflex™ range for the K2E SoC is 1.103- to 0.7 V in 64 steps with each step separated by approximately 6.396 mV. The TPS544C25 uses the V_{OUT}_COMMAND register to modify the VREF reference voltage to the error ampifier. The VREF voltage will be set to the initial voltage required for the SoC based on the RSET resistor value. For this design, the 7.87-KΩ resistor will set the initial value of VREF to 1.05 V. A reference voltage of 1.05 V on one leg of the error amplifier causes the TPS544C25 to generate 1.05 V at V_{OUT} to eliminate the voltage difference at the input of the error amplifier. The voltage at the FB pin, V_{FB}, is V_{DIFFO} + VR1. The power supply circuit attempts to regulate V_{OUT} so that V_{FB} is equal to V_{REF}. Because the current flow through R1 is normally in the nA range, a 6.81-K resistor for VR1 results in a µV drop and V_{OUT} closely approximates V_{DIFFO}. The Output Voltage Control Diagram for the device is shown in Figure 4.

In this design, the value of VREF is changed by modifying the value in the V_{OUT}_COMMAND register. Software running on the K2E SoC reads the required voltage level from the SmartReflex ™subsystem registers and send the proper V_{OUT} command using the I^2C interface connected to the PMBus input of the TPS544C25. When the value is written to the V_{OUT}_COMMAND register the VREF voltage at the error amplifier causes the TPS544C25 to drive V_{OUT} to the commanded voltage.

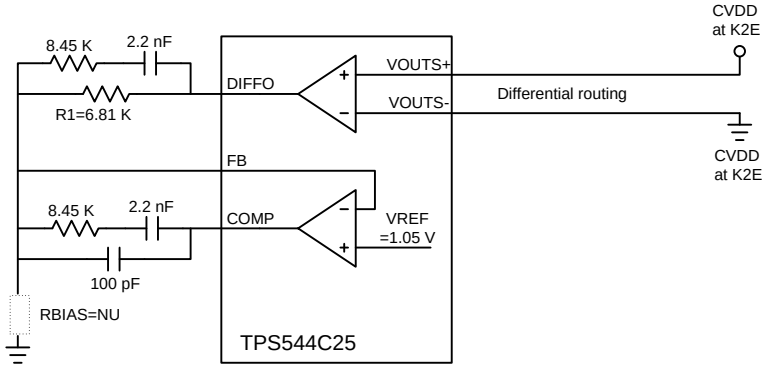

Figure 4. Output Voltage Control Diagram

3.3.2 Input Voltage

The VIN on the K2E SoC is 12 V, based on the source voltage for AMCC-compliant platforms. The TPS544C25 supports input voltages ranging from 4.5 V to 18 V and is more efficient at lower voltages. If you require an input voltage other than 12 V, check with the data manual and design collateral for the TPS544C25 to choose the correct support components.

3.3.3 Initial Voltage Control

The initial voltage required for the K2E SoC is 1.05 V, based on TI recommended operation conditions listed in the data manual, *Generating the AVS SmartReflex Core Voltage for the K2E Using the TPS544C25 and the LM10011* (TIDUA86). The TPS455C25 uses a resistor connected to the VSET pin to determine the initial voltage level of the part. In this design, V_{OUT} is set to 1.05 V as an initial voltage with a 7.87-kΩ resistor connected between the VSET pin and ground. The 7.87-kΩ resistor generates the V_{OUT}_COMMAND for 1.05 V.

3.3.4 Sense Voltage

The K2E SoC includes two sets of pins to monitor the CVDD voltage. The pins are connected to CVDD and GND as close to the die as possible to best represent of the voltage levels at the processing elements of the SoC. Either pair of pins can be used for the V_{OUT}S+ and V_{OUT}S- inputs to the TPS544C25. The traces for V_{OUT}+ and V_{OUT}- must be routed as a tightly-coupled differential pair. The design includes 10-Ω series resistors as well as a 100-Ω resistor to CVDD and a 100-Ω resistor to ground placed on the far side of the SoC. The 100-Ω resistors are included to ensure that the sense lines cannot float due to improper connection to the ball under the SoC. An unconnected ball can cause the power supply to regulate to a voltage beyond the limits allow by the SoC.

3.3.5 PMBus Connection

One of the I^2C ports of the K2E SoC must connect to the PMBus interface of the TPS544C25. The I2C interfaces for the K2E SoC operates at a voltage of 1.8 V, and the TPS544C25 requires a 3.3-V I^2C interface. Only I^2C level converters must convert the bus from 1.8 V to 3.3 V. TI designed the PCA9306 specifically for this function. The PCA9306 meets the I^2C bus requirements on both sides of the device. Simple level converters may not meet this requirement. Pullup resisters to the appropriate voltage must be included on both sides of the level converter.

4 Software Requirements

The K2E SoC device uses SmartReflex™ class 0 with temperature compensation to set the optimum core voltage level for each device. The K2E SoC has a SmartReflex™ controller, which is enabled once the device is removed from reset by releasing the PORz and the RESETFULLz. The SmartReflex™ controller sends the required VID values to the power supply using the VCNTL interface. For this design, the VCNTL interface is not used. Software must be used to read the required voltage and generate a V_{OUT} command. The command is transmitted to the TPS544C25 using an I^2C interface connected to the PMBus of the TPS544C25. Examples of the software for SmartReflex using the PMBus interface can be found in the latest MCSDK release supporting the K2E SoC. A copy of the *Smart Reflex Class0 Temperature Compensation User's Guide* is included with the documents for this TI Design.

5 PCB Layout Considerations

As with any high-current power supply design, the PCB layout must be correct to ensure the proper operation of the circuit and to minimize the switching noise introduced to the board. The schematic for this design highlights a number of layout considerations but lacks the requirements in the data manual, Generating the AVS SmartReflex Core Voltage for the K2E Using the TPS544C25 and the LM10011 (TIDUA86), and the requirements must be carefully reviewed. Some of the requirements for the K2E SoC PCB are shown in Figure 5.

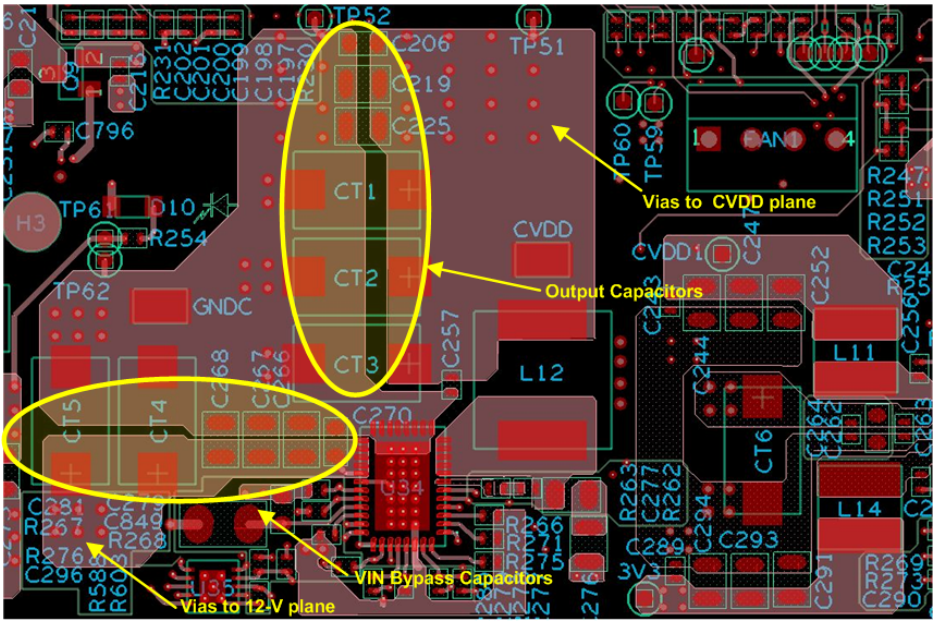

Figure 5. K2E SoC PCB Top Layer

5.1 Capacitor Placement

Proper placement of the VIN bypass capacitors and the output capacitors is required to reduce the loop inductance and to minimize noise. How the capacitors should be placed are shown in Figure 6 and Figure 7. All capacitors on the schematic page for the TPS544C25 are required to properly operate the power supply, and must be placed based on the layout guidelines provided in the data manual. All capacitors associated with VIN are on the top layer of the board with the high-frequency capacitors closest to the VIN pins of the TPS544C25. Local 12-V and ground planes are included for the capacitors on the top layer to reduce the loop inductance and to keep any ripple off the internal planes. Vias connect the local top layer planes with the internal planes. Multiple vias are required to support the necessary current flow. The output capacitors were connected in a similar fashion with local ground and CVDD planes on the top layer of the board.

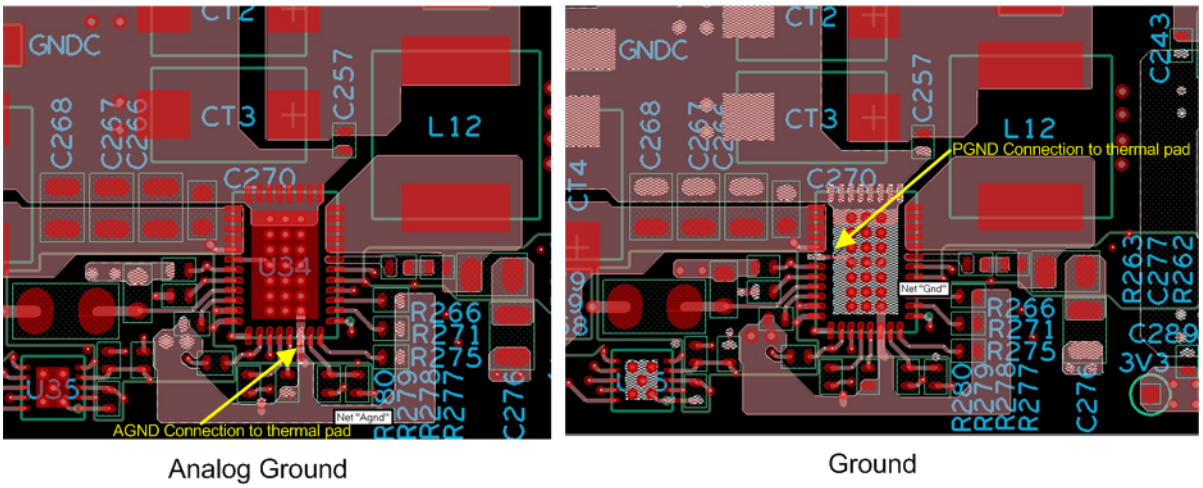

Figure 6. Analog Ground and Ground

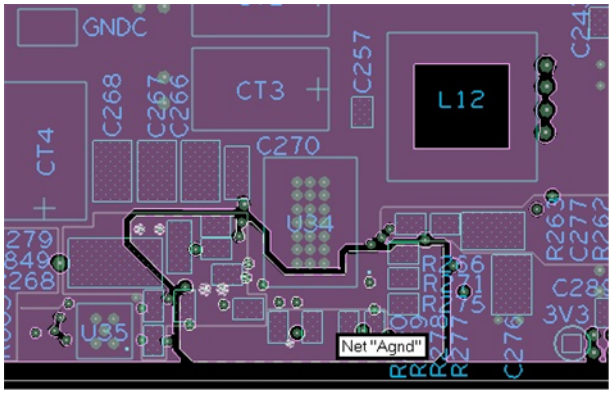

Figure 7. Analog Ground on Layer 2

5.2 Ground Layer Connections

The TPS544C25 device includes pins labeled AGND and PGND. The AGND and PGND pins are separate grounds. These pins must be routed as different planes and attached at a single point. The device uses a thermal pad under the body to dissipate heat to the PCB. The thermal pad is connected to a similar shape on the bottom of the board and to the ground planes with an array of vias. The top layer ground plane for the input and output capacitors must be connected to pins 13 to 20 and to the thermal pad on the top layer. A single trace on the top layer between the thermal pad, and pin 26 must be included. The BP3, BP6, and VDD Bypass Position is shown in Figure 8.

The analog ground is used by components on one side of the TPS544C25. A small plane is included to connect these components on the top layer. This is connected to a small cutout AGND plane on layer 2. A single point of connection to the board ground is made between the thermal pad and pin 38 using a trace on the top layer. AGND and PGND are not shorted in the schematic provided. A line and a layout note represent the single connection point between the thermal pad and the AGND pin 38, but AGND and GND appear as different nets in the netlist.

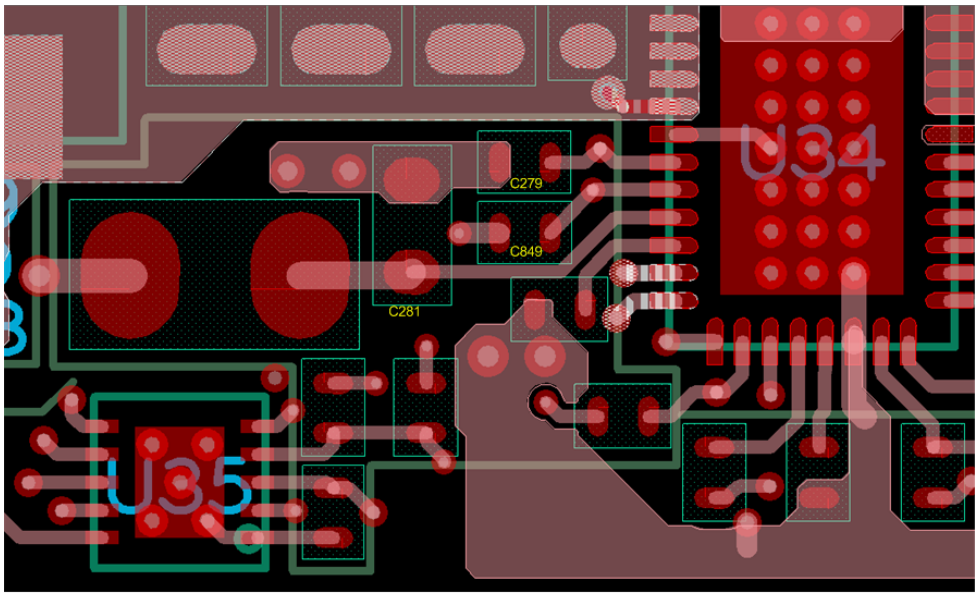

Figure 8. BP3, BP6, and VDD Bypass Position

5.3 Bypass for BP3, BP6, and VDD

The TPS544C25 has two internal regulators to provide power for the internal circuitry of the device. A bypass capacitor is required for each of these internal regulators on pins BP3 and BP6. A 2.2-µF capacitor is connected between BP6 and board ground. This capacitor is placed directly adjacent to the pin. A 2.2-µF capacitor is connected between BP3 and analog ground. This capacitor is also place directly adjacent to the pin. The VDD pin is the supply pin for the internal regulators. This pin is connected to the top layer 12-V VIN plane through a resistor and a bypass capacitor. The capacitors are also connected to analog ground. These components are also placed close to the TPS544C25.

5.4 Sense Line Routing

The sense lines terminating at $V_{OUT}S+$ and $V_{OUT}S–$ are connected to the CVDDCMON (J10) and VSSCMON (J9) pins on the K2E SoC. The R545 and R547 series resistors and R544 and R546 protection resistors are above the K2E SoC. A tightly-coupled differential trace pair is routed on inner layers approximately on the path shown in Figure 9. The sense line is routed around the area of the board for the DDR3 routing.

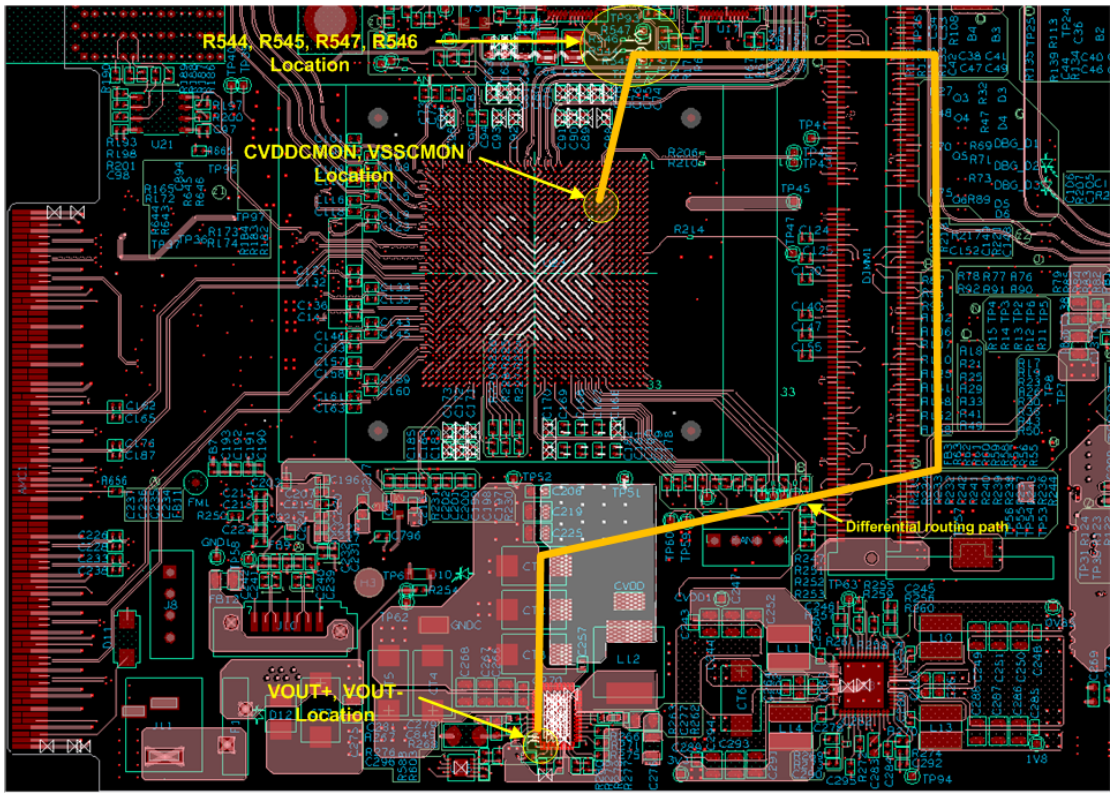

Figure 9. Sense Line Routing

5.5 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP0042.

6 References

1. *TPS544x25 4.5-V to 18-V, 20-A and 30-A SWIFT™ Synchronous Buck Converters with PMBus and Frequency Synchronization* (SLUSC81)
2. *PCA9306 Dual Bi-Directional I2C-Bus and SMBus Voltage Level-Translator* (SCPS113K)
3. *66AK2E05, 66AK2E02 Multicore DSP+ARM® KeyStone II System-on-Chip (SoC)* (SPRS865C)
4. *AM5K2E04, AM5K2E02 Multicore ARM KeyStone II System-on-Chip (SoC)* (SPRS864C)

7 About the Author

William Taboada is an application engineer at TI, where he supports the KeyStone I and KeyStone II multicore processor families. William brings to this role his extensive experience designing processor-based systems use DDR3 memory architecture and high-speed serial interfaces. William earned a Bachelor of Science (BS) from Lehigh University and a Master of Science (MS) from The George Washington University.

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