*TI Designs*

# *60-W, 24-V, High-Efficiency Industrial Power Supply With Precision Voltage, Current, and Power Limit*

## TI Designs

The TIDA-00702 is a 60-W, industrial AC-DC power supply designed for use in industrial and instrumentation systems such as process controls, factory automation, and machinery control. This reference design is a Quasi-resonant (QR) flyback converter implemented using the UCC28740 CC-CV flyback controller with optocoupled feedback for voltage and primary-side regulation (PSR) for constant current regulation, with all the necessary protections built-in. Hardware is designed and tested to pass conducted emissions, surge, and EFT requirements.

The key highlights of reference design:

- Reduced component count design to achieve NEC Class-2 and Limited Power Source (LPS) norms
- Meets ENERGY STAR® rating and 2013 EU eco-design directive Energy-related Products (ErP) Lot 6
- Robust output supply protected for output overcurrent, output short-circuit, output overvoltage, and over-temperature conditions

## Design Resources

| | |
|---|---|
| TIDA-00702 | Design Folder |
| UCC28740 | Product Folder |
| UCC24630 | Product Folder |
| LM5050-2 | Product Folder |
| TMP302 | Product Folder |
| CSD18504Q5A | Product Folder |

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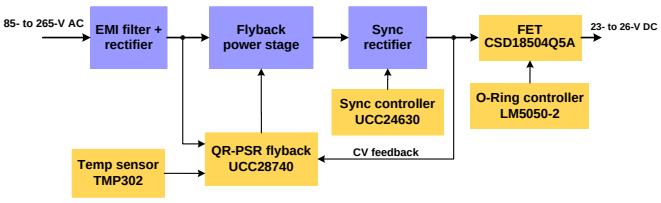
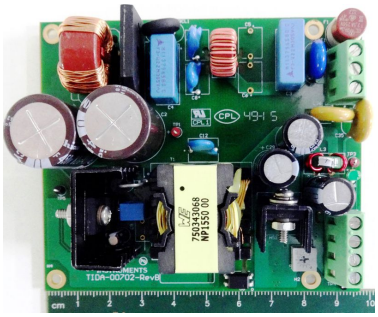
## Design Features

- Wide Operating Input Range of 85-V to 265-V AC With Full Power Delivery Over Entire Range
- Designed to Drive Wide Range of Downstream 24-V Industrial Systems and Motor Drives up to 60 W
- High Efficiency of > 89% at 115-V AC and > 91% at 230-V AC for Wide Load Range From 30% to 100% Load; No External Cooling Needed up to 60°C Ambient Operation
- Meets Current THD Regulations as per IEC 61000-3-2, Class-A
- Precision Current Limit Within ±1% Ensures Maximum Power Delivery for Entire AC Voltage Range
- Very Low Standby Power of < 200 mW
- Start-up With High Load Capacitance up to 8500 µF
- Built-in Lossless ORing Feature for Paralleling Multiple Modules
- Meets the Requirements of Conducted Emissions Standard – EN55011 Class B, EFT Norm IEC6000-4-4 – Level-3, and Surge Norm IEC61000-4-5 – Level-3
- Power Supply With Small PCB Form Factor (96 × 82 mm)

## Featured Applications

- Industrial DIN Rail Power
  - Process Control
  - Factory Automation
- Industrial LED Lighting
- Medical Power Supplies
- Security Systems



# 1 Key System Specifications

**Table 1. Key System Specifications**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CONDITIONS** | | | | | | |
| Input voltage | $V_{INAC}$ | | 85 | 115/230 | 265 | VAC |
| Frequency | $f_{LINE}$ | | 47 | 50 | 60 | Hz |
| No load power | $P_{NL}$ | $V_{INAC}$ = 230 V<br>$I_{OUT}$ = 0 A | | 0.17 | | W |
| Brownout voltage | $V_{IN\_UVLO}$ | | | | | |
| **OUTPUT CONDITIONS** | | | | | | |
| Output voltage | $V_{OUT}$ | | 23 | 24 | 26 | V |
| Output current | $I_{OUT}$ | | | | 2.5 | A |
| Line regulation | | | | | 0.3 | % |
| Load regulation | | | | | 1 | % |
| Output voltage ripple | $V_{RIPPLE}$ | | | 20 | 50 | mV |
| Output power | $P_{OUT}$ | | | 60 | 65 | W |
| Hold-up time | $t_{hold}$ | $V_{INAC}$ = 115 V | | > 22 | | ms |
| | | $V_{INAC}$ = 230 V | | > 100 | | ms |
| Primary-to-secondary insulation | | | | 4 | | kV |
| **SYSTEM CHARACTERISTICS** | | | | | | |
| Efficiency | η | $V_{IN}$ = $V_{NOM}$<br>$I_{OUT}$ = 20%, 40%, 60%, 80%, and 100% full load | 89 | | 91.7 | % |
| Protections | | Output overvoltage | | | | |
| | | Output overcurrent | | | | |
| | | Output short circuit | | | | |
| | | Input UVLO | | | | |
| | | Thermal shutdown | | | | |
| | | Output open loop protection | | | | |
| Operating ambient | | Open frame | –40 | 25 | 60 | °C |
| Power line harmonics | | | As per IEC61000-3-2 Class-A | | | |
| Conducted emissions | | | As per EN55022/11 Class-B | | | |
| EFT | | | As per IEC-61000-4-4, Level-3 | | | |
| Surge | | | As per IEC-61000-4-5, Level-3 | | | |
| Dimensions | | Length × Breadth × Height | 96 × 82 × 40 | | | mm |

## 2 System Description

Industrial power supplies are used in various applications such as process control, data logging, machinery control, instrumentation, factory automation, and security systems. These AC-DC supplies provide a convenient means for powering DC operated devices including programmable logic controllers (PLCs), sensors, transmitters or receivers, analyzers, motors, actuators, solenoids, relays, and so on. These supplies are convection cooled, so no cooling fans are needed. The AC/DC power supplies can deliver full load over a wide operating input voltage range from 85- to 265-V AC. The output voltages from these supplies range from 5 V up to 56 V with power ratings from 7.5 W up to 480 W. Many of these supplies can be connected in parallel for higher power applications. A typical block diagram of <100-W industrial power supply without PFC converter is shown in Figure 1.

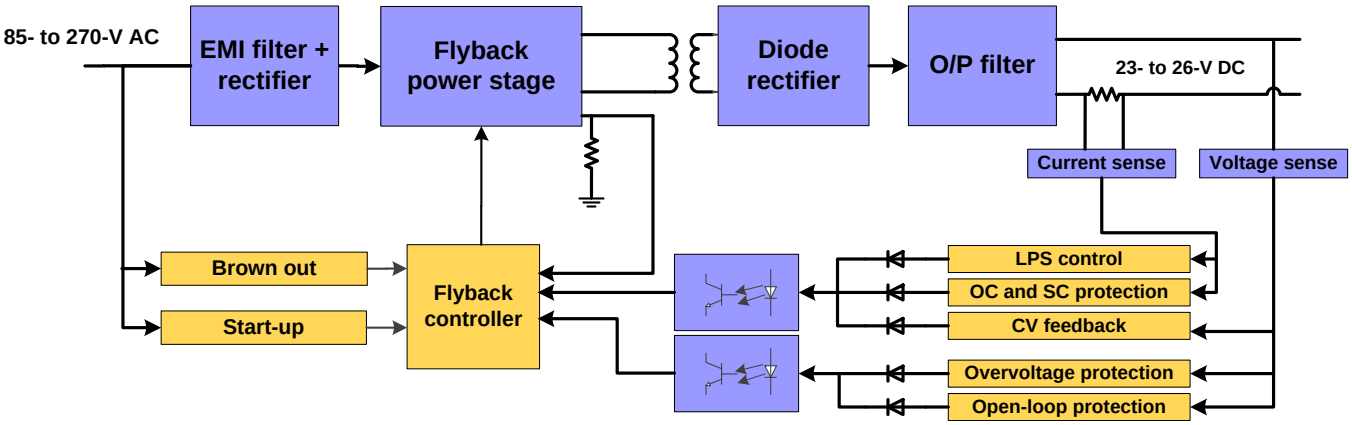



**Figure 1. Typical Block Diagram of 60- to 100-W Industrial Power Supply**

This reference design is a 60-W industrial power supply, designed with specific focus to meet the NEC Class-2 and Limited Power Source (LPS) norms. The design consists of a QR PSR flyback DC/DC converter and synchronous controller for secondary side rectification. Input voltage range is 85-V to 265-V AC RMS and the output voltage range is 23 to 26 V, with 24-V nominal operation. The output voltage range is set using the potentiometer present on the board. Industrial power supplies require high efficiency over their entire operating voltage range and wide load variations from 50% to 100%. This design demonstrates high efficiency operation in a small form factor (96 × 82 mm) and delivers continuous 60-W power over entire operating range from 85-V to 265-V AC with >91% efficiency for 230-V AC nominal operation and >89% for 115-V AC nominal operation.

This reference design eliminates multiple feedback loops for open loop detection, current limit and power limiting, by using a precise CC-CV flyback controller UCC28740. Block diagram of industrial power supply implemented with PSR and reduced feedback loops is shown in Figure 2. The elimination of discrete circuitry and associated components, generally used to implement multiple feedback loops for protection and power limiting, aids in increasing the product life. In addition, the high efficiency of the DC/DC converter is achieved with the UCC28740 controller's built-in quasi-resonant valley-switching operation.

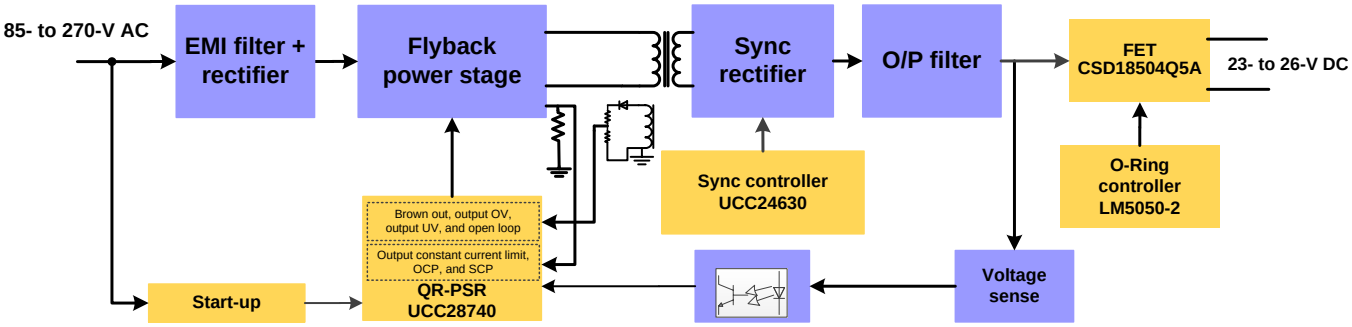



**Figure 2. Block Diagram of Industrial Power Supply Implemented With PSR and Reduced Feedback Loops**

The design has secondary side rectification implemented using the UCC28630 synchronous rectification controller to achieve high efficiency and optimize power loss. The design has lossless ORing circuit implemented using the LM5050-2 ORing controller for paralleling multiple modules to meet extended high power needs. The design has low standby power of < 200 mW and meets ENERGY STAR rating requirements as well as 2013 EU eco-design directive ErP Lot 6.

The EMI filter is designed to meet EN55011/22 class-B conducted emission levels. The design is fully tested and validated for various parameters such as regulation, efficiency, EMI signature, output ripple, start-up, and switching stresses.

Overall, the design meets the key challenges of industrial power supplies to provide safe and reliable power with all protections built-in, while delivering high performance with low power consumption and low bill-of-material (BOM) cost.

## 3 Block Diagram

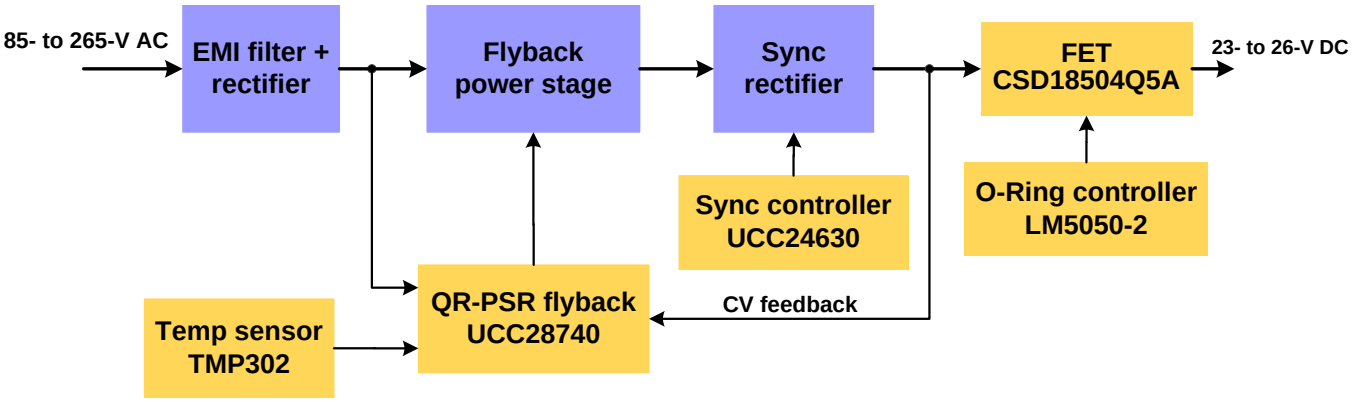



**Figure 3. Block Diagram of 60-W DIN Rail Power Supply**

### *3.1 Highlighted Products and Key Advantages*

This TI Design uses the following products. This section highlights key features that make these devices suitable for this reference design. Find the complete details of the highlighted devices in their respective datasheets.

#### 3.1.1 UCC28740 CV-CC Flyback Controller

To implement the high-performance, small form factor flyback designs up to 100-W power, the UCC28740 is preferred controller as it offers a series of benefits to address the next generation industrial power supply needs of a reduced number of feedback loops for precision current and power limits, eliminating the need of current sensing on secondary side and multiple optocoupler feedback loops for open-loop detection and power limiting.

The UCC28740 isolated-flyback power supply controller provides CV output regulation using an optical coupler to improve transient response under large load steps. CC regulation is accomplished through the PSR technique. This device processes information from optocoupled feedback and from an auxiliary flyback winding for precise high-performance control of output voltage and current. An internal 700-V start-up switch, dynamically-controlled operating states and a tailored modulation profile support ultra-low standby power without sacrificing start-up time or output transient response. The drive output interfaces to a MOSFET power switch. Discontinuous conduction mode (DCM) with valley-switching reduces switching losses. Modulation of switching frequency and primary current peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges.

Key features that make this device unique are:

- Optocoupled feedback regulation for CV and PSR for CC
- Enables ±1% voltage regulation and ±5% current regulation across line and load
- 100-kHz max. switching frequency enables high-power density designs
- QR valley switching operation for highest overall efficiency
- Frequency jitter scheme to ease EMI compliance
- Wide VDD range (35 V) allows small bias capacitor
- Drive output for MOSFET
- Enables <10-mW system standby power
- Protection functions: Overvoltage, low line, and overcurrent
- SOIC-7 package

### 3.1.2 UCC24630 Synchronous Rectifier Controller With Ultra-Low Standby Current

High-efficiency designs need synchronous rectification to optimize the power loss. The UCC24630 offers great benefits and simplicity in design, offering near-ideal diode rectifier function.

The UCC24630 SR controller is a high-performance controller and driver for N-channel power MOSFET devices used for secondary-side synchronous rectification. The combination of the controller and MOSFET driver emulates a near ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier but also reduces primary-side losses as well, due to compounding of efficiency gains. Utilizing TI's patented volt-second balancing control method, the UCC24630 is ideal for flyback power supplies over a wide output voltage range because the IC is not connected directly to the MOSFET drain. The UCC24630 controller offers a programmable false-trigger filter, a frequency detector to automatically switch to standby mode during low power conditions and pin fault protections. The UCC24630 is compatible with DCM, TM, and CCM operation. The wide VDD operating range, wide programming range of the VPC voltage, and blanking time allow use in a variety of flyback converter designs.

Key features that make this device unique are:

- Volt-second balance SR on-time control
- 5- to 24-V output voltage flyback converters
- 150-µA IC current consumption at no load
- Auto low power detect and standby mode for minimal standby power impact
- Compact SOT-23-6 package
- Operating frequency up to 200 kHz
- Pin fault protection for open and short

### 3.1.3 LM5050-2 High-Side ORing FET Controller

Using a diode for the ORing function results in heavy loss due to its high forward voltage drop. As the ORing function results in continuous power dissipation, it is preferred to have FET for reduced losses. The LM5050-2 is the best fit as it provides accurate high-voltage ORing FET control in a tiny package.

The LM5050-2 controller provides charge pump gate drive for an external N-Channel MOSFET and a fast response comparator to turn off the FET when current flows in the reverse direction.

Key features that make this device unique are:

- Wide operating input voltage range, $V_{IN}$: 5 to 75 V
- 100-V transient capability
- Charge pump gate driver for external N-Channel MOSFET
- Fast 50-ns response to current reversal
- FET test mode indicates shorted FET
- 2-A peak gate turn-off current
- Minimum $V_{DS}$ clamp for faster turn-off
- Package: SOT-6 (Thin SOT-23-6)

### 3.1.4 TMP302 Easy-to-Use, Low-Power, Low-Supply Temperature Switch

The TMP302 is a temperature switch in a micro package (SOT563). The TMP302 offers low power (15-µA maximum) and ease-of-use through pin selectable trip points and hysteresis. These devices require no additional components for operation. They can function independent of microprocessors or microcontrollers. The TMP302 is available in several different versions.

Key features that make this device unique are:

- Low supply voltage range: 1.4 to 3.6 V
- Low power: 15 µA (maximum)
- Trip-point accuracy: ±0.2°C (typical) from 40°C to 125°C
- Pin-selectable trip points
- Open-drain output
- Pin-selectable hysteresis: 5°C and 10°C

### 3.1.5 CSD18504Q5A 40-V N-Channel NexFET™ Power MOSFET

For continuous ON ORing functions, it is important to select a MOSFET with low $R_{DS(ON)}$ and compatible with ORing controller. Due to these requirements, the CSD18504Q5A is the best fit.

Key features that make this device unique are:

- Very low $R_{DS(ON)}$ of 5.6 mΩ
- Ultra-low $Q_g$ and $Q_{gd}$
- Low thermal resistance

# 4 System Design Theory

This reference design provides 60 W of continuous power over a wide AC input range from 85- to 230-V AC. The design has flyback power stage implemented using UCC28740 QR PSR CC-CV flyback controller to deliver 24 V and 2.5 A. The total system efficiency is over 91% with a 230-V AC input and over 89% with a 115-V AC input under full load conditions. The design has precise current limit and limits the power to ≤ 60 W under all fault conditions. In addition, several protections are embedded into this design, which includes input undervoltage protection and output short circuit protection.

In addition, the main focus of this design is a low EMI, high efficiency, to meet IEC-61000-2-3 norms, and a protected DC power rail for targeted applications.

## *4.1 QR Flyback Converter With PSR*

Flyback converters provide a cost effective solution for AC/DC conversion needs. They are widely used for AC/DC converters up to 150 W. There are three modes of operation namely discontinuous mode (DCM), QR Mode (QRM) and continuous conduction mode (CCM). For lower power applications, the DCM or QR mode is preferred as they have reduced power losses and optimal peak currents in low-power applications. As the output wattage increases, CCM becomes more efficient due to the reduced peak and RMS currents.

Flyback converters designed with PSR flyback controllers eliminate the use of conventional optocoupler based feedback. The PSR flyback controllers sense the voltage feedback through auxiliary winding and current feedback through the current sense resistor used in series with switching FET. In addition, Texas Instruments PSR flyback controllers provide a wide range of protections and accurate limiting of both current and power. The UCC28740 controller has both PSR feedback and opto-feedback, enhancing the reliability of the system.

## *4.2 Flyback Circuit Component Design*

The UCC28740 is a flyback controller that provides both CV mode and constant current (CC) mode control for precise output regulation. While in CV operating range, the controller uses an optocoupler for tight voltage regulation and improved transient response to large load steps. Accurate regulation while in CC mode is provided by primary side control. The UCC28740 uses frequency modulation, peak primary current modulation, valley switching, and valley hopping in its control algorithm to maximize efficiency over the entire operating range.

The design process and component selection for this design are illustrated in the following sections. All design calculations are available in "TIDA-00702_Design_Calculator".

### 4.2.1 Design Goal Parameters

Table 2 elucidates the design goal parameters for this design. These parameters will be used in further calculations to select components.

**Table 2. Design Goal Parameters**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| $V_{IN}$ | Input voltage | 85 | 115/230 | 265 | VAC |
| $f_{LINE}$ | Input frequency | 47 | 50/60 | 63 | Hz |
| | Brown out voltage | | 70 | | VAC |
| **OUTPUT** | | | | | |
| $V_{OUT}$ | Output voltage | 23 | 24 | 26 | VDC |
| $I_{OUT}$ | Output current | | 2.5 | | VDC |
| $P_{OUT}$ | Output power | | 60 | | W |
| | Line regulation | | | 5% | |
| | Load regulation | | | 5% | |
| $F_{MAX}$ | Maximum desired switching frequency | | | 65 | kHz |
| η | Targeted efficiency | | 85% | | |

### 4.2.2 Input Bulk Capacitance and Minimum Bulk Voltage

The value of the bulk capacitor used determines the minimum input voltage for the flyback converter. This in turn determines the primary-to-secondary turns ratio of the transformer.

Input capacitance value, $C_{BULK}$ , is based on the maximum load power, converter efficiency, minimum operational input voltage, and minimal operational input frequency.

Maximum AC input power is determined by the $V_{OCV}$, $I_{OCC}$, and full-load efficiency targets.

Primary output: $V_{OUT} = V_{OCV} = 24$ V

The converter is designed for 2.5 A of maximum output current on primary output and is designed to limit the current at 2.5 A for overload conditions. So, $I_{OCC} = 2.5$ A.

Total maximum output power need is

$$P_{OUT} = V_{OUT} \times I_{OCC}$$

$$P_{OUT} = 24 \times 2.5 = 60.0 \text{ W} \quad (1)$$

To calculate component specifications, the minimum targeted efficiency is considered as η =85 %.

$$P_{IN} = \left(\frac{P_{OUT}}{\eta}\right) = \frac{60.0}{0.85} = 70.6 \text{ W} \quad (2)$$

Equation 3 provides an accurate solution for input capacitance needed to achieve a minimum bulk valley voltage target $V_{BULK(min)}$. Alternatively, if a given input capacitance value is prescribed, one can calculate the $V_{BULK(min)}$ expected for that capacitance.

$$C_{BULK} = \frac{2P_{IN} \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right)}{\left(2V_{IN(min)}^{2} - V_{BULK(min)}^{2}\right) \times f_{LINE}} \quad (3)$$

The minimum recommended valley voltage on the input bulk capacitors is taken as 60% of the peak of the minimum AC voltage.

$$V_{BULK(min)} = V_{IN(min)} \times \sqrt{2} \times 0.6$$

$$V_{BULK(min)} = 85 \times \sqrt{2} \times 0.6 = 72.14\ V \tag{4}$$

$$C_{BULK} \geq \frac{2 \times 70.6\,W \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{72.14\ V}{\sqrt{2} \times 85\ V}\right)\right)}{\left(2 \times 85\ V^2 - 72.14\ V^2\right) \times 50}$$

$$C_{BULK} \geq 107.7\ \mu F$$

To meet the needs of hold up time, bulk capacitance is selected higher than this calculated value. The bulk capacitor selected is 82 µF × 2 = 164 µF.

Using Equation 3 and $C_{BULK}$ = 164 µF, $V_{BULK(min)}$ = 86.7 V.

Calculate input capacitor charge time ($t_{CH}$) based on $V_{BULK(min)}$:

$$t_{CH} = \frac{1 - \sin^{-1}\left[\frac{\sqrt{2} \times V_{IN(min)} - V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right]}{4 \times 50\ Hz}$$

$$t_{CH} = \frac{1 - \sin^{-1}\left[\frac{\sqrt{2} \times 85\ V - 86.7\ V}{\sqrt{2} \times 85\ V}\right]}{4 \times 50} = 3.6\ ms \tag{5}$$

To calculate the longest period of the rectified line voltage (full bridge rectification):

$$t_{RL} = \frac{1}{2 \times 47} = 10.6\ ms \tag{6}$$

The minimum input capacitor RMS ripple current rating is given by

$$I_{CINripple} = \frac{C_{BULK} \times \left(\sqrt{2} \times V_{IN(min)} - V_{BULK(min)}\right)}{t_{RL} - t_{CH}} \times \sqrt{3}$$

$$I_{CINripple} = \frac{164\ \mu F \times \left(\sqrt{2} \times 85\ V - 86.7\ V\right)}{10.6\ ms - 3.6\ ms} \times \sqrt{3} = 1359.4\ mA \tag{7}$$

For this design, two capacitors (C2 and C3) with a 450-V rating need to be used to meet the maximum AC voltage rating of 300-V AC. To ensure high temperature long life product, a capacitor load life of 10,000 to 12,000 hours at 105°C operation is recommended. This design uses Nichicon part number UCY2W820MHD6.

### 4.2.3 Bridge Rectifier and Fuse Selection

To calculate peak AC input current:

$$I_{PKAC} = \left( \frac{2 \times \frac{P_{IN}}{V_{BULK(min)}}}{\sqrt{\frac{t_{CH}}{t_{RL}}}} \right)$$

$$I_{PKAC} = \left( \frac{2 \times \frac{70.6\ W}{86.7\ V}}{\sqrt{\frac{3.6\ ms}{21.27\ ms}}} \right) = 3.96\ A \quad (8)$$

The bridge rectifier current rating is determined by current at minimum bulk voltage:

$$I_{DAPK} = \left( \frac{2 \times P_{IN}}{V_{BULK(min)}} \right)$$

$$I_{DAPK} = \left( \frac{2 \times 70.6\ W}{86.7\ V} \right) = 1.63\ A \quad (9)$$

As the input AC voltage can go up to 300-V AC, the DC voltage can reach voltage levels of up to 425-V DC. A higher rated current bridge rectifier can help reduce the power loss in rectifier; therefore, this design uses a 600-V, 6-A GBU6J for input rectification.

The bridge rectifier losses are determined by average bridge rectifier current. The average bridge rectifier current is highest at minimum AC line voltage and is determined by

$$I_{DA} = \left( \frac{P_{IN}}{\frac{2}{\pi} \times \sqrt{2} \times V_{IN(min)}} \right)$$

$$I_{DA} = \left( \frac{70.6\ W}{\frac{2}{\pi} \times \sqrt{2} \times 85} \right) = 0.92\ A \quad (10)$$

Forward voltage drop of bridge rectifier diode, $V_{FDA}$ = 0.90 V.

Estimated power dissipated in bridge rectifier diode ($P_{DA}$) is

$$P_{DA} = V_{DA} \times I_{DA} = 2 \times 0.9 \times 0.92 = 1.656\ W \quad (11)$$

### 4.2.4 Transformer Parameter Calculations: Turns Ratio, Primary Inductance, and Peak Primary Current

The target maximum switching frequency at full-load, the minimum input-capacitor bulk voltage, and the estimated DCM QR time determine the maximum primary-to-secondary turns-ratio of the transformer.

First determine the maximum-available total duty-cycle of the on-time and secondary conduction time based on the target switching frequency, $F_{MAX}$, and DCM resonant time. For DCM resonant frequency, assume 500 kHz if an estimate from previous designs is not available. At the transition-mode operation limit of DCM, the interval required from the end of secondary current conduction to the first valley of the $V_{DS}$ voltage is half of the DCM resonant period ($t_R$), or 1 µs assuming a 500-kHz resonant frequency. The maximum allowable MOSFET on-time $D_{MAX}$ is determined using Equation 12.

$$D_{MAX} = 1 - D_{MAGCC} - F_{MAX} \times \frac{t_R}{2} \tag{12}$$

where

- $t_R$ is the estimated period of the LC resonant frequency at the switch node
- $D_{MAGCC}$ is defined as the secondary-diode conduction duty-cycle during CC operation and is fixed internally by the UCC28740 at 0.425

$$t_R = 2\,\mu s$$

$$D_{MAX} = 1 - 0.425 - 65\ kHz \times \frac{2\ \mu s}{2} = 0.51$$

When $D_{MAX}$ is known, the maximum primary-to-secondary turns-ratio is determined with Equation 13. Calculate the total voltage on the secondary winding by adding $V_{OCV}$, $V_F$, and $V_{OCBC}$.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times \left(V_{OCV} + V_F + V_{OCBC}\right)} \tag{13}$$

$V_{OCBC}$ is the additional voltage drop of post filter inductor and any other target cable-compensation voltage added to $V_{OCV}$ (provided by an external adjustment circuit applied to the shunt-regulator). Set $V_{OCV}$ equal to 0 V if not used. In the current design as post LC filter is used, $V_{OCBC}$ is considered as voltage drop across the inductor.

$$V_{OCBC} = DCR_L \times I_{OCC} = 6.75\ m\Omega \times 2.5\ A = 16.875\ mV$$

$$N_{PS(max)} = \frac{0.51 \times 86.7\ V}{0.425 \times \left(24\ V + 0.4\ V + 0.01688\ V\right)} = 4.261$$

A higher turns-ratio generally improves efficiency, but may limit operation at low input voltage.

The transformer turns ratio selected affects the MOSFET $V_{DS}$ and secondary rectifier reverse voltage, so these should be reviewed. The UCC28740 requires a minimum on time of the MOSFET ($t_{ON(min)}$) and minimum secondary rectifier conduction time ($t_{DM(min)}$) in the high line and minimum load condition. The selection of $F_{MAX}$, $L_P$, and $R_{CS}$ affects the minimum $t_{ON(min)}$ and $t_{DM(min)}$.

The secondary rectifier and MOSFET voltage stress can be determined by Equation 14 and Equation 15, respectively.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \tag{14}$$

For the MOSFET $V_{DS}$ voltage stress, include an estimated leakage inductance voltage spike ($V_{LK}$).

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F + V_{OCBC}\right) \times N_{PS} + V_{LK} \tag{15}$$

Equation 16 determines if $t_{ON(min)}$ exceeds the minimum $t_{ON}$ target of 280 ns (maximum $t_{CSLEB}$). Equation 17 verifies that $t_{DM(min)}$ exceeds the minimum $t_{DM}$ target of 1.2 µs.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \tag{16}$$

where

- $K_{AM}$ denotes the AM control ratio

$$t_{DM(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \tag{17}$$

To determine the optimum turns-ratio $N_{PS}$, design iterations are generally necessary to optimize and evaluate system-level performance trade-offs and parameters mentioned in Equation 14 to Equation 17. The design spreadsheet provides an easy way to iterate and arrive at the optimum value for $N_{PS}$.

When the optimum turns-ratio $N_{PS}$ is determined from a detailed transformer design, use this ratio for the following parameters. For this design, $N_{PS}$ = 3.9 is selected on optimization.

The UCC28740 CC regulation is achieved by maintaining $D_{MAGCC}$ at the maximum primary peak current setting. The product of $D_{MAGCC}$ and $V_{CST(max)}$ defines a CC-regulating voltage factor $V_{CCR}$, which is used with $N_{PS}$ to determine the current-sense resistor value necessary to achieve the regulated CC target, $I_{OCC}$ (see Equation 18).

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \tag{18}$$

Because a small portion of the energy stored in the transformer does not transfer to the output, a transformer efficiency term is included in Equation 18. This efficiency number includes the core and winding losses, the leakage-inductance ratio, and a bias-power to maximum-output-power ratio. For example, an overall transformer efficiency of 0.9 is a good estimate based on 3.5% leakage inductance, 5% core and winding loss, and 0.5% bias power. Adjust these estimates as needed based on each specific application.

$$R_{CS} = \frac{0.318\ V \times 3.9 \times \sqrt{0.9}}{2 \times 2.5\ A} = 0.235\ \Omega$$

$V_{CCR(min)}$ is the minimum CC regulation factor and device parameter = 0.318 V

The standard value of the current sense resistor selected is $R_{CS}$ = 0.26 Ω; a parallel resistor to $R_{CS}$ is added in the schematic to easily adjust values.

For primary inductance calculation, determine the transformer primary peak current using Equation 19. Peak primary current is the maximum current-sense threshold divided by the current-sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \tag{19}$$

$$I_{PP(max)} = \frac{0.81\ V}{0.26\ \Omega} = 3.115\ A$$

$$I_{PP(nom)} = \frac{0.773\ V}{0.26\ \Omega} = 2.973\ A$$

The primary transformer inductance is calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output voltage and current targets, and transformer power losses are included in Equation 19. First, determine the transformer primary peak current using Equation 20. Peak primary current is the maximum current-sense threshold divided by the current-sense resistance.

$$L_P = \frac{2\left(V_{OCV} + V_F\ V_{OCBC}\right) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \tag{20}$$

$$L_P = \frac{2 \times (24\ V + 0.4\ V + 0.01688\ V) \times 2.5}{0.9 \times 2.973\ A^2 \times 65\ kHz} = 236\ \mu H$$

The actual primary inductance selected is $L_P$ = 240 µH.

$N_{AS}$ is determined by the lowest target operating output voltage while in CC regulation and by the VDD UVLO turn-off threshold of the UCC28740. Additional energy is supplied to VDD from the transformer leakage-inductance, which allows a lower turns-ratio to be used in many designs.

$$N_{AS} = \frac{V_{VDD(off)} + V_{FA}}{V_{OCC} + V_F} \tag{21}$$

$$N_{AS} = \frac{8.15\ V + 0.9\ V}{12\ V + 0.4\ V} = 0.73$$

### 4.2.5 Transformer Parameter Calculations: Primary and Secondary RMS Currents

With a primary inductance of 230 µH, the absolute maximum switching frequency is calculated from Equation 20:

$$f_{MAX} = \frac{2 \times (24\ V + 0.4\ V + 0.01688\ V) \times 2.5}{0.9 \times 2.973\ A^2 \times 240\ \mu H} = 56.72\ kHz \quad (22)$$

The maximum switching period is

$$t_{SW} = \frac{1}{f_{MAX}} = \frac{1}{56.72\ kHz} = 17.63\ \mu s \quad (23)$$

The actual maximum ON-time is given by

$$t_{ON(max)} = \frac{I_{PP(nom)} \times L_P}{V_{BULK(min)}}$$

$$t_{ON(max)} = \frac{2.973\ A \times 240\ \mu H}{86.7\ V} = 8.23\ \mu s \quad (24)$$

The maximum duty cycle of operation $D_{MAX}$ is

$$D_{MAX} = \frac{t_{ON(max)}}{t_{SW}} = \frac{8.23\ \mu s}{17.63\ \mu s} = 0.467 \quad (25)$$

The transformer primary RMS current ($I_{PRMS}$) is

$$I_{PRI\_RMS} = I_{PP(nom)} \times \sqrt{\frac{D_{MAX}}{3}}$$

$$I_{PRI\_RMS} = 2.973\ A \times \sqrt{\frac{0.467}{3}} = 1.173\ A \quad (26)$$

The transformer secondary peak current RMS current ($I_{SPK}$) is

$$I_{SP(max)} = I_{PP(nom)} \times N_{PS} = 2.973\ A \times 3.9 = 11.595\ A \quad (27)$$

The transformer secondary RMS current ($I_{SRMS}$) is

$$I_{SEC\_RMS} = I_{SP(max)} \times \sqrt{\frac{D_{MAG}}{3}}$$

$$I_{SEC\_RMS} = 11.595 \times \sqrt{\frac{0.425}{3}} = 4.364\ A \quad (28)$$

Based on these calculations, a Wurth Electronik transformer was designed for this application (part number 750343068), which has the following specifications:

- $N_{PS}$ = 3.9
- $N_{PA}$ = 5
- $L_P$ = 240 µH
- $L_{LK}$ = 3.5 µH
- LLK denotes the primary leakage inductance

### 4.2.6 Main Switching Power MOSFET Selection

The drain-to-source RMS current, $I_{DS\_RMS}$, through switching FET is calculated as

$$I_{DS\_RMS} = \frac{I_{PP(max)}}{\sqrt{3}} \times \sqrt{D_{MAX}}$$

$$I_{DS\_RMS} = \frac{3.115}{\sqrt{3}} \times \sqrt{0.467} = 1.229 \text{ A} \quad (29)$$

It is recommend to select a MOSFET with five times the $I_{DS\_RMS}$ calculated in Equation 29.

Estimate the maximum voltage across the FET using Equation 15. Considering a de-rating of 5%, the voltage rating of the MOSFET should be 650-V DC. The AOTF11S65L MOSFET of 650 V and 11 A at 25°C or 8 A at 100°C is selected for this TI Design.

The recommended clamping voltage on the drain is

$$V_{DRAIN\_Clamp} = 0.95 \times V_{DS} - \left(\sqrt{2} \times V_{IN(max)} + N_{PS} \times \left(V_{OCV} + V_F + V_{OCBC}\right)\right)$$

$$V_{DRAIN\_Clamp} = 0.95 \times 650 \text{ V} - \left(\sqrt{2} \times 265 \text{ V} + 3.9 \times \left(24.4169 \text{ V}\right)\right) = 147.55 \text{ V} \quad (30)$$

### 4.2.7 Rectifying Diode and Synchronous Rectification MOSFET Selection

Calculate the secondary output diode or synchronous rectifier FET reverse voltage or blocking voltage needed ($V_{DIODE\_BLOCKING}$) with

$$V_{DIODE\_BLOCKING} = \frac{\sqrt{2} \times V_{IN(max)} + V_{DRAIN\_Clamp}}{N_{PS}} + V_{OUT\_OVP} + V_{OCBC}$$

$$V_{DIODE\_BLOCKING} = \frac{\sqrt{2} \times 265 \text{ V} + 147.55 \text{ V}}{3.9} + 30 \text{ V} + .0169 \text{ V} = 163.93 \text{ V} \quad (31)$$

The required minimum rectified output current is $I_{DOUT} = I_{DS\_RMS} = 4.364$ A.

A synchronous rectifier FET is recommended for low power loss and high efficiency needs. This design uses the IRFI4227PBF-ND to optimize the on-state losses.

### 4.2.8 Select Output Capacitors

For this design, the output capacitor ($C_{OUT}$) for output was selected to prevent $V_{OUT}$ (24 V) from dropping below the minimum output voltage ($V_{OTRM}$) during transients up to 0.30 ms and a ripple voltage less than 50 mV.

$$V_{OTRM} = 23.7 \text{ V}$$

$$C_{OUT} \geq \frac{\frac{I_{OUT}}{2} \times (t)}{V_{OUT} - V_{ORTM}}$$

$$C_{OUT} \geq \frac{\frac{2.5 \text{ A}}{2} \times (0.30 \text{ ms})}{(24 - 23.7)} = 1250 \text{ µF} \quad (32)$$

Considering the allowable output ripple voltage of 120 mV (5%), the ESR of the capacitor should be

$$ESR = \frac{V_{OUT\_RIPPLE}}{I_{SEC(max)}} = \frac{120 \text{ mV}}{11.595 \text{ A}} = 10.35 \text{ m}\Omega \quad (33)$$

$$I_{COUT\_RMS} = \sqrt{\left(I_{SEC\_RMS}\right)^2 - \left(I_{OUT}\right)^2}$$

$$I_{COUT\_RMS} = \sqrt{(4.364)^2 - (2.5)^2} = 3.576 \text{ A} \quad (34)$$

An 820-µF × 2, 35-V capacitor was selected on the output. A post LC filter suppresses the differential mode noise at the output.

### 4.2.9 Capacitance on VDD Pin

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in CC regulation.

The capacitance on VDD must supply the primary-side operating current used during start-up and between low frequency switching pulses. The largest result of two independent calculations denoted in Equation 35 and Equation 36 determines the value of $C_{VDD}$.

At start-up, when $V_{VDD(on)}$ is reached, $C_{VDD}$ alone supplies the device operating current and MOSFET gate current until the output of the converter reaches the target minimum-operating voltage in CC regulation, $V_{OCC}$. Now the auxiliary winding sustains VDD for the UCC28740 above the UVLO. The total output current available to the load and to charge the output capacitors is the CC-regulation target, $I_{OCC}$. Equation 35 assumes that all of the output current of the converter is available to charge the output capacitance until $V_{OCC}$ is achieved. For typical applications, Equation 35 includes an estimated $Q_G f_{SW(max)}$ of average gate-drive current and a 1-V margin added to $V_{VDD}$.

$$C_{VDD} \geq \frac{\left(I_{RUN} + Q_G f_{SW(max)}\right) \times \left(\frac{C_{OUT} \times V_{OCC}}{I_{OCC}}\right)}{V_{VDD(on)} - \left(V_{VDD(off)} + 1\,V\right)} \tag{35}$$

$$C_{VDD} \geq \frac{(1\,mA + 2.65\,mA) \times (2110\,\mu F \times 12)}{(23\,V - 8.15\,V - 1) \times 2.5\,A} = 2.67\,\mu F$$

During a worst-case load transient event from full-load to no-load, $C_{OUT}$ overcharges above the normal regulation level for duration of $t_{OV}$ until the output shunt-regulator loading is able to drain $V_{OUT}$ back to regulation. During $t_{OV}$, the voltage feedback loop and optocoupler are saturated, driving maximum $I_{FB}$ and temporarily switching at $f_{SW(min)}$. The auxiliary bias current expended during this situation exceeds what is normally required during the steady-state no-load condition. Equation 36 calculates the value of $C_{VDD}$ (with a safety factor of 2) required to ride through the $t_{OV}$ duration until steady-state no-load operation is achieved

$$C_{VDD} \geq \frac{2 \times I_{AUXNL(max)} \times t_{OV}}{V_{VDDFL} - \left(V_{VDD(off)} + 1\,V\right)} \tag{36}$$

$$C_{VDD} \geq \frac{2 \times (1.2\,mA) \times (20\,ms)}{(18.2\,V - 8.15\,V - 1)} = 5.33\,\mu F$$

To address the start-up of the converter for heavy capacitive loads (which is around 8000 to 10,000 µF), a higher value of $C_{VDD}$ is needed. This TI Design uses a 10-µF capacitor.

### 4.2.10 Open-Loop Voltage Regulation VS Pin Resistor Divider, Line Compensation Resistor

The resistor divider at the VS pin determines the output voltage regulation point of the flyback converter, and the high-side divider resistor ($R_{S1}$) determines the line voltage at which the controller enables continuous DRV operation. $R_{S1}$ is initially determined based on the transformer auxiliary-to-primary turns ratio and desired input voltage operating threshold:

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \tag{37}$$

where

- $N_{PA}$ is the transformer primary-to-auxiliary turns-ratio
- $V_{IN(run)}$ is the AC RMS voltage to enable turn-on of the controller (run); in case of DC input, leave out the $\sqrt{2}$ term in the equation
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the switch on-time (see Electrical Characteristics of the UCC28740 datasheet)

$$R_{S1} = \frac{70\ \text{VAC} \times 1.414}{5 \times 275\ \mu\text{A}} = 71.98\ \text{k}\Omega$$

A standard resistor of 71.5 kΩ is selected.

The low-side VS pin resistor is selected based on the desired $V_{OUT}$ regulation voltage in open-loop conditions and sets the maximum allowable voltage during open-loop conditions.

$$R_{S2} = \frac{R_{S1} \times V_{OVPTH}}{N_{AS} \times \left(V_{OV} - V_F - V_{OVPTH}\right)} \tag{38}$$

Where

- $V_{OV}$ is the maximum allowable peak voltage at the converter output
- $V_F$ is the output-rectifier forward drop at near-zero current
- $N_{AS}$ is the transformer auxiliary-to-secondary turns-ratio
- $R_{S1}$ is the VS divider high-side resistance
- $V_{OVPTH}$ is the overvoltage detection threshold at the VS input (see Electrical Characteristics).

$$R_{S2} = \frac{71.5\ \text{k}\Omega \times 4.6\ \text{V}}{0.78 \times \left(28\ \text{V} - 0.4\ \text{V} - 4.6\ \text{V}\right)} = 16.86\ \text{k}\Omega$$

A standard resistor of 16.9 kΩ is selected.

The UCC28740 maintains a tight CC regulation over varying input lines by using the line-compensation feature. The line-compensation resistor ($R_{LC}$) value is determined by current flowing in $R_{S1}$ and the total internal gate-drive and external MOSFET turn-off delay. Assuming an internal delay of 50 ns in the UCC28740:

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \tag{39}$$

where

- $R_{CS}$ is the current-sense resistor value
- $t_D$ is the current-sense delay including MOSFET turn-off delay, add ~50 ns to MOSFET delay
- $N_{PA}$ is the transformer primary-to-auxiliary turns ratio
- $L_P$ is the transformer primary inductance
- $K_{LC}$ is a current-scaling constant (see the Electrical Characteristics table of the UCC28740 datasheet).

$$R_{LC} = \frac{28.6 \times 71.5\ \text{k}\Omega \times 0.26\ \Omega \times \left(77\ \text{ns} + 50\ \text{ns}\right) \times 3.9}{240\ \mu\text{H}} = 1.097\ \text{k}\Omega$$

A standard resistor of 1.21 kΩ is selected.

### 4.2.11 Feedback Elements

The output voltage is set through the sense-network resistors $R_{FB1}$ and $R_{FB2}$. A potentiometer provides flexibility of setting the range of output voltage between 23 to 26 V. The design spreadsheet has all relevant equations to characterize the optocoupler and its adjustments of the initial values to accommodate variations of the UCC28740. Also using the design sheet, the shunt-regulator parameters can be optimized for overall system performance.

The shunt-regulator compensation network, $Z_{FB}$, is determined using well-established design techniques for control-loop stability. Typically, a type-II compensation network is used.

## 4.3 Synchronous Rectifier Controller Component Design

The UCC24630 is a high-performance controller driver for N-channel MOSFET power devices used for secondary-side synchronous rectification. The UCC24630 is designed to operate as a companion device to a primary-side controller to help achieve efficient synchronous rectification in switching power supplies. The controller features a high-speed driver and provides appropriately timed logic circuitry that seamlessly generates an efficient synchronous rectification system. With its current emulator architecture, the UCC24630 has enough versatility to be applied in DCM, TM, and CCM. The UCC24630 SR on-time adjustability allows optimizing for PSR and SSR applications. Additional features such as pin fault protection, dynamic VPC threshold sensing, and voltage sense blanking time make the UCC24630 a robust synchronous controller. CCM dead-time protection shuts off the DRV signal in the event of an unstable switching frequency.

The design procedure for selecting the component circuitry for use with the UCC24630 is detailed in the following sections.

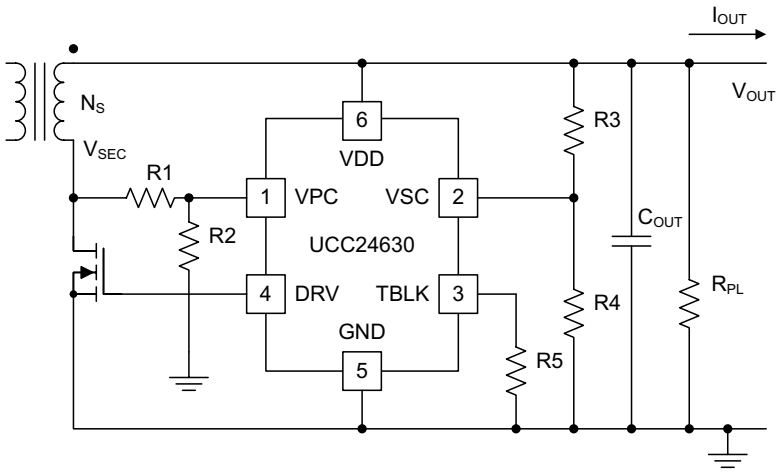



**Figure 4. UCC24630 Circuit Component Design**

### 4.3.1 VPC Pin Elements

Determining the VPC and VSC divider resistors is based on the operating voltage ranges of the converter and $Ratio_{VPC-VSC}$ gain ratio. Referring to Figure 4, Equation 40 determines the VPC divider values. For R2, a value of 10 kΩ is recommended for minimal impact on time delay and low-resistor dissipation. A higher R2 value reduces resistor divider dissipation but may increase the DRV turn-on delay due to the time constant of ~2-pF pin capacitance and divider resistance. A lower R2 value can be used with the tradeoff of higher dissipation in the resistor divider. A factor of 10% over the VPC threshold, $V_{VPCEN}$, is shown in Equation 40 for the design margin.

For minimal power dissipation: R2 = 10 kΩ

$$R1 = \frac{\frac{V_{IN(min)}}{N_{PS}} + V_{OUT(min)} - V_{VPC\_EN} \times 1.1}{V_{VPC\_EN}} \quad (40)$$

where

- $V_{IN(min)}$ is the converter minimum primary bulk capacitor voltage
- $V_{OUT(min)}$ is the minimum converter output voltage in normal operation
- $V_{VPCEN}$ is the VPC enable threshold, use the specified maximum value
- $N_{PS}$ is the transformer primary-to-secondary turns ratio

$$R1 = \frac{\frac{60}{3.9} + 22\ V - 0.45\ V \times 1.1}{0.45\ V} \times R2 = 765.7\ k\Omega$$

A standard resistor of 750 kΩ is selected.

The operating voltage range on the VPC pin should be within 0.45 to 2 V. Referring to Figure 4, if $V_{VPC}$ is greater than 2.3 V, the dynamic range is exceeded and $Ratio_{VPC\_VSC}$ is reduced; in this condition, the DRV on-time is less than expected. If $V_{VPC}$ is greater than 2.6 V for 500 ns, a fault is generated and DRV is disabled for the cycle. To ensure the maximum voltage is within range, confirm with Equation 41.

$$V_{VPC(max)} = \frac{\left(\frac{V_{IN(max)}}{N_{PS}} + V_{OUT(max)}\right) \times R2}{R1 + R2} \tag{41}$$

where

- $V_{IN(max)}$ is the converter maximum primary bulk capacitor voltage
- $V_{OUT(max)}$ is the maximum converter output voltage at OVP
- $N_{PS}$ is the transformer primary-to-secondary turns ratio

$$V_{VPC(max)} = \frac{\left(\frac{410}{3.9} + 26\ V\right) \times 10\ k\Omega}{760\ k\Omega} = 1.725\ V$$

$$V_{VPC(min)} = \frac{\left(\frac{60}{3.9} + 22\ V\right) \times 10\ k\Omega}{760\ k\Omega} = 0.492\ V$$

Therefore, $V_{VPC}$ is within the recommended range of 0.45 to 2 V.

### 4.3.2 VSC Pin Elements

The program voltage on the VSC pin is determined by the VPC divider ratio and the device's parameter, $Ratio_{VPC\_VSC}$. The current emulator ramp gain is higher on the VPC pin by the multiple $Ratio_{VPC\_VSC}$, so the VSC resistor divider ratio is reduced by the same $Ratio_{VPC\_VSC}$ accordingly. Determine the VSC divider resistors using Equation 42. To minimize resistor divider dissipation, a recommended range for R4 is 25 to 50 kΩ. Higher R4 values increase offset due to VSC input current, $I_{VSC}$. Lower R4 values increase the resistor divider dissipation. To ensure the DRV turns off slightly before the secondary current reaches zero, a 10% margin is considered for initial values.

A standard resistor of 47.5 kΩ is selected for R4.

$$R3 = \left[\left(\frac{\frac{R1 + R2}{R2}}{Ratio_{VPC\_VSC} \times 1.1}\right) - 1\right] \times R4 \tag{42}$$

where

- $Ratio_{VPC\_VSC}$ is the device parameter VPC and VSC gain ratio, use a value of 4.15

$$R3 = \left(\frac{\frac{(750 + 10)\ k\Omega}{10\ k\Omega}}{4.15 \times 1.1} - 1\right) \times 47.5\ k\Omega = 743.3\ k\Omega$$

A standard resistor of 750 kΩ is selected for R3.

The operating voltage range on the VSC pin should be from 0.3 to 2 V. Referring to Figure 4, if $V_{VSC}$ is greater than 2.3 V, the dynamic range is exceeded and $Ratio_{VPC\_VSC}$ is increased; in this condition, the DRV on-time is more than expected. To ensure the VSC voltage is within range, confirm with Equation 43 and Equation 44.

$$\frac{R4}{R3 + R4} \times V_{OUT(min)} \geq 0.3\ V \tag{43}$$

$$\frac{R4}{R3 + R4} \times V_{OUT(max)} \leq 2.0\ V \tag{44}$$

where

- $V_{OUT(min)}$ is the maximum converter output operating voltage of the SR controller
- $V_{OUT(max)}$ is the maximum converter output operating voltage of the voltage at OVP

$$V_{VSC(max)} = \frac{(10\ k\Omega) \times 26\ V}{760\ k\Omega} = 0.342\ V \tag{45}$$

$$V_{VSC(min)} = \frac{(10\ k\Omega) \times 22\ V}{760\ k\Omega} = 0.289\ V \tag{46}$$

Therefore, $V_{VSC}$ is within the recommended range of 0.3 to 2 V.

### 4.3.3 $t_{BLK}$ Input

The blanking time is set with resistor R5. Select the blanking time to meet the following criteria based on minimum primary on-time at high line:

$$t_{VPC\_BLK} = (t_{PRI} \times 0.85) - 120\ ns$$

$$t_{VPC\_BLK} = (650\ ns \times 0.85) - 120\ ns = 432.5\ ns \tag{47}$$

To determine the resistor value for $t_{VPC\_BLK}$, use Equation 48 to select from a range of 200 ns to 1 µs.

$$R5 = \frac{t_{VPC\_BLK} - 100\ ns}{18\ pF} \tag{48}$$

where

- $t_{VPC\_BLK}$ is the target blanking time

$$R5 = \frac{(432.5\ ns - 100\ ns)}{18\ pF} = 18.47\ k\Omega$$

A standard resistor of 18 kΩ is selected.

### 4.4 LM5050-2 ORing Circuit Component Design

The important MOSFET electrical parameters are the maximum continuous drain current ID, the maximum source current (or body diode), the maximum drain-to-source voltage $V_{DS(max)}$, the gate-to-source threshold voltage $V_{GS(TH)}$, the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source ON resistance $R_{DS(ON)}$. The rating for the maximum continuous drain current, ID, must exceed the maximum continuous load current. The rating for the maximum current through the body diode, IS, is typically rated the same as, or slightly higher than, the drain current, but the body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$: Gate charge time = $Q_g$ / $I_{GATE(ON)}$.

The maximum drain-to-source voltage, $V_{DS(max)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the LM5050 gate drive capabilities. Logic level MOSFETs are recommended, but sub-logic level MOSFETs can also be used.

The dominate MOSFET loss for the LM5050 active ORing controller is conduction loss due to the source-to-drain current to the output load and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

- Reverse transition detection: A higher $R_{DS(ON)}$ will provide increased voltage information to the LM5050 Reverse Comparator at a lower reverse current level. This will give an earlier MOSFET turn-off condition should the input voltage become shorted to ground. This minimizes any disturbance of the redundant bus.
- Reverse current leakage: In cases where multiple input supplies are closely matched, it may be possible for some small current to flow continuously through the MOSFET drain to source (that is, in reverse) without activating the LM5050 Reverse Comparator. A higher $R_{DS(ON)}$ reduces this reverse current level.

Selecting a MOSFET with an $R_{DS(ON)}$ that is too large will result in excessive power dissipation. Additionally, the MOSFET gate will be charged to the full value that the LM5050 can provide as it attempts to drive the drain-to-source voltage down to the $V_{SD(REG)}$ of 20 mV typical. This increased gate charge requires some finite amount of additional discharge time when the MOSFET needs to be turned off.

As a guideline, select $R_{DS(ON)}$ to provide at least 20 mV and no more than 100 mV at the nominal load current.

Based on this analysis, this TI Design uses the CSD18504Q5A.

Power dissipation in MOSFET:

$$P_{DISS} = I_D^2 \times (R_{DS(ON)})max \tag{49}$$

$$P_{DISS} = 2.5\ A^2 \times 6.6\ m\Omega = 41.45\ mW$$

# 5 Getting Started Hardware

## 5.1 Test Equipment Needed for Board Validation

1. Isolated AC source
2. Single-phase power analyzer
3. Digital oscilloscope
4. Multi-meters
5. Electronic or resistive load

## 5.2 Test Conditions

**Input voltage range**
AC source must be capable of varying between $V_{INAC}$: 85-V and 265-V AC. Set the input current limit to 2.5 A.

**Output**
Connect an electronic load capable of 40 V and a load variable in range from 0 to 3 A. A rheostat or resistive decade box can be used in place of an electronic load.

## 5.3 Test Procedure

1. Connect the AC source at input terminals (Pin-2 and Pin-3 of connector J1) of the reference board.
2. Connect output terminals (Pin-3,4 and Pin-1,2 of connector J2) to the electronic load or rheostat, maintaining correct polarity. Pin-3,4 are $V_{OUT}$ output terminal pins, and Pin-1,2 are GND terminal pins
3. Set and maintain a minimum load of about 10 mA.
4. Increase gradually the input voltage from 0 V to turn on voltage of 85-V AC.
5. Turn on the load to draw current from the output terminals of the converter.
6. Observe the start-up conditions for smooth switching waveforms.

# 6 Test Results

The test results are divided into multiple sections that cover the steady state performance measurements, functional performance waveforms and test data, transient performance waveforms, thermal measurements, conducted emission measurements, and Surge and EFT measurements.

## 6.1 Performance Data

### 6.1.1 Efficiency and Regulation With Load Variation

Table 3 shows the efficiency and regulation performance data at a 115-V AC input for both constant voltage (CV) and constant current (CC) operation.

**Table 3. Efficiency and Regulation Performance at 115-V AC Input**

| $V_{INAC}$ (V) | $I_{INAC}$ (A) | $P_{INAC}$ (W) | $V_{OUT}$ (V) | $I_{OUT}$ (A) | $P_{OUT}$ (W) | EFFICIENCY (%) |
|---|---|---|---|---|---|---|
| **CV OPERATION** | | | | | | |
| 115 | 0.14 | 6.7 | 24 | 0.25 | 6.0 | 89.6 |
| 115 | 0.25 | 13.3 | 24 | 0.50 | 12.0 | 90.5 |
| 115 | 0.48 | 26.9 | 24 | 1.00 | 24.0 | 89.6 |
| 115 | 0.68 | 40.5 | 24 | 1.50 | 36.1 | 89.2 |
| 115 | 0.90 | 53.8 | 24 | 2.00 | 48.0 | 89.3 |
| 115 | 1.10 | 67.0 | 24 | 2.50 | 60.0 | 89.4 |
| **CC OPERATION** | | | | | | |
| 115 | 1.00 | 60.8 | 22 | 2.50 | 55.1 | 90.6 |
| 115 | 0.92 | 55.3 | 20 | 2.51 | 50.2 | 90.7 |
| 115 | 0.84 | 50.0 | 18 | 2.51 | 45.2 | 90.6 |
| 115 | 0.76 | 44.5 | 16 | 2.52 | 40.3 | 90.5 |
| 115 | 0.68 | 39.1 | 14 | 2.52 | 35.3 | 90.3 |

Table 4 shows the efficiency and regulation performance data at a 230-V AC input for both CV and CC operation.

**Table 4. Efficiency and Regulation Performance at 230-V AC Input**

| $V_{INAC}$ (V) | $I_{INAC}$ (A) | $P_{INAC}$ (W) | $V_{OUT}$ (V) | $I_{OUT}$ (A) | $P_{OUT}$ (W) | EFFICIENCY (%) |
|---|---|---|---|---|---|---|
| **CV OPERATION** | | | | | | |
| 230 | 0.09 | 7.0 | 24 | 0.25 | 6.0 | 86.2 |
| 230 | 0.15 | 13.5 | 24 | 0.50 | 12.1 | 89.5 |
| 230 | 0.26 | 26.4 | 24 | 1.00 | 24.1 | 91.1 |
| 230 | 0.38 | 39.4 | 24 | 1.50 | 36.0 | 91.5 |
| 230 | 0.50 | 52.5 | 24 | 2.00 | 48.0 | 91.5 |
| 230 | 0.63 | 65.4 | 24 | 2.50 | 59.9 | 91.6 |
| **CC OPERATION** | | | | | | |
| 230 | 0.58 | 60.1 | 22 | 2.50 | 55.0 | 91.6 |
| 230 | 0.53 | 54.7 | 20 | 2.50 | 50.1 | 91.6 |
| 230 | 0.49 | 49.4 | 18 | 2.51 | 45.2 | 91.5 |
| 230 | 0.44 | 44.0 | 16 | 2.51 | 40.2 | 91.3 |
| 230 | 0.39 | 38.7 | 14 | 2.51 | 35.2 | 91.0 |

### 6.1.2 Standby Power

The standby power was noted at multiple AC input voltages with a constant no load on the output DC bus. Table 5 lists the results:

**Table 5. Standby Power Loss of Converter**

| $V_{INAC}$ (VAC) | $I_{INAC}$ (mA) | $P_{INAC}$ (W) | $V_{OUT}$ (V) |
|---|---|---|---|
| 115 | 18 | 0.125 | 24 |
| 230 | 35 | 0.170 | 24 |

No load power is contributed by:

- Resistors used X-capacitor discharge
- Controller operation during No load

## 6.2 Performance Curves

### 6.2.1 Efficiency With Load Variation

Figure 5 and Figure 6 show the measured efficiency of the system with AC input voltage variation during CV and CC operations, respectively.

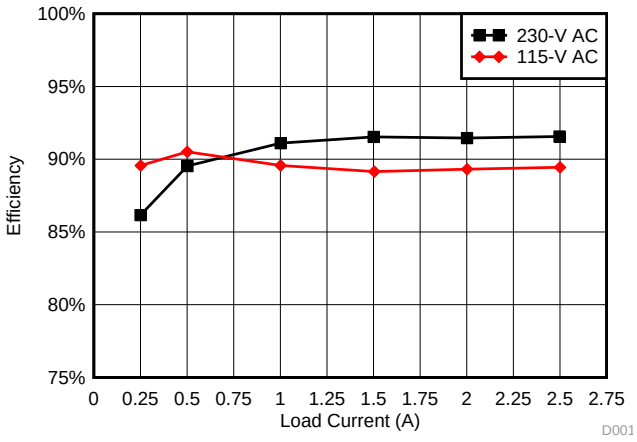



**Figure 5. Efficiency versus Output Load Current in CV Mode**

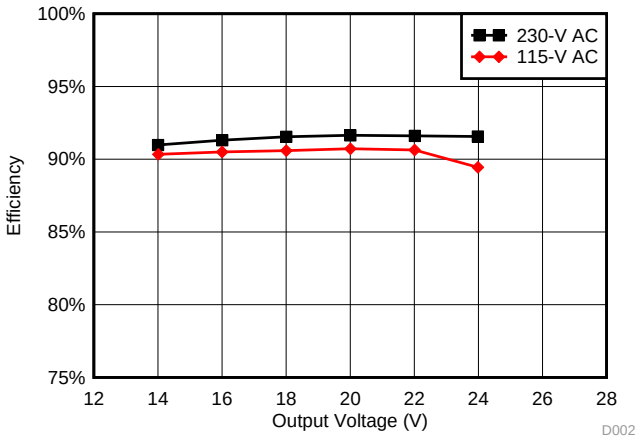



**Figure 6. Efficiency versus Output Load Voltage in CC Mode**

### 6.2.2 Load Regulation in CV and CC Modes

Figure 7 and Figure 8 show the measured load regulation of the PSU.

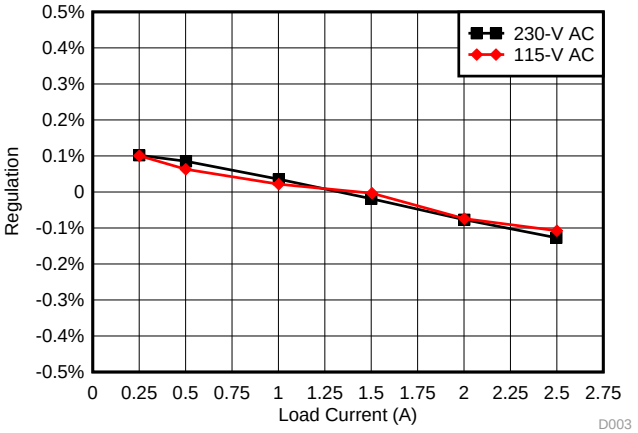



**Figure 7. Output Voltage Variation With Load Current in CV Mode**

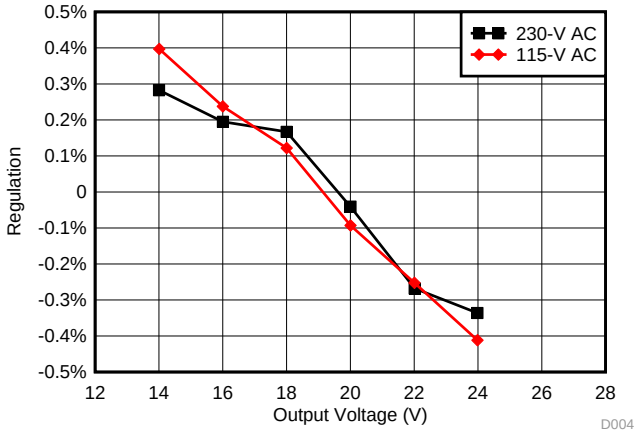



**Figure 8. Output Current Variation With Load Voltage in CC Mode**

### 6.2.3 AC Line Regulation and Efficiency With AC Input Voltage Variation

Figure 9 shows the efficiency variation of the PSU with respect to the AC line voltage variation, and Figure 10 shows the output voltage regulation with AC line voltage variation.

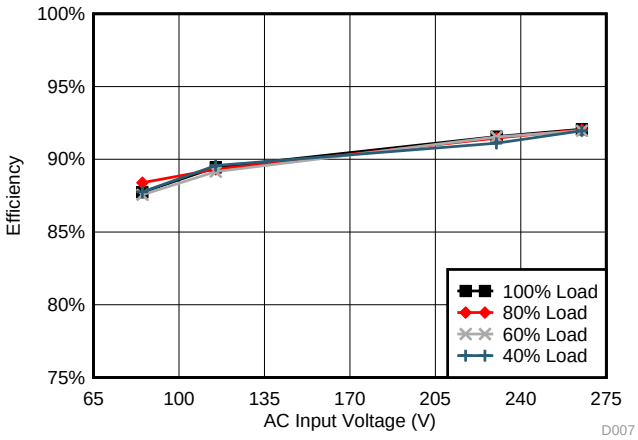



**Figure 9. Efficiency Variation With AC Input Voltage Variation in CV Mode**

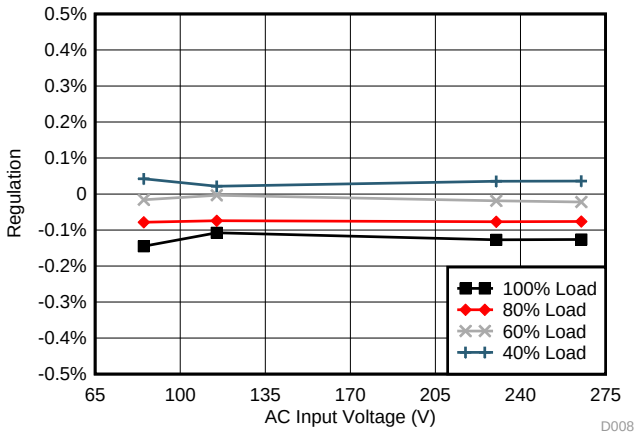



**Figure 10. Output Voltage Variation With AC Input Voltage Variation in CV Mode**

### 6.2.4 CC-CV Operation, Power Limit, and Foldback

Figure 11 shows the transition of CV and CC modes, and Figure 12 shows the power limiting feature of the converter with output voltage foldback for high load conditions.

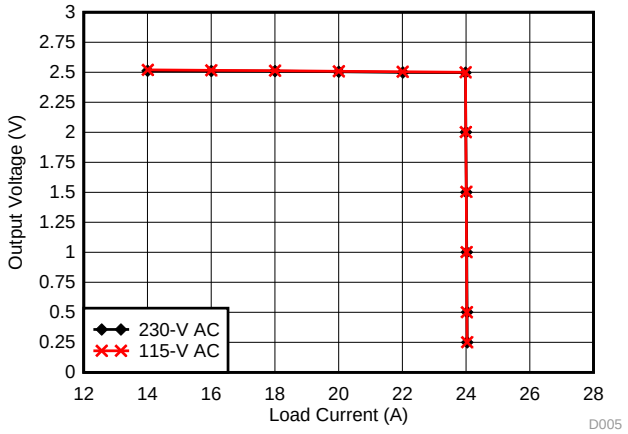



Figure 11. CC-CV Operation

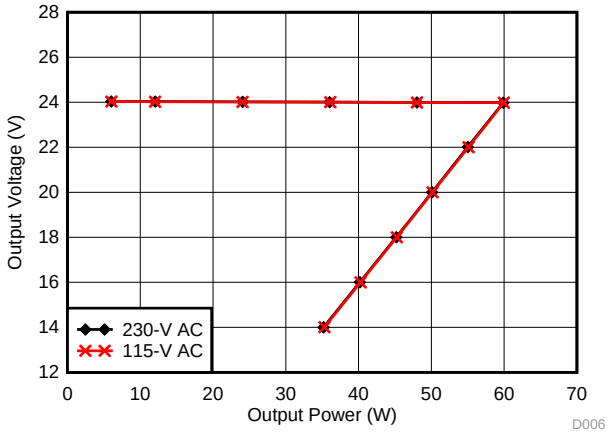



Figure 12. Power Limit and Foldback Characteristics

## 6.3 Functional Waveforms

### 6.3.1 Flyback MOSFET Switching Node Waveforms

Waveforms at the flyback switching node (SW) were observed along with the MOSFET current for 115- and 230-V AC under full load (2.5 A) conditions.

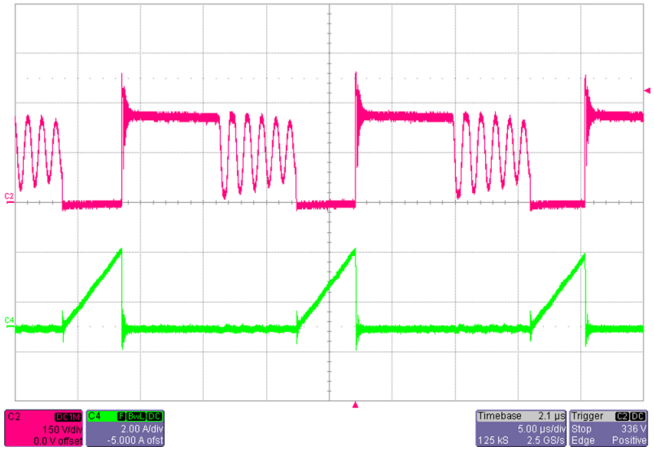


Figure 13. SW Node Waveform and MOSFET Current at $V_{INAC}$ = 115-V AC, Full Load

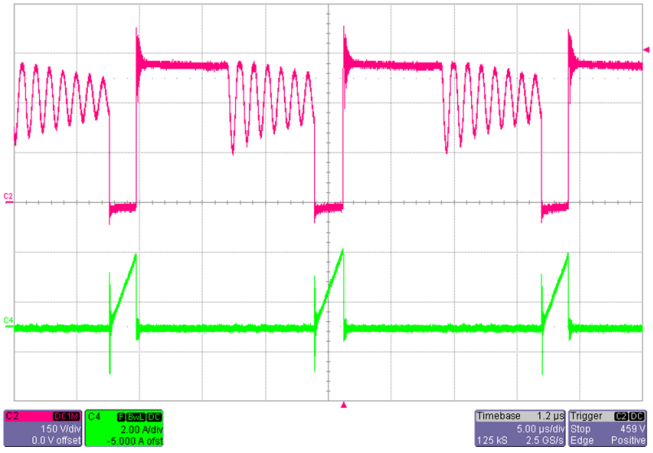


Figure 14. SW Node Waveform and MOSFET Current at $V_{INAC}$ = 230-V AC, Full Load

**NOTE:** Red trace: Drain voltage, 150 V/div; Green trace: Drain current, 2 A/div.

### 6.3.2 Output Synchronous Rectifier Drain-to-Source Voltage ($V_{DS}$) Waveforms

Waveforms at the secondary output across the synchronous rectifier were observed along at both 115- and 230-V AC under full load (2.5 A) conditions. The maximum voltage across the synchronous switching FET is well within the maximum $V_{DS}$ breakdown voltage of FET.

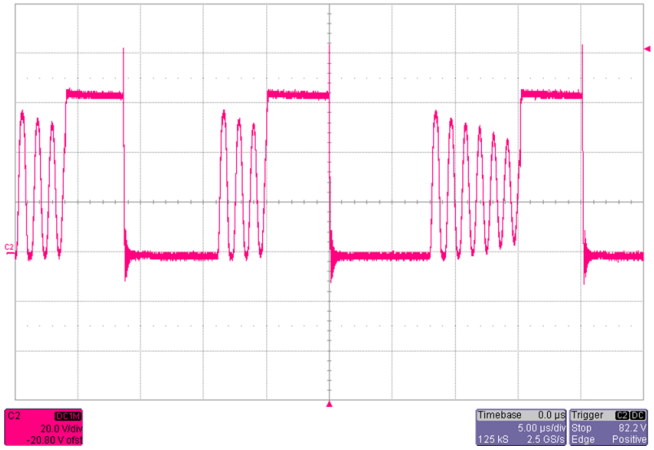



**Figure 15. Output Synchronous FET $V_{DS}$ Waveform at $V_{INAC}$ = 115-V AC, Full Load**

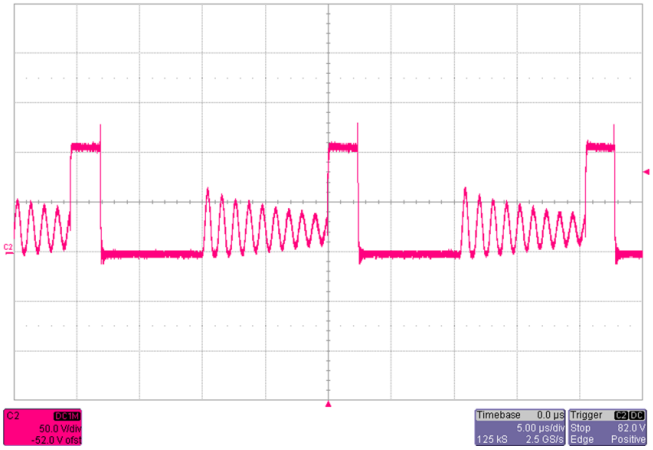



**Figure 16. Output Synchronous FET $V_{DS}$ Waveform at $V_{INAC}$ = 230-V AC, Full Load**

**NOTE:** Red trace: Drain-to-source voltage

### 6.3.3 Inrush Current Waveform

Inrush current drawn by the system is observed and recorded at maximum input voltage of 230-V AC.

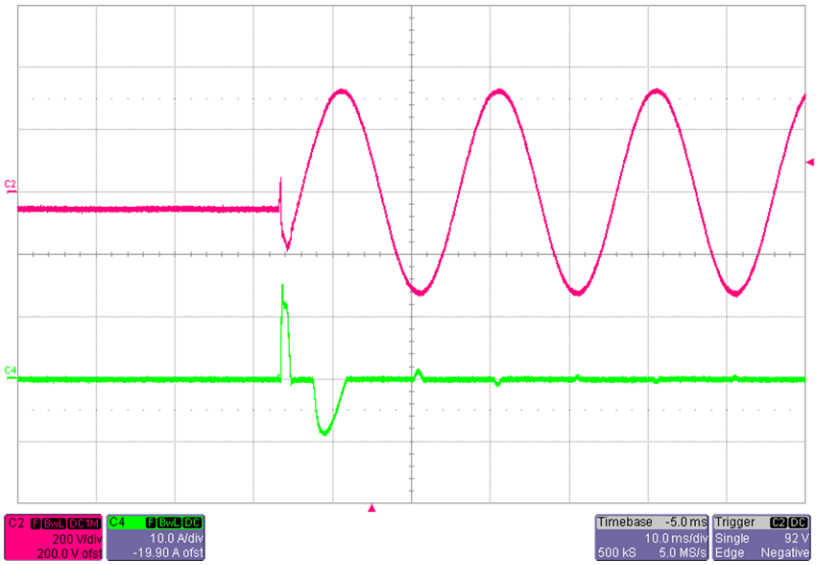



**Figure 17. Input Voltage and Input Inrush Current**

**NOTE:** Red trace: Drain voltage, 200 V/div; Green trace: Drain current, 10 A/div

### 6.3.4 Output Ripple

The output ripple is observed at a 24-V DC output and full load 2.5 A at both 115- and 230-V AC. The peak-to-peak ripple voltage is less than 20 mV.

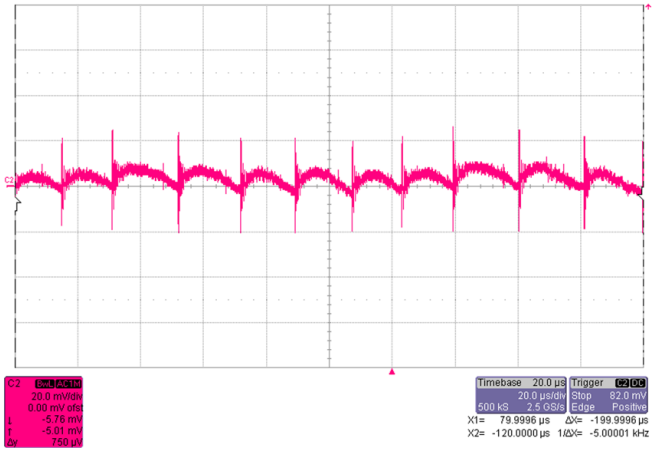



**Figure 18. Output Voltage Ripple at $V_{INAC}$ = 115 V, Full Load**

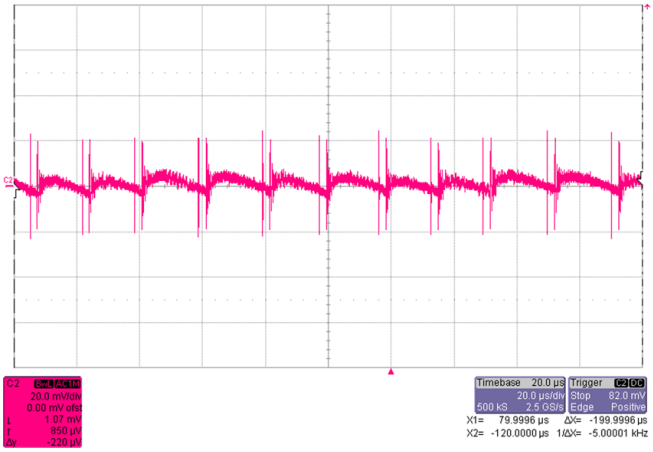



**Figure 19. Output Voltage Ripple at $V_{INAC}$ = 230 V, Full Load**

## 6.4 Transient Waveforms

### 6.4.1 Turn-On Characteristics

The 24-V output turn on with resistive load (9.6 Ω) and a CC load of 2 A at the output.

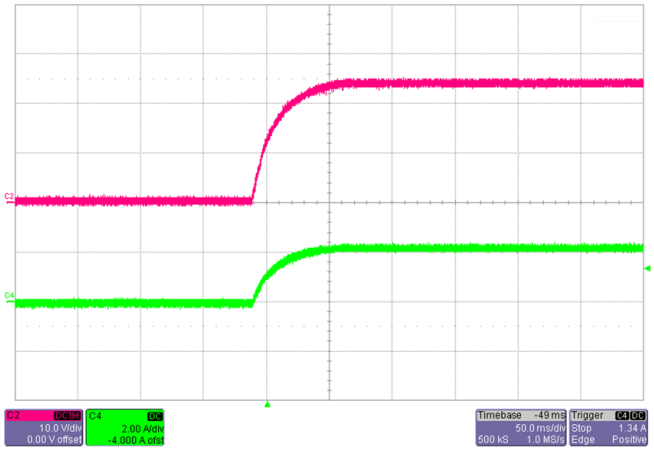


**Figure 20. Output Turn ON Waveform With Resistive Load of 9.6 Ω**

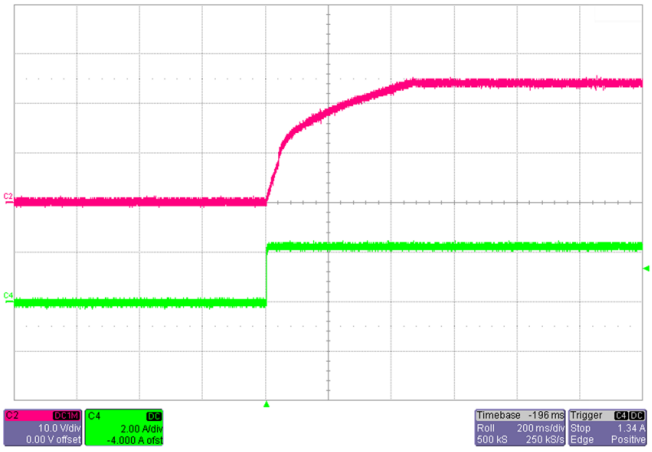


**Figure 21. Output Turn ON Waveform With CC Load of 2 A**

**NOTE:** Red trace: Output voltage, 10 V/div; Green trace: Output current, 2 A/div.

### 6.4.2 Turn-On Characteristics With Heavy Capacitive Load of 8500 µF

Turn-on performance observed with heavy capacitive load by adding additional capacitance of 8500 µF externally. The behavior is recorded with no load and full load conditions.

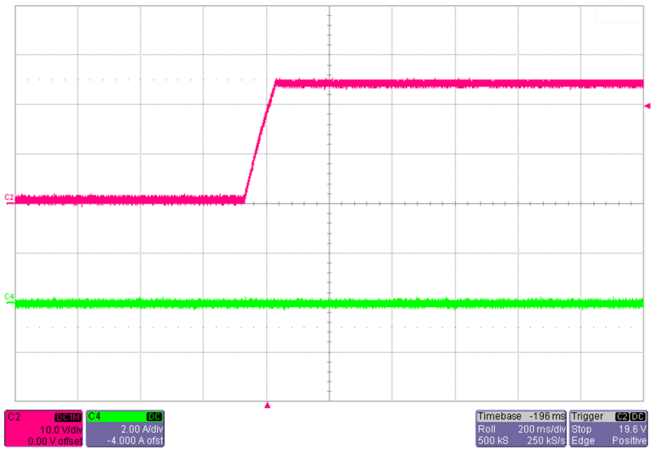


**Figure 22. Output Turn ON Waveform With Additional 8500-µF Capacitance at Output Under No Load**

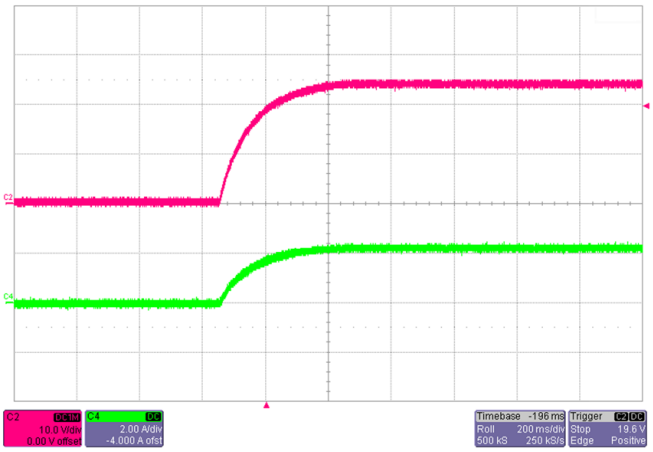


**Figure 23. Output Turn ON Waveform With Additional 8500-µF Capacitance at Output and Resistive Load of 9.6 Ω**

**NOTE:** Red trace: Output voltage, 10 V/div; Green trace: Output current, 2 A/div.

### 6.4.3 Hold-up Time and Start-up Delay Characteristics

Hold-up time is observed at 115- and 230-V AC under full load conditions. The unit can support full load operation for > ms at 115-V AC and > 100 ms at 230-V AC operation.

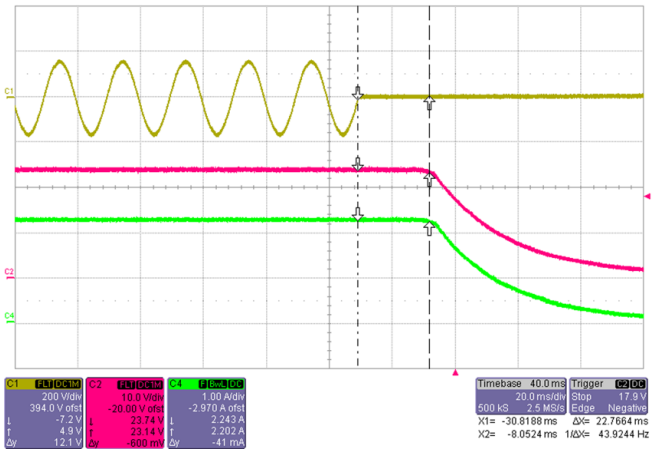


**Figure 24. Hold-Up Time at 115-V AC**

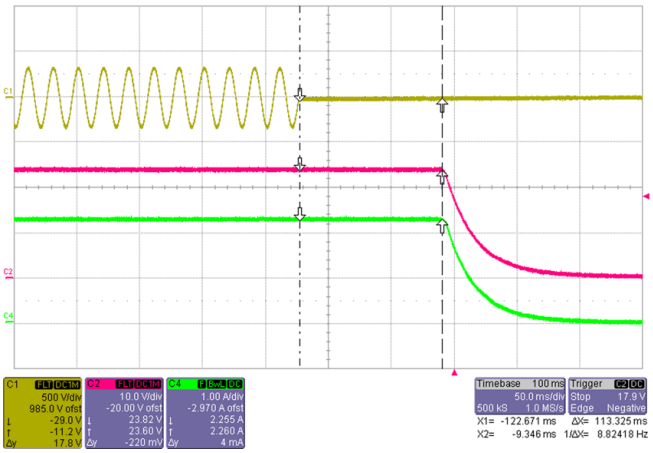


**Figure 25. Hold-Up Time at 230-V AC**

**NOTE:** Red trace: Output voltage, 10 V/div; Green trace: Output current,1 A/div; Yellow trace: Input AC voltage

Start-up delay time is observed at 115- and 230-V AC with no load conditions. The delay measured is shown in Figure 26 and Figure 26.

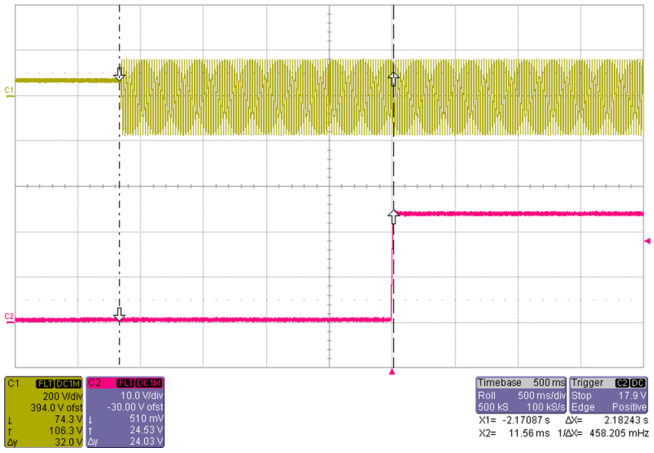


**Figure 26. Start-up Delay at 115-V AC**

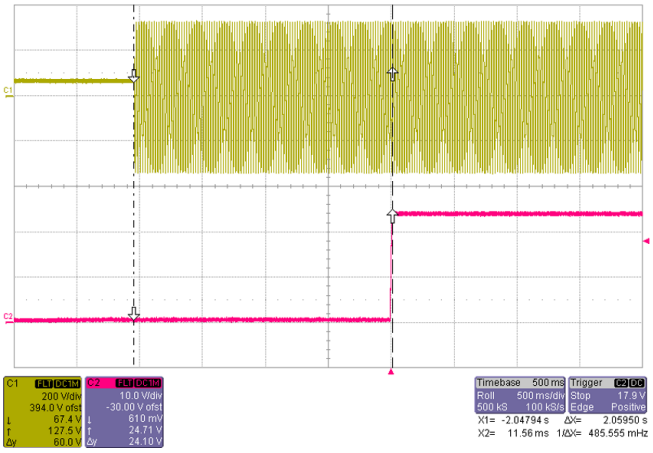


**Figure 27. Start-up Delay at 230-V AC**

**NOTE:** Red trace: Output voltage, 10 V/div; Yellow trace: Input AC voltage: 200 V/div.

### 6.4.4 Transient Load Response

Load transient performance is observed with load switched at a 0.2-m wire length. The output load is switched using electronic load.

$V_{IN}$ = 230-V AC, load transient from 0.5 to 2.5 A, and vice-versa performance at a 24-V output.

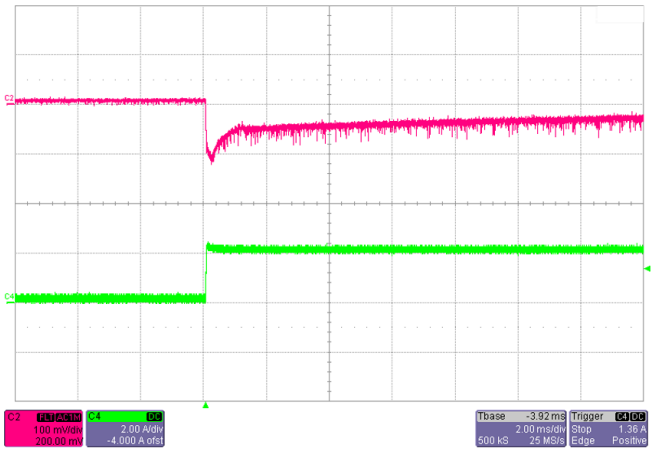


**Figure 28. Output Voltage and Current Waveform, Load Transient From 0.5 to 2.5 A**

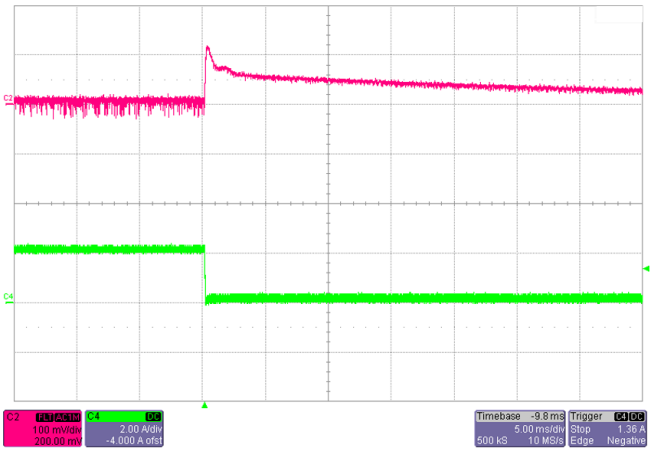


**Figure 29. Output Voltage and Current Waveform, Load Transient From 2.5 to 0.5 A**

**NOTE:** Red trace: Output voltage, 100 mV/div, AC coupling; Green trace: Output current, 2 A/div.

### 6.4.5 Overload and Overcurrent Response

The converter is driven to an overcurrent condition by applying a step change in load from a 50% load to a 150% load. The performance of the converter output was observed and shown in Figure 30 and Figure 31.

During overcurrent conditions, the maximum current is limited to 2.5 A, and the output voltage is drooped to regulate the power within the limits. When the overcurrent condition is removed, the converter recovers back to CV operation.

**NOTE:** Red trace: Output voltage, 10 V/div; Green trace: Output current, 2 A/div.

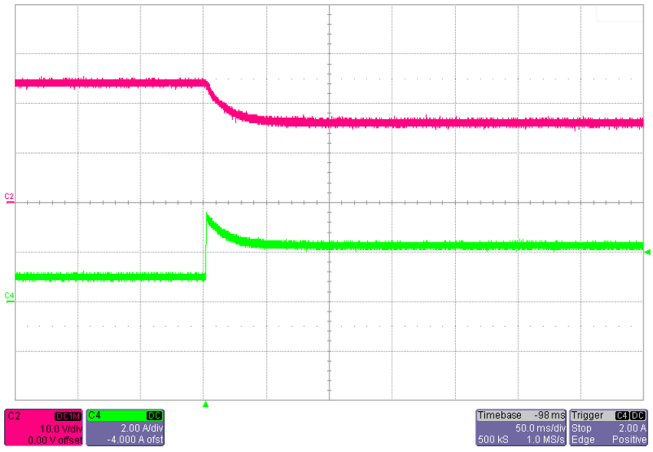


**Figure 30. Output Voltage and Current Waveform, Step-Load Transient From 50% Load to 150% Load**

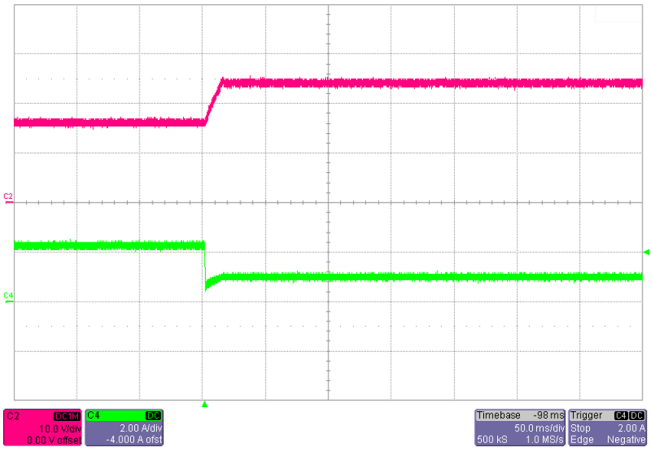


**Figure 31. Output Voltage and Current Waveform, Step-Load Transient from 150% Load to 50% Load**

### 6.4.6 Short Circuit Response

A short circuit was applied and removed to observe the output turn-off and auto-recovery cycle. When the short is applied, the converter shuts down and goes into hiccup mode. When the short is removed, the converter recovers back to normal operation.

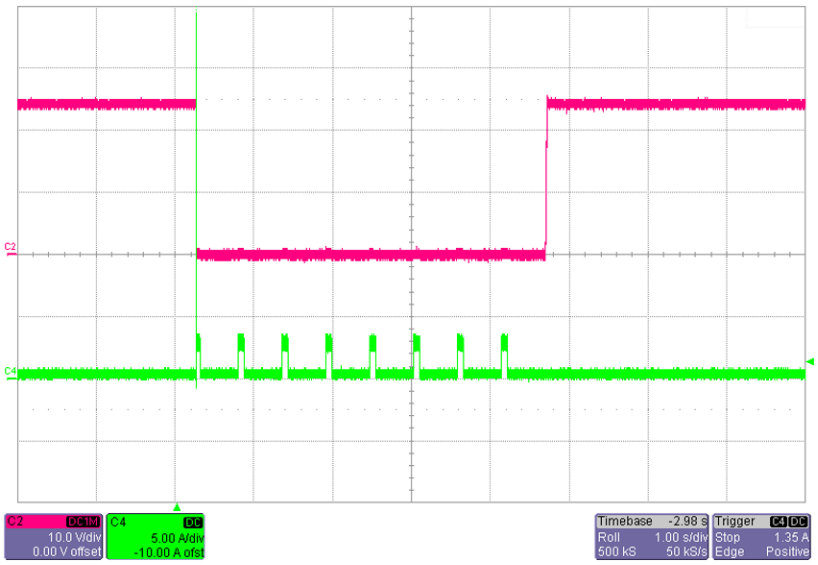



**Figure 32. Response During Short Circuit and Auto-Recovery When Short is Removed**

**NOTE:** Red trace: Output voltage, 10 V/div; Green trace: Output current, 5 A/div.

## 6.5 Conducted Emissions

Generally conducted emissions will be more at full load. So, this operating point is chosen to measure the conducted EMI.

### 6.5.1 With Resistive Load at Output

A 230-V AC input, 2.5-A resistive load is connected to the PSU with short leads. The conducted emissions in a pre-compliance test setup were compared against EN55011 class-B limits and found to meet the class-B limits comfortably.

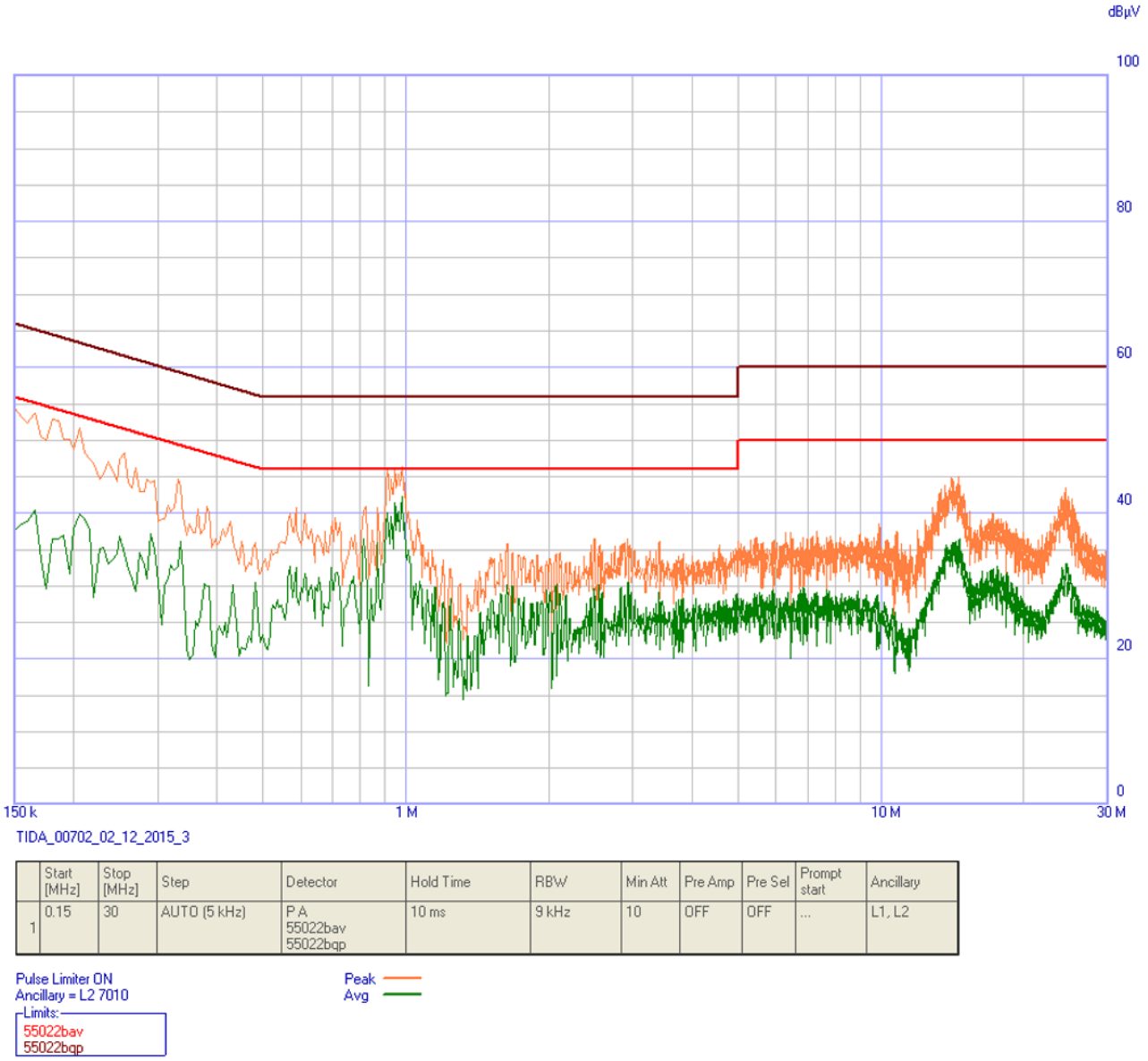



**Figure 33. Conducted Emissions as per EN55011 Class B**

## 6.6 Surge and EFT Test

Surge and EFT testing is done on the boards as per EN55014. The test condition and test results are tabulated in Table 6.

**Table 6. Surge and EFT Test Results**

| BASIC STANDARD | PORT | REQUIREMENTS OF IEC 61000-6-2/EN 50082-2: IMMUNITY STANDARD FOR INDUSTRIAL ENVIRONMENTS | PERFORMANCE CRITERION REQUIRED | TEST RESULT |
|---|---|---|---|---|
| IEC/EN 61000-4-4: EFT, Level-3 | AC input | ±2 kV, 5 kHz | B(1) | Passed with performance criterion A(2) |
| IEC/EN 61000-4-5: Surge, Level-3 | AC input | ±4 kV line to earth, ±2 kV line to line | B(1) | Passed with performance criterion A(2) |

(1) Temporary loss of function or degradation of performance which ceases after the disturbance ceases
(2) Normal performance within limits specified by the design or manufacturer

## 6.7 Thermal Measurements

Thermal images are plotted at room temperature (25°C) with closed enclosure, no airflow, and full load conditions. The board runs for 30 minutes before capturing thermal image.

### 6.7.1 Thermal Image for Lo-Line (115-V AC) Operation

In Figure 34, the input voltage is 115-V AC, and the load on 24-V DC bus is 2.5 A with a 60-W power output.

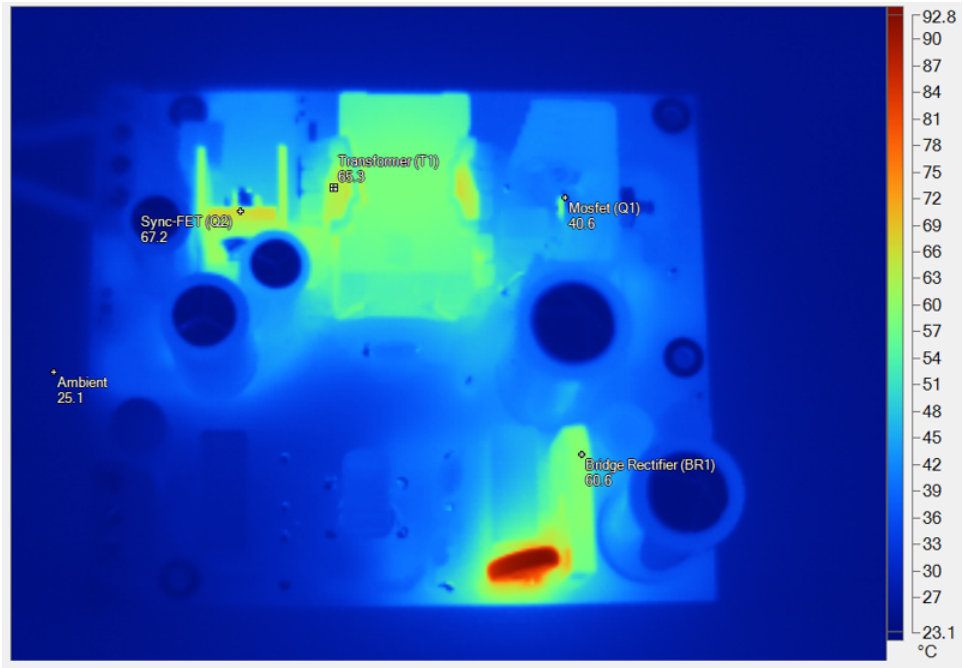



**Figure 34. Top-Side Temperatures at 115-V AC Input and 60-W Output**

**Table 7. Highlighted Image Markers**

| NAME | TEMPERATURE |
|---|---|
| Ambient | 25.1°C |
| Flyback FET (Q1) | 40.6°C |
| Synchronous rectifier FET (Q2) | 67.2°C |
| Transformer (T1) | 65.3°C |
| Bridge rectifier (BR1) | 60.6°C |

The temperatures are well contained to low values and have higher margins from respective device junction temperatures.

### 6.7.2 Thermal Image for Lo-Line (230-V AC) Operation

For Figure 35, the input voltage is 230-V AC, and the load on 24-V DC bus is 2.5 A with a 60-W power output.

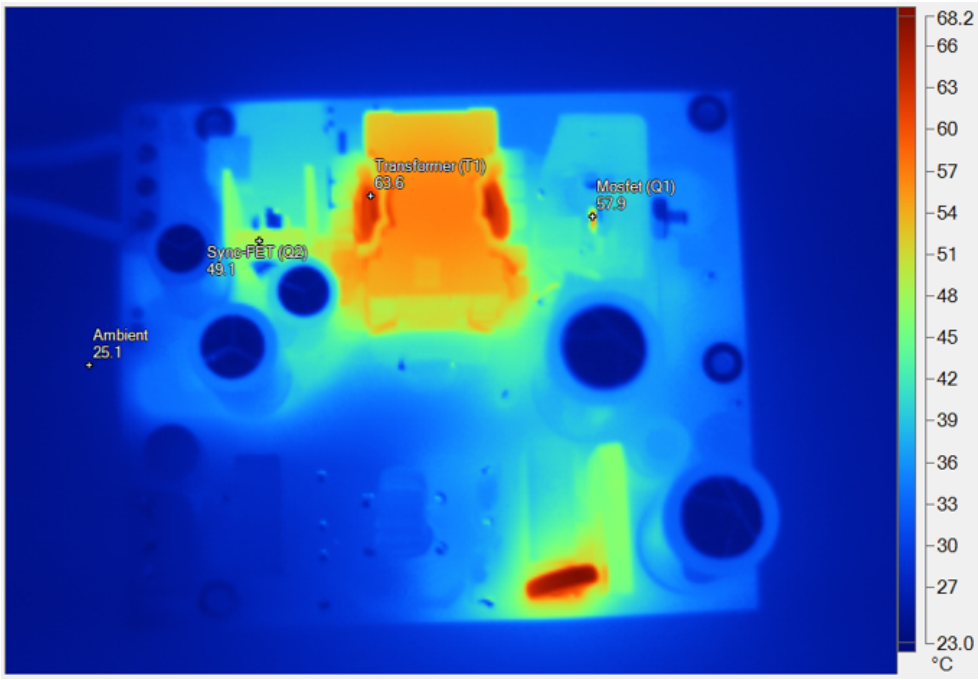



**Figure 35. Top-Side Temperatures at 230-V AC Input and 91.2-W Output**

**Table 8. Highlighted Image Markers**

| NAME | TEMPERATURE |
|---|---|
| Ambient | 25.1°C |
| Flyback FET (Q1) | 57.9°C |
| Synchronous rectifier FET (Q2) | 49.1°C |
| Transformer (T1) | 63.6°C |

The temperatures are well contained to low values and have higher margins from respective device junction temperatures.

# 7 Design Files

## 7.1 Schematics

To download the schematics, see the design files at TIDA-00702.

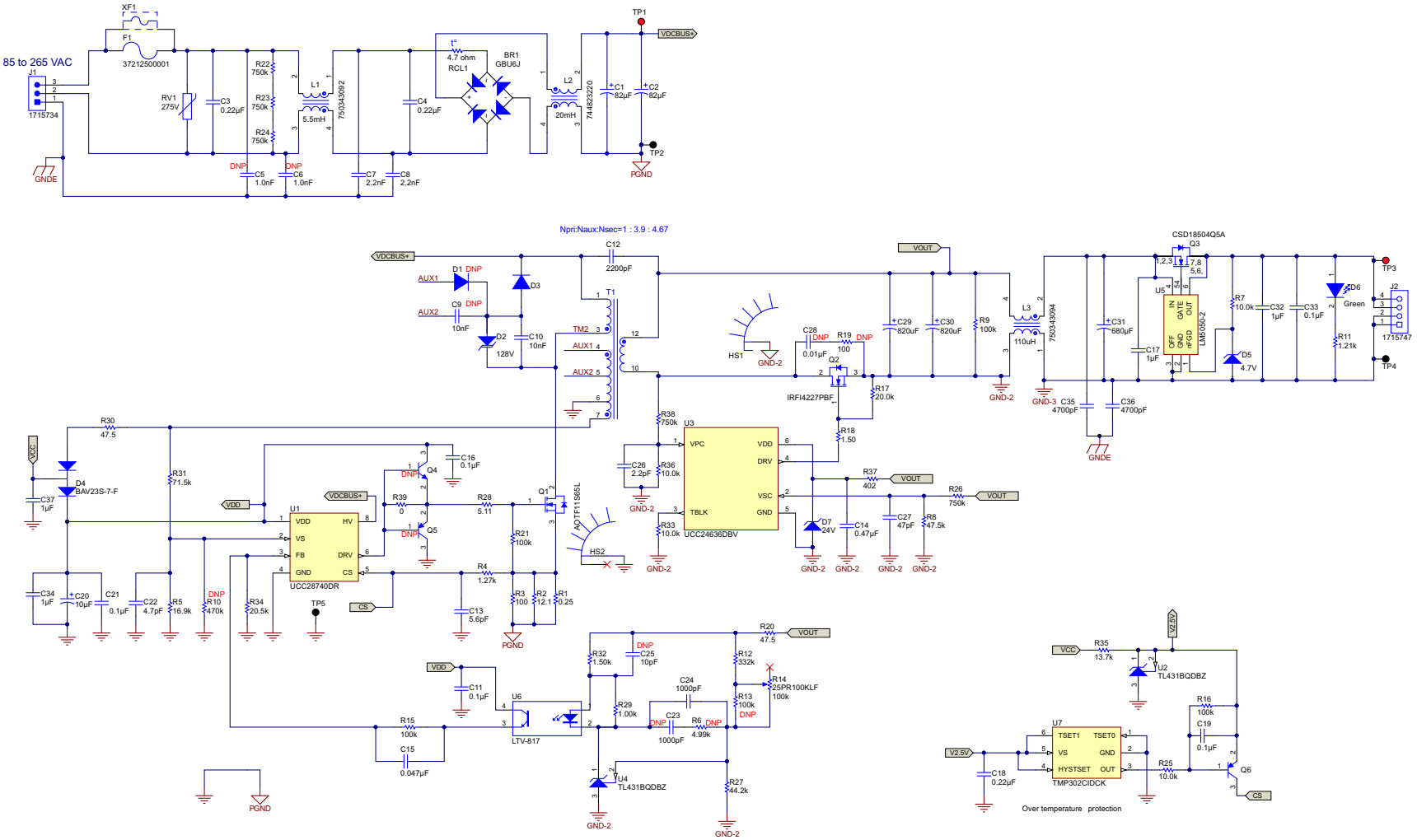



**Figure 36. 60-W, High-Efficiency Industrial Power Supply Schematic**

## 7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00702.

## 7.3 Layout Guidelines

A careful PCB layout is critical and extremely important in a high-current fast-switching circuit to properly operate the controller devices and attain the design's robustness. As with all switching power supplies, attention to detail in the layout can save much time in troubleshooting later on.

### 7.3.1 Power Stage Specific Guidelines

Follow these key guidelines to route power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high frequency switching currents. This helps to reduce EMI and improve converter overall performance.
- Keep the switch node as short as possible. A short and optimal trace width helps to reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dt potential and high di/dt capability away from or shielded from sensitive signal traces with adequate clearance and ground shielding.
- For each power supply stage, keep power ground and control ground separate. Tie them together (if they are electrically connected) in one point near DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, keep the layout symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance will see higher peak currents and become hotter (i2R).
- Tie the heat-sinks of all the power switching components to their respective power grounds.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route them with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current as per IPC2152 as well as acceptable DC and AC impedances. Also, the traces should withstand the fault currents (such as short circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various traces of the circuit according to the requirements of applicable standards. For this design, follow the UL 60950-1 safety standard to maintain the creepage and clearance from live line to neutral line and to safety ground as defined in the Tables 2K through 2N of this standard.
- Adapt thermal management to fit the end-equipment requirements.

### 7.3.2 Controller Specific Guidelines

Follow these key guidelines to route controller components and signal circuits:

- The optimum placement of decoupling capacitor is closest to the VCC/VDD and GND terminals of the device. Minimize the loop area formed by the bypass-capacitor connection and the GND terminal of the IC.
- Make the reference ground for the control devices, a low current signal ground (SGND), a copper plane or island.
- Locate all controller support components at specific signal pins close to their connection pin. Connect the other end of the component to the SGND with shortest trace length.
- The trace routing for the voltage sensing and current sensing circuit components to the device should be as short as possible to reduce parasitic effects on the current limit and current and voltage monitoring accuracy. These traces should not have any coupling to switching signals on the board.
- Connect the SGND plane to high current ground (main power ground) at a single point that is at the negative terminal of DC IO capacitor respectively.
- If there is an overlap, keep signal traces perpendicular to high-frequency and high-current traces to signal traces, not parallel to them. Shielding signal traces with ground traces can help reduce noise pick up.
- Give sufficient PCB trace spacing between the high-voltage connections (such as HV pin of UCC28740) and any low-voltage nets.
- See the placement and routing guidelines and layout example in the UCC28740 datasheet.

### 7.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-00702.

## 7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00702.

## 7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00702.

## 7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00702.

## 7.7 Design Calculator Spreadsheet

To download the design spreadsheet calculator for this reference design, see the design files at TIDA-00702.

## 8 References


1. Texas Instruments, *Control Challenges for Low Power AC/DC Converters*, Unitrode Power Supply Design Seminar SEM2100, Topic 5 (SLUP325)
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5. Texas Instruments, *Understanding Noise-Spreading Techniques and their Effects in Switch-Mode Power Applications*, Unitrode Power Supply Design Seminar SEM1800, Topic-2 (PDF)
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## 9 Terminology

TI Glossary: This glossary lists and explains terms, acronyms, and definitions (SLYZ022)

**PWM—** Pulse width modulation

**FETs, MOSFETs—** Metal–oxide–semiconductor field-effect transistor

**IGBT—** Insulated gate bipolar transistor

**ESD—** Electrostatic discharge

**RMS—** Root mean square

## 10 About the Authors

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