66AK2L06 DSP+ARM® Processor JESD204B Attach to ADC14X250/DAC38J84 Design Getting Started Guide

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ABSTRACT

The TI 66AK2L06 system-on-chip (SoC) is the industry's first JESD204B-compliant multicore DSP+ARM SoC that can interface with high performance JESD204B data convertors. The device also includes a digital front-end (DFE) that can process TX and RX signals, forming a system optimized alternative to FPGAs. This demonstration focuses on the JESD attach and digital front-end (DFE) signal processing capabilities of the 66AK2L06 SoC interfaced with TI's high performance ADC14X250 and DAC38J84 wideband data convertors. The demo consists of transmitting a sample file from the SoC through the DAC and looping it back via the ADC into the SoC. The available sample data files include dual-tone test patterns and multi-tone test patterns.

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1 System Description

The DSP provides baseband data for one 80 MHz antenna carrier (F_S = 122.88 Msps/carrier) to the digital front-end (DFE) of the 66AK2L06 SOC. Carrier data is up-sampled from 122.88 Msps at baseband to provide 245.76 Msps at the JESD interface. Although there are 4 JESD Lanes on the 66AK2L06 SoC, only one is used. ADC works in a real mode, and the JESD204B Serdes link rate is 4.9152 Gbps. Figure 1 shows the system block diagram.
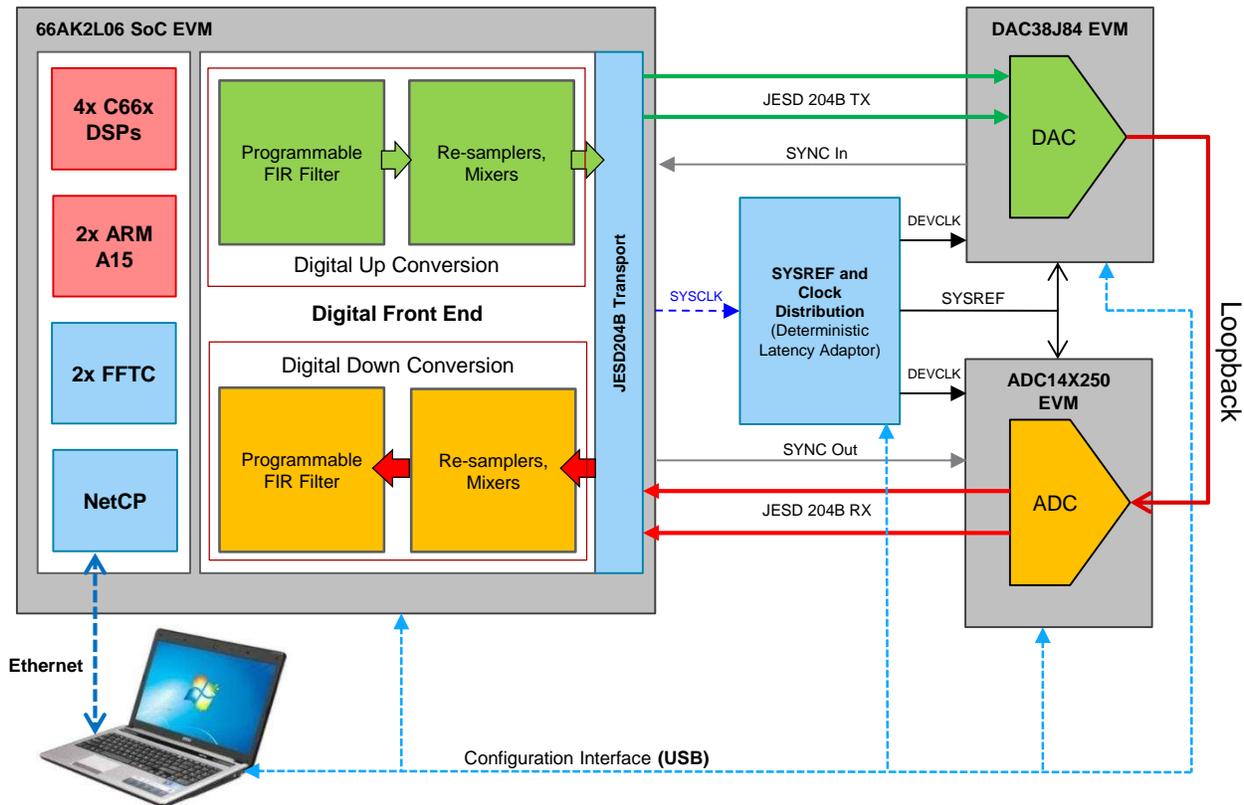

Figure 1. System Block Diagram

The DAC38J84 receives the JESD204B as parallel IQ data with a byte clock of 245.76 MHz. The DAC output rate is 491.52 Msps with an interpolation ratio of 2. The output of the DAC is centered at 61.44 MHz by default.

TI reccomends using a spectrum analyzer to check the DAC output before running the loopback test. In the loopback case, the DAC output signal is sent to the ADC14X250 through a low-pass filter. The device clock provided on the ADC14X250 is 245.76 MHz. The ADC14X250 sends real data to the DFE over JESD204B with a byte clock of 245.76 MHz.

On the RX side, the DFE inside of the 66AK2L06 SOC down-samples the data steam to 122.88 Msps.

2 Getting Started

2.1 Required Hardware and Software Components

Hardware Components:

- The 66AK2L06 EVM, rev. 3.0, with the following accessories:
  - A 12 V power supply
  - A mini-USB cable for UART connection
  - An Ethernet cable
- The K2L-HSP FMC Adapter Rev.A (also called Deterministic latency card - DLC) with the following accessories:
  - A mini-USB cable for connection with a PC
- The DAC38J84, rev. D, with the following accessories:
  - A 5-V DC power supply
  - A mini-USB cable for the GUI SPI program
- The ADC14X250 EVM with the following accessories:
  - A 5-V DC power supply
  - A mini-USB cable for the GUI SPI program
- DC-120 MHz low-pass filter
- SMA cables

Software Components:(download the links provided for the GUI installers)
The demo package is provided as a Windows installer executable. Running this installer on the Windows host extracts the various software components as per the following directory structure:

- RFSDK2_<latest_version>: Top level directory, includes:
  - RFSDK2_<latest_version>_full-bin.tar.gz: Demo package to be installed on top of the MCSDK 3.1.4.7 on the 66AK2L06 EVM.
  - RFSDK2_<latest_version>-66AK2L06-Design-Demo_Win_GUI_Configs.zip: Board initialization and configuration files for ADC14X250 and DAC38J84 EVM GUIs.
  - mcsdk314_rfsdk.tar.gz: MCSDK patches for the demo.
  - RFSDK2_<latest_version>-doc.tar.gz: Documentation and Release notes.
- Configuration GUIs for Data convertor EVMs (Windows based)
  - ADC14X250 EVM GUI: http://www.ti.com/tool/adc14x250evm
  - DAC38J84 EVM GUI: http://www.ti.com/lit/zip/slac644
- Configuration GUIs for K2L-HSP FMC Adapter EVMs (Windows® based)
  - For more information about the DLC and DLC GUI, contact TI support in the E2E Keystone Multicore Forum.

2.2 Setup Hardware

To connect the 66AK2L06, DAC38J84, and ADC14X250 EVMs:

1. Plug the FMC male connector of the ADC14X250 into J11 (FMC female) of the DLC.

2. Plug the DAC38J84 EVM's FMC male connector into J10 (FMC female) of the DLC.

3. Plug the J4 FMC female connector of the DLC into CN16 (FMC female) of the 66AK2L06 EVM. For a review of the setup with all boards connected, see Figure 2.

To connect the clocks:

1. Connect an SMA cable from J15 of the DLC to the CLK input (J4) of the ADC14X250 EVM.

> **NOTE:** The LMK04828 on the Deterministic Latency Card is a dual-PLL clock chip. The clock-in reference for PLL1 comes from the 66AK2L06 EVM (122.88 MHz). The on-board VCXO of 122.88 MHz on the DLC is used as reference for PLL2. The output of LMK04828 provides device clock to both DAC38J84 and ADC14X250.

Connecting the DAC output to the ADC input (the loopback configuration):

1. Connect the DAC output at J2 (IOUTAP) to the low-pass filter.

2. Connect the other end of the DC-120 MHz low-pass filter to J3 (VIN-) of ADC14X250 EVM to complete the loopback.

3. Figure 3 shows the setup with all of the clock and loopback connections made previously.

USB and Ethernet Connections:

1. The 66AK2L06 EVM has two mini-USB connectors and one of them, J6, provides the BMC (Board Management Controller) and Linux® serial terminal interfaces (multiplexed onto the same port).

2. Connect the mini-USB port J6 on 66AK2L06 EVM to the PC using a mini-USB cable.

3. Connect the ADC14X250 EVM, DAC38J84 EVM

4. Connect the DLC to the Windows host with mini-USB cables.

5. Connect the 66AK2L06 EVM ETH-0 (lower port) to the same network as the Windows host over a 1Gbps connection (either directly or through a Gigabit Switch).

Power

1. Provide +5V to the ADC14X250 EVM and +5V to the DAC38J84 EVM using the provided 5V DC power supplies.

2. Provide +12V to the 66AK2L06 EVM using the provided 12V DC power supply.

Miscellaneous

• For initial test and debug purposes, check the output of the DAC on a spectrum analyzer before trying to get the loopback working.

• To get the loopback working again, connect the DAC38J84 EVM J2 (IOUTAP) to the spectrum analyzer input.

• When the DAC38J84 J2 output is working, configure and connect the DAC38J84 and the ADC14X250 to loop back.

Figure 2 shows the boards connected together, and Figure 3 shows the complete setup with the cables and power supplies connected.
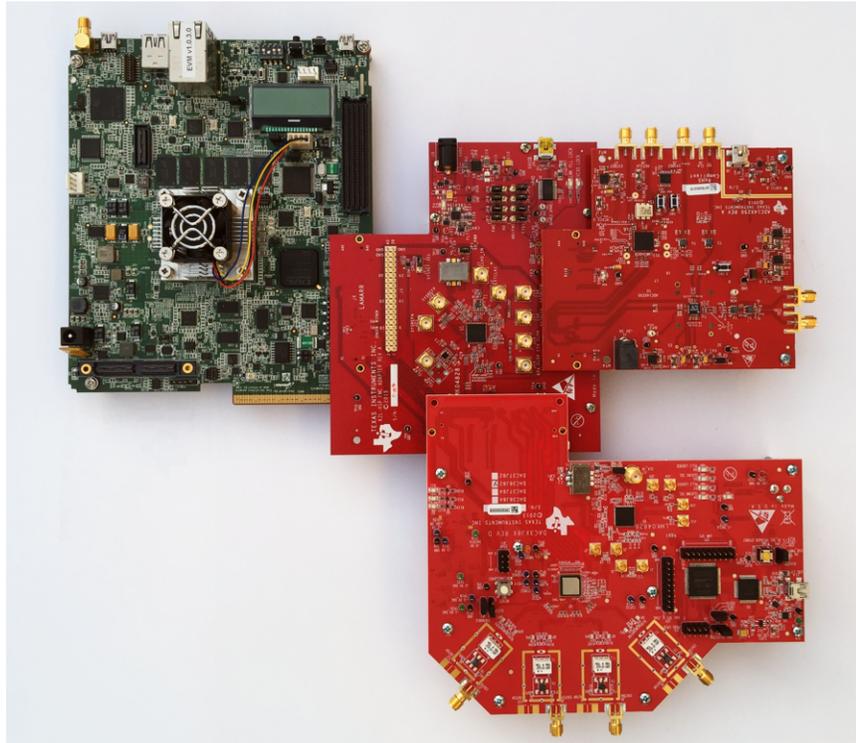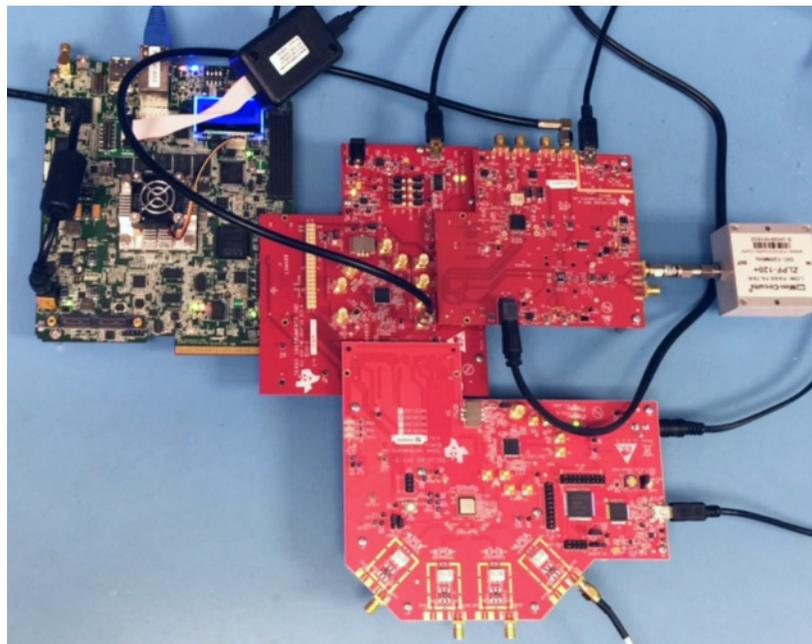

Figure 2. Boards Connected Together

Figure 3. Complete Setup With Cables and Power Supplies Connected

2.3 Setup Software

2.3.1 Getting the 66AK2L06 EVM Ready

1. Connect a terminal program (for example, Tera Term) to the 66AK2L06 EVM Linux COM port.

2. Use the following serial port settings in the terminal program:

> **NOTE:** You must have the Silicon Labs cp210x vcp driver installed on the Windows host in order to enumerate the 66AK2L06 EVM virtual COM ports in the Windows Device Manager.

Figure 4 shows the 66AK2L06 EVM virtual COM ports.

Figure 4. 66AK2L06 EVM Virtual COM Ports

The COM port for Linux is the higher numbered port, for example, COM10 in this case (the port numbers on your system may be different).

Follow the procedure below to prepare the 66AK2L06 EVM for the demo:

Update the UBIFS Image on the 66AK2L06EVM:

1. The factory installed MCSDK image on the 66AK2L06 must be updated to the image provided with MCSDK 3.01.04.07.

2. A tftp server is required to update the UBIFS image on the 66AK2L06 EVM.

3. Download the appropriate MCSDK installer (mcsdk_3_01_04_07_setupwin32.exe for Windows or mcsdk_3_01_04_07_setuplinux.bin for Linux) for your tftp host.

4. Run the installer and follow the prompts to install the new MCSDK on your tftp host machine.

5. Once installed, the UBIFS image for 66AK2L EVM is available in the images sub-directory under the MCSDK install directory.

6. The image is named **k2l-evm-ubifs.ubi**.

7. Follow the instructions given in the Keystone-II MCSDK user guide under the Using UBIFS file system section to update the existing image on the EVM with the UBIFS image (mentioned in step 6).

> **NOTE:** The image and directory names given in this section may not match with the image name given above, however, the general procedure is the same. Use the appropriate *tftp_root* directory path, image name and *serverip* according to your setup.

> **NOTE:** TI recommends using the automated u-boot scripts, namely *get_ubi_net* and *burn_ubi* as defined in the update instructions to download and flash the UBIFS image, respectively.

Install the Device Tree Binary (dtb) Patch:

1. Once the UBIFS image on the 66AK2L06 EVM is updated as described in Step-1, the dtb file on the EVM needs to be updated (replaced) with the one provided under mcsdk314_rfsdk.tar.gz in the Demo package.

2. Extract the dtb binary file from mcsdk314_rfsdk.tar.gz.

3. Follow the instructions given in the Keystone-II MCSDK user guide under the Updating Boot volume images from Linux kernel section.

   - The name of the patched dtb provided in the demo package may be different than the working dtb filename in the boot volume on the EVM.

NOTE: Remember the original dtb filename and ensure that you copy the new dtb file to the boot volume with the same name. Failing to do so will cause a Linux boot failure when the board is restarted.

Install the Demo Package: (user interactions are italicized)

1. The Demo software is provided as a compressed archive named RFSDK2_<latest_version.tar.gz> in the Demo package. Copy this file to the tftp root directory of your tftp server.

2. With Linux booted, copy the above file to /home/root on the EVM (using tftp or scp).
   root@k2l-evm:~# *pwd*
   /home/root
   root@k2l-evm:~# *tftp -g -r* RFSDK2_<latest_version.tar.gz> *<tftp_server_ip_addr>*

3. Extract RFSDK2_<latest_version>-full-bin.tar.gz in the root directory
   root@k2l-evm:~# *cd /*
   root@k2l-evm:/# *tar xvf /home/root/* RFSDK2_<latest_version>-full-bin.tar.gz

4. Create a soft link to the default board configuration to finalize the installation
   root@k2l-evm:/# *cd /etc/radio/board*
   root@k2l-evm:/etc/radio/board# *ln -s lamarr-evm-demo2-mcsdk3147 default*
   root@k2l-evm:/etc/radio/board# *ls -l default*
   lrwxrwxrwx 1 root 42005 18 Dec 12 21:30 default → *lamarr-evm-demo2-mcsdk3147*

5. Reboot Linux on the EVM.

2.3.2 Installing PC Side Software

Download GUI installers for the DAC34J84 and ADC14X250 EVMs from the links provided in the Section 2 section, and follow the steps given below to install the corresponding GUIs.

1. Install ADC12X250 GUI

2. Go to the Configuration Files directory after the ADC12X250 GUI is installed.

   • The directory is typically located at *C:\Program Files (x86\Texas Instruments\ADC14X250EVM\Configuration Files*.

3. Replace ADC14X250_Cal.cfg with the corresponding file provided under RFSDK2_<latest_version>.66AK2Lx-Design-Demo-Win-GUI-Configs in the demo package.

4. Install the DAC34J84 GUI.

3   Running the Demo

3.1   Setting Up the DAC and ADC EVMs

3.1.1   Powering Up

Power up the boards in the following sequence:

1. 66AK2L06 EVM
2. ADC12X250 EVM
3. DAC38J84 EVM

3.1.2   K2L-HSP FMC Adapter

1. Start the K2L-HSP FMC Adapter GUI.
2. Ensure the USB Status indicator is green.
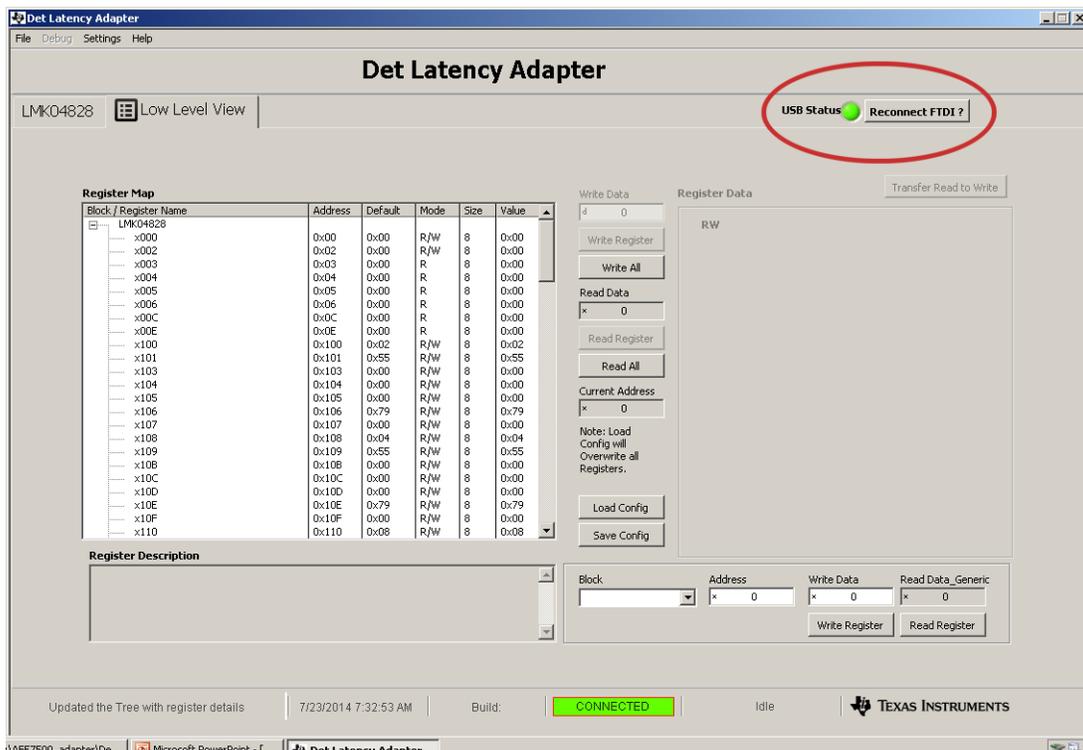
    Figure 5 shows the K2L-HSP FMC adapter GUI.

Figure 5. K2L-HSP FMC Adapter GUI

3. Click on the *Load Config* button.
4. Select the file named *66AK2L06_dac491_adc245_demo2.cfg* provided under
    RFSDK2_<latest_version>.66AK2Lx-Design-Demo-Win-GUI-Configs in the demo package. This will
    program the required registers of the LMK04828.

Figure 6 shows the GUI-Load cfg.
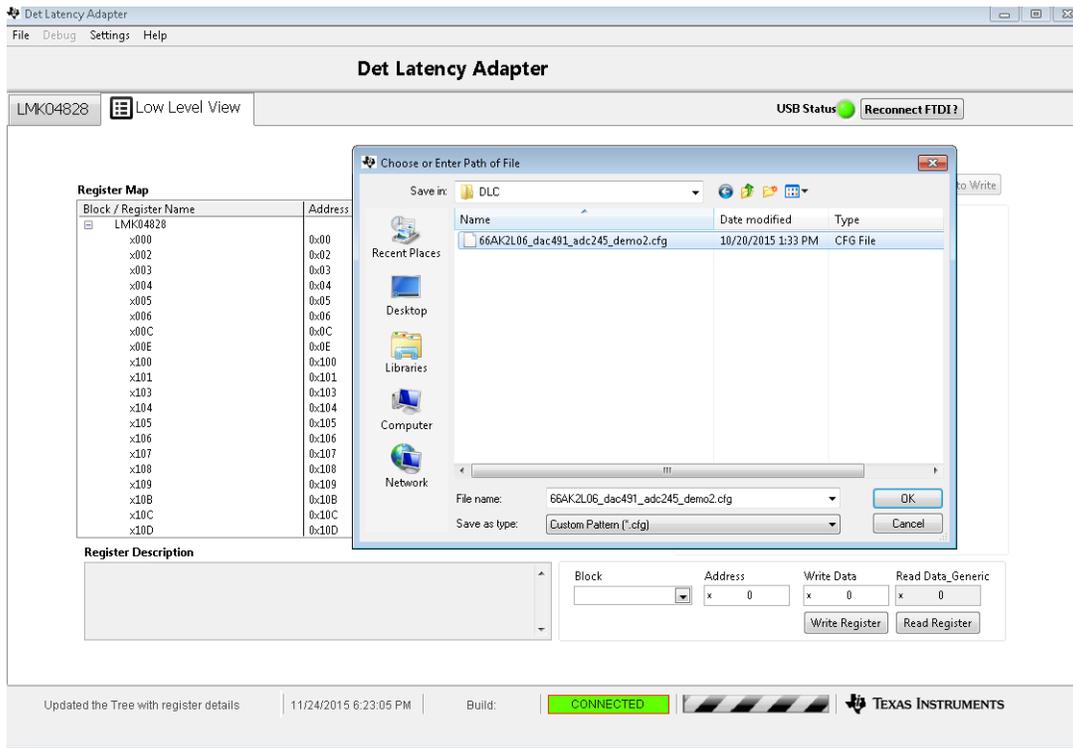
Figure 6. GUI-Load CFG

Figure 7 shows the GUI-Clock outputs.
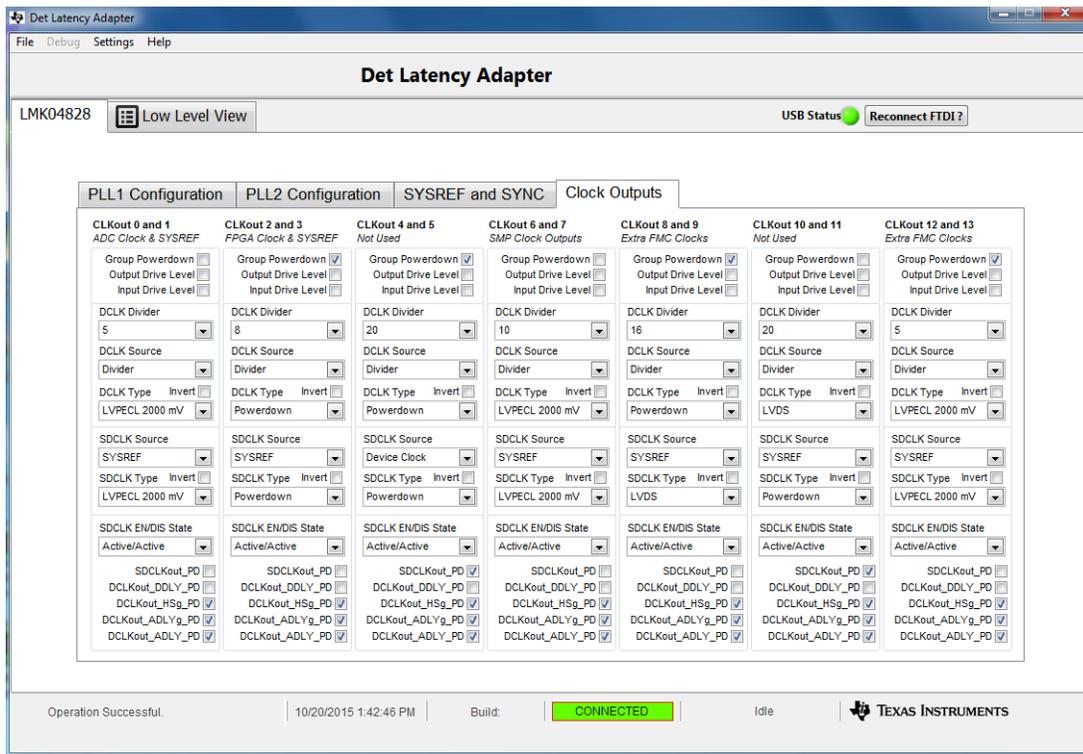
Figure 7. GUI-Clock Outputs

Details on the clock configuration:

- **CLKOUT 6:** ADC14X250 Device CLK is GTX CLKP (J15), div 10 for 245.76 MHz, LVPECL. ADC12J4000 SysRef is not used.

- **CLKOUT 0:** DAC38J84 Device CLK, div 5 for 491.52 MHz, LVPECL. DAC38J8x SysRef CLK is SDCLKOUT 1, LVPECL.

- On a successful configuration, the *PLL2 LOCK* and *LMK LOCK LEDS* on the DLC should be ON as shown. Make sure that the *LMK LOCK LED* is bright, otherwise, power-cycle the DLC and follow the configuration instructions again.

Figure 8 shows the LED status.

Figure 8. LED Status

3.1.3 DAC38J8x EVM GUI

1. Start the DAC3xJ8x GUI (Start→All Programs→Texas Instruments DACs→DAC3xJ8x GUI).
2. Make sure that the *USB Status* is green.
3. Set the EVM Clocking Mode to *Onboard*.
4. Select Device as DAC38J82 (this demo uses 2 of the 4 DAC channels on the DAC38J84).
5. Select DAC Data Input Rate as 245.76 Msps.
6. Select Number of Serdes Lanes as 2 and Interpolation as 2.
7. Click the *Program LMK04828 and DAC3XJ8X* button.

    Figure 9 shows the DAC38J8x GUI start page.
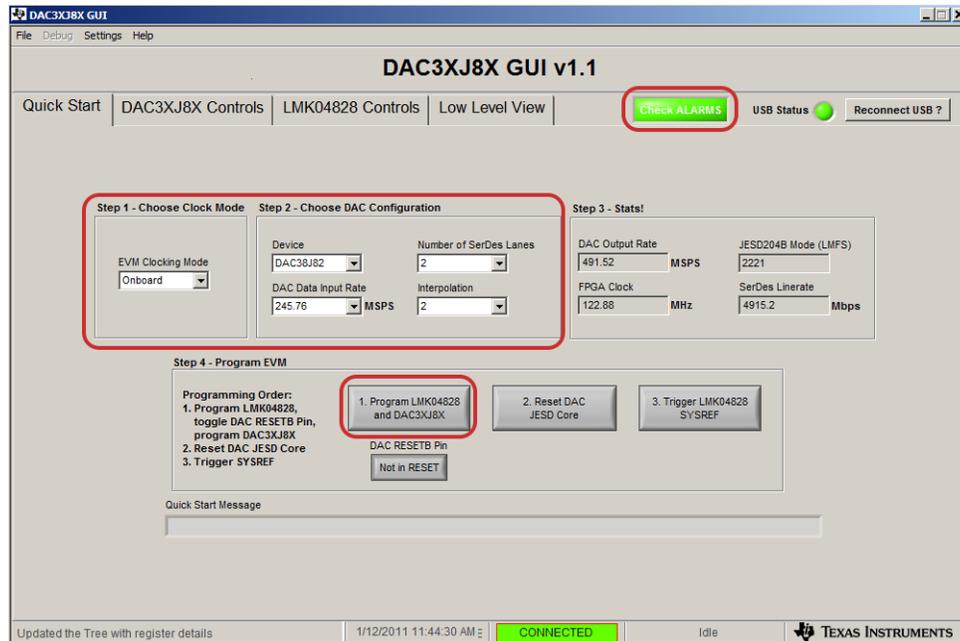
Figure 9. DAC38J8x GUI Start Page

8. Click the *Low Level View* tab and the *Load Config* button once the programming is complete. See Figure 10 for the low level view to load registers.
9. Load the file *K16_66AK2L06_rev3_491p52_demo2.cfg* provided under RFSDK2_<latest_version>.66AK2Lx-Design-Demo-Win-GUI-Configs in the demo package.

10. Under the tab *DAC3XJ8X Controls/ Dig Block 1*, press the *Perform SIF Synch* button, as shown in Figure 11.
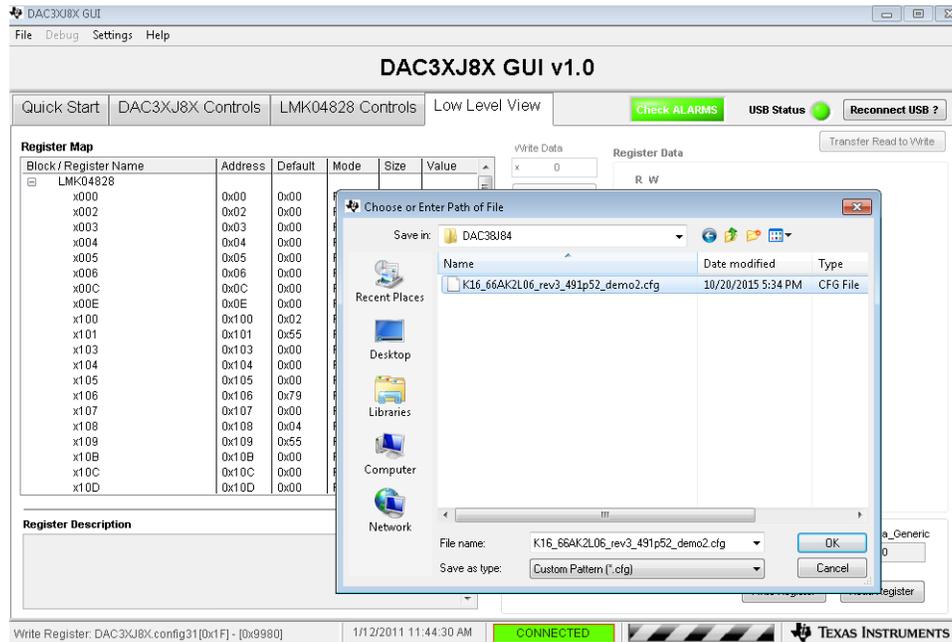
Figure 10. Low Level View to Load Registers

Figure 11 shows the DAC38J8x GUI course mixer setting.
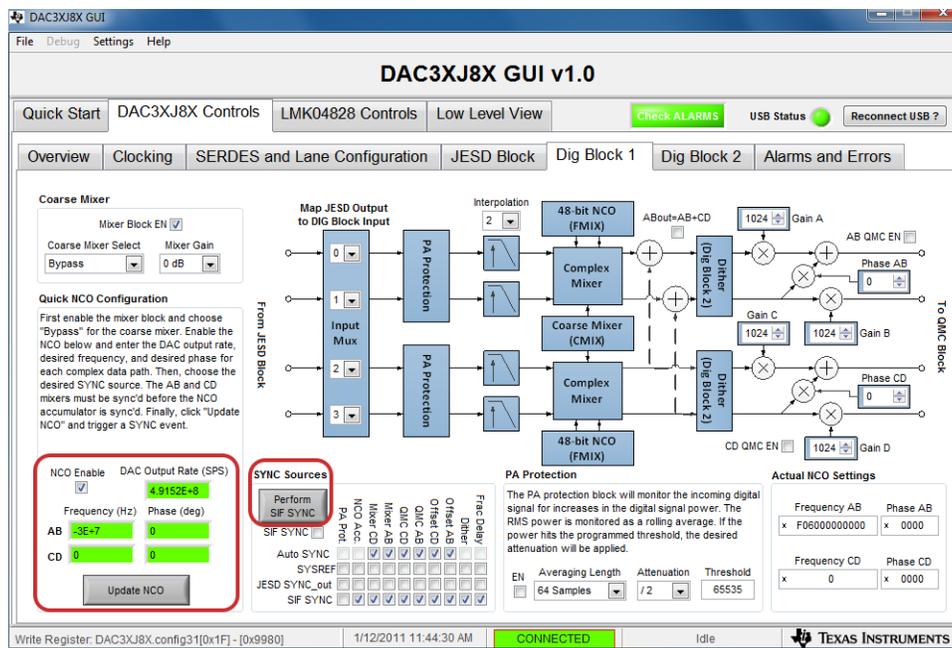
Figure 11. DAC38J8x GUI Course Mixer Setting

It is optional to test with a DAC frequency shift. The list below explains the DAC mixer setting and control procedure when a frequency shift is desired.

1. The mixer block is now enabled, however, the course mixer is bypassed.
2. The signal is shifted by setting the NCO value.
3. The sample rate is set to 491.52 Msps.
4. The default NCO is 0 Hz.
5. If you want to shift the signal, by –30 MHz for example, set the AB value of –3E07 as shown in Figure 11.
6. Click Update NCO.
7. Click Perform SIF Sync.
8. The range to test is from –50 MHz to +50 MHz.

Figure 12 shows the DAC38J8x GUI SERDES lane configuration.
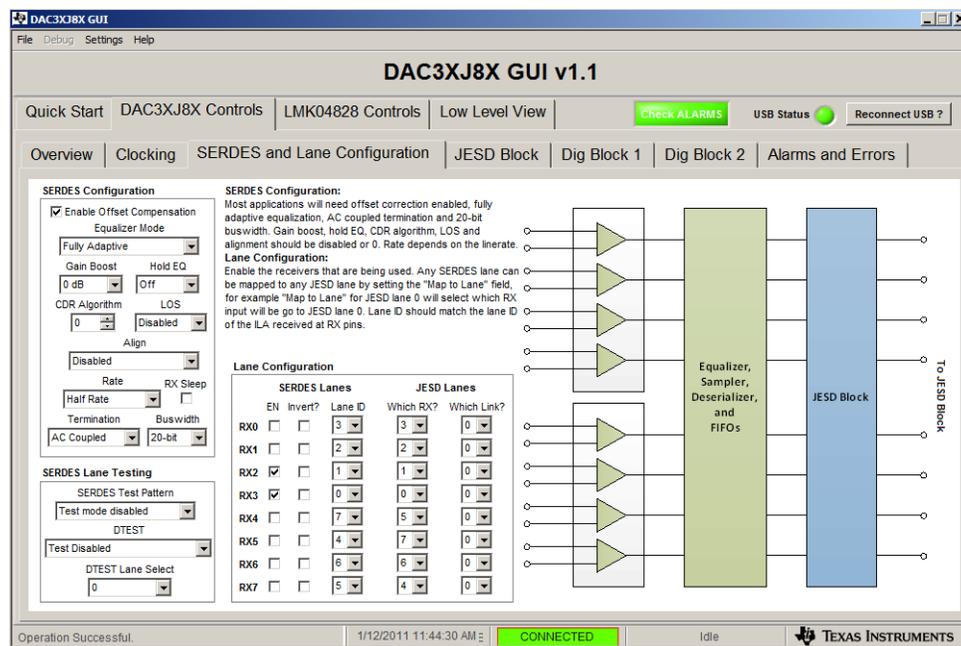
Figure 12. DAC38J8x GUI SERDES Lane Configuration

3.1.4 ADC14X250 GUI

1. Start the ADC14X250 GUI (Start→All Programs→Texas Instruments ADCs→ADC12X250EVM GUI).

2. Make sure that the USB status is green.

3. If the GUI does not connect to the board, click on the *Reconnect FTDI* button until the GUI connects to the board. This connection is indicated by a green USB Status.

4. Click on *Calibrate ADC14X250*.

Figure 13 shows the ADC14X250 EVM GUI start page.
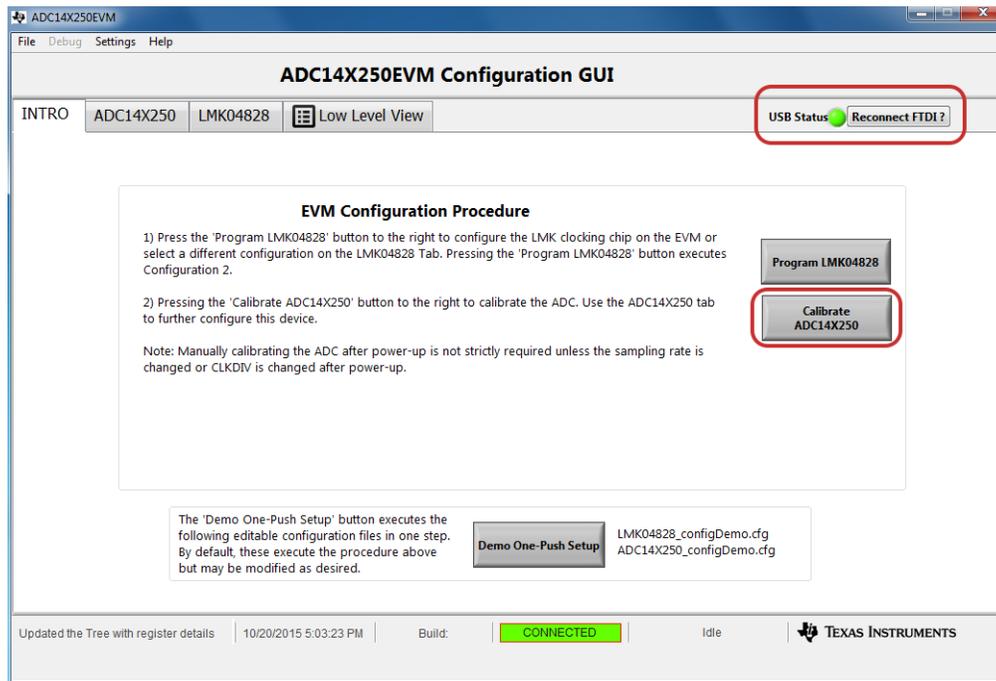
Figure 13. ADC14X250 EVM GUI Start Page

Figure 14 shows the ADC14X250-JESD204B tab on the GUI after the default program is loaded. K is 16 when the ADC14X250_Cal.cfg is replaced.
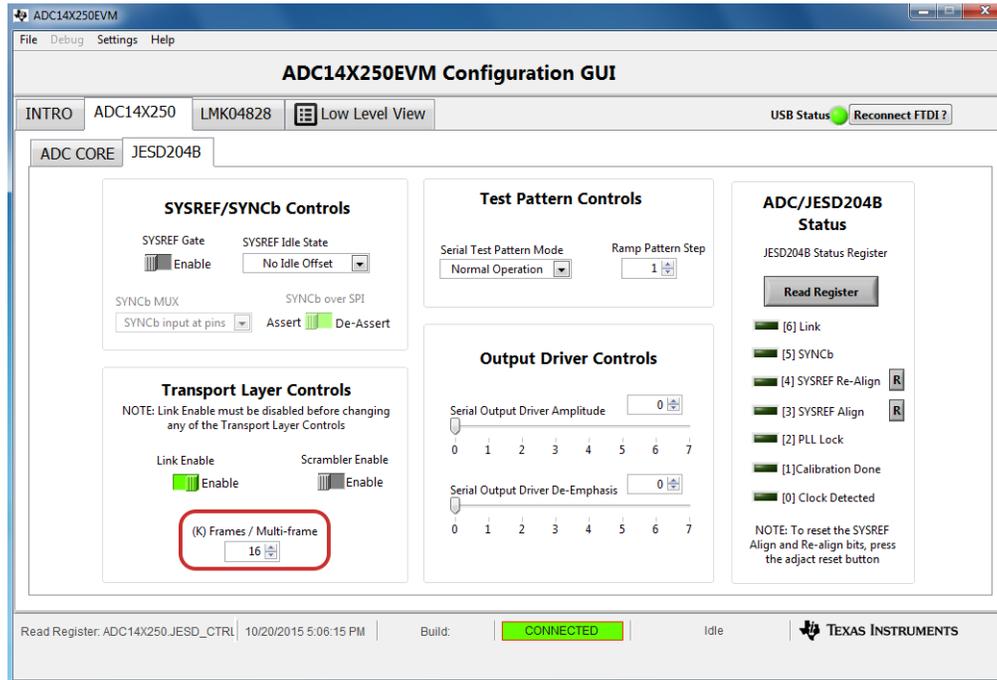
Figure 14. ADC14X250EVM GUI–JESD204B

3.2 Starting the Demo on the 66AK2L06 EVM

1. Connect a terminal program (for example, Tera Term) to the 66AK2L06 EVM Linux COM port and log in as the root user.

2. Determine the IP address assigned to the board using *ifconfig*, as shown in Figure 15.

Figure 15. Querying the Board IP Address

3. Type "touch /tmp/rfsdk_stubbed_afe" in the 66AK2L06 Linux terminal. This is required running a loop back test with ADC and DAC, not when JESDlpbk configuration is selected.

4. Open a web browser on the PC and point the browser to *<EVM_IP_ADDRESS>:8080*. This should open the RFSDK Web GUI, as shown in Figure 16.

5. Press "High IF Sampling Receiver ADC14X250 Demo".

Figure 16. RFSDK Web GUI

6. The web GUI will navigate to the RFSDK v2.0 DEMO2 Mode.

7. Press the *Select* button once the reset is complete to open the *Radio Configuration Dialog*, as shown
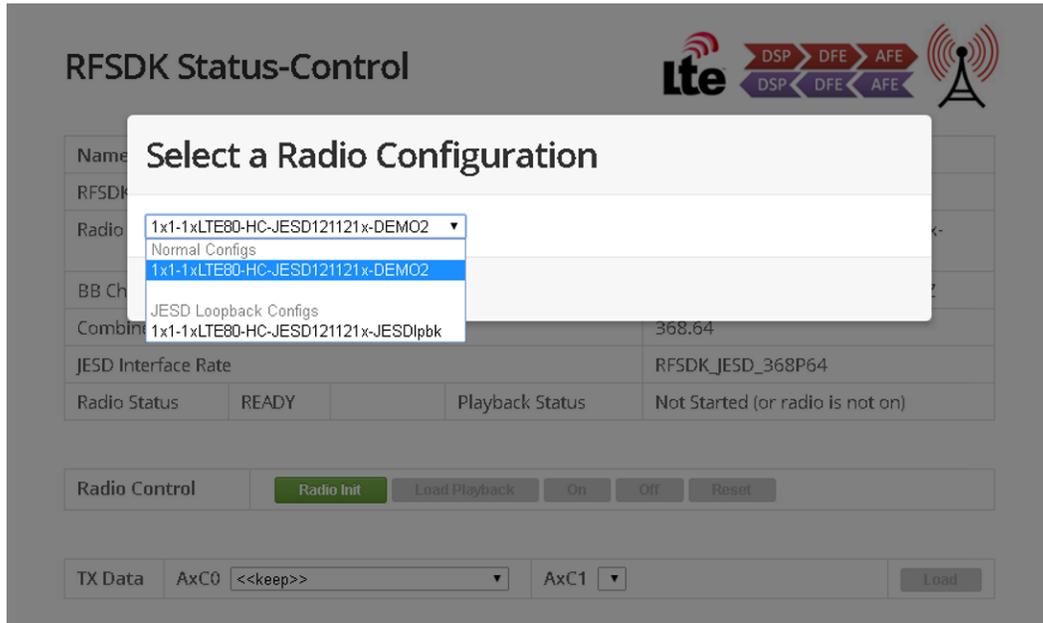   in Figure 17.

Figure 17. Radio Configuration Selection

8. Select a configuration from 1×1-1xLTE80-HC-JESD121121x-DEMO2, or 1×1-1xLTE80--HC-
    JESD121121x-JESDlpbk. Press *Select*.

9. In "Radio Contrl", press "Radio init", then "Load Playback", and then "On" in sequence to start the playback demonstration. (The status of playback should change to Started/Alive, which indicates the test is running).

Figure 18. DEMO 2–Status Control

10. Click the AxC0 drop-down menu and select "Fs=122.88 2 tones, −1 MHz and +2 MHz" or "Fs=122.88 200 tones(100MHz BW)", which span from −50 to 50 MHz. (This loads the selected signal patterns into the corresponding transmit buffers.) Click the "load" button. The test patterns can be changed without having to stop the test.

Figure 19. DEMO 2−Loading Test Patterns

11. Navigate to the *TX Signal Capture @ DSP Page* and press *Refresh Capture*. This sends a request to the DSP to perform a signal capture of the baseband data on the TX side (that is, before the signal data is sent to the DFE).
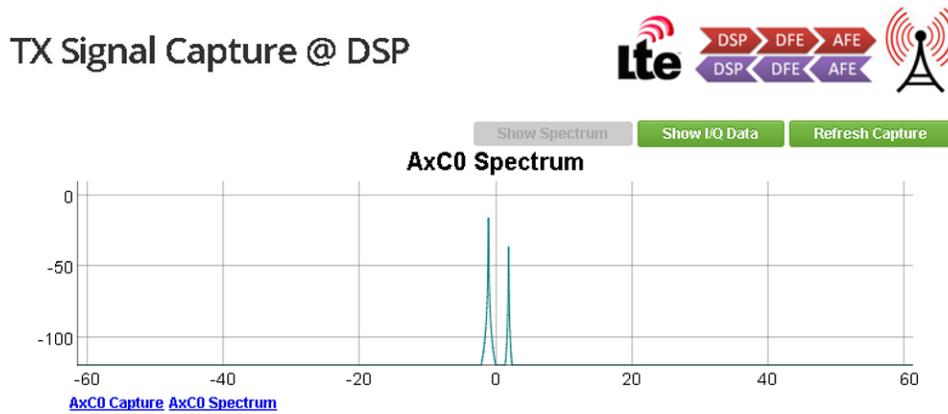

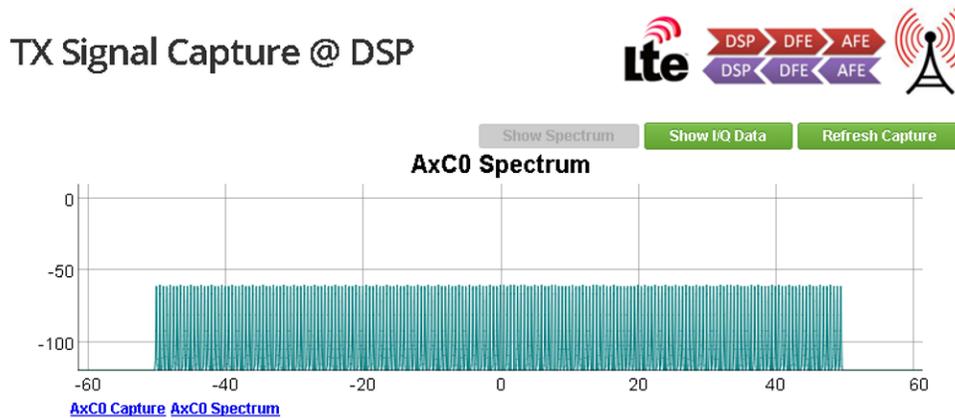**Figure 20. TX Signal Capture at DSP (2–Tone Data Pattern)**

Figure 21. TX Signal Capture at DSP (200–Tone Data Pattern)

12. Navigate to the *RX Signal Capture @ DSP page* and press *Refresh Capture*. This sends a request to the DSP to perform a signal capture of the baseband data on the RX side (that is, after it has been looped back from the DAC38J84 to the ADC14X250 and after being down-converted and filtered by the DFE). The test pattern transmitted is recovered at the DSP after the DAC38J84 to ADC14X250 loopback. To view the RX signal capture at DSP, see Figure 22.
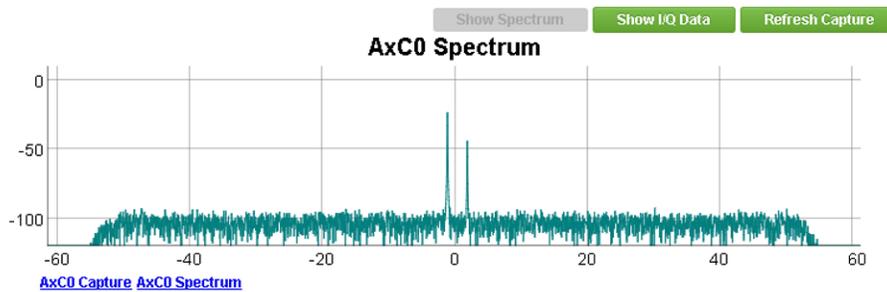

Figure 22. RX Signal Capture at DSP (2–Tone Data Pattern)

13. The RX captured data can be picked up by the FFTC co-processor and displayed as shown in Figure 23.
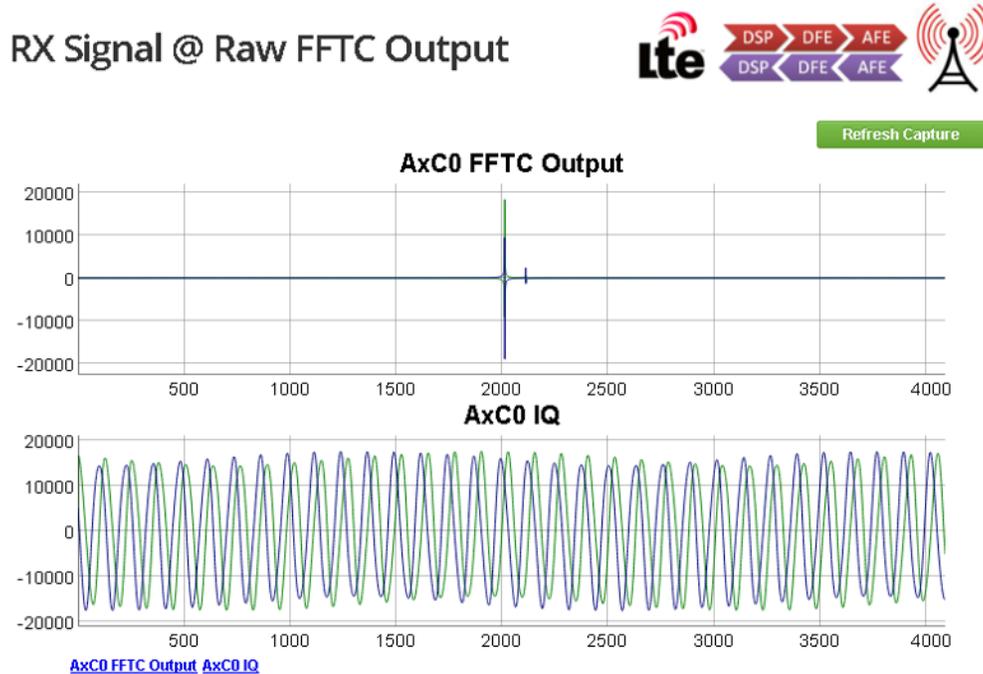

Figure 23. FFTC Output

14. Drag the mouse to zoom in on the graphs both vertically (to change the amplitude scale) and horizontally (to change the frequency scale). To view the zoom-in on the graphs, see Figure 24 and Figure 25.
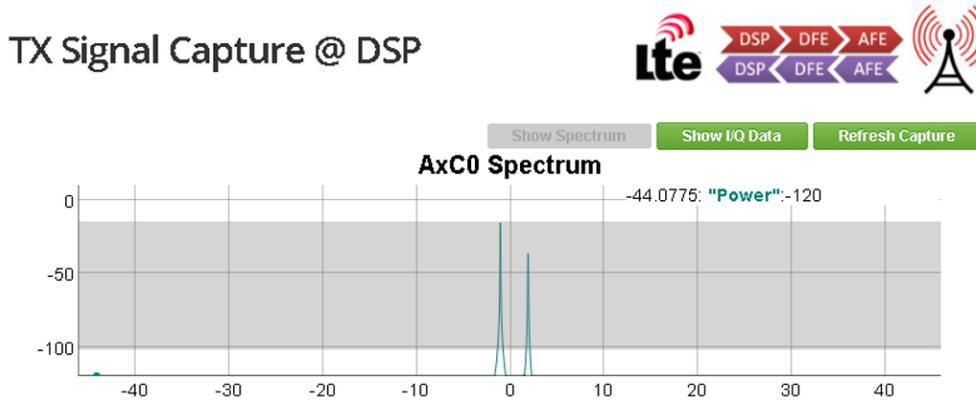

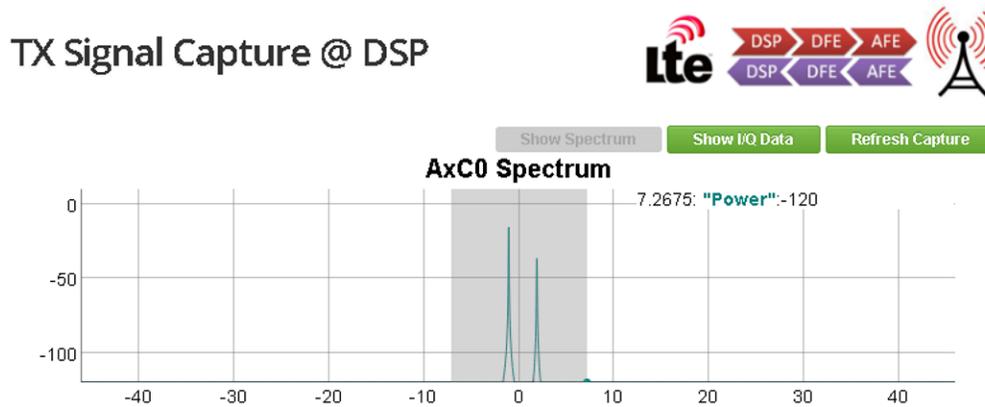**Figure 24. Changing the Amplitude Scale on the GUI**

Figure 25. Changing the Frequency Scale on the GUI

When loading the 200-tone data pattern, the RX capture is shown in Figure 26:
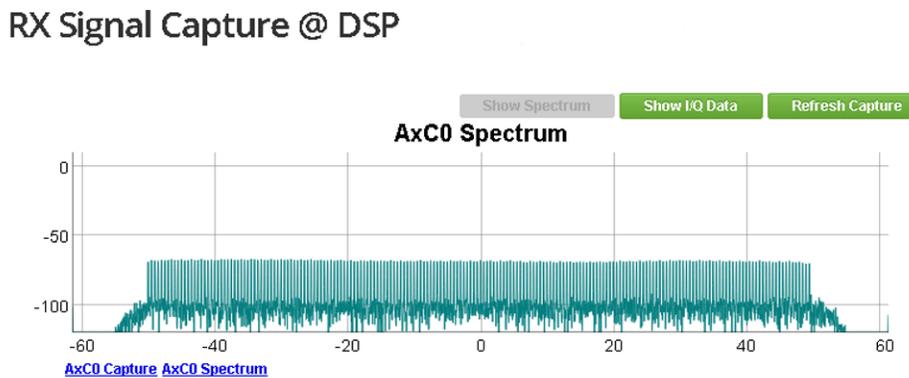
Figure 26. RX Signal Capture at DSP (200–Tone Data Pattern)

15. To stop the test, press "Off" (stop playback) and "Reset" (radio reset) on the Status-Control page.

4   Test and Debug

TI recommends checking the DAC38J8x output using spectrum analyzer for the first time setup. The two-tone output and 200-tones output are shown in Figure 27 and Figure 28.
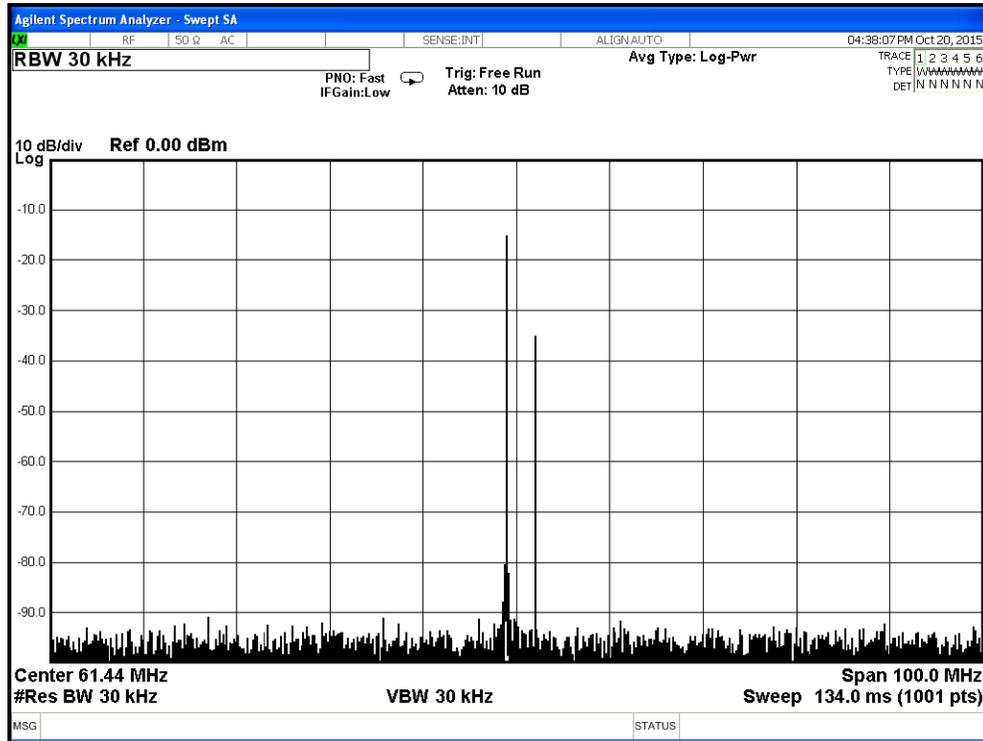
Figure 27. DAC Output–Two-tone Data
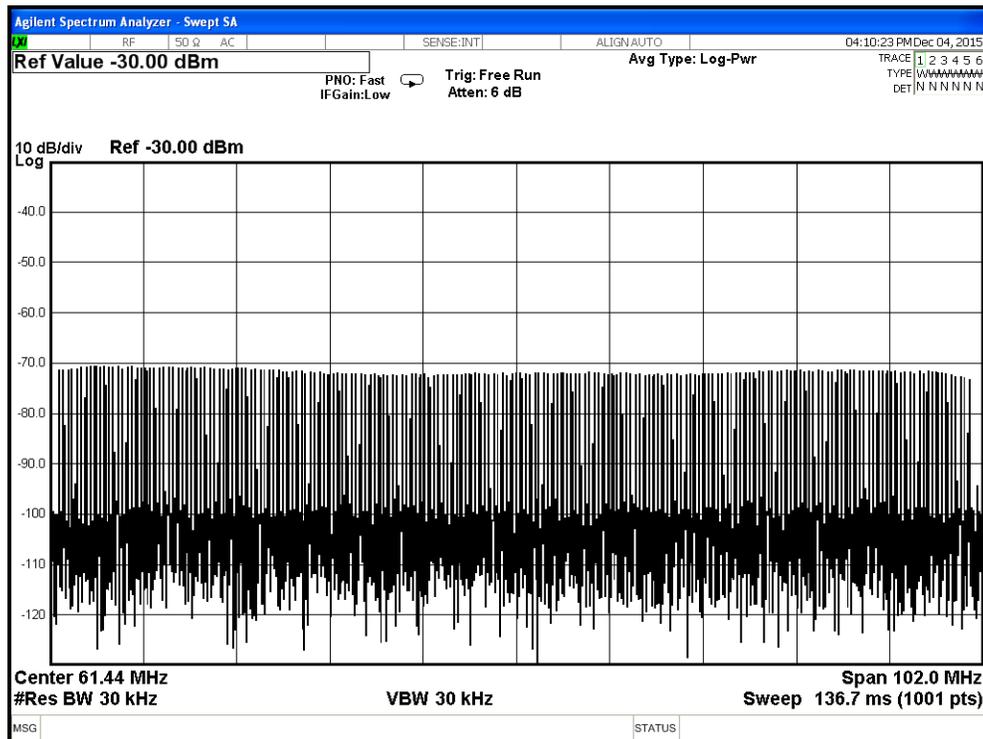
Figure 28. DAC Output– 200 Tones Data Pattern

5 References

Refer to the following links for more information related to the various hardware and software components used in this demo:

1. 66AK2L06 EVM: https://www.einfochips.com/index.php/partnerships/texas-instruments/k2l-evm.html#5-resources

2. DAC38J84 EVM: http://www.ti.com/tool/dac38j84evm

3. ADC14X250 EVM: http://www.ti.com/tool/adc14x250evm

4. Keystone-II MCSDK User Guide: http://processors.wiki.ti.com/index.php/MCSDK_User_Guide_for_KeyStone_II

5. Keystone-II Architecture DFE user guide: http://www.ti.com/lit/ug/spruhx8/spruhx8.pdf

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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