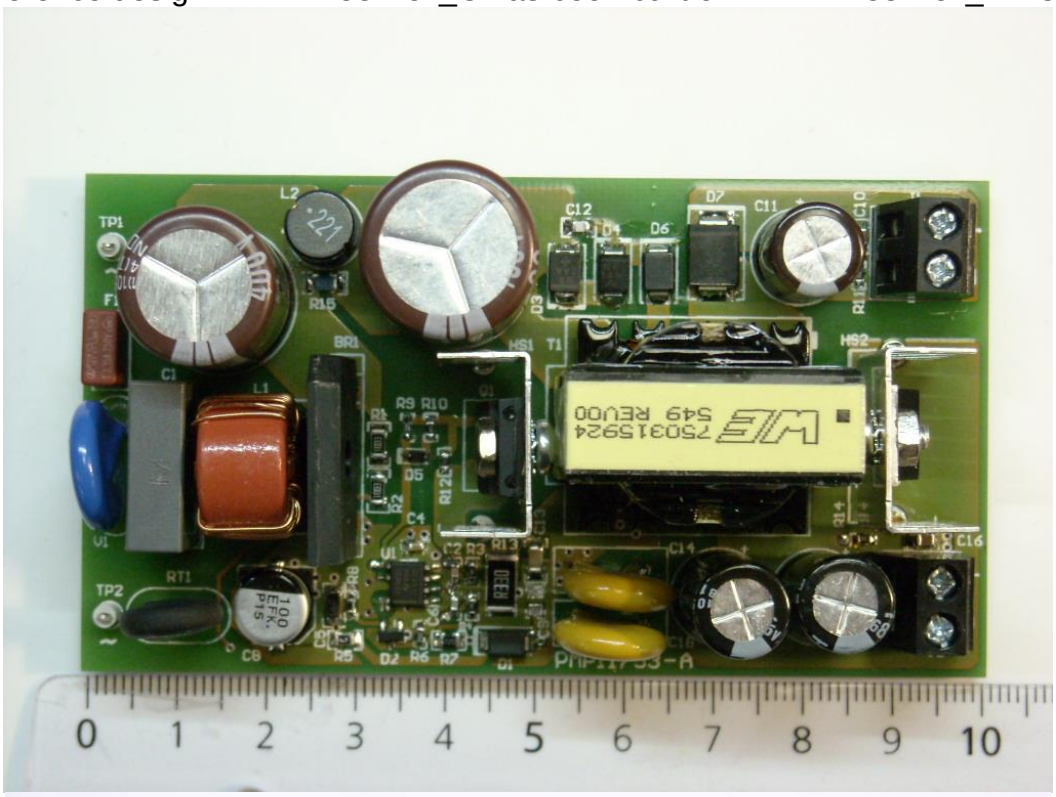
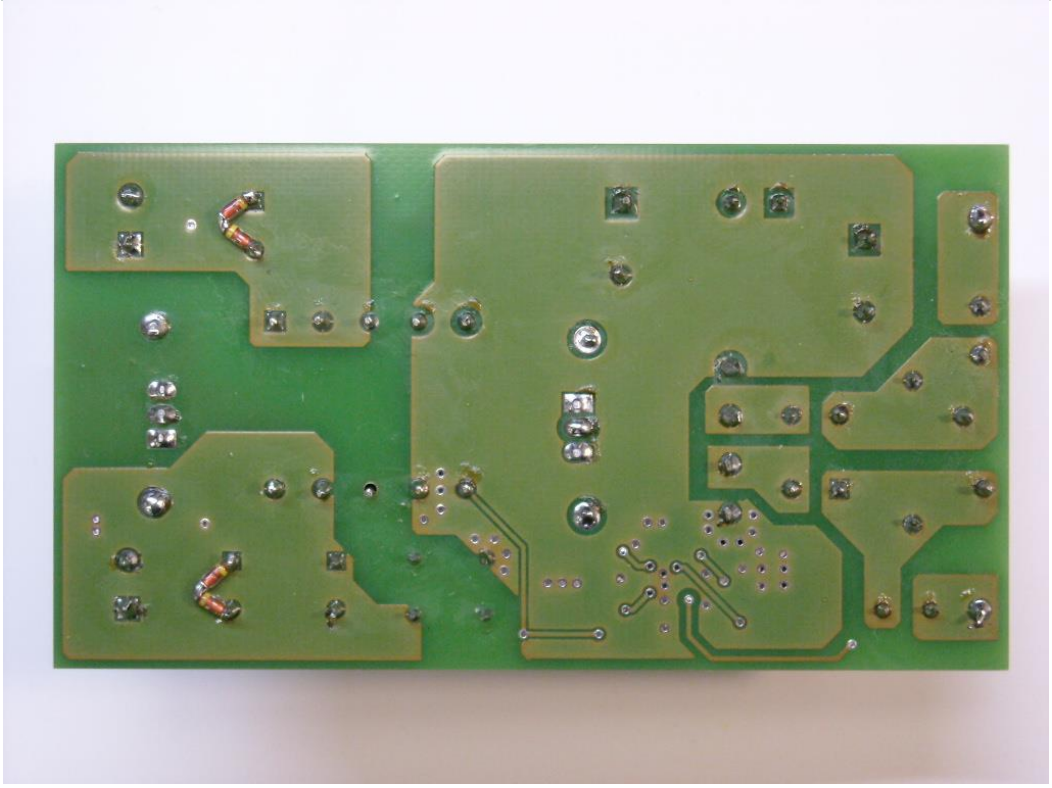
1 Photo of the prototype:

The reference design PMP11753 Rev_C has been built on PMP11753 Rev_A PCB



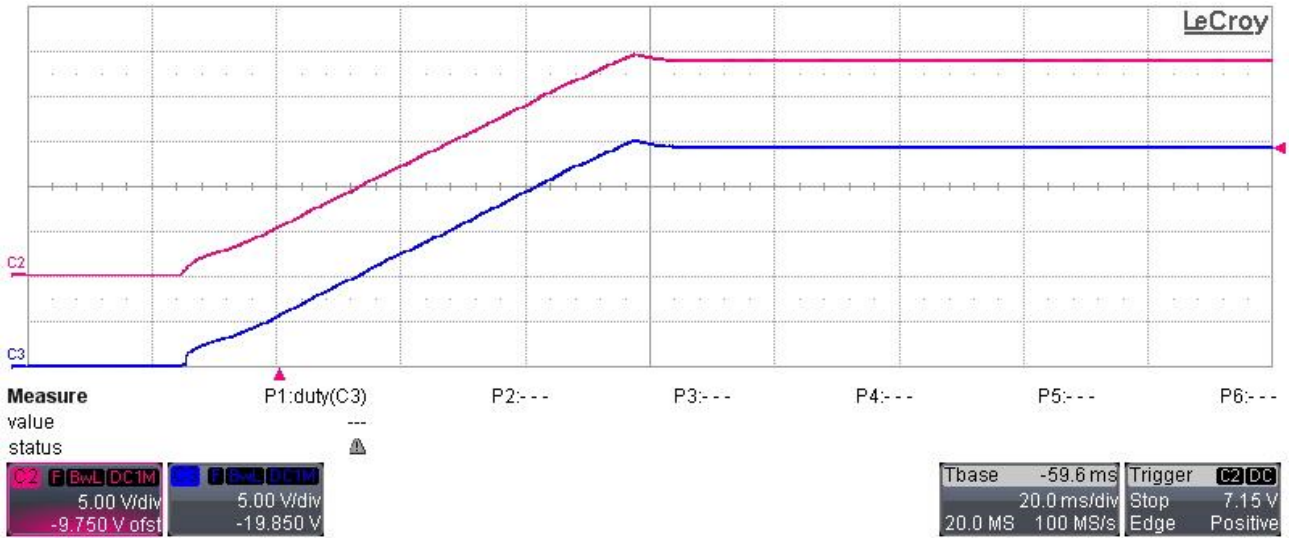


2 Startup

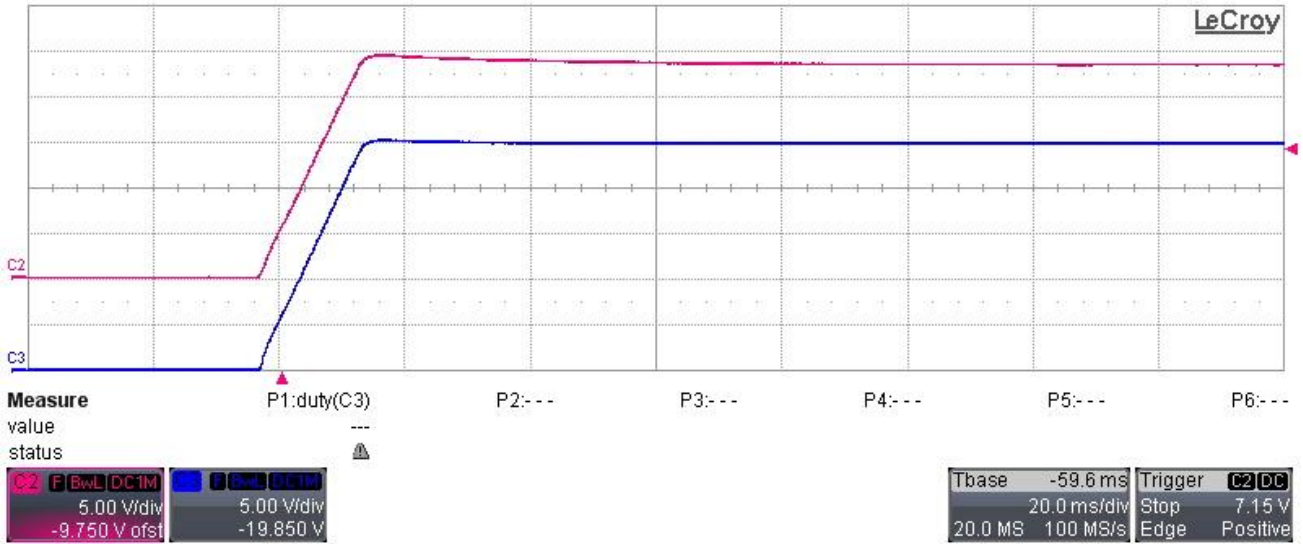
The output voltage behavior for both outputs is shown in the images below. The input voltage was set to 325Vdc. The outputs were fully loaded for the upper picture and unloaded for the bottom one.

Ch.2: Vout_1 (5V/div, 20ms/div, 20MHz BWL)
Ch.3: Vout_2 (5V/div, 20MHz BWL)

Full load on both outputs:

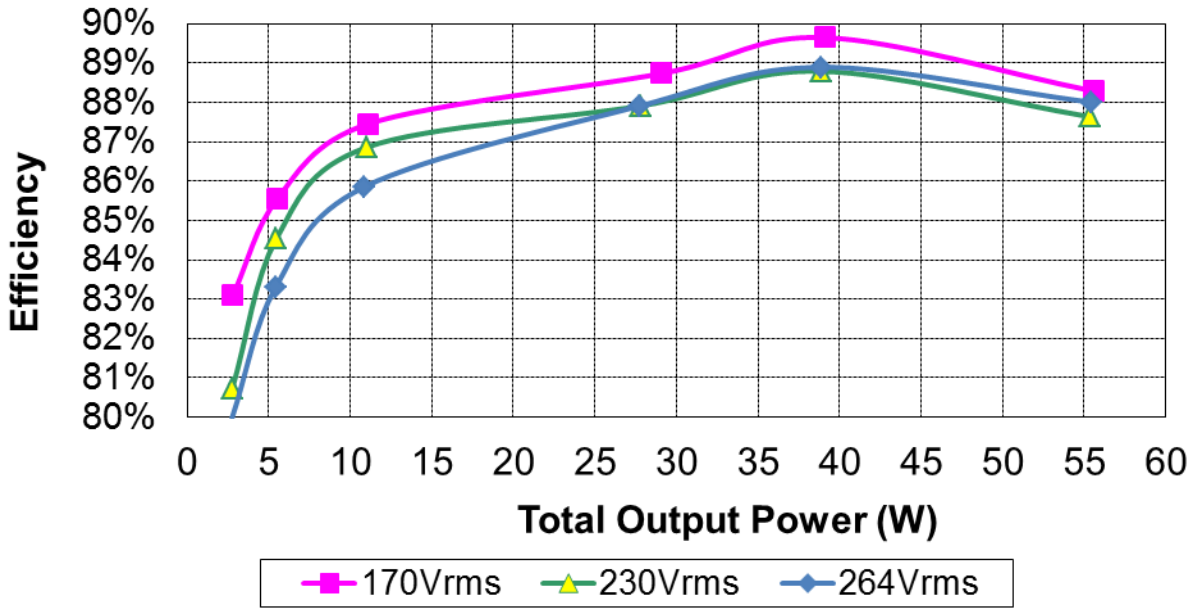


No load on both outputs:



3 Efficiency

The efficiency data are shown in the tables and graphs below.
The input voltage has been set respectively to 170Vrms, 230Vrms and 264Vrms.
Both outputs have been loaded from 0 to full load proportionally.



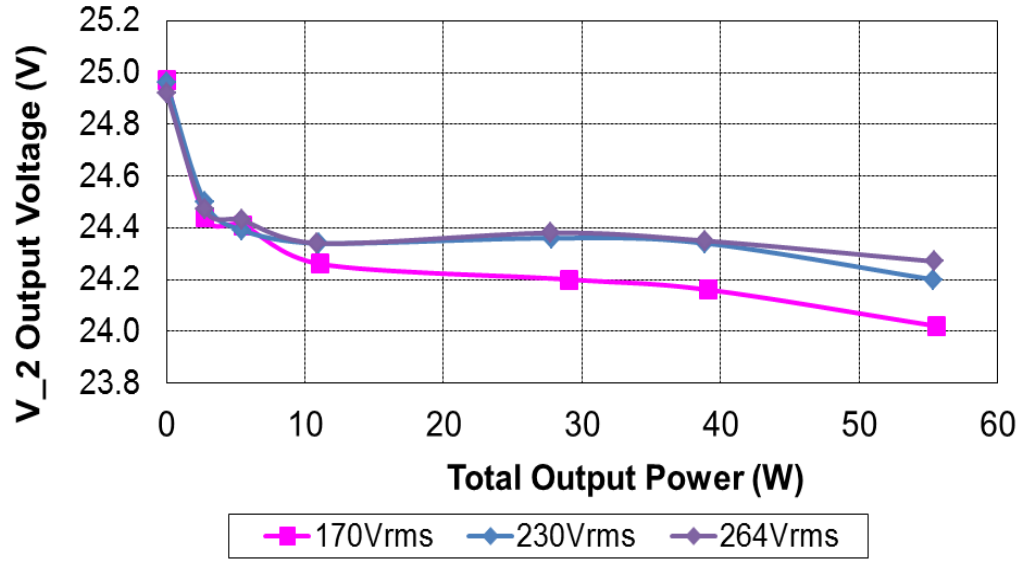
Vin (Vrms)	V_2 (V)	I_2 (mA)	V_1 (V)	I_1 (mA)	Pout (W)	Pin (W)	Eff. (%)
170	24.97	0.0	23.77	0.0	0.00	0.075	0.0%
170	24.44	98.5	23.88	16.1	2.79	3.360	83.1%
170	24.41	195.8	23.86	32.1	5.55	6.481	85.6%
170	24.26	397.4	23.77	61.5	11.10	12.695	87.5%
170	24.20	1055	23.76	149.7	29.09	32.78	88.7%
170	24.16	1412	23.74	211.4	39.13	43.65	89.7%
170	24.02	2017	23.64	302.3	55.59	62.97	88.3%

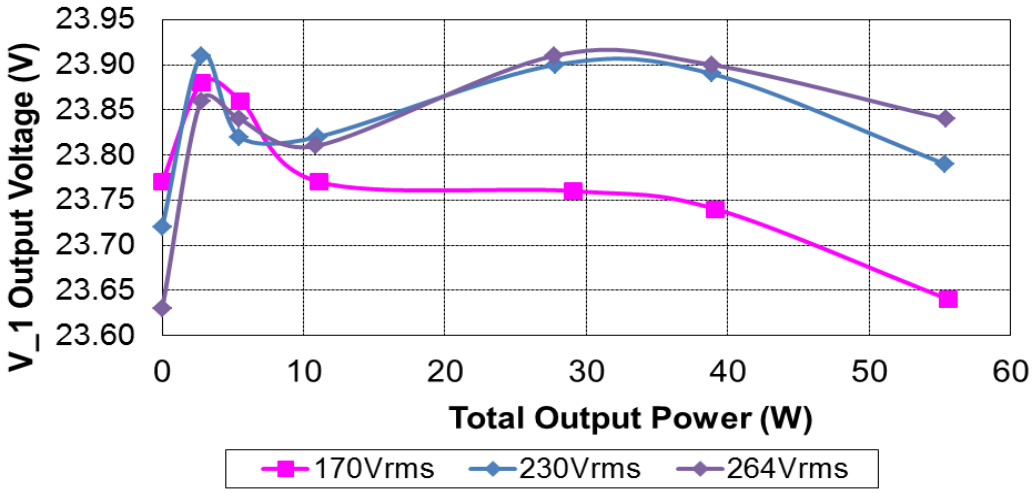
Vin (Vrms)	V_2 (V)	I_2 (mA)	V_1 (V)	I_1 (mA)	Pout (W)	Pin (W)	Eff. (%)
230	24.96	0.0	23.72	0.0	0.00	0.065	0.0%
230	24.50	97.1	23.91	16.0	2.76	3.421	80.7%
230	24.39	193.0	23.82	32.0	5.47	6.470	84.5%
230	24.34	391.6	23.82	61.5	11.00	12.660	86.9%
230	24.36	996	23.90	149.7	27.84	31.67	87.9%
230	24.34	1389	23.89	211.3	38.86	43.76	88.8%
230	24.20	1990	23.79	302.0	55.34	63.15	87.6%

Vin (Vrms)	V_2 (V)	I_2 (mA)	V_1 (V)	I_1 (mA)	Pout (W)	Pin (W)	Eff. (%)
264	24.92	0.0	23.63	0.0	0.00	0.08	0.0%
264	24.47	96.5	23.86	16.0	2.74	3.430	80.0%
264	24.43	191.1	23.84	32.0	5.43	6.520	83.3%
264	24.34	387.3	23.81	61.5	10.89	12.685	85.9%
264	24.38	991	23.91	149.6	27.74	31.56	87.9%
264	24.35	1388	23.90	211.3	38.85	43.70	88.9%
264	24.27	1986	23.84	302.0	55.40	62.95	88.0%

4 Output Voltage Regulation versus Output Power

The output voltage variation of both outputs versus total load, for the three input voltages, is plotted below.





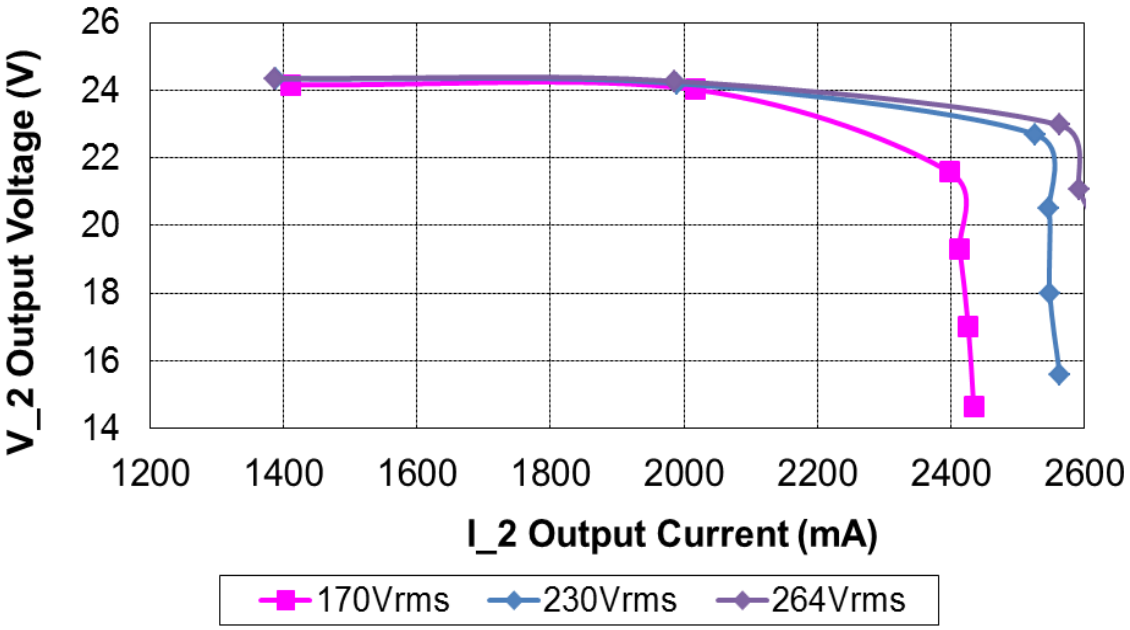
5 Cross Regulation

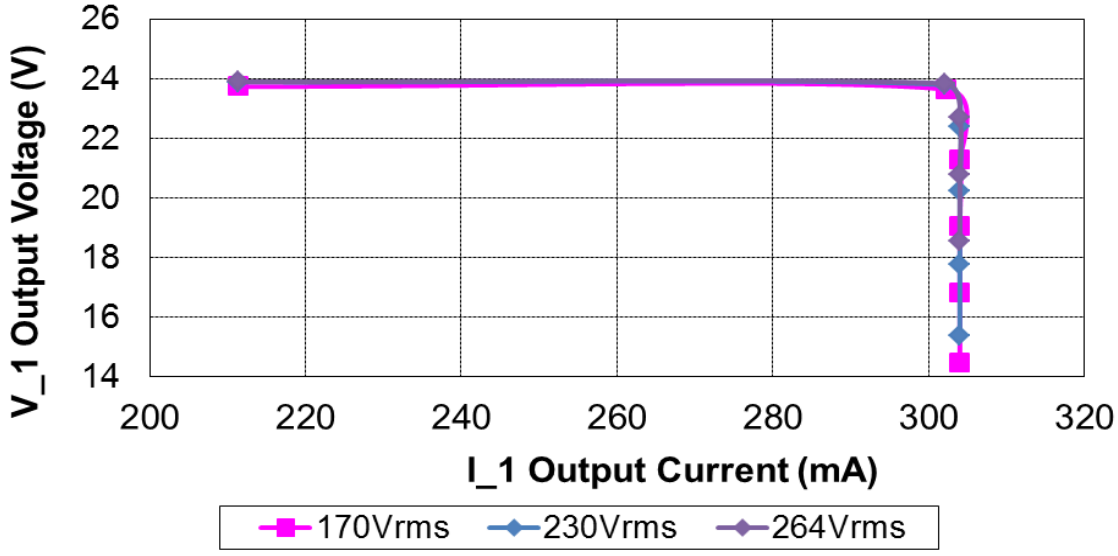
The output voltage variation, by unbalancing the outputs, has been measured with the converter supplied at 230Vrms. The results are shown in the table below:

Iout_1 Current	Iout_2 Current	Vout_1 Voltage	Vout_2 Voltage
0	2A	26.46V	24.06V
302mA	0	22.39V	26.95V

6 Current Limit

The current limit behavior is shown in the graphs below.





7 Parallel of two units (on Vout_2 output only)

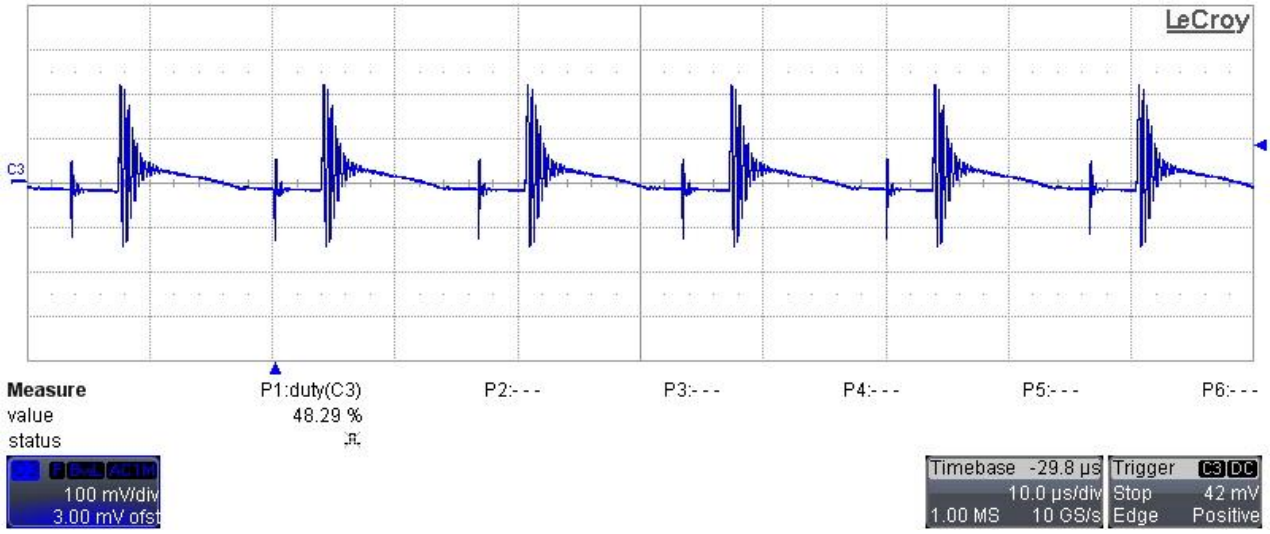
The table below shows how two converters behave when connected with the outputs “Vout_2” in parallel. The input voltage has been set to 230Vrms and each output current has been measured. The “Delta” variation is referred in % to the average output current. The output Vout_1 on each converter has been loaded proportionally to Vout_2 and separately.

Vin (Vrms)	V_2 (V)	I_2_1 (mA)	I_2_2 (mA)	Itot (mA)	Delta (%)	V_1 (V)	I_1 (mA)
230	24.72	0	0	0	0	23.1	0.0
230	25.01	102.7	77.3	180	14	23.0	16.0
230	24.67	279.2	199.0	478	17	23.0	32.0
230	24.44	590.0	402.6	993	19	23.3	61.5
230	24.20	973	1025	1998	-3	23.7	149.6
230	23.98	1370	1637	3007	-9	23.8	211.3
230	23.72	1721	2311	4032	-15	23.8	302.0
230	23.55	2168	2461	4629	-6	23.6	211.3
230	22.22	2537	2482	5019	1	22.3	302.0

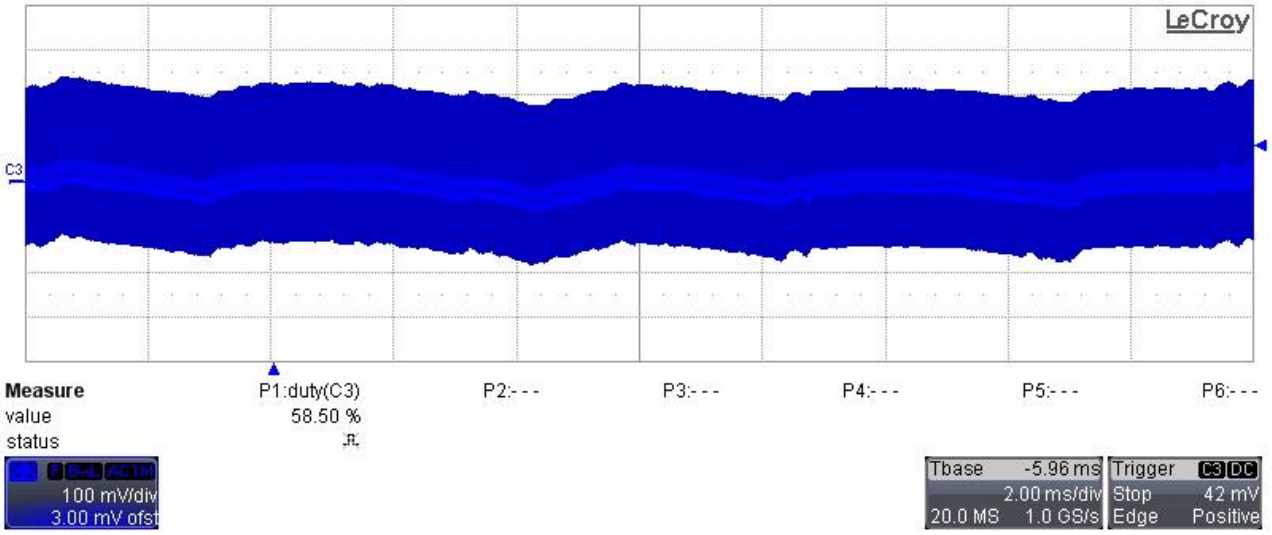
8 Output Ripple Voltage

The output ripple voltage on both outputs have been measured by supplying the converter @ 230Vrms, 50Hz with both outputs fully loaded (20MHz BWL for all waveforms).

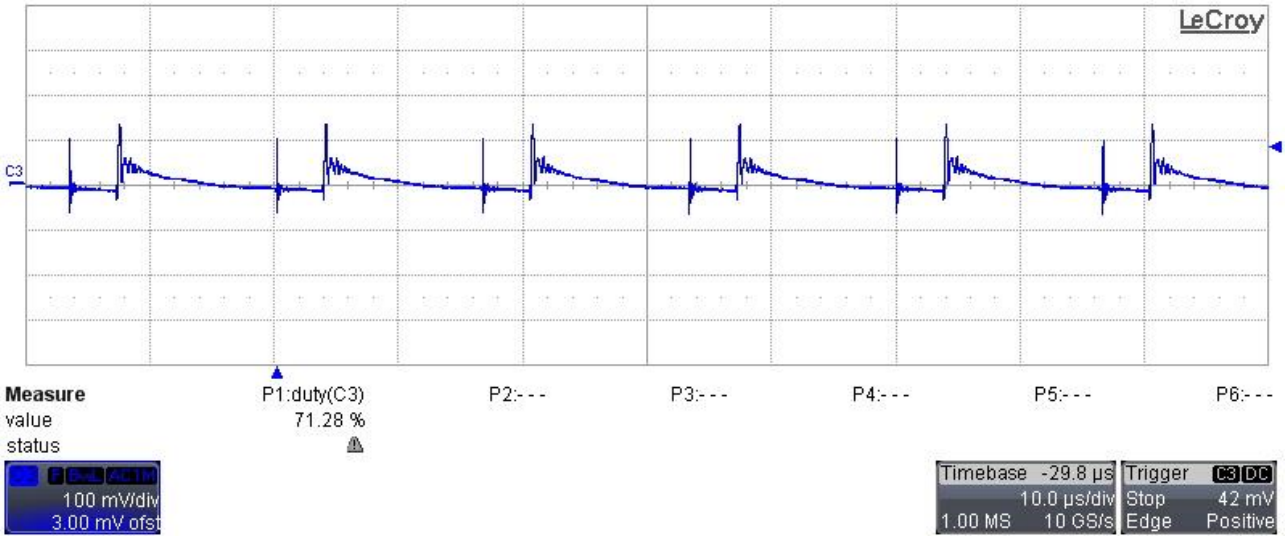
Ch.3: Vout_2 (100mV/div, 10us/div, AC coupling)



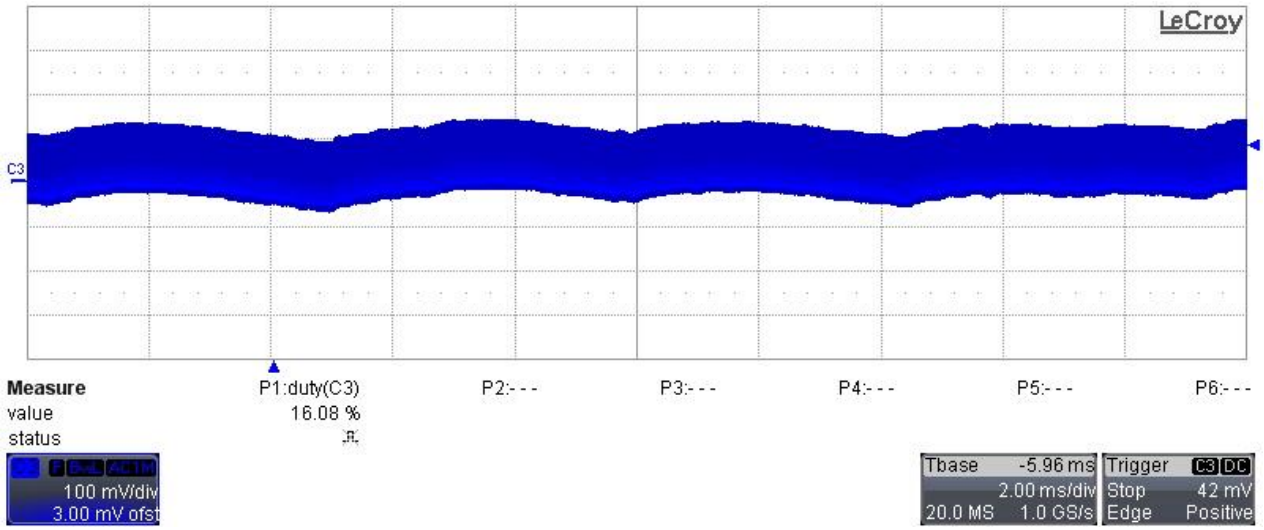
Ch.3: Vout_2 (100mV/div, 2ms/div, AC coupling)



Ch.3: Vout_1 (100mV/div, 10us/div, AC coupling)



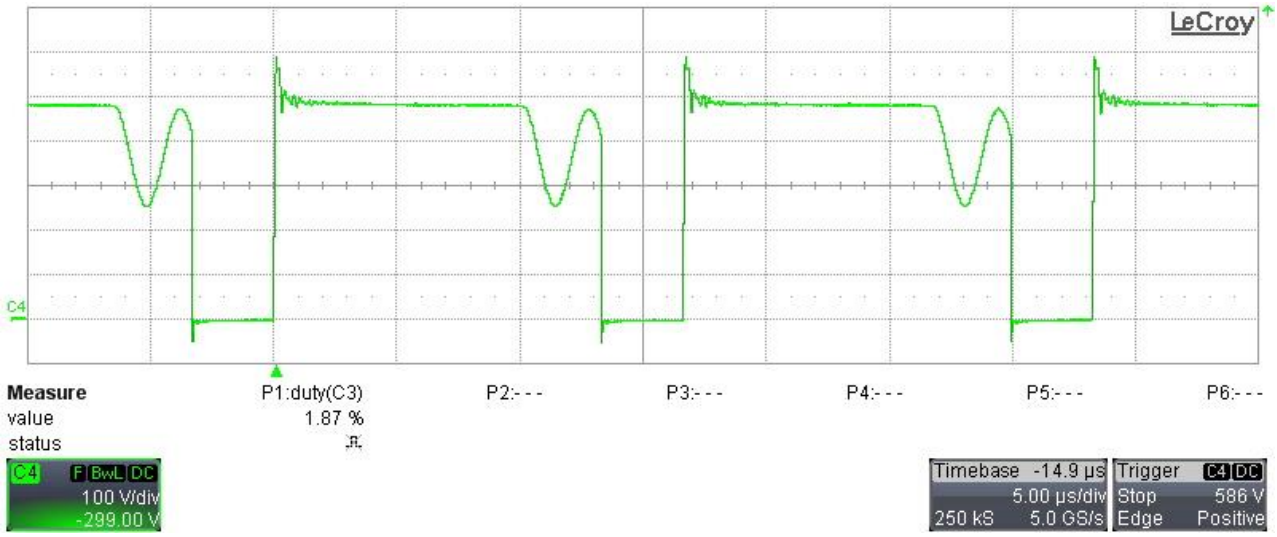
Ch.3: Vout_1 (100mV/div, 2ms/div, AC coupling)



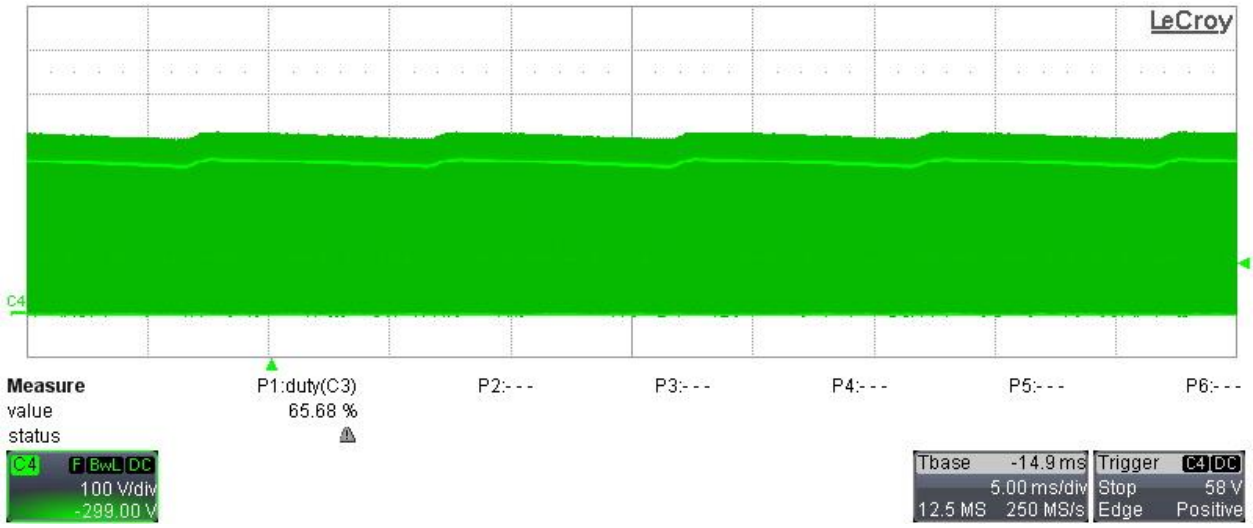
9 Switch-node

The image below shows the drain voltage of Q1, taken at 264Vrms input voltage and full load on both outputs.

Ch.4: Q1 Drain voltage (100V/div, 5us/div, DC coupling, 200MHz BWL)



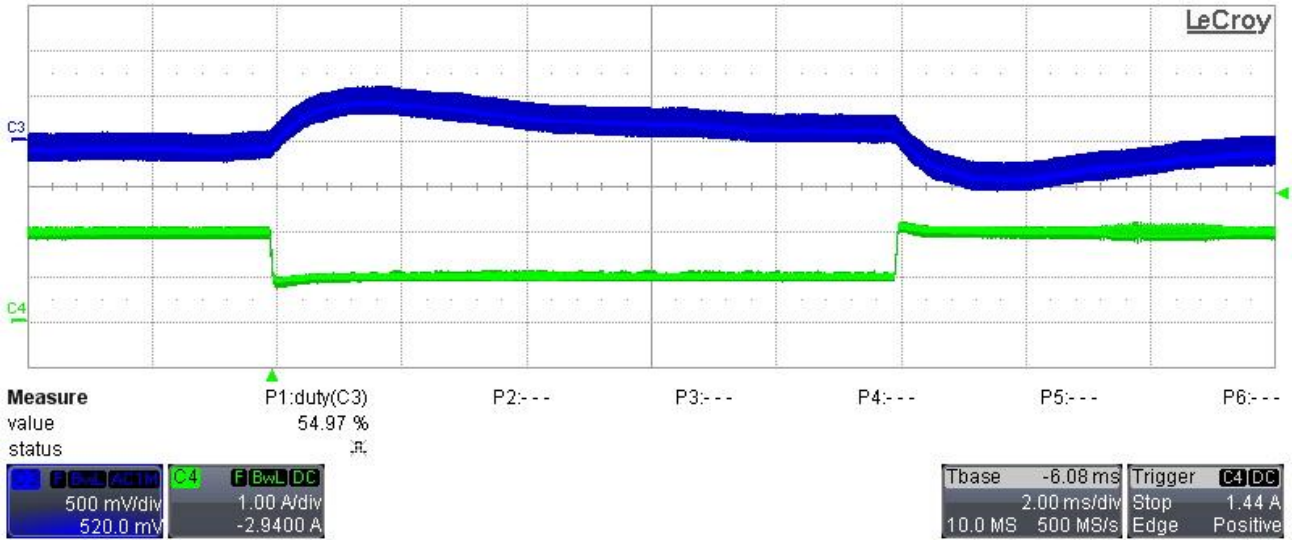
Ch.4: Q1 Drain voltage (100V/div, 5ms/div, DC coupling, 200MHz BWL)
Note the white envelop due to 100 Hz ripple.



10 Transient Response

The image below shows the transient response of the main output Vout_2 when its load was switched between 1A and 2A, while the load on Vout_1 was constantly set to 300mA, and Vin set to 230Vrms.

Ch.3: Vout_2 (500mV/div, 2ms/div, AC coupling, 20MHz BWL)
Ch.4: Iout_2 (1A/div, DC coupling, 20MHz BWL)



11 Thermal Analysis

During the thermal analysis, the converter has been placed horizontally on the bench in still air conditions, while fully loaded and supplied @ 230Vrms.

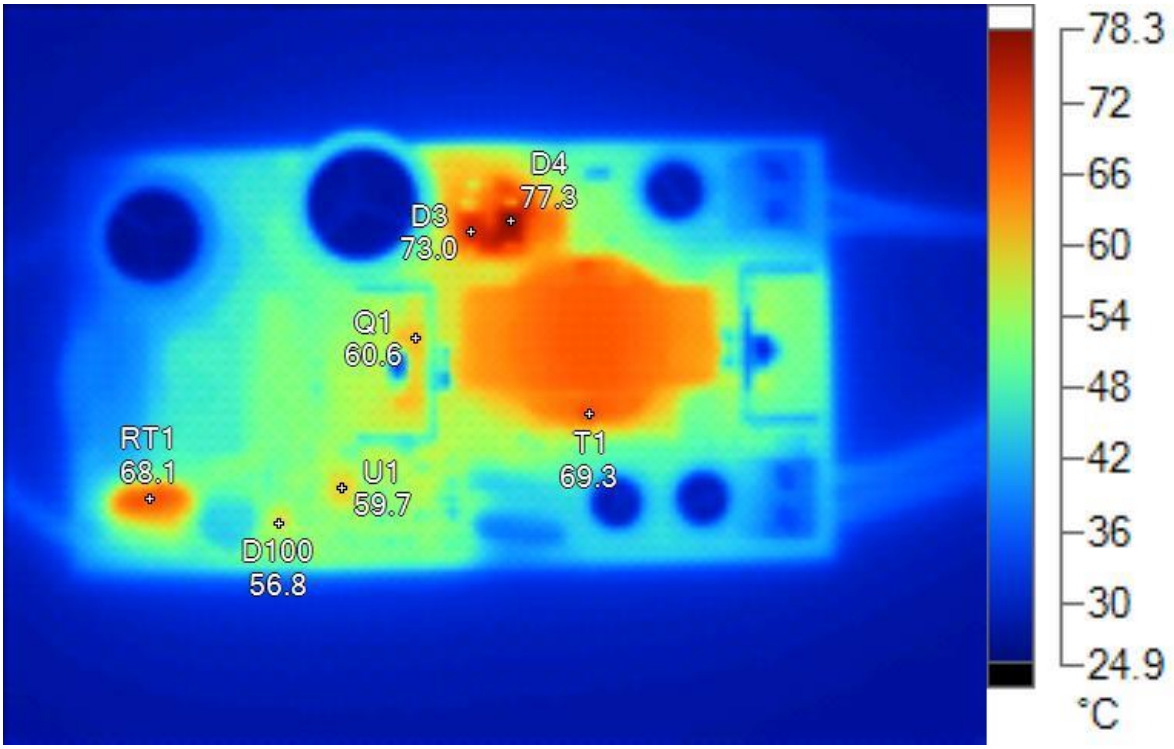


Image Info

Background temperature	24.0°C
Average Temperature	37.7°C
Image Range	25.9°C to 77.3°C
Camera Model	Ti40FT
Camera Manufacturer	Fluke
Image Time	12/18/2015 7:19:41 PM

Main Image Markers

Name	Temperature
T1	69.3°C
Q1	60.6°C
D4	77.3°C
P3	68.1°C
U1	59.7°C
D100	56.8°C
D3	73.0°C

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