TI Designs

5-V, 1-A, Low EMI, 94% Efficiency DC/DC Module in Single Layer TO-247 Form Factor Reference Design

Description

The TI Design TIDA-00948 demonstrates a small, high efficiency, low EMI DC/DC module to replace LDOs in major home appliance applications. This drastically improves efficiency, saving in both size and cost, as heat sinks are no longer required. The TPS54202, as a power converter, enables supplying with the same input current, a higher output current, and having lower power consumption at full load, low load, and standby operation.

This module is the same size with a TO-247 package and is pin compatible with the TO-220 LDO, enabling a quick evaluation and time to market.

Resources

TIDA-00948	Design Folder
TPS54202	Product Folder

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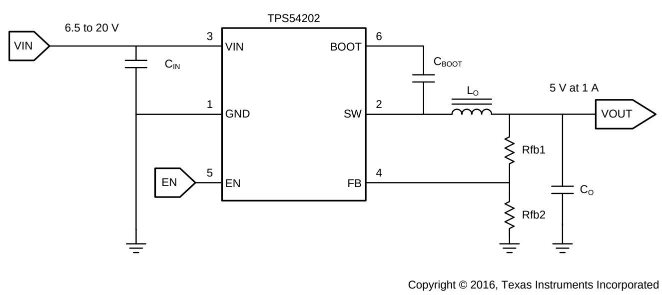
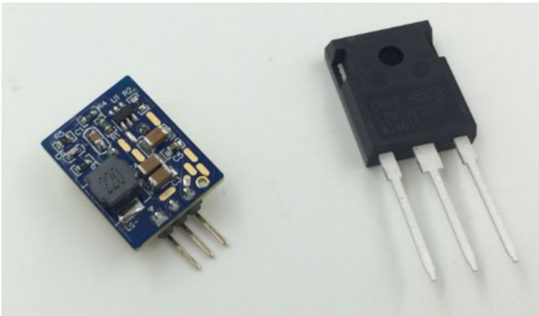
Features

- 5 V Regulated, up to 1-A Output Load
- 94% Efficiency
- 2.5-µA Standby Current and 89-µA No Load Current
- Small Form Factor: Pin-Compatible With TO-220 and Size-Compatible With TO-247 (15 mm × 20 mm)
- Less Than 30ºC Increase at Full Load, Which Eliminates the Need of Heat Sink
- Reduces Onboard DC/DC Design Complexity, Saves R&D Time and Efforts for Switching Power Supply EMC Design (Quicker to Market)

Applications

- Washing Machine and Dryer
- Refrigerator and Freezer
- Dishwasher
- Air Conditioner Indoor Units





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1 System Overview

1.1 System Description

Traditionally, low dropout regulators (LDO) are used in home appliances to generate 5 V or 3.3 V from the 12-V rail. These LDOs are chosen mainly for their cost and size.

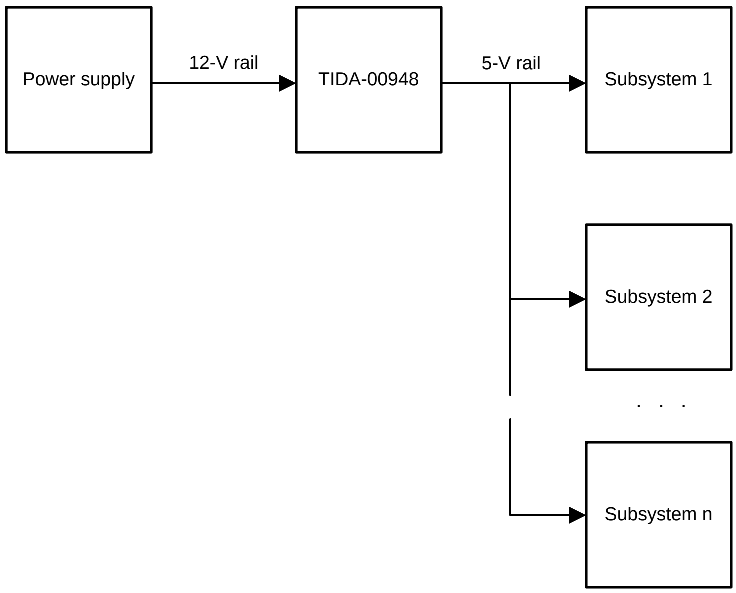

Figure 1. System Diagram

With the tightening requirements on active and standby power consumption and the increasing current needs due to the addition of new features (for example, the Wi-Fi module), the LDOs become an obstacle to achieving stringent energy ratings.

The TIDA-00948 was developed to answer this need of higher efficiency and current capability with the additional benefit of saving space by eliminating the heat sink, which is normally used in order to allow the LDOs to dissipate the losses.

1.2 Key System Specifications

The specifications of the TIDA-00948 are listed in Table 1:

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	6.5 to 20 V	—
Output voltage and max current	5 V at 1 A	—
Efficiency (full load, rated load, and light load)	93%: 12 V → 5 V at 1 A; 94.5%: 12 V → 5 V at 500 mA; 82%: 12 V → 5 V at 10 mA	Section 4.2.1
EMI performance	EN55022 class B, >6-dB margin	Section 4.2.10
Regulation (line and load)	±1% across the input range and load current range	Section 4.2.3
Transient response	±5% from 0.1 to 1.0 A	Section 4.2.5
Protections	Short-circuit, hiccup mode OCP for both FETs, OTP, OVP	Section 4.2.7
Operating ambient temperature	–30°C to 65°C	Section 4.2.2

1.3 Block Diagram

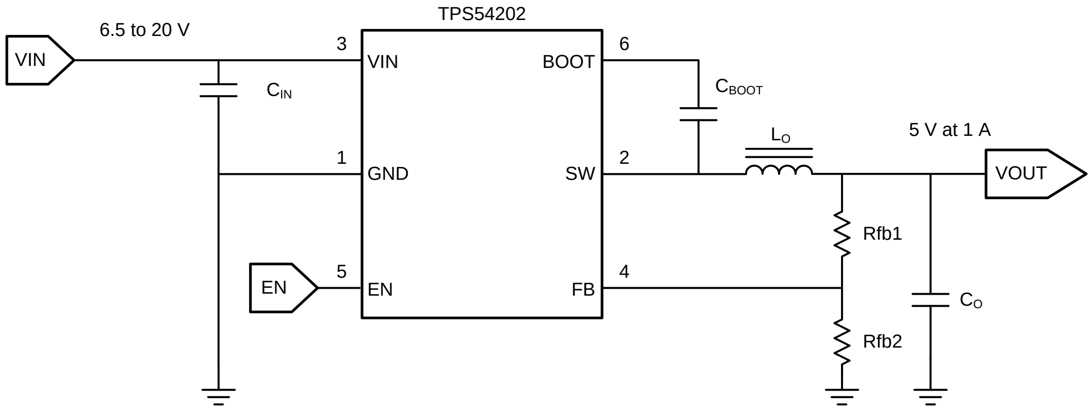

Figure 2. Block Diagram

1.4 Highlighted Products

1.4.1 TPS54202

The TPS54202 is a 4.5- to 28-V input voltage range, 2-A synchronous buck converter. The device includes two integrated switching FETs, internal loop compensation, and a 5-ms internal soft start to reduce component count.

By integrating the MOSFETs and employing the SOT-23 package, the TPS54202 achieves high power density and offers a small footprint on the PCB.

Advanced Eco-mode™ implementation maximizes light-load efficiency and reduces power loss.

In the TPS54202, the frequency spread spectrum operation is introduced for EMI reduction.

Cycle-by-cycle current limit in both high-side MOSFETs protect the converter in an overload condition and is enhanced by a low-side MOSFET freewheeling current limit, which prevents current runaway. Hiccup mode protection is triggered if the overcurrent condition has persisted for longer than the present time.

Features:

- 4.5- to 28-V wide input voltage range
- Integrated 148-mΩ and 78-mΩ MOSFETs for 2-A, continuous output current
- Low 2-µA shutdown, 45-µA quiescent current
- Internal 5-ms soft start
- Fixed 500-kHz switching frequency
- Frequency spread spectrum to reduce EMI
- Advanced Eco-mode pulse skip
- Peak current mode control
- Internal loop compensation
- Overcurrent protection for both MOSFETs with hiccup mode protection
- Overvoltage protection
- Thermal shutdown
- SOT-23 (6) package

1.5 System Design Theory

LDOs are devices that regulate the output voltage, while the output current is the same as the input current. This implies losses are proportional to the dropout between input and output voltage and the output current, as shown in Equation 1. These losses are the root cause of poor efficiency in LDOs. This translates to a limitation of the ratio between input and output voltage and maximum output current as well as the need of a heat sink. That heat sink will add cost and size to the overall solution.

A DC/DC switch mode power supply, including a Buck topology as in this project, present the advantage of having a higher efficiency, allowing them to be used in a wider variety of applications as well as being competitive with an LDO-based design with respect to cost and size (including all components and heat sink). More details on how a Buck topology works can be found in the application report *Understanding Buck Power Stages In Switchmode Power Supplies* (SLVA057).

Compare the efficiency of the TIDA-00948 and an LDO based design. The efficiency data for the TIDA-00948 can be found in Section 4.2.1. In an LDO, the power to be dissipated can be estimated by Equation 1.

$$P_{DISSIPATED} = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \tag{1}$$

Now calculate the power dissipated by a 12-V input, 5-V output design at 1 A, 500 mA, and 100 mA to see what the performances are for the TIDA-00948 and for the LDO-based design.

For 1 A, the efficiency of the TIDA-00948 is 93% (10% loss). With 5 W at the output, 0.35 W are dissipated. For the LDO-based design, Equation 1 gives 7 W to be dissipated by the LDO.

For 500 mA, the efficiency of the TIDA-00948 is 94.5% (5.5% loss). With 2.5 W at the output, 0.1375 W are dissipated. This is to be compared with 3.5 W for the LDO.

Finally for 100 mA, 0.055 W needs to be dissipated for the TIDA-00948 (89% efficiency) versus 0.7 W for the LDO-based design.

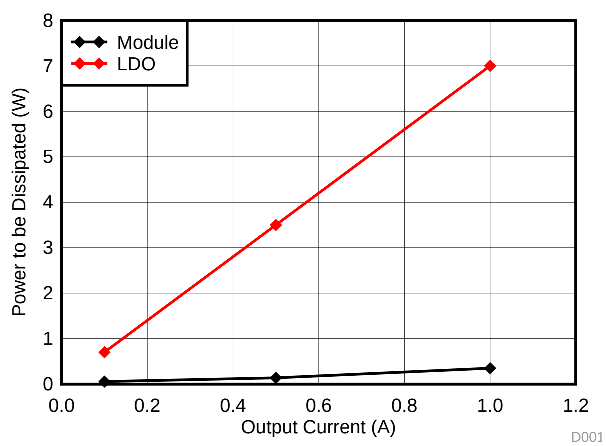

Figure 3. Comparison of Power Dissipated

As shown in Figure 3, the LDO-based design needs to dissipate much more power than the TIDA-00948 design, which impacts both power consumption and cost and size due to the necessity of a heat sink.

2 Circuit Design and Component Selection

2.1 Part and Topology Selection

The first step of the design is to select the circuit topology. As cost and space are key in home appliance design and no isolation is needed for the 12-V to 5-V conversion, a Buck topology is chosen. Still, with the aim to reduce bill of material cost and size, a synchronous converter with integrated FET is preferred.

With this in mind, as well as the specification in Section 1.2, the TPS54202 was chosen. The converter includes two integrated switching FETs, internal loop compensation, and a 5-ms internal soft start to reduce component count. It integrates a 148-mΩ and a 78-mΩ MOSFET for up to 2-A continuous output current operation with 2-µA shutdown and 45-µA quiescent current.

2.2 Design Steps and Passive Components Selection

The first step is to set the output voltage, which is adjusted by the resistor divider (R3 and R5). First set the range of the resistors; higher values will decrease the losses in the resistor divider but make the feedback signal more sensitive to noise, while lower values will make the feedback signal more robust against noise but increase losses. On this project, a good trade-off is setting R3 at 100 kΩ and use Equation 2 to calculate R5.

$$R5 = \frac{R3 \times V_{REF}}{V_{OUT} - V_{REF}} \tag{2}$$

where

- R3 = 100 kΩ
- V_{OUT} = 5 V
- V_{REF} = 0.596 V

Equation 2 gives R5 = 13.53 kΩ. A resistor value of 13.3 kΩ is then used for R5. By reversing Equation 2, an effective output voltage of V_{OUT} = 5.077 V is given.

Then comes the choice of the inductor (L1). For this the inductance value, the RMS and peak current are considered.

The minimum inductor value of the inductor is calculated in Equation 3. To calculate the minimum inductor value, use the maximum input voltage (20 V), the maximum output voltage (5 V), the maximum output current (1 A), the switching frequency (500 kHz), and the coefficient that represents the amount of inductor ripple relative to the maximum output current (K_{IND}). For low ESR output capacitors, K_{IND} must be 0.3 (0.2 for higher ESR output capacitors). Equation 3 indicates that L1 must ideally be higher than 25 µH. 22 µH is used as value for L1 in this design.

$$L_{MIN} = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times K_{IND} \times I_{OUT} \times F_{SW}} \tag{3}$$

With the output inductor value, the RMS and peak current can be calculated with Equation 4 and Equation 5, which respectively gives 1.008 A and 1.213 A. With these parameters in mind, the inductor can be selected. After reviewing the cost and performance of several inductor from various manufacturers, the THPC6045MF-220M from Taitech was selected.

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times F_{SW}}\right)^2} \tag{4}$$

$$I_{L\_PEAK} = I_{OUT} \times \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{1.6 \times V_{IN\_MAX} \times L \times F_{SW}} \tag{5}$$

The maximum allowable output voltage ripple and the transient response to load changes determine the value of the output capacitors. C_{OUT} is selected based on the most stringent of the following equations.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{F_{SW} \times \Delta V_{OUT}} \tag{6}$$

where

- ΔI_{OUT} is the load step of the output current from the output current under light load (0.1 A) and full load (1 A)
- ΔV_{OUT} is the allowable change of output voltage during the load step

$$C_{OUT} > \frac{1}{8 \times F_{SW}} \times \frac{1}{\frac{V_{OUT\_RIPPLE}}{K_{IND} \times I_{OUT}}} \tag{7}$$

where

- V_{OUT_RIPPLE} is the maximum output ripple required

The output capacitors also influence the crossover frequency. In the case of the TPS54202, the crossover frequency must be lower than 40 kHz without considering the feed forward capacitor.

$$C_{OUT} > \frac{3.95}{V_{OUT} \times F_{CO}} \tag{8}$$

C_{OUT} must be selected based on the most stringent of the previous equations. Equation 6, Equation 7, and Equation 8 indicate that C_{OUT} must be higher than 19 μF. Including some margin for aging, temperature and DC bias, two 22 μF in parallel where chosen to fit the C_{OUT} requirements.

Equation 9 calculates the maximum ESR of the output capacitor needed to meet the maximum output ripple required. The equivalent ESR of the output capacitors C3 and C4 must be lower than 0.5 Ω.

$$R_{ESR} < \frac{V_{OUT\_RIPPLE}}{I_{L\_RIPPLE}} \tag{9}$$

A feed forward capacitor (C6) is used in parallel with R3 to improve the phase boost at the crossover frequency. Equation 10 shows the feed forward capacitor must be higher than 90 pF, so 100 pF was used.

$$C6 > \frac{V_{OUT} \times C_{OUT}}{2 \times \pi \times 3.95} \times \frac{1}{R3} \tag{10}$$

The last step is to set the enable threshold. If an external signal is used, then no additional components are required. But if no external enable signal is used, then the resistor divider, composed of R2 and R4, is used. Equation 11 and Equation 12 are used to select R2 and R4 values.

$$R2 = \frac{V_{START} \times \dfrac{V_{EN\_FALLING}}{V_{EN\_RISING}} - V_{STOP}}{I_P \times \left(1 - \dfrac{V_{EN\_FALLING}}{V_{EN\_RISING}}\right) + I_H} \tag{11}$$

$$R4 = \frac{R2 \times V_{EN\_FALLING}}{V_{STOP} - V_{EN\_FALLING} + R2 \times (I_P + I_H)} \tag{12}$$

where

- V_{START} is the voltage at which the converter begin operation (6.2 V here)
- $V_{STOP}$is the voltage below which the converter should be turned off (5.3 V here)
- $V_{EN\_FALLING}$ and V_{EN_RISING} are the falling and rising values of the internal UVLO (1.19 V and 1.21 V, respectively)
- I_P is the enable input current (0.7 μA)
- I_H is the hysteresis current (1.55 μA)

Equation 11 gives 510.7 kΩ for R2, so 510 kΩ was used. This makes Equation 12 result in 115.4 kΩ for R4, so 118 kΩ was used.

As required, a bootstrap capacitor (C1) of 0.1 μF (X7R or X5R) has to be added between the BOOT pin and the SW pin.

Finally a 0-Ω resistor (R1) was added next to the bootstrap for test purposes (EMC tests). Results of the tests show that this resistor is not needed.

3 Getting Started Hardware

3.1 PCB Overview

A picture of the PCB with the functional blocks is shown in Figure 4.

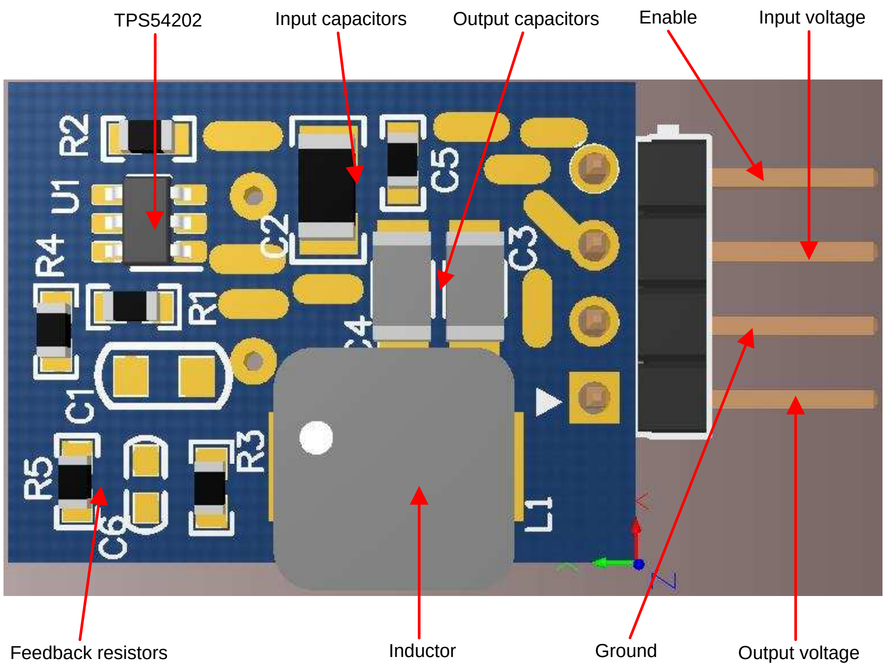

Figure 4. TIDA-00948 PCB With Functional Blocks

3.2 Connectors Settings

Table 2. Connector Settings

CONNECTOR	FUNCTION
J1-1	EN
J1-2	V_{IN}
J1-3	GND
J1-4	V_{OUT}

4 Testing and Results

4.1 Setup

Figure 5 shows the setup and the test equipment used.

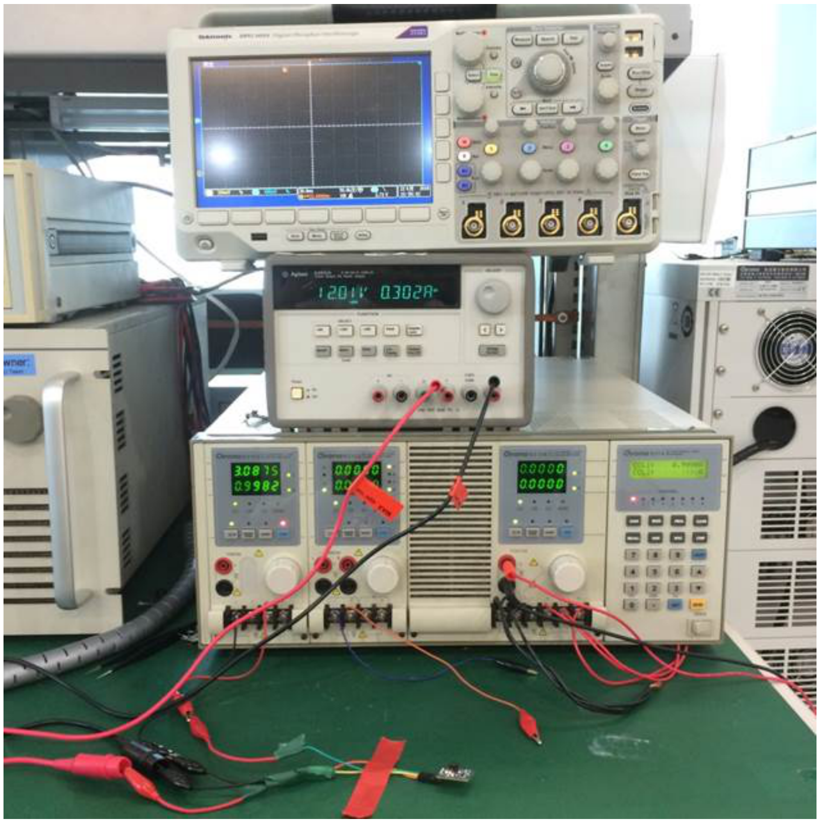

Figure 5. Picture of Test Setup for TIDA-00948

Table 3 lists the test equipment used to test the TIDA-00948.

Table 3. Test Equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Tektronix DPO 3054
Voltage probe	Tektronix P6139A
Current probe	Tektronix TCP202
Multimeter	Fluke 287C
Power supply	Agilent E3631A
Electronic load	Chroma 63103 and 63102
Thermal camera	Fluke TI110

4.2 Test Results

4.2.1 Efficiency

To test the efficiency, four multimeters are used; two are set up as voltmeters to measure the input and output voltages, and two are set up as ampmeters to measure the input and output currents.

The measurements are done at a room temperature of 22.5ºC.

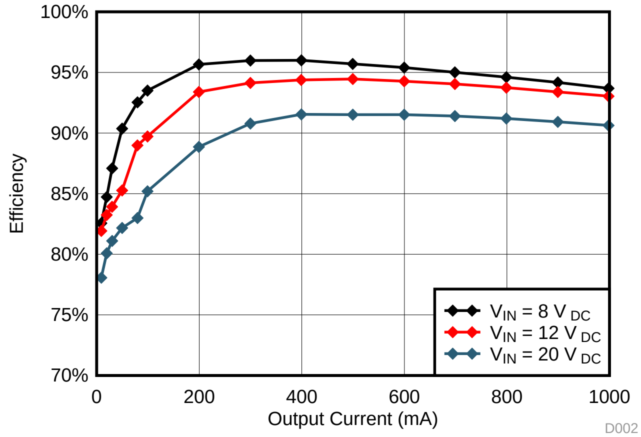

Figure 6. TIDA-00948 Efficiency

Table 4, Table 5, and Table 6 list the details of the efficiency curves shown in Figure 6.

Table 4. Efficiency With 8-V Input

V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (mA)	η
8.062	6.850	5.076	8.982	82.563
8.017	14.557	5.076	19.481	84.727
7.975	21.890	5.075	29.962	87.094
7.898	35.138	5.073	49.434	90.370
7.778	55.967	5.072	79.420	92.537
7.698	69.700	5.072	98.920	93.507
7.999	132.060	5.071	199.270	95.663
7.945	199.260	5.071	299.670	95.980
7.892	267.000	5.070	399.000	95.999
7.836	337.440	5.069	499.200	95.704
7.778	409.600	5.069	599.600	95.402
7.718	482.740	5.069	698.400	95.009
7.655	559.000	5.068	798.800	94.610
7.589	637.660	5.068	899.300	94.173
7.520	717.800	5.067	998.000	93.688

Table 5. Efficiency With 12-V Input

V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (mA)	η
12.077	4.590	5.080	8.94	81.927
12.047	9.840	5.076	19.44	83.247
12.018	15.060	5.076	29.92	83.917
11.963	24.575	5.075	49.40	85.270
11.887	38.074	5.073	79.38	88.983
11.835	47.240	5.073	98.88	89.721
11.570	93.500	5.071	199.23	93.392
12.015	134.300	5.070	299.63	94.137
11.987	178.570	5.068	398.60	94.382
11.960	224.000	5.067	499.40	94.460
11.930	270.100	5.066	599.60	94.273
11.898	316.200	5.065	698.50	94.045
11.868	363.660	5.064	798.90	93.743
11.836	411.880	5.063	899.20	93.393
11.803	460.130	5.062	998.10	93.037

Table 6. Efficiency With 20-V Input

V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (mA)	η
20.090	2.912	5.083	8.985	78.068
20.070	6.156	5.079	19.483	80.084
20.055	9.350	5.075	29.968	81.107
20.023	15.250	5.075	49.444	82.177
19.974	24.310	5.074	79.430	82.996
19.946	29.528	5.072	98.930	85.201
19.796	57.429	5.069	199.290	88.857
19.648	85.135	5.067	299.690	90.785
19.493	113.269	5.066	399.000	91.541
20.054	137.780	5.064	499.300	91.514
20.044	165.520	5.064	599.600	91.519
20.032	193.200	5.065	698.500	91.405
20.020	221.640	5.066	798.800	91.201
20.010	250.460	5.067	899.300	90.924
19.999	279.130	5.069	998.100	90.630

4.2.2 Thermal

The thermal pictures in Figure 7 and Figure 8 was taken at a room temperature of 26°C, with a 12-V input, 5 V at 1-A output without airflow.

The hottest point of the design is the TPS54202 at 56.2°C. This is an increase of 30°C. Because the acceptable ambient temperature range is –30°C to 65°C, no heat sink is required for the TIDA-00948 to function properly.

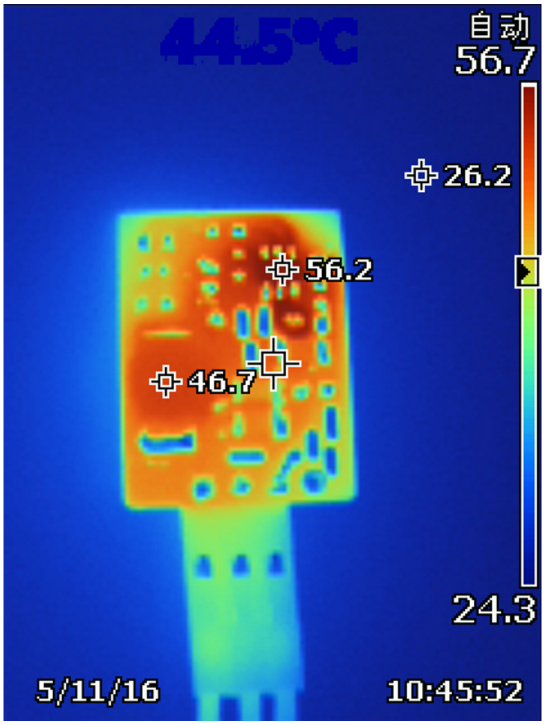

Figure 7. Top-Side Thermal Picture With 12-V_{IN}, 5 V at 1-A Output

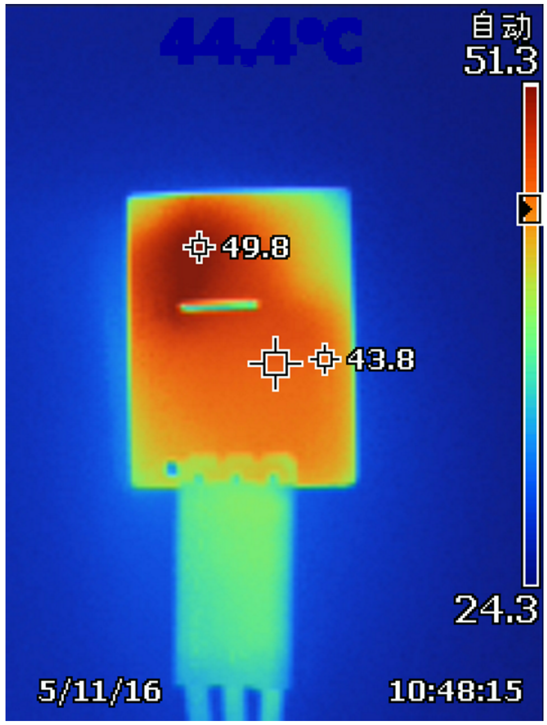

Figure 8. Bottom-Side Thermal Picture With 12-V_{IN}, 5 V at 1-A Output

4.2.3 Line and Load Regulation

Figure 9 and Figure 10 show the output voltage variation, depending load current and input voltage. Across all input voltages and output currents, the output voltage varies between 5.0614 and 5.074 V, well below the ±1% that was the initial target.

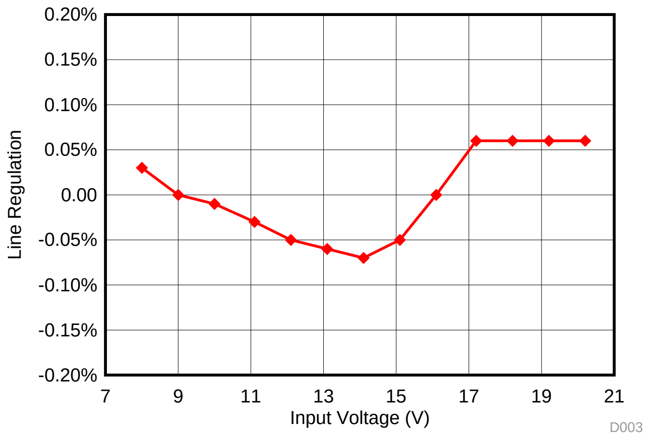

Figure 9. Line Regulation at 1-A Load

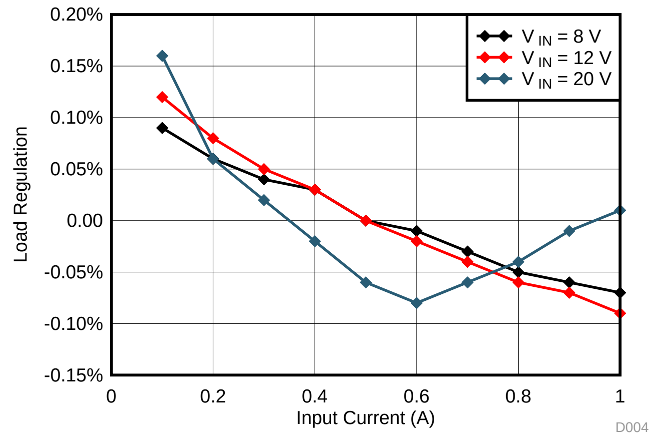

Figure 10. Load Regulation

Table 7, Table 8, Table 9, and Table 10 list the details of the regulation curves shown in Figure 9 and Figure 10.

Table 7. Line Regulation

V_{IN}	V_{OUT}	REGULATION (%)
8.0	5.0664	0.03
9.0	5.0652	0
10.0	5.0644	–0.01
11.1	5.0635	–0.03
12.1	5.0625	–0.05
13.1	5.0619	–0.06
14.1	5.0614	–0.07
15.1	5.0624	–0.05
16.1	5.0650	0
17.2	5.0679	0.06
18.2	5.0682	0.06
19.2	5.0678	0.06
20.2	5.0679	0.06

Table 8. Load Regulation at V_{IN} = 8 V

I_{OUT}	V_{OUT}	REGULATION (%)
0.1	5.0715	0.09
0.2	5.0704	0.06
0.3	5.0693	0.04
0.4	5.0685	0.03
0.5	5.0672	0
0.6	5.0665	–0.01
0.7	5.0657	–0.03
0.8	5.0648	–0.05
0.9	5.0641	–0.06
1.0	5.0634	–0.07

Table 9. Load Regulation at V_{IN} = 12 V

I_{OUT}	V_{OUT}	REGULATION (%)
0.1	5.0730	0.12
0.2	5.0711	0.08
0.3	5.0696	0.05
0.4	5.0684	0.03
0.5	5.0673	0
0.6	5.0663	–0.02
0.7	5.0653	–0.04
0.8	5.0643	–0.06
0.9	5.0633	–0.07
1.0	5.0624	–0.09

Table 10. Load Regulation at V_{IN} = 20 V

I_{OUT}	V_{OUT}	REGULATION (%)
0.1	5.0740	0.16
0.2	5.0690	0.06
0.3	5.0666	0.02
0.4	5.0648	–0.02
0.5	5.0628	–0.06
0.6	5.0619	–0.08
0.7	5.0625	–0.06
0.8	5.0639	–0.04
0.9	5.0653	–0.01
1.0	5.0663	0.01

4.2.4 Output Voltage Ripple

The output voltage ripple remains below 30 mVpp under full load (1 A), low load (10 mA), or no load. This is well below the initial requirements of ±1%.

Measurements were done at 22.5ºC room temperature with 12-V input voltage. The upper curve (1) is the output voltage with oscilloscope in AC-coupling mode with 20 mV/div. The lower curve (2) is the switch node (pin 2 of the TPS54202) with 5 V/div.

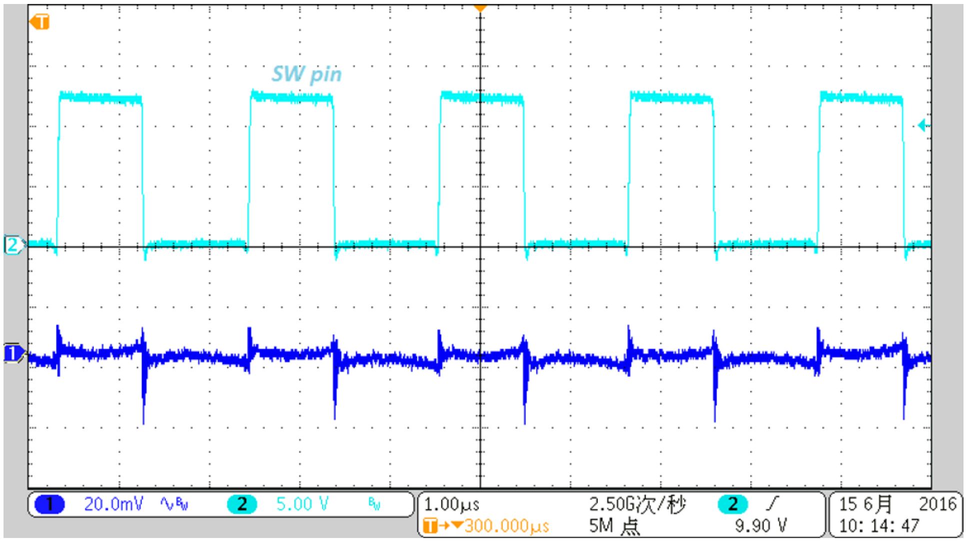

Figure 11. Output Voltage Ripple at 1-A Output Load

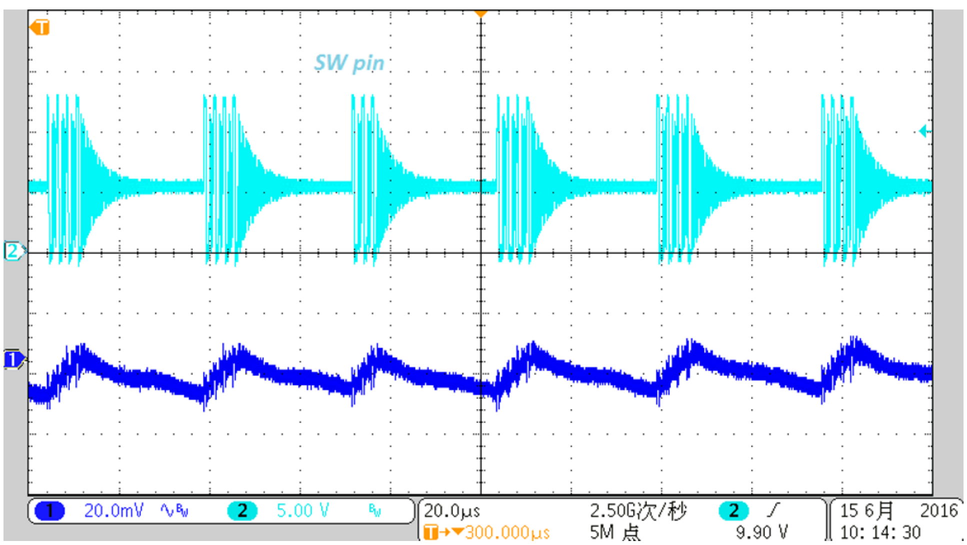

Figure 12. Output Voltage Ripple at 10-mA Output Load

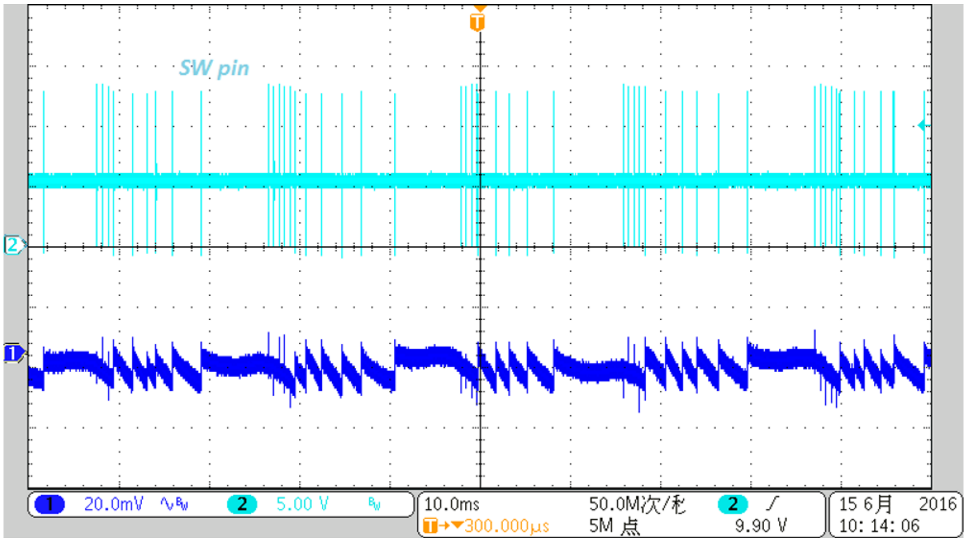

Figure 13. Output Voltage Ripple at No Load Output

4.2.5 Transient Response

The transient response is below ±200 mV for load steps between 10 mA and 1 A, which were the design requirements (±5%).

Measurements were done at 22.5°C room temperature with 12-V input voltage. The upper curve (1) is the output voltage with oscilloscope in AC-coupling mode with 100 mV/div. The lower curve (4) is the output current with 1 A/div. The load step is applied with a 1-A/ms slew rate.

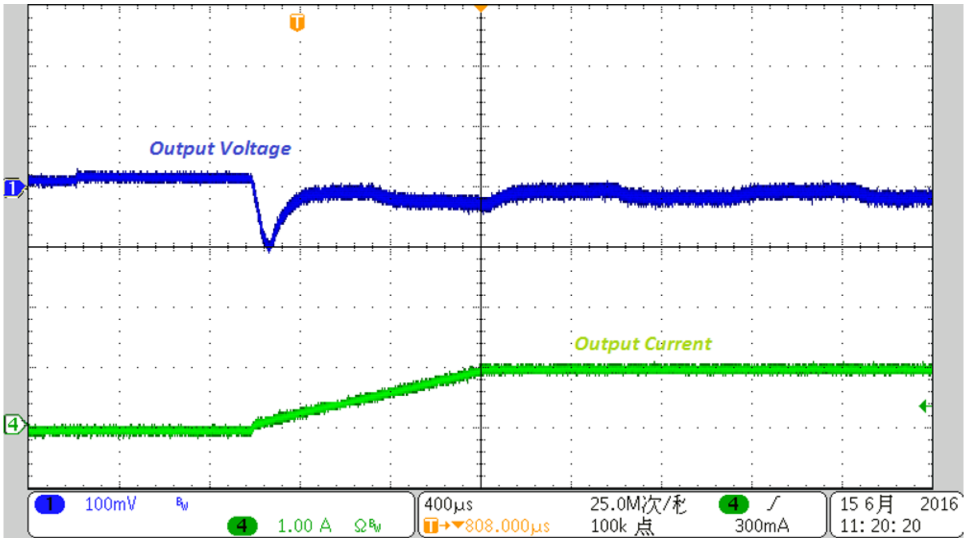

Figure 14. Transient Response From 10-mA to 1-A Output Load

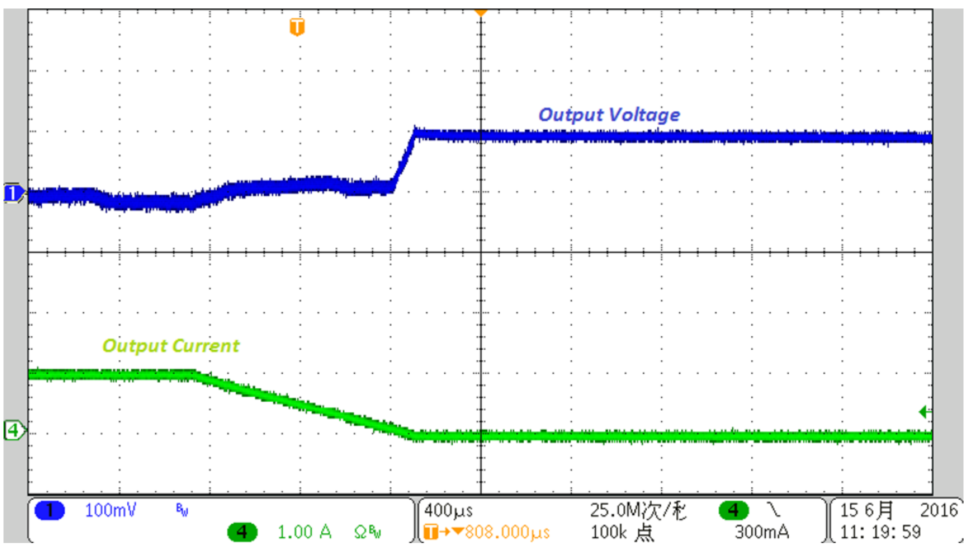

Figure 15. Transient Response From 1-A to 10-mA Output Load

4.2.6 Start-up and Shutdown

For the start-up and the shutdown behavior, 12 V is applied at the input with a 1-A load at the output.

Measurements were done at 22.5ºC room temperature. The upper curve (3) is the EN pin with oscilloscope in DC-coupling mode with 2 V/div. The lower curve (2) is the switch node pin signal with oscilloscope in DC-coupling mode with 10 V/div. The upper curve (1) is the output voltage with oscilloscope in DC-coupling mode with 5 V/div. The lower curve (4) is the output current with 1 A/div.

The TIDA-00948 takes 7 ms to provide 5 V. The output voltage is reached without overshoot.

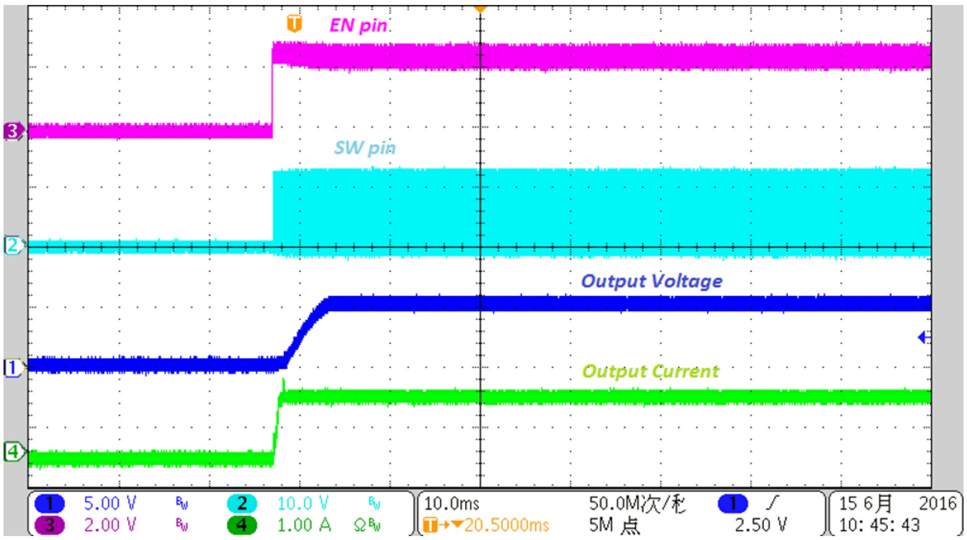

Figure 16. Start-up at 12-V Input and 1-A Output Load

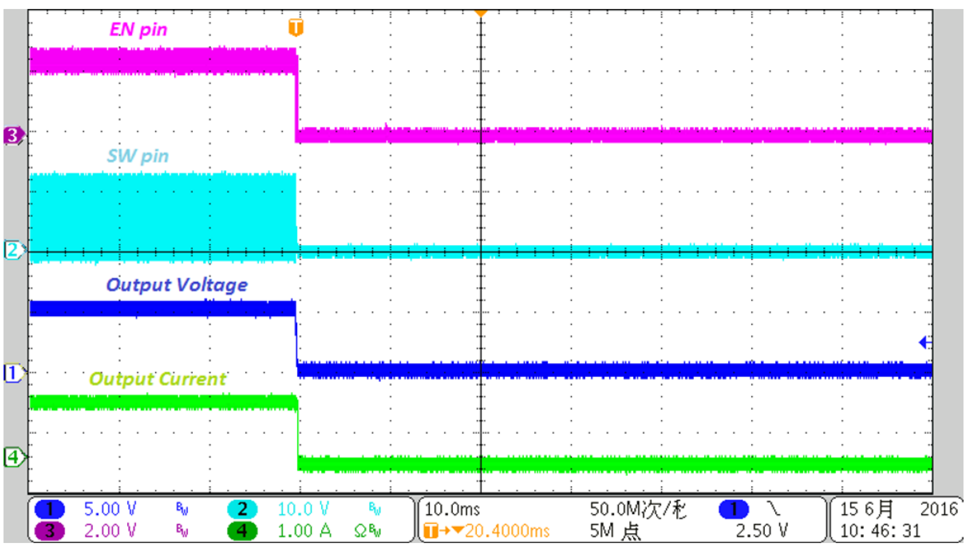

Figure 17. Shutdown at 12-V Input and 1-A Output Load

4.2.7 Overcurrent and Short-Circuit Test

The overcurrent protection was tested by having a transient load from 1- to 3-A output current while the board is supplied with 12 V. The short-circuit protection was tested by shorting the output pin to ground.

The upper curve (1) is the output voltage with oscilloscope in DC-coupling mode with 2 V/div (Figure 18) and 1 V/div (Figure 19). The lower curve (4) is the output current with 2 A/div.

As shown in Figure 18 and Figure 19, when the current is rising to the current limit level, the device enters overcurrent protection as described in the TPS54202 datasheet (SLVSD26). After waiting the pre-programmed time, the device tries to restart. Once the fault condition is removed, the device starts normally.

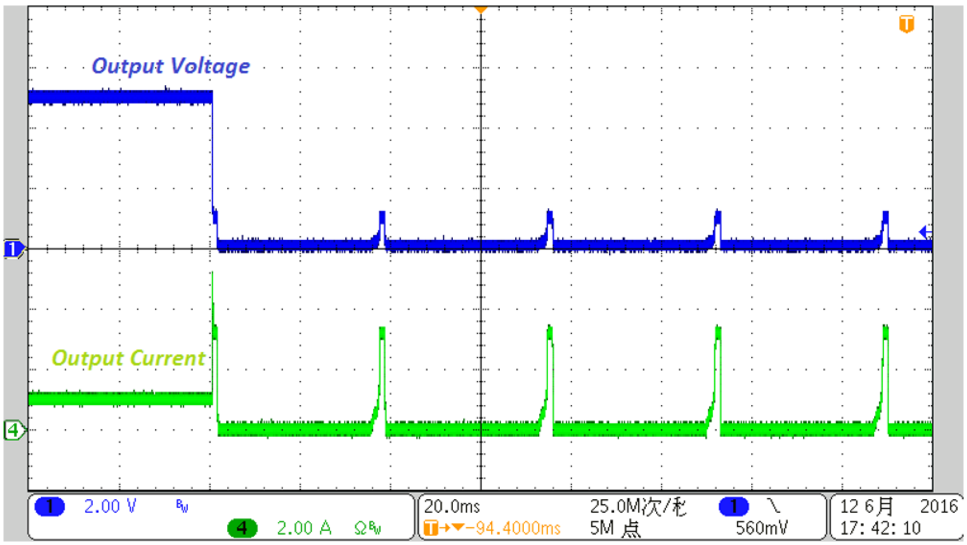

Figure 18. Overcurrent Protection

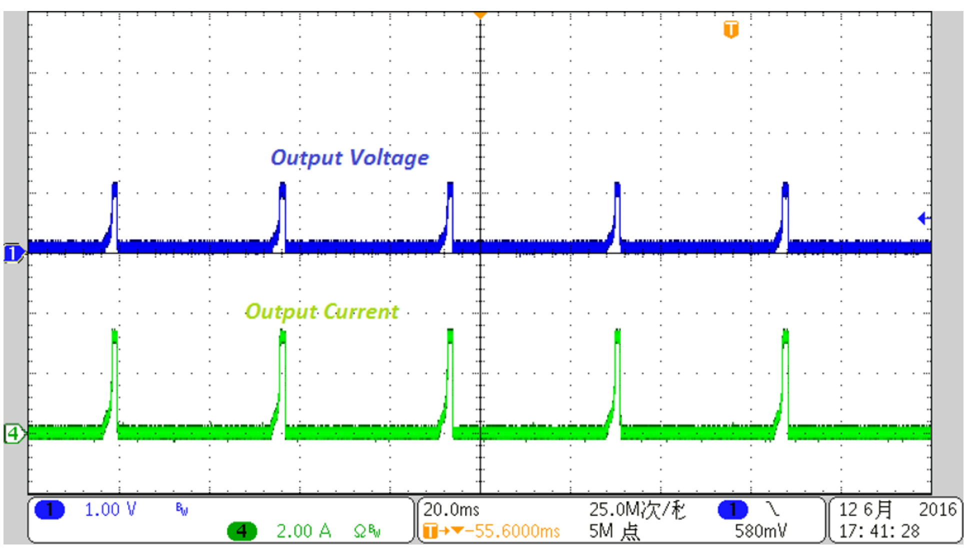

Figure 19. Short-Circuit Protection

4.2.8 Overvoltage Test

The overvoltage protection was tested by applying 6 V at the output of the TIDA-00948 board while the board is supplied with 12 V and with a 1-A output load.

The upper curve (1) is the output voltage with oscilloscope in DC-coupling mode with 2 V/div. The lower curve (2) is voltage at the switch node with 5 V/div.

As described in page 11 of the TPS54202 datasheet (SLVSD26), if the voltage on the FB pin is higher than 108% of the V_{REF}, the high-side MOSFET is turned off. Once the fault condition is removed, the device starts switching normally again.

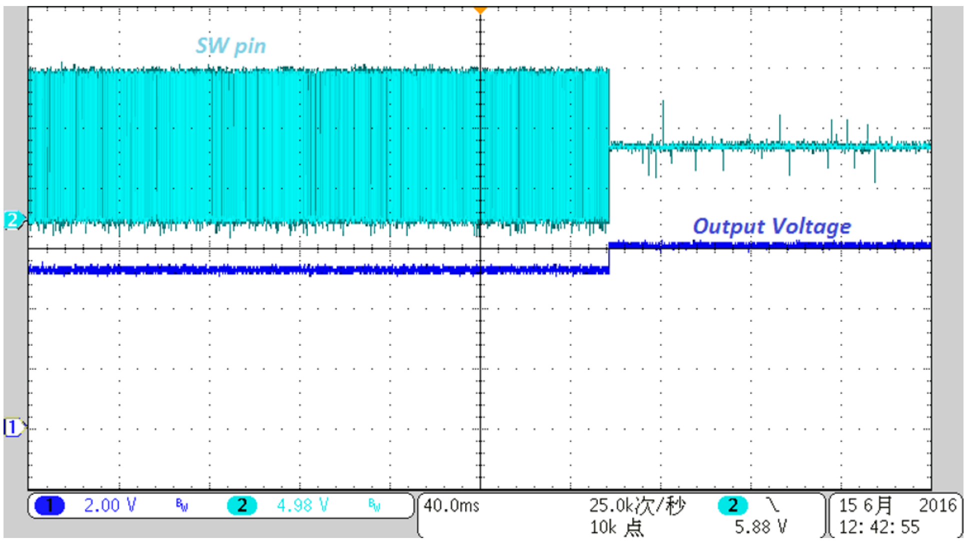

Figure 20. Overvoltage Protection From 5 to 6 V

4.2.9 Standby and No-Load Currents

The standby current was measured with an ampmeter at 22.5°C room temperature with a 12-V input voltage. The enable pin was set low through the connector, and the enable setting resistors (R2 and R4) not populated. The standby current was measured at 2.5 μA.

The no-load current was measured with an ampmeter at 22.5°C room temperature with a 12-V input voltage, with the enable setting resistors (R2 and R4) populated and no load attached at the output. The no-load current was measured at 89 μA.

4.2.10 EMC Tests

The TIDA-00948 TI Design has been tested for EMI according to EN55022 Class B conducted emissions. The EMC tests were performed by the Shanghai Institute of Measurement and Testing Technology Fundamental Performance Test Centre (China).

Figure 21. Conducted Emission Test Setup

A small filter (10-µF capacitor and 5-µH inductor) was added at the input, which allows the board to pass the conducted emission test with more than 7 dB of margin.

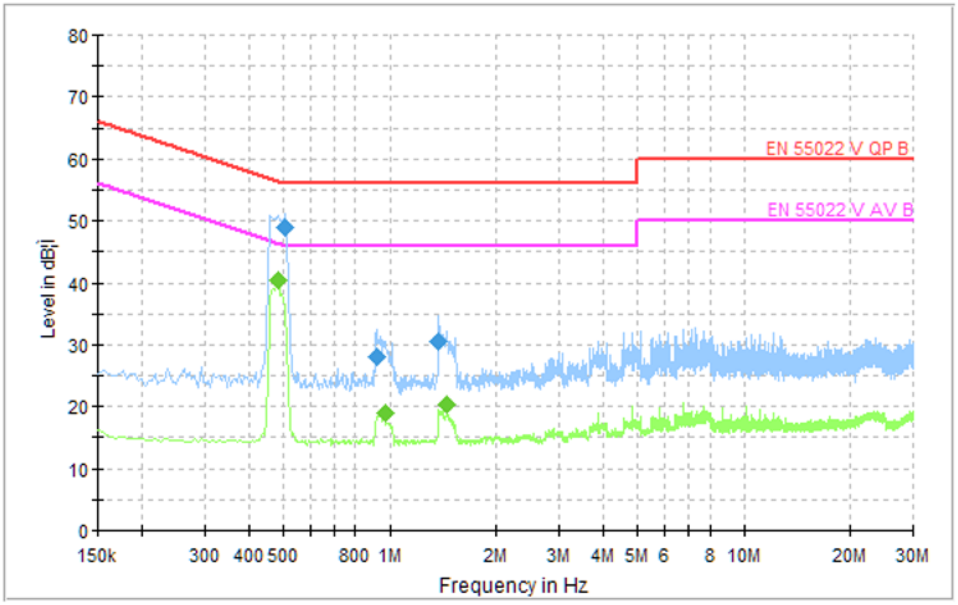

Figure 22. Conducted Emission Test Result With Filter

Table 11. Final Result 1

FREQ (MHz)	QUASIPEAK (dB¦ÌV)	MEAS TIME (ms)	BANDWIDTH (kHz)	PE	LINE	CORR (dB)	MARGIN (dB)	LIMIT (dB¦ÌV)
0.5090	48.9	1000	9	FLO	L1	20.4	7.1	56
0.9185	28.1	1000	9	FLO	L1	20.5	27.9	56
1.3775	30.6	1000	9	FLO	L1	20.5	25.4	56

Table 12. Final Result 2

FREQ (MHz)	AVERAGE (dB¦ÌV)	MEAS TIME (ms)	BANDWIDTH (kHz)	PE	LINE	CORR (dB)	MARGIN (dB)	LIMIT (dB¦ÌV)
0.4830	40.3	1000	9	FLO	L1	20.4	6.0	46.3
0.9680	18.9	1000	9	FLO	L1	20.5	27.1	46.0
1.4495	20.5	1000	9	FLO	L1	20.5	25.5	46.0

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00948.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00948.

5.3 PCB Layout Recommendations

In switch mode DC/DC, take care to avoid coupling between the different loops to improve performances. In a Buck topology, the input loop is particularly critical; for this reason, the input capacitors must be placed as close as possible to the TPS54202.

This is done by separating the noise sensitive loop (feedback and enable) from the high di/dt loops (input, switch node, bootstrap). This is done by placing the components and traces of the feedback and enable loop as far as possible from components and traces with high di/dt.

Special attention was also given to the ground plane; trying to make it as large and as solid as possible, to both reduce noise sensitivity, and help thermal dissipation.

With regards to thermal dissipation, the input and output voltage planes must also made as large and solid as possible to help keep the board as cool as possible.

Lastly, the soldering pad for the inductor was slightly enlarged to allow the tests of several inductors.

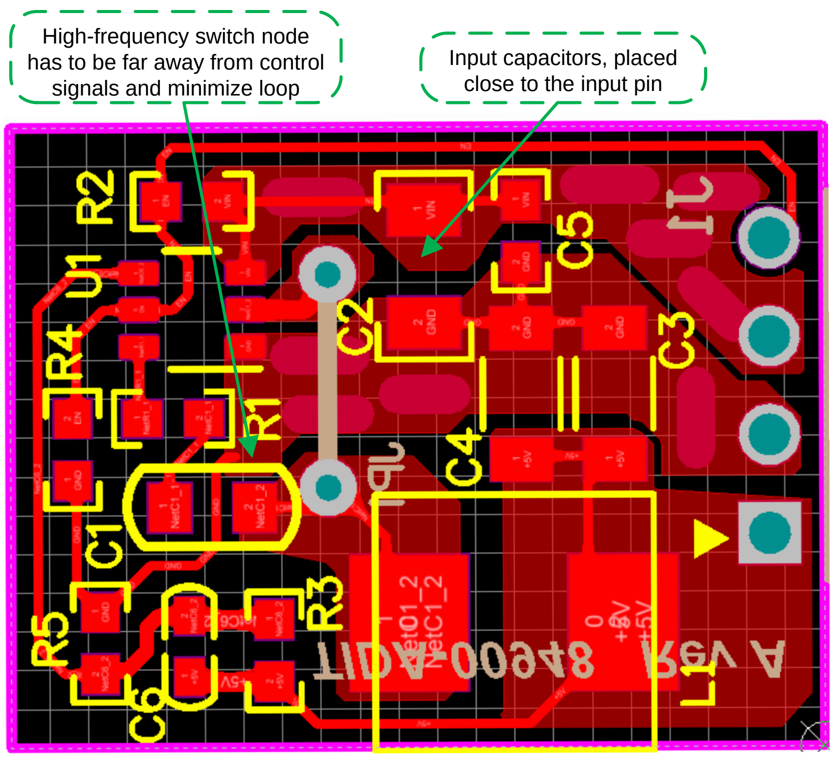

Figure 23. Top Layer

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00948.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00948.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00948.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00948.

6 References

1. Texas Instruments, *Understanding Buck Power Stages In Switchmode Power Supplies*, Application Report (SLVA057)
2. Texas Instruments, *Layout Tips for EMI Reduction in DC / DC Converters*, AN-2155 Application Report (SNVA638)
3. Texas Instruments, *Simple Success With Conducted EMI From DCDC Converters*, AN-2162 Application Report (SNVA489)

6.1 Trademarks

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7 About the Authors

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2016) to A Revision	Page
• Changed from preview page	1

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