TI Designs

Cascade Dual Charger Reference Design for 1S Li-Ion Battery-Powered End Equipment

Description

Smartphones and other handheld devices with 3AHr+ 1S Li-Ion batteries require 3 A of charger current or greater for fast charging. Parallel chargers allow for high-charge current which result in shorter charge time, which simultaneously distribute the heat losses across the end-equipment PCB, thereby preventing hotspots. This design uses a cascade configuration with the PMID pin of a master charger connected to the VBUS pin of a slave charger; the input current limit management is handled through a master charger, which simplifies software development.

Resources

PMP15011	Design Folder
bq25890	Product Folder
bq25898C	Product Folder

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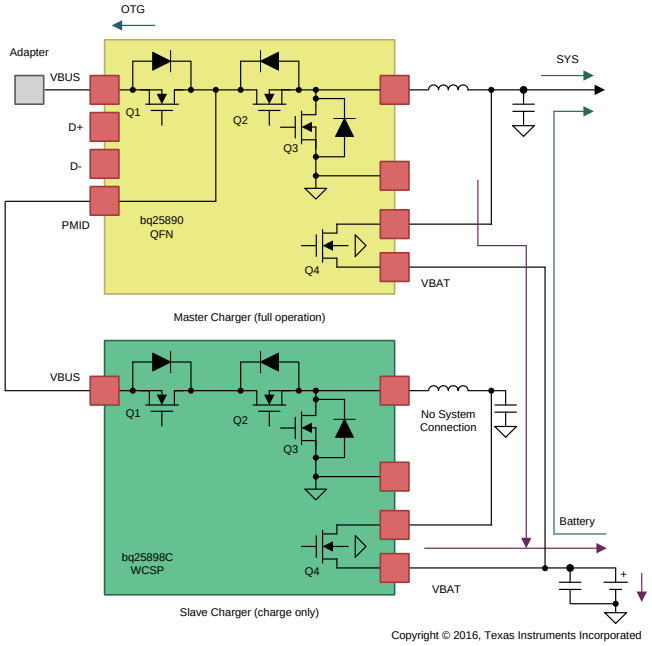
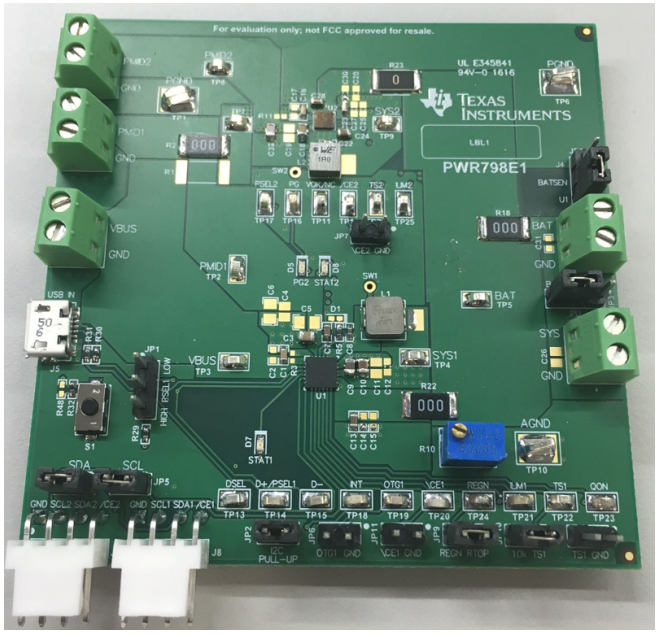
Features

- Master Charger: Provides System Power, Charging Current, Supplement Mode, Temperature Profile and 2.4-A USB On-the-Go Boost Current in 4×4-mm QFN Package
- Slave Charger: Exclusively Provides Extra-Fast Charge Current, up to 3 A in 2.8×2.5-mm WCSP Package
- Innovative Input Source Detection and Current Optimizer (ICO) with Input Dynamic Power Management (DPM)
- Integrated 7-Bit ADC for Battery and Adaptor Monitoring

Applications

- Smartphones
- Tablets
- Portable Media Players
- Other Portable Handheld Equipment with 3AHr+ 1S Li-Ion Batteries





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1 System Overview

1.1 System Description

Smartphones and other handheld equipment with 3AHr+ 1S Li-ion batteries require 3-A+ charging current for fast charging. Parallel chargers allow for high charge current, resulting in shorter charge time, while distributing the heat losses across the end equipment PCB. This feature prevents PCB hotspots and exceeding the thermal budget of a product. In cascade configuration, with the PMID pin of the master charger 1 connected to VBUS of the slave charger, input voltage and current limit is primarily managed through the master charger, thereby simplifying software development.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	VALUE	UNITS
VADPTR	Adapter output voltage = VBUS voltage	9	V
IADPTR	Adapter output current = IBUS current	3.5	A
ISYS	Expected maximum stead state system load current	1.5	A
ICHRG	Total charge current	4.5	A
ICHRG1	Charge current I^2C register setting for bq25890	2.25	A
ICHRG2	Charge current I^2C register setting for bq25898C	2.25	A
IINDPM1	Input current limit I^2C register setting for bq25890	3.25 (1)	A
INDPM2	Input current limit I^2C register setting for bq25898C	2.25 (2)	A
VINDPM1	Minimum VBUS I^2C register setting for bq25890	8.5 (3)	V
VINDPM2	Minimum VBUS I^2C register setting for bq25898C	8.2 (4)	V
VBATREG1	Battery regulation voltage I^2C register setting for bq25890	4.208	V
VBATREG2	Battery regulation voltage I^2C register setting for bq25898C	4.192 to 4.208 (5)	V
ITERM1	Termination current I^2C register setting for bq25890	128	mA
ITERM2	Termination current I^2C register setting for bq25898C	384 to 512 (5)	mA

(1) A power balance has been used to determine input current limit (adapter current): eff = Po / Pin → 0.92 = (4.2 V × (1.5 A + 4.5 A)) / (9 V × IINDPM1) → IINDPM1 => 3.0 A. ILIM pin has been disabled.

(2) INDPM2 is typically set to the current required to provide charging current at the VINDPM2 setting. ILIM pin and ICO is disabled on the slave charger.

(3) VINDPM1 has been set to adapter minimum regulation voltage.

(4) VINDPM2 has been set to VINDPM1 – INDPM2 × RDSON_Q1.

(5) To ensure that the slave charger terminates before the master charger, set the slave charger termination voltage lower than the master charger.

1.3 Block Diagram

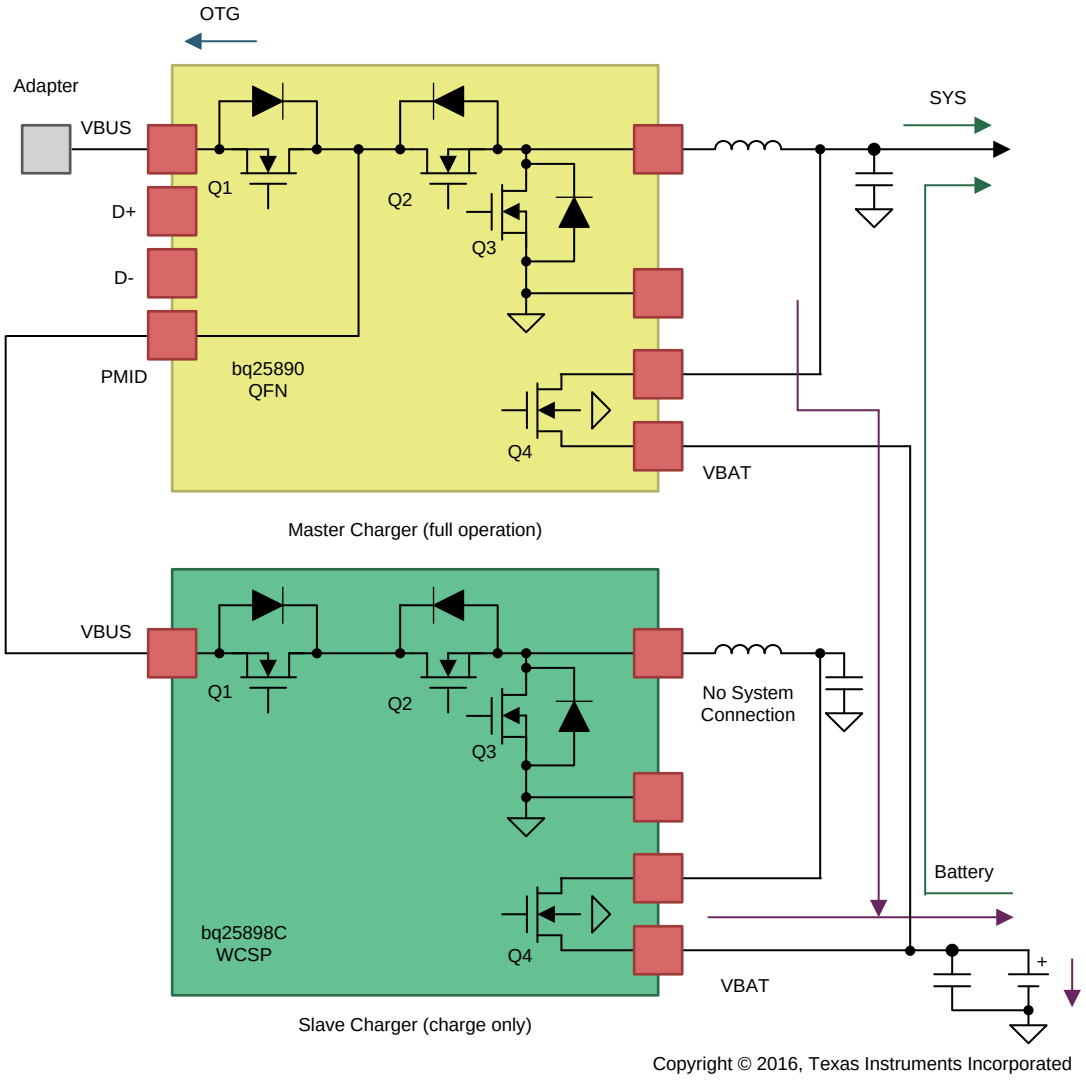

Figure 1. PMP15011 Block Diagram

1.4 Highlighted Products

1.4.1 bq25890

- Autonomous single input 5-A NVDC charger designed for high voltage, fast charging
  - Input voltage from 3.9 V to 14 V (22V absolute max voltage)
- > 91% efficiency at VBUS = 9 V and ICHRG up to 3.0 A
- Supports high-voltage dedicated charging port (HVDCP) and MediaTek Pump Express (MTK-PE) protocol
  - Supports D+/D– USB detection and non-standard adapters
- Adjustable USB on-the-go (OTG) up-to 2.4 A or 1.5 A with accurate ±15% overcurrent protection (OVP)
- High voltage V_{IN} and wide I_{IN} based dynamic power management
  - Input current limit up-to 3 A with 50-mA resolution
  - Input voltage limit up-to 14 V with 100-mV resolution

- Input current limit optimization (ICO) maximizes adapter output current without stressing the adapter
- Integrated analog-to-digital converter (ADC) to provide system and battery monitoring
- Programmable thermal regulation to maximize charge current
- High integration
  - Integrated 10-mΩ battery field-effect transistor (FET)
  - All FETs are current sensing
  - IR compensation for fast charging
- 4×4-mm thin QFN-24 package

1.4.2 bq25898C

- Autonomous single input 3-A NVDC charger designed for high voltage, fast charging
  - Input voltage from 3.9 V to 14 V (22-V absolute maximum voltage)
- > 92% Efficiency at VBUS = 9 V and ICHRG > 1.5 A
- High voltage V_{IN} and wide I_{IN} based dynamic power management
  - Input current limit up to 3 A with 50-mA resolution
  - Input voltage limit up to 14 V with 100-mV resolution
- Low power PFM mode for both buck and boost operations
- Integrated ADC to provide system and battery monitoring
- Programmable thermal regulation to maximize charge current
- High integration
  - Integrated 5-mΩ Battery FET
  - All FETs are current sensing
- 2.8×2.5-mm WCSP package

2 System Design Theory

2.1 Thermal Management

Historically, losses from higher power chargers have been distributed through the printed-circuit board (PCB) ground plane by careful placement of external field-effect transistors (FETs) on a charge controller integrated circuit (IC). While this practice is still an option in smaller portable devices, charge controllers are typically more complex to design and require significant board area for the controller IC, two FETs, diodes, and supporting passives.

Using the same concept of thermal distribution across the PCB, a simpler alternative is to use two integrated FET (I-FET) chargers in parallel, referred to as a dual-charger configuration.

2.2 Paralleling Charger Outputs

In general, connecting the output of two synchronous buck switching converters is not recommended, and for two reasons: unequal current sharing and reverse current. Regarding current sharing, because each converter has its own internal reference with a fixed tolerance, the output of each converter slightly varies, which results in one converter providing a higher regulated output than the other. This action results in the higher output converter providing more of the load current than the other. Second, a synchronous converter allows for some reverse current. The lower output converter may try to pull down the output voltage of the higher output converter by sinking current. Fortunately, by using the dynamic power-path management (DPPM) topology of a buck-switching converter-based charger, with the battery FET between the SYS regulated output and the BAT pin, this allows for the BAT pins of each charger to be tied together. When in constant-current (CC) charge mode, this is equivalent to tying the outputs of two current sources together. When in constant voltage mode, TI recommends to ensure that the slave charger terminates before the master charger, by either setting the termination voltage of the slave lower than the master, setting the slave termination current higher than the master, or both.

2.3 Input Power Management

Key features of the bq2589x family include: detecting the current capabilities of various HVDCP adapters at start-up, input current dynamic power management (IINDPM) with input current optimization (ICO), and input voltage DPM (VINDPM). If the VBUS pins of two chargers are connected in parallel, the ICO function of both chargers must be disabled to prevent inaccurate optimization results. In addition, their VINDPM thresholds must be set far apart to prevent instability. When connected in cascade configuration, in which the master charger PMID pin is connected to the slave charger VBUS pin, the master charger uses D+/D– to initially set the total input current limit for both chargers. In addition, the master charger can fully utilize its ICO and VINDPM functions. As a redundant protection, the slave charger VINDPM threshold can be set slightly lower than that of the master. The slave charger IINDPM is set only high enough to allow it to provide maximum charge current with no load. Using only one charger for input power management simplifies software development. When powered by adapters outputting 7 V – 13.5 V, the maximum input current limit setting of the master charger (up to 3.25 A) is high enough to provide 4.5 A and higher total charge current while still having enough input power left to power the system at SYS.

3 Getting Started Hardware

3.1 Hardware

This design is not available for order; however, the design files can be downloaded at TI.com. The design can be implemented by connecting and configuring the two orderable EVMs present in the schematic, downloadable in Section 5.1. The charging profile can be set for each charger as they have two different I^2C addresses.

4 Testing and Results

4.1 Test Setup

The following Figure 2 shows the test setup for the PMP15011 design. Power supply 2 (PS#2) drives the inverting voltage follower input to KEPCO battery simulator. The RC from PS#2 to the KEPCO causes the KEPCO output to slowly rise to the final voltage (VBATREG), simulating a battery charging. The bqStudio software was used to configure each charger, which Section 6 covers in greater detail.

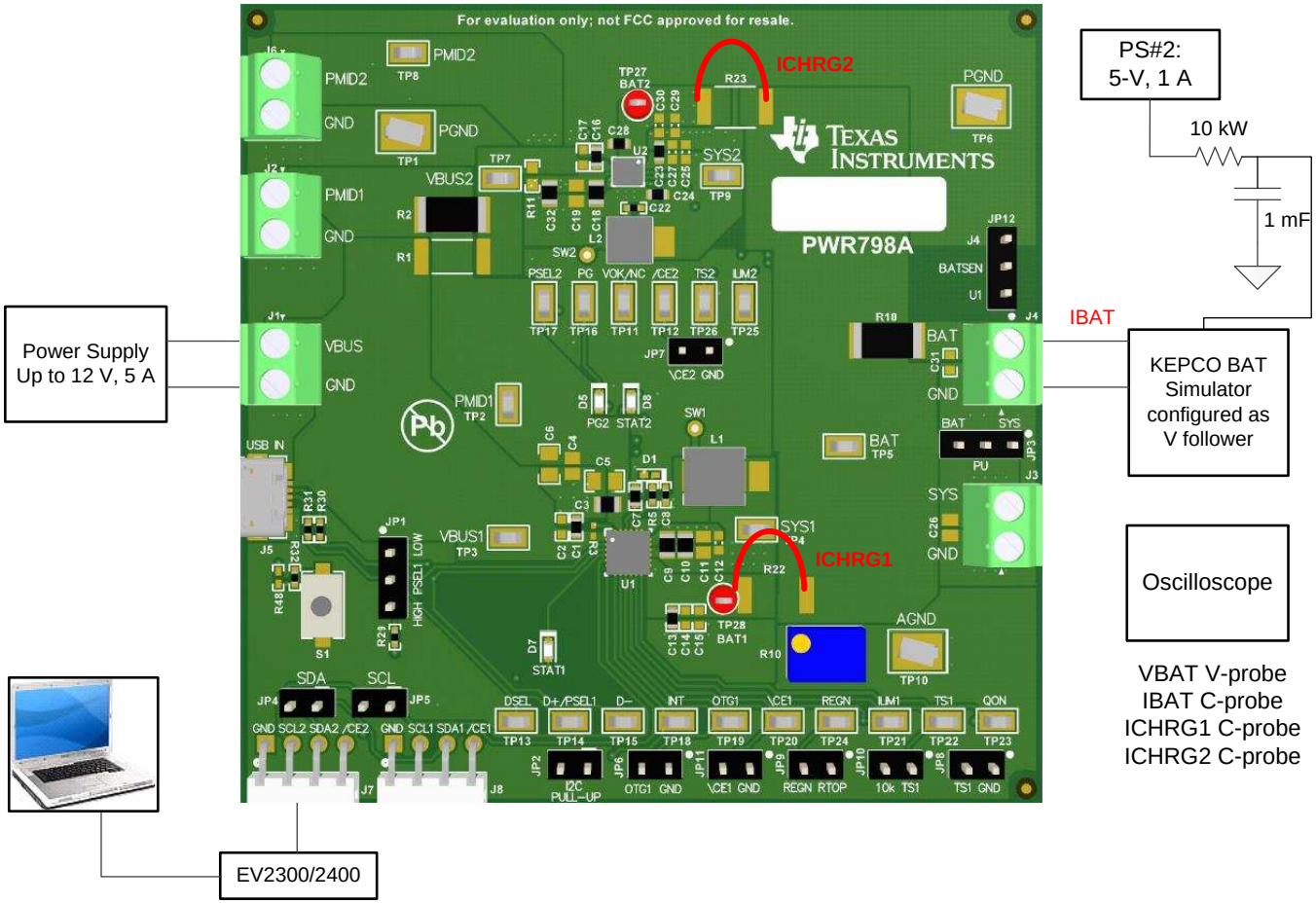

Figure 2. Test Setup for Simulated Charge Cycle

4.2 Test Data and Results

4.2.1 Simulated Charge Cycle

Using the test setup in setup in Figure 2 to simulate a charge cycle, the following results were achieved with both chargers set to a 2.25-A charge current, the master charger BATREG set to 4.2 V, and the slave charger set to 4.19 BATREG to ensure the slave charger turns off before the master charger (see Figure 3).

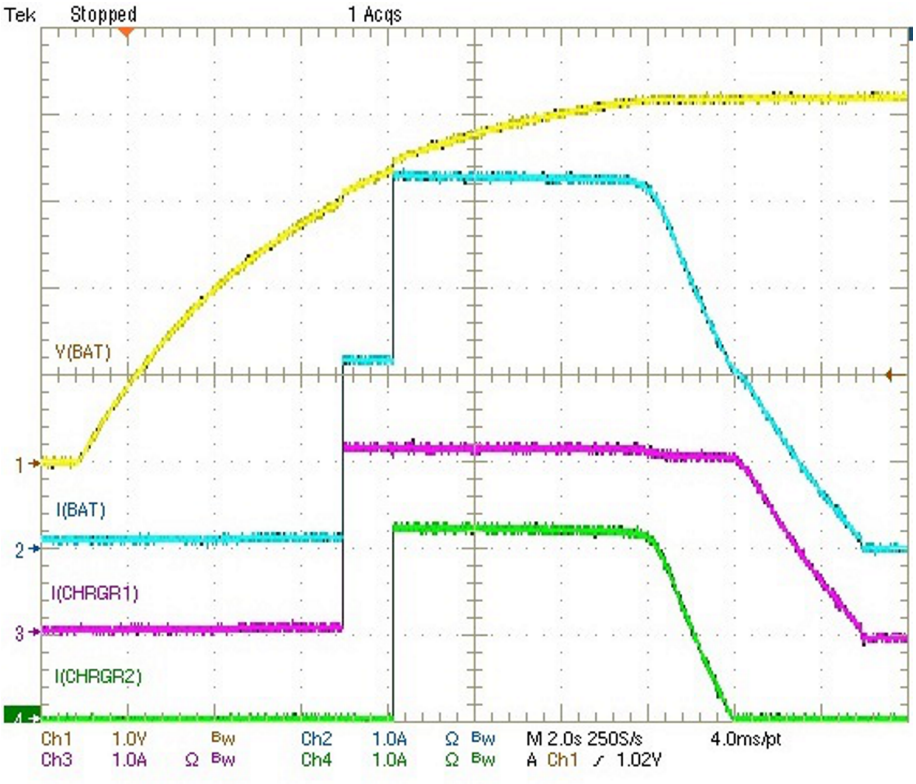

Figure 3. Simulated Charge Cycle

4.2.2 Thermal Data

Using a thermal camera, the following data was collected at V(VBUS) = 9 V and V(BAT) = 3.8 V on the EVM with four layers and 1-oz copper. The exposed pad of the bq25890 device was tied through thermal vias to large copper pours on one internal layer and the bottom layer. The bq25898C VBUS, SYS, GND, and PGND pins were tied to large copper areas on at least two layers. Refer to Section 5.3.1 for more details.

Table 2. Thermal Data Summary

CONFIGURATIONS	I_{CHARGE} (A)	TOTAL POWER LOSS (W)(1)	BOARD EDGE TEMP (°C)	IC MAX TEMP (°C)	TEMP RISE (°C)
Single bq25890	4.5	2.0	35	74	39
Single bq25890	2.25	0.77	26	40	14
Single bq25898C	2.25	0.64	26	39	13
bq25890 and bq25898C	2.25 + 2.25	1.41	32	48 / 45	16 / 13

(1) See efficiency curves in the Section 4.2.3.

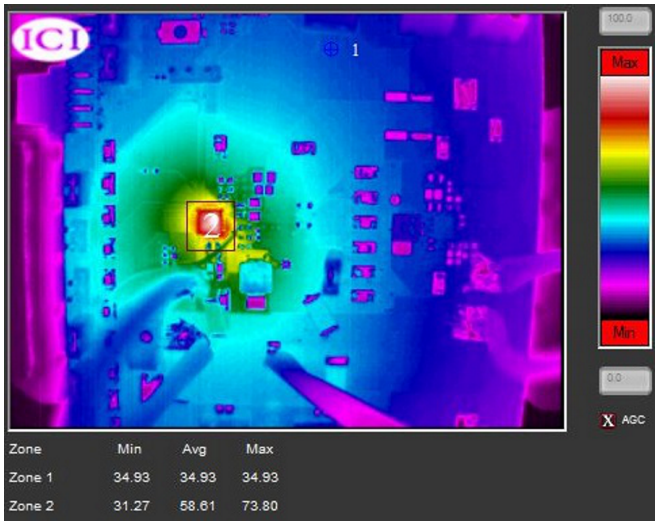

Figure 4. bq25890 With I_{CHARGE} = 4.5 A and bq25898C Disabled

Figure 5. bq25890 With I_{CHARGE} = 2.25 A and bq25898C Disabled

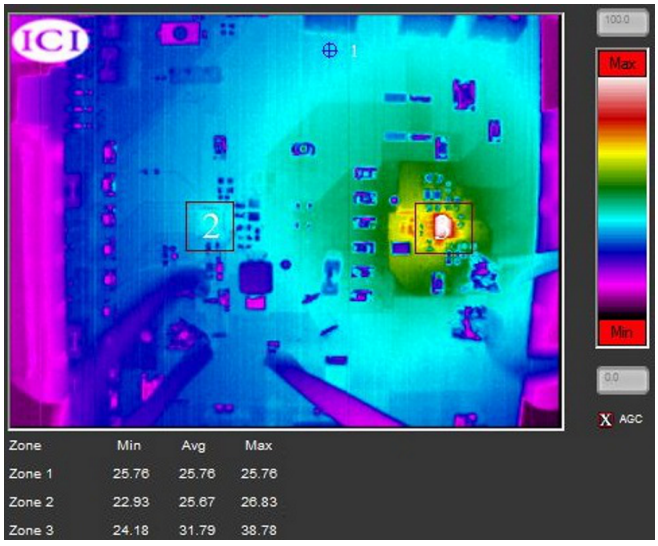

Figure 6. bq25890 Disabled and bq25898C With I_{CHARGE} = 2.25 A

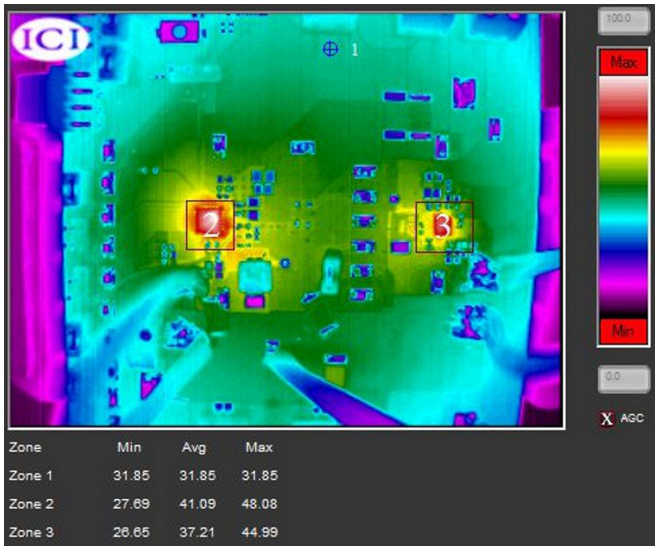

Figure 7. bq25890 With I_{CHARGE} = 2.25 A and bq25898C With I_{CHARGE} = 2.25 A

4.2.3 Data Sheet Efficiency Curves

Figure 8 and Figure 9 show the efficiency curves copied from the data sheets of each charger.

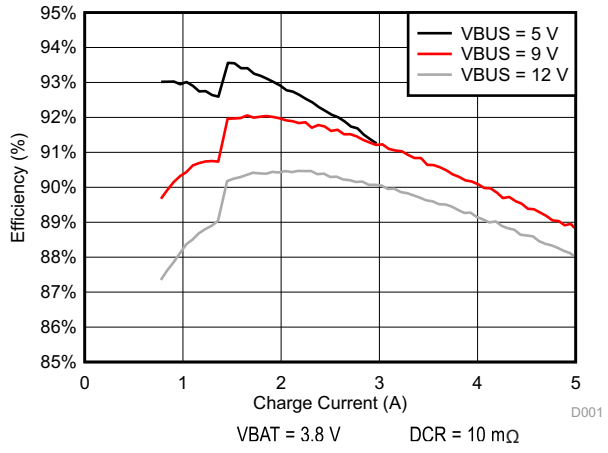

Figure 8. bq25890 Charge Efficiency

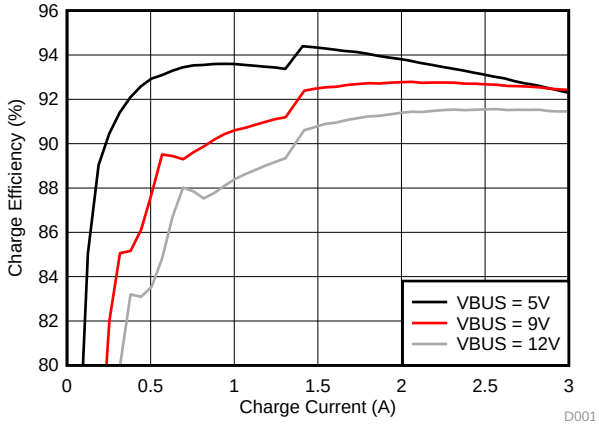

Figure 9. bq25898C Charge Efficiency

5 Design Files

5.1 Schematics

To download the schematics, see the design files at PMP15011.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at PMP15011.

5.3 PCB Layout Recommendations

For best thermal performance, connect the thermal pad of the QFN package and the multi-bump outputs of the WCSP package in as close proximity to the top-, internal-, and bottom-layer copper as possible. The priority of buck converter external passive placement is as follows:

1. PMID capacitor as close as possible between IC PMID and GND pins
2. SYS capacitor as close as possible between IC SYS and GND pins
3. BAT capacitor as close as possible between IC BAT and GND pins
4. Short trace from SW pin to inductor

Using multiple vias to connect one side of the above components through different layers is okay. When routing ground for non-power components (for example, REGN capacitor and TS resistor), it is best to either route away from the power ground return path or create a separate non-power island that only connects to the IC GND pin with a thin trace. Ensure that the switching signals SDA and SCL either do not cross or cross at 90° to analog signals BATSENSE and TS.

5.3.1 Layout Prints

To download the layer plots, see the design files at PMP15011.

5.4 Altium Project

To download the Altium project files, see the design files at PMP15011.

5.5 Gerber Files

To download the Gerber files, see the design files at PMP15011.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at PMP15011.

6 Software Files

To download the graphical user interface (GUI) used for setting the I^2C registers for this reference design, refer to http://www.ti.com/tool/bqStudio. Because members of the same charger family are used but have different I^2C addresses, both of the I^2C SDA and SCL pins of the charger are on the same I^2C bus and software development is easy. The following subsections instruct on when and how to configure the registers.

6.1 Power On Reset (POR) Initialization

1. The master charger is enabled for input current detection and charge (REG03[4]=1)
2. The slave charger is charge disabled (REG03[4]=0)
3. Configure the master charger
   - Set Pre-Charge Current limit (REG05[7:4])
   - Set Fast Charge Current limit to 2.25 A (REG04[6:0]) (assume total 4.5-A charge)
   - Set Termination Current limit (REG05[3:0])
   - Set Charge Voltage limit (REG06[7:2])
   - Set VINDPM offset threshold for typical 5-V adapter (REG01[4:0])
4. Configure the slave charger
   - Set Pre-Charge Current limit (REG05[7:4])
   - Set Fast Charge Current limit to 2.25 A (REG04[6:0]) (assume total 4.5-A charge)
   - Set Termination Current limit (REG05[3:0]) higher than that of the master charger to ensure it terminates first
   - Set Charge Voltage limit (REG06[7:2]) lower than that of the slave charger to ensure it terminates first
   - Set VINDPM threshold below the master charger
     – Set FORCE_VINDPM (REG0D[7])=1
     – Set VINDPM (REG0D[6:0])=0001101

6.2 Input Power Plug-In

1. The master charger charge is disabled.
2. The slave charger detects the input source and handshakes with an HVDCP adapter when conditions meet.
3. Set the master charger input current limit by writing to CHRG1 REG00[5:0].
4. The master charger starts charging with 2.25 A.
5. Read VBUS voltage information from the master charger ADC register.
6. Force CHGR1 ICO (set REG09[7]=1), then read the current ICO input current limit (REG13[5:0]) from CHRG1 when ICO is optimized (REG14[6]=1).
7. Divide the input current limit by half and write to CHGR2 REG00[5:0].
8. The slave charger enables charging as long as any of following conditions do not exist:
   - VBAT < VSYSMIN
   - 5-V adapter with lower than 2-A input current
   - 9-V adapter with lower than 1-A input current
   - Charge terminated

6.3 During CC and CV

1. During CC mode, ICHG1 and ICHG2 are controlled by each charger.
2. Period reads of each charger VBUS, ICHRG, and VBAT ADC registers are recommended to monitor operation and ensure load sharing.
3. During CV mode, the ICHGR1 and ICHGR2 can be used at the same time due to guaranteed tight ±0.5% CV tolerance.
4. Both the master charger and the slave charger terminate automatically without host interference, as indicated by STAT voltage change and INT signal.

7 References

1. Texas Instruments, *bq25890, bq25892 Dual Cascade Charger EVM (PWR692)*, bq25890 and bq25892 User's Guide (SLUUBB8)

8 About the Author

JEFF FALIN is an applications engineer with over 16 years of experience supporting DC-DC converters and battery chargers. Jeff earned his Masters of Science in Electrical Engineering (MSEE) from University of Tennessee.

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