TI Designs: TIDA-01590

Reference Design for 1200-V, Isolated, I²C, High-Side Current Sensing for Solar Combiner Boxes

Description

This reference design is an isolated high-side current sensing design for a smart combiner box in a grounded or ungrounded system. The current sensing topology enables multichannel, sub ±1% error, isolated current sensing for high-voltage systems up to 1200-V DC, limited by the DC/DC transformer.

Resources

TIDA-01590	Design Folder
INA260	Product Folder
ISO7842	Product Folder
TPS709	Product Folder
SN6505A	Product Folder

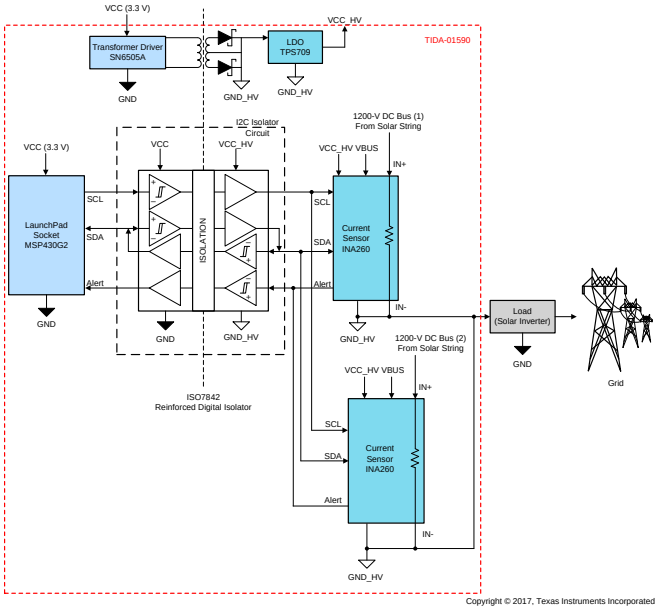
TI E2E™ Community — ASK Our E2E™ Experts

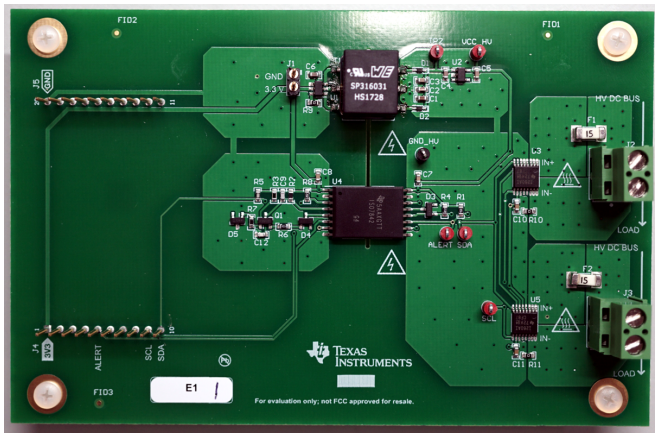
Features

- Isolated High-Side Current Sensing of Multiple Photovoltaic Strings
- Capable of Monitoring Current Within ±1% Full Scale Accuracy
- Supports 1200-V isolated I²C Current Sensing in Smart Combiner Boxes
- Option to Connect Additional INA260 Devices to I²C Bus

Applications

- Smart Combiner Boxes
- Solar Inverters





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

While the deployment of photovoltaic (PV) systems has grown exponentially over the past 10 years, solar energy still powers only a small percentage of the grid. The two major challenges are cost (amount per watt) and efficiency. When developing new solar technology (solar inverters, power optimizers, and so on), a system designer must increase efficiency through intelligent system and subsystem topologies that also decrease the cost per watt.

For PV arrays with a power capacity greater than 50 kW, it is necessary to combine the PV strings into a high-voltage direct current (DC) bus before the inverter. This system is known as a solar combiner box. The solar combiner box in relation to the solar power system is shown in Figure 1.

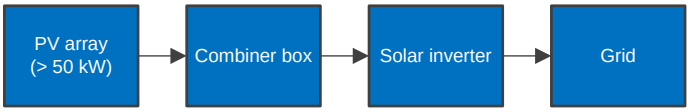


Figure 1. Solar Power System

The solar combiner box reduces the total system cost by decreasing the external cabling and copper DC buses. Solar combiner boxes are connected to one or more PV strings. One PV string is typically rated to 600-V, 1000-V, 1200-V, or 1500-V DC, and rated 8 to 25 A. This varies depending on the layout of the PV array and the solar power system.

Traditionally, power monitoring occurred at a multi-string level, but now, with increasing array sizes, string level power monitoring becomes critical to immediately detect a solar panel operating at a diminished capacity and the corresponding damage. The solar combiner box became the smart combiner box when current and voltage sensing technology was moved from the solar inverter (multi-string level) to the solar combiner box. The smart combiner box with a basic feature set is displayed in Figure 2.

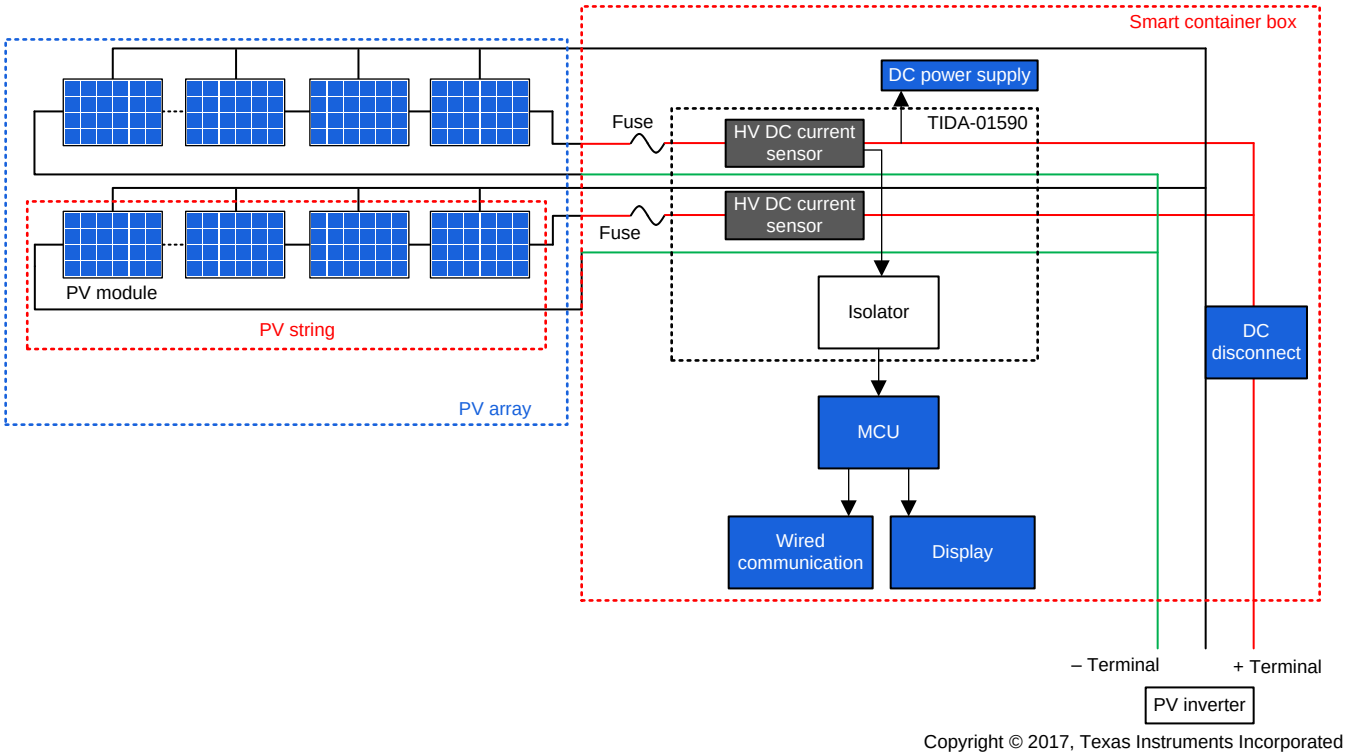


Figure 2. Smart Combiner Box in PV System (1)

This reference design is the power sensing subsystem shown within the black dotted box in Figure 2. The board is also designed to enable connection to an MCU.

(1) http://www.homepower.com/articles/solar-electricity/equipment-products/pv-combiner-box-buyers-guide

1.1 Power Sensing Subsystem

Isolated sensors can take measurements even if there is high common-mode voltage. Isolation also protects the sensitive MCU from the high-voltage side of the board. With high-voltage considerations taken into account for the schematic design and PCB layout, isolated current sensing is the best option for this sensing topology.

The currents of PV strings can be measured with high-side or low-side sensing techniques, depending on the solar power system's accuracy requirements and grounding configuration. In the United States, the National Electric Code requires PV modules or strings over 50-V DC to be a grounded system to decrease safety risks. A grounded system is defined as either the positive or negative terminal being tied directly to earth ground. [(2)]Low-side and high-side sensing are viable options for a grounded system. The majority of regional standards regarding solar power systems worldwide do not require PV installations to be grounded systems. Grounded and ungrounded systems are pictured in Figure 3.

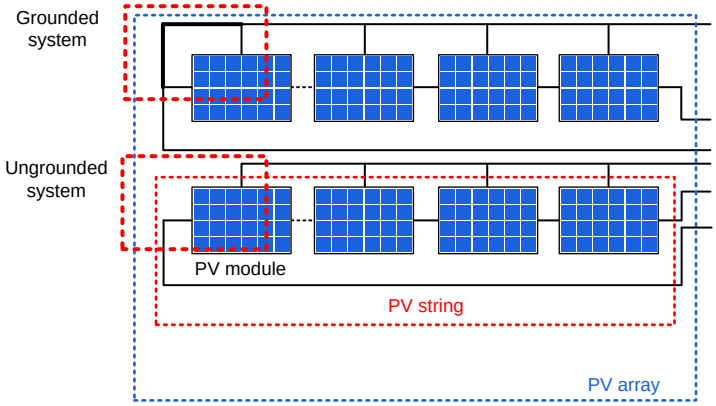


Figure 3. Smart Combiner Box With Ungrounded and Grounded Systems

Low-side current sensing is less expensive than the high-side sensing. However, this method cannot detect load shorts in ungrounded or grounded systems and cannot account for grounding inconsistencies. High-side current sensing directly measures the current through the load (before DC combination) and can accurately measure the current in relation to a common ground, the PV string ground. When the smart combiner box is connected to a grounded system and high-accuracy current sensing is not a requirement, low-side current sensing could be the preferred option. When accuracy, load shorts, or grounding inconsistencies are a concern, high-side sensing is the preferred method. Consequently, the majority of smart combiner boxes employ high-side current sensing.

Smart combiner boxes also measure PV string voltage. Because the PV strings are connected in parallel, the string voltages are all equal. Consequently, one voltage measurement is necessary for power monitoring. In a grounded or ungrounded system, TI's power monitor can be used for DC bus voltage and current measurements. The bus voltage and current are measured in relation to PV string ground.

This reference design evaluates isolated high-side current sensing for ungrounded and grounded systems. Figure 4 and Figure 5 depict how to connect the reference design within a smart combiner box in an ungrounded or grounded system. The current of the PV string are sensed in relation to the negative terminal of the PV string. This current sensing reference design measures a maximum of 15 A of the 1200-V DC bus at ±1% full scale.

(2) http://solarabcs.org/about/publications/reports/systemgrounding/pdfs/SystemGrounding_studyreport.pdf

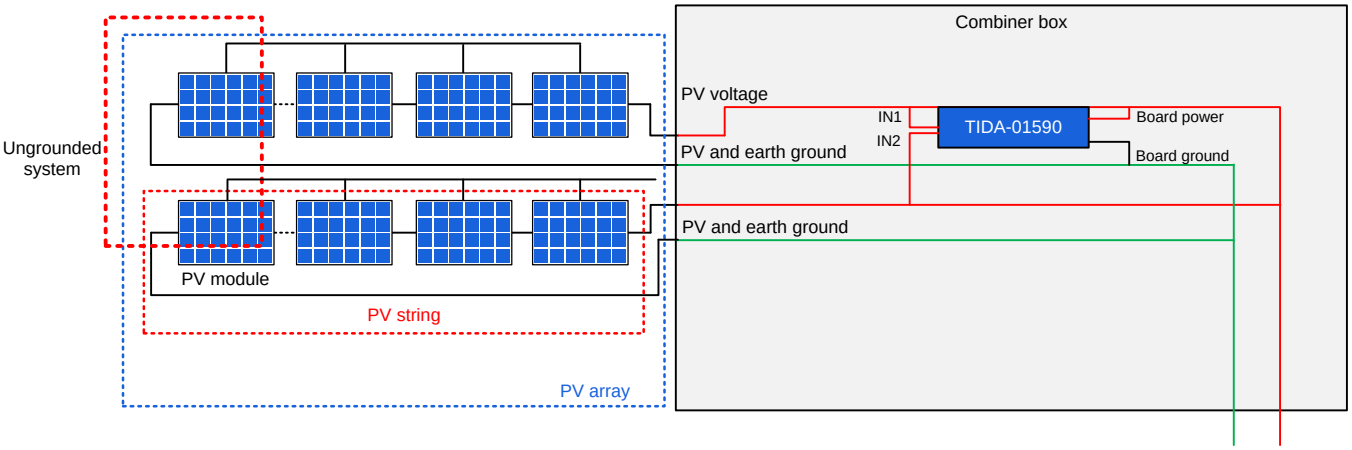


Figure 4. TIDA-01590 in Ungrounded PV System

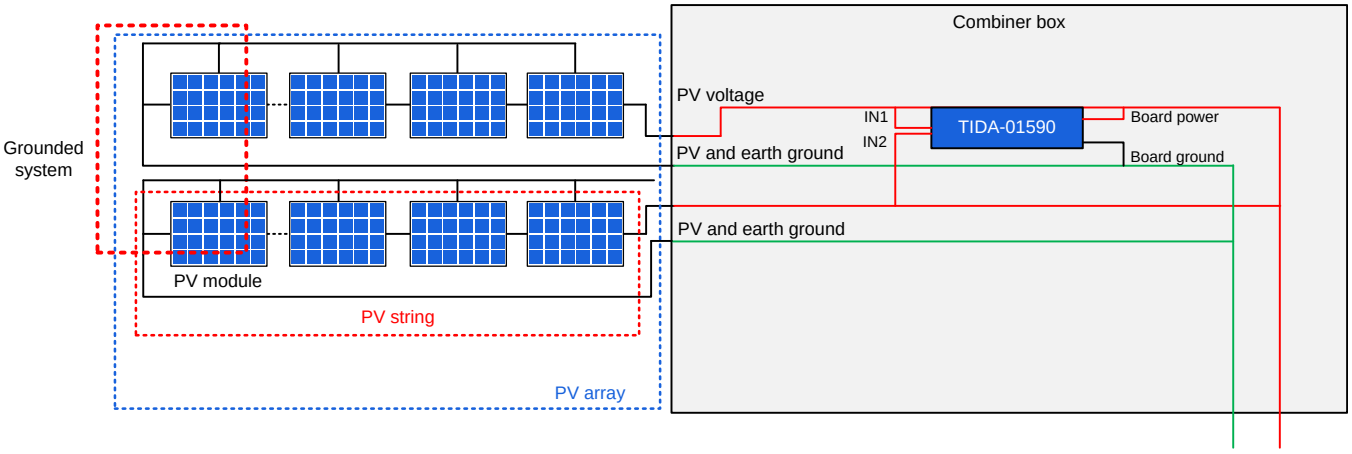


Figure 5. TIDA-01590 in Grounded PV System

1.2 Key System Specifications

Table 1. System Specifications

PARAMETER	SPECIFICATION
I_{SENSE} accuracy	±1% full scale
DC bus current	0.5 to 15 A
DC bus minimum voltage	95 V
DC bus maximum voltage	1200 V
Number of PV string inputs	2 per board
Operating temperature range	–40ºC to +85ºC

2 System Overview

2.1 Block Diagram

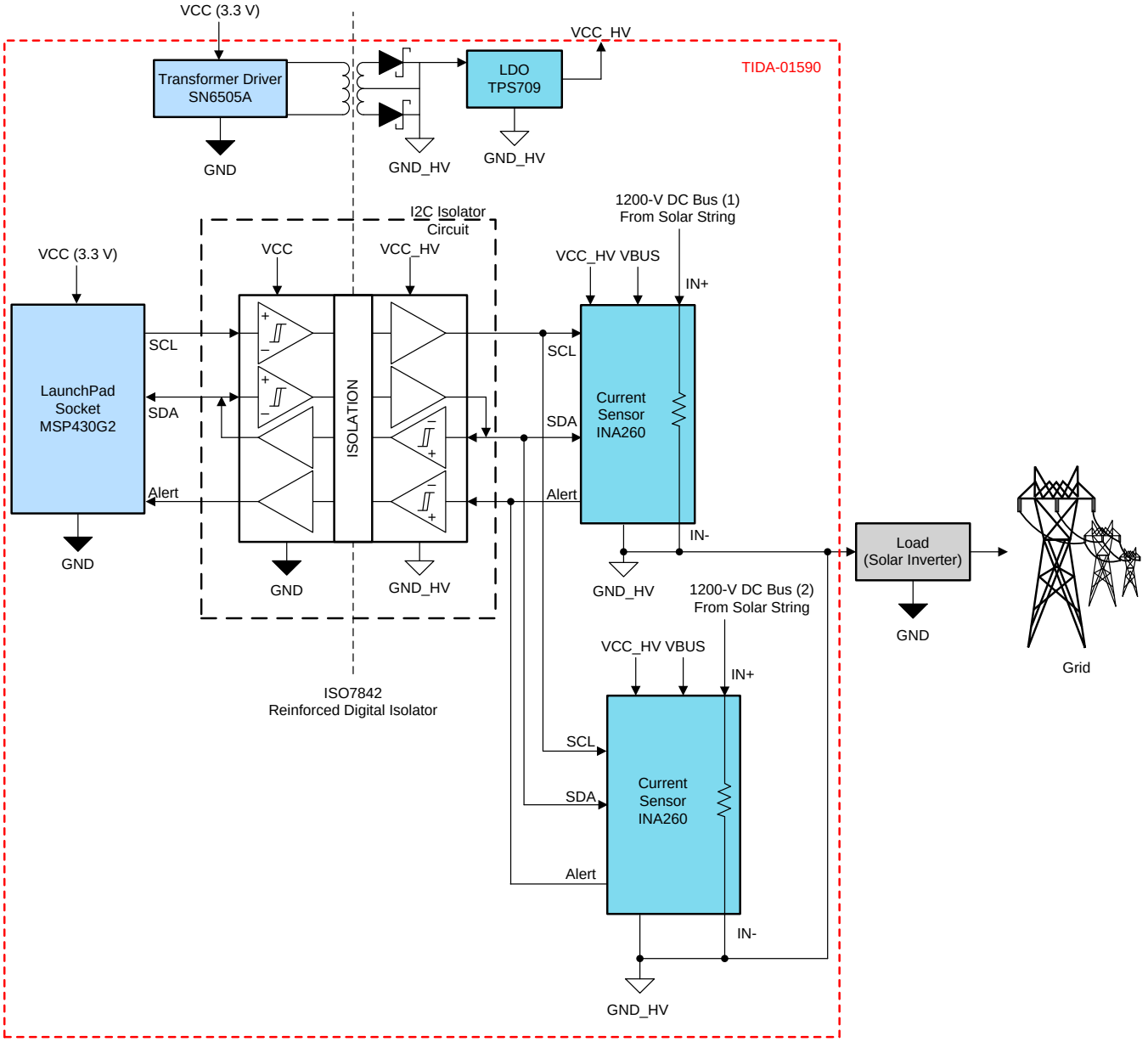


Figure 6. TIDA-01590 Block Diagram

2.2 Highlighted Products

This reference design features the following devices:

- SN6505A: 160-kHz transformer driver for isolated power supplies
- TPS709: 30-V LDO with ultra-low quiescent current and reverse current protection
- INA260: Digital current and power monitor with integrated 2-mΩ shunt resistor
- ISO7842: Reinforced four-channel 2/2 digital isolator

2.2.1 SN6505A

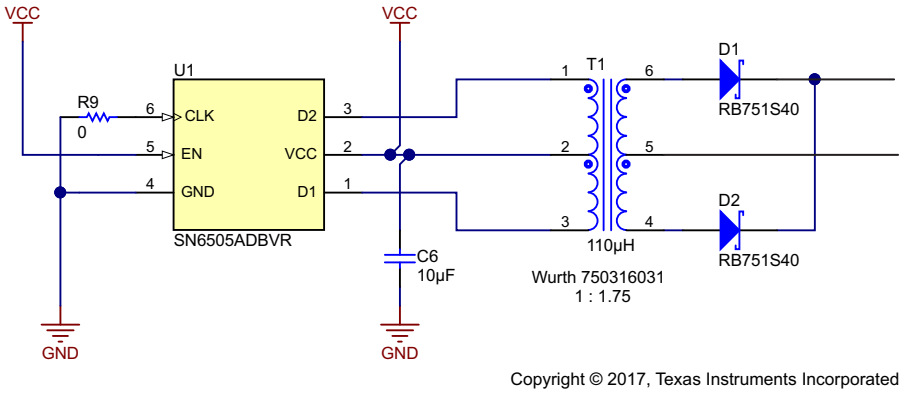


Figure 7. Transformer Driver and Isolation Transformer Schematic

The SN60505A is a low-noise, low-EMI push-pull transformer driver for isolated power supplies. Key features for this device include:

- Wide input voltage range: 2.25 to 5.5 V
- High output drive: 1 A at 5-V supply
- Precision internal oscillation: 160 kHz
- Small 6-pin SOT23/DBV package
- Thermal shutdown
- Ultra-low EMI
- The SN60505A uses the Schottky diode RB751S40. The low forward voltage provides as much voltage to the converter output as possible. The short recovery time of the diode is ideal for high-frequency switching and prevents leakage at temperatures > 85ºC.

This device also uses the 750316031 transformer, which is a recommended isolation transformer optimized for SN6505A (see Table 3 of the device datasheet). This transformer allows use of a 3.3-V supply to power both sides of the board. This 3.3-V supply is required for MSP430™ and ISO I^2C interface configuration. The 1 to 1.75 turn ratio also places the 3.3-V input voltage at 5.775 V, which is above dropout range of LDO. The large body of the transformer is necessary to meet voltage isolation requirements and creepage and clearance standards.

The 0-Ω resistor, R9, connects GND and CLK on the SN6505A. This is to ensure the I^2C switching noise does not causes issues with the internal pulldown.

2.2.2 TPS709

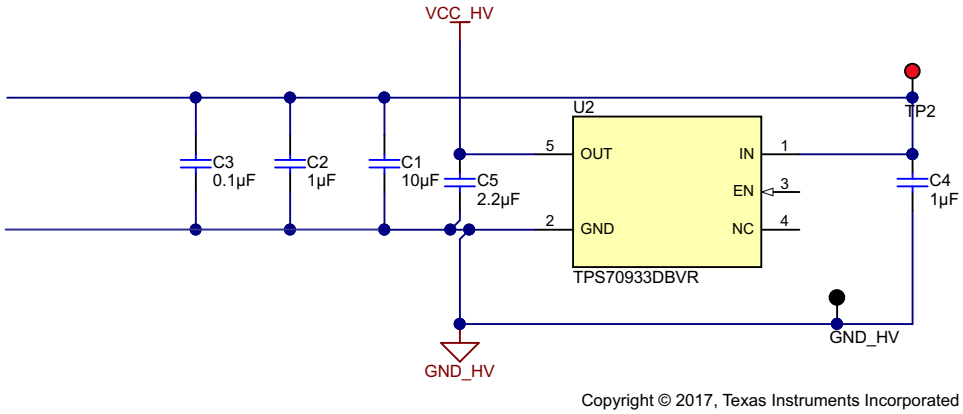


Figure 8. Low Dropout Regulator Schematic

The TPS709 is a ultra-low quiescent current LDO designed for power sensitive applications. Key features of the device include:

- Quiescent current: 1 µA
- Voltage output: 3.3 V
- Current output: 50 to 150 mA
- Dropout voltage: 0.96 V at 150 mA
  - $V_{I\text{-}min} = V_{DO\text{-}max} + V_{O\text{-}max}$
  - $V_{I\text{-}min} = 1.4 + 3.3 = 4.7$ V
- Thermal shutdown and overcurrent protection

2.2.3 INA260

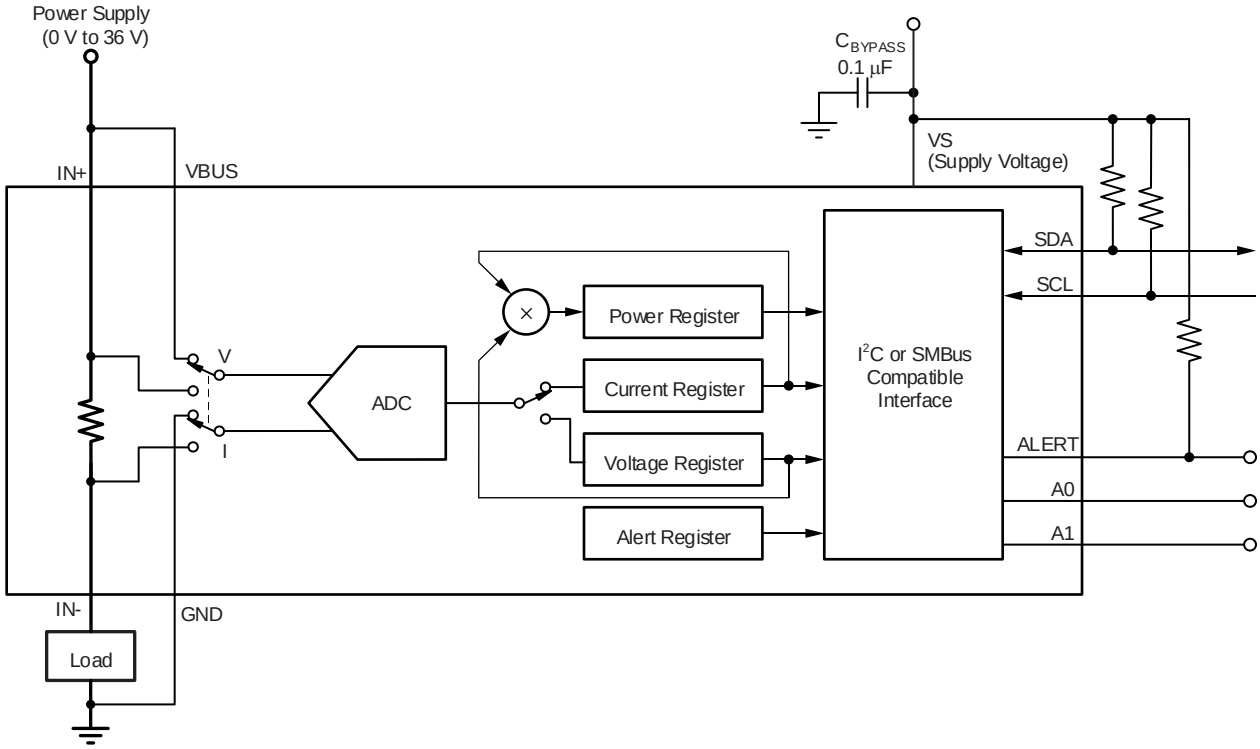


Figure 9. INA260 Block Diagram

The INA260 is a precision digital current monitor with an integrated shunt current. Key features of this device include:

- Current sense resistance: 2 mΩ
- 15 A continuous from –40ºC to +85ºC
- High accuracy:
  - 0.15% system gain error (max)
  - 5-mA offset (max)
- Configurable averaging options
- 16 programmable addresses
- I^2C and SMBus compatible
- Programmable alert thresholds

2.2.4 ISO7842

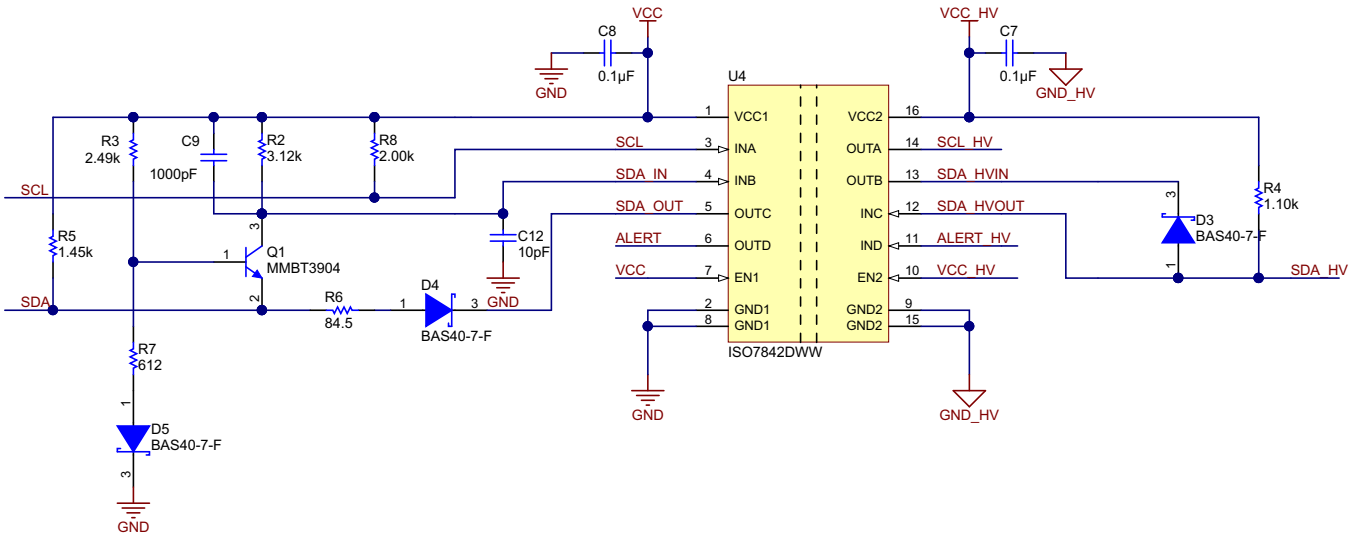


Figure 10. Digital Isolator Schematic

The ISO7842 is a high-performance, 8000-V_{PK} reinforced quad-channel digital isolator. Key features of this device include:

- Signaling rate: Up to 100 Mbps
- Wide temperature range: –55°C to +125°C
- 300-mA maximum output current
- Low-power consumption: typical 1.7 mA per channel at 1 Mbps
- Industry leading CMTI (min): ±100 kV/µs
- Extra-wide body package
- Safety and regulatory approvals:
  - 8000-V_{PK} reinforced isolation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - 5.7-kV_{RMS} isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IE 60950-1 and IEC 60601-1 End Equipment Standards
  - CQC certification per GB4943.1-2011
  - TUV certification per EN 61010-1 and EN 60950-1
  - All DW package certifications complete; DWW package certifications complete per UL, VDE, TUV and planned for CSA and CQC

This device also uses the 750316031 MID-PPTI Push-Pull Transformer for SN6505A. This transformer complies with requirements as defined by these specifications.

2.3 System Design Theory

This reference design is a shunt-based current sensing subsystem for a smart combiner box, as pictured in Figure 6. Integrated in the INA260 chip, the shunt resistor is on the high-side of the load, directly measuring the current flowing into the load from each input. The integrated shunt device is chosen to minimize system complexity while maximizing accuracy of the current sensing circuit. The shunt resistance of 2 mΩ lowers the power losses to a negligible level. At maximum current, the power dissipation for one channel can be calculated as shown in the following equations.

$$\text{Maximum power dissipation} = V_{SENSE} \times I_{SHUNT} = 30\ \text{mV} \times 15\ \text{A} = 0.45\ \text{W} \quad (1)$$

$$\%\ \text{power dissipation from shunt} = \frac{\text{Maximum power dissipation}}{\text{Maximum total power}} \times 100 = \frac{0.45\ \text{W}}{1200\ \text{V} \times 15\ \text{A}} \times 100 \quad (2)$$

when

- $V_{SENSE} = R_{SHUNT} \times I_{SHUNT} = 2\ \text{m}\Omega \times 15\ \text{A} = 30\ \text{mV}$

The 2-mΩ shunt resistor is rated at 0.1% tolerance and 10 ppm/°C temperature coefficient.

Smart combiner boxes are typically powered by an internal power supply from a PV string. The DC/DC power supply block is not within the scope of this reference design, so an external power supply is used. For more information about possible DC/DC converter topologies for the power supply, TI offers power reference designs to evaluate power subsystems. See Section 2.3.2 for more details on the power supply for this reference design.

Smart combiner boxes monitor temperature within the box using a temperature sensor. The smart combiner box is typically outside and risks becoming overheated. Monitoring the temperature is necessary to verify the internal temperature is less than the operating temperature of the box. This design does not include a temperature sensor device as it is not the emphasis of the subsystem. The recommended temperature sensor for this application is the LMT84. The ±0.4°C accuracy and wide temperature range of –50°C to +150°C make it ideal for detecting temperatures outside of the system operating range.

2.3.1 High-Side Current Sensing

Current measurements are taken by the INA260 device. This model is used for its high accuracy and ease of implementation. The device also meets the current requirements of ±15 A. The integrated precision shunt resistor, programmability, and digital output significantly contribute to simplifying designs. Connections to the current sense resistor are optimized to achieve the best measurement accuracy and temperature stability. The integrated shunt [1] simplifies PCB design and allows less room for error. The value of the resistor is already calibrated and set internally so returned values for current are easily converted to amperes. Other digital solutions require programming the value of the current sense resistor, either internally or in the host processor so the returned current readings are scaled appropriately.

This integrated shunt resistor has the following characteristics:

- Precise
- Low-drift
- Four-wire connected resistor
- Current sense resistor and current sensing amplifier are precisely matched to one another

This design makes use of the device's alert function. This function compares the measured value to a programmed alert register value following each conversion. The alert pin is pulled up to VCC by a 7.5-kΩ resistor.

The INA260 has multiple programmable modes based on the needs of the user. For this application, it is recommended to run the device in continuous mode for consistent current monitoring. The user also has the ability to control conversion time, averaging, and other measurement considerations. Find more information on programming the device and how these design choices affect performance in the INA260 datasheet.

2.3.1.1 Over and Under Current-Limit Alerts

The INA260 device contains an alert limit register, which enables the device to be programmed to respond to a variety of specific alert conditions; including:

- Shunt Over Current-Limit (OCL)
- Shunt Under Current-Limit (UCL)
- Bus Voltage Over-Limit (BOL)
- Bus Voltage Under-Limit (BUL)
- Power Over-Limit (POL)

Because the architecture of this reference design does not monitor the bus voltage, only the over and under current limits are available for use.

By using the built-in functionality of the INA260, the system can detect and respond to potential fault conditions and take appropriate action before it is detected in software. A short circuit in a module of one of the strings connected to a combiner box can potentially drop the output voltage of the string, allowing current to flow from the good strings through the faulty one, leading to overheating and potential destruction of the string. This condition is normally handled through string diodes and fuses, but an active solution can add an additional layer of protection to the strings.

The alert functionality of the INA260 is software based. As such its response time is dependent on the conversion time of the internal ADC. For the full signal path, once the current flowing through the internal shunt causes the ADC conversion output to cross the alert register threshold, the alert pin is asserted low. The conversion time of the ADC is configurable depending on the needs of the system. This is done through the ISHCT register of the INA260 and can vary from 140 µs to 8.2 ms.

The delay between the measured event and assertion of the alert pin is also dependent on when in the ADC sample window the event occurs. The actual real world delay is at best one ADC cycle, and at worst two. For example, at the fastest conversion rate, the alert is between 140 and 280 µs. See Figure 11 for an example of this.

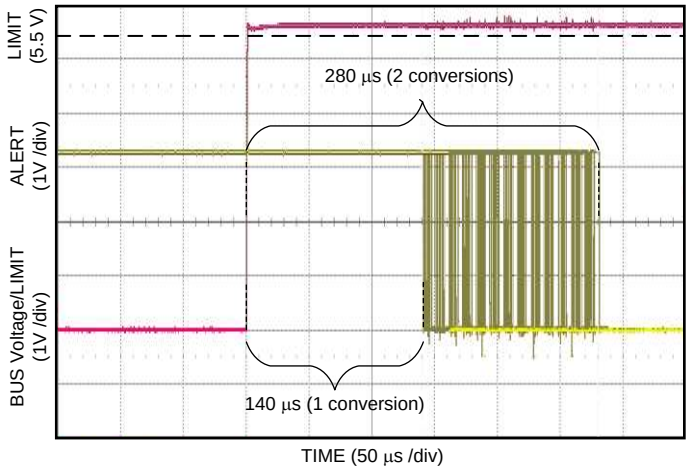


Figure 11. Alert Signal Delay of INA260

The alert signal output of the INA260 is brought across the high-voltage barrier using the extra channel available on the ISO7842. This device has a propagation delay of 11 ns and is negligible compared to the delay of the conversion time of the INA260. For additional information on optimizing the INA260 conversion time, see the device datasheet.

2.3.2 Board Power Supply

The board is powered by a 3.3-V external supply through the terminal block input, J1. The ground terminal of this power supply is connected to the PV string ground (load ground) and the terminal block input, J1, which stabilizes the ground plane of the PCB. The 3.3-V voltage rail powers the SN6505A, ISO7842, and the LaunchPad™ socket on the low-voltage side of the board. The transformer driver and power transformer translate the 3.3-V supply to the high-voltage side of the board, where it powers the INA206 and ISO7842.

The isolated power supply for the MCU, digital isolator, and the current sensor is generated using a push-pull driver for isolated power supplies, the SN6505A. The transformer used in this application is the Würth 750316031 (1:1.75 → 3.3:5.775). The transformer package is selected to have a working isolating voltage of > 1.2 kV and creepage and clearance ratings of > 11 mm. The only limiting factor for performing a 1.5-kV current sensing using this same design is the clearance of the transformer.

The TPS709 LDO provides a clean supply to the INA260 current sensors, maximizing accuracy.

2.3.3 Digital Isolator

The ISO7842 provides reinforced isolation in an extra wide (14 mm) package. This quad-channel isolator has two channels in the forward direction and two in the reverse. The device provides the required 1.5 kV working voltage isolation between the current sensing circuit and the MCU. Used in conjunction with isolated power supplies, this device helps prevent noise currents on data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The large package size is necessary to meet customer creepage and clearance specifications.

The I^2C bus uses open-drain technology, thus requiring the serial data line (SDA) and serial clock line (SCL) to be connected to VCC by pullup resistors. The I^2C enabled isolators currently produced by TI do not meet the requirements of this system. For standard digital isolators, external circuitry is necessary to separate the bidirectional SDA bus into two unidirectional signal paths without introducing significant propagation delay. The I^2C technical brief [2] shows the solution that the design configuration is based on.

2.3.4 MCU LaunchPad Socket

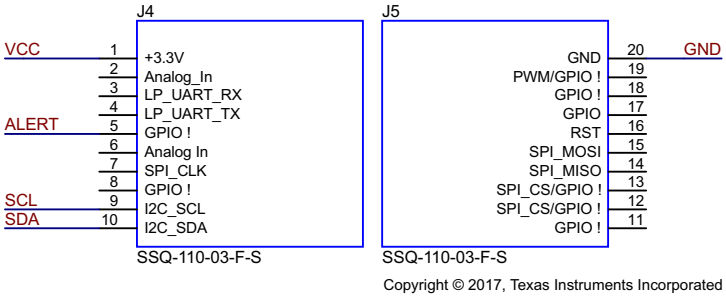


Figure 12. LaunchPad Socket Schematic

The standard LaunchPad socket is onboard to enable connection to an MCU. The LaunchPad enables I^2C and UART communication.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

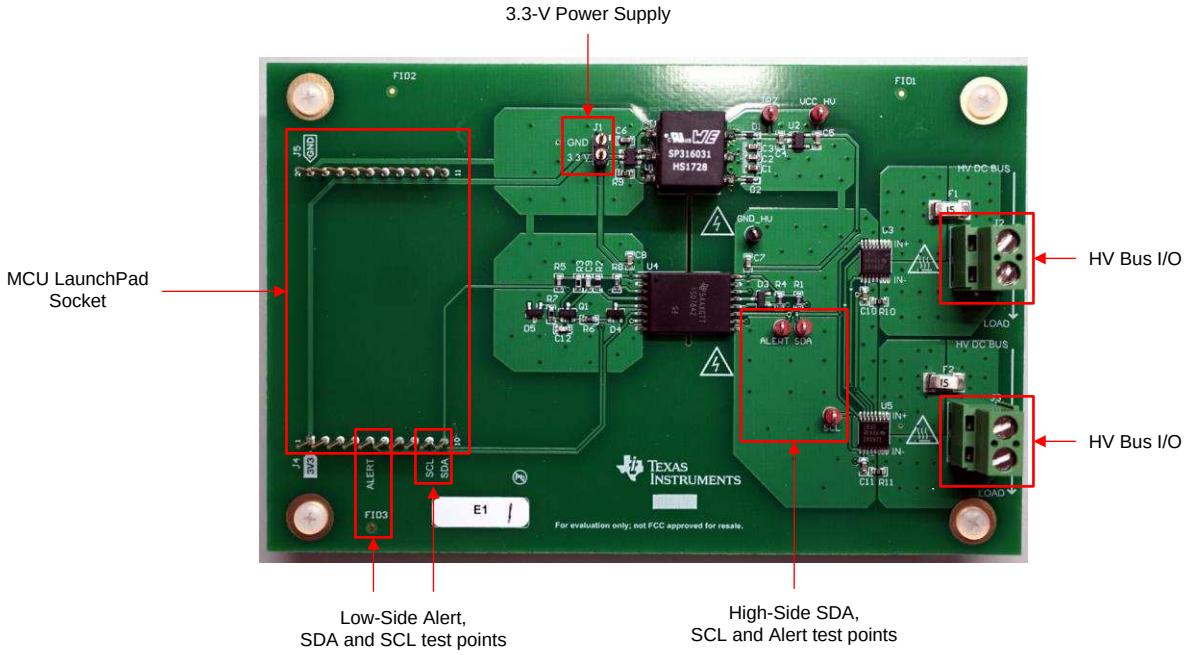


Figure 13. TIDA-01590 PCB

3.1.1 Board Setup

1. Connect the two high-power inputs to terminal screw blocks J2-2 and J3-2, labeled HV DC BUS on the board. These inputs are rated for 1200 V and 16 A. If the current ratings are exceeded, the fuse will blow.
2. Connect the two high-power outputs to the terminal screw blocks J2-1 and J3-1, labeled LOAD.
3. Optional: Connect a LaunchPad board to the LaunchPad socket J4/J5. The INA260 I^2C slave addresses are preconfigured in this board to "10000000" on U3 and "10000001" on U4.
4. Connect an external 3.3-V DC power supply to J1 to power on this reference design.
5. Begin evaluating the performance of the design through the appropriate headers and test points, as described in Section 3.1.2.
6. Connect an external 5-V DC power supply to J10 to power on the reference design board.
7. Begin evaluating the performance of the design through the appropriate headers and test points, as described in Section 3.1.2.

3.1.2 Evaluation Headers and Test Points

Table 2. Evaluation Headers and Test Points

COMPONENT DESIGNATOR	PIN NUMBER	SIGNAL
HIGH-VOLTAGE TEST POINT		
VCC_HV	1	VCC_HV
GND_HV	1	GND_HV
I2C TEST POINT		
SDA	1	High-side SDA
SCL	1	High-side SCL
Alert	1	High-side Alert
J4	5	Low-side Alert
	9	Low-side SCL
	10	Low-side SDA
LOW-VOLTAGE TEST POINT		
J1	1	GND
	2	3.3V

3.2 Testing and Results

3.2.1 Test Setup

3.2.1.1 Test Setup of Current Accuracy

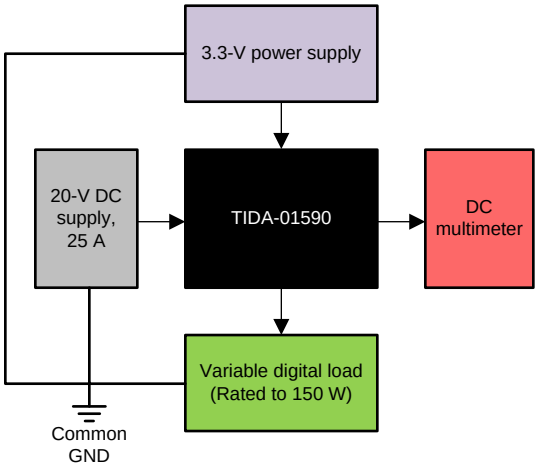


Figure 14. Test Setup of Current Sensing Accuracy

Table 3. Test Equipments

EQUIPMENT TYPE	NAME	ELECTRICAL CHARACTERISTICS
DC power supply	HP 6552A	20 V/25 A
DC power supply	GW Instek GPS-3303	30 V/3 A
Electronic load	Kikusui PLZ 152 WA	150 W
Multimeter	Fluke 8846A	1000 V/10 A
Thermometer	Fluke 52 K/J	—

An HP power supply rated at 20-V DC and 25 A is used to connect to the terminal block inputs (J2-2, J3-2). The variable digital load is connected to the output of the reference design through the terminal block outputs (J2-1, J3-1). The power supply and digital load simulate the DC bus connected to the solar inverter.

The 3.3-V external power supply is connected to the terminal block J1. The ground from the 3.3-V power supply is connected to the low-voltage side of the PCB ground plane, and it must also be connected to the ground of the load and DC power supply to create a common ground.

The DC multimeter is used to monitor the DC current corresponding to the voltage sense or current sense measurement. Table 2 calls out the header pins tested to measure the current and voltage sense accuracy. The results are described in Section 3.2.2.

3.2.1.2 INA260 EVM GUI

The INA260EVM GUI and TI SM-USB-DIG are used to interpret the data output from the board. This is a quick way to evaluate the I²C output coming from the INA260. The GUI has settings to control each of the INA registers. Each point collected during testing comes from one poll data (see Figure 15).

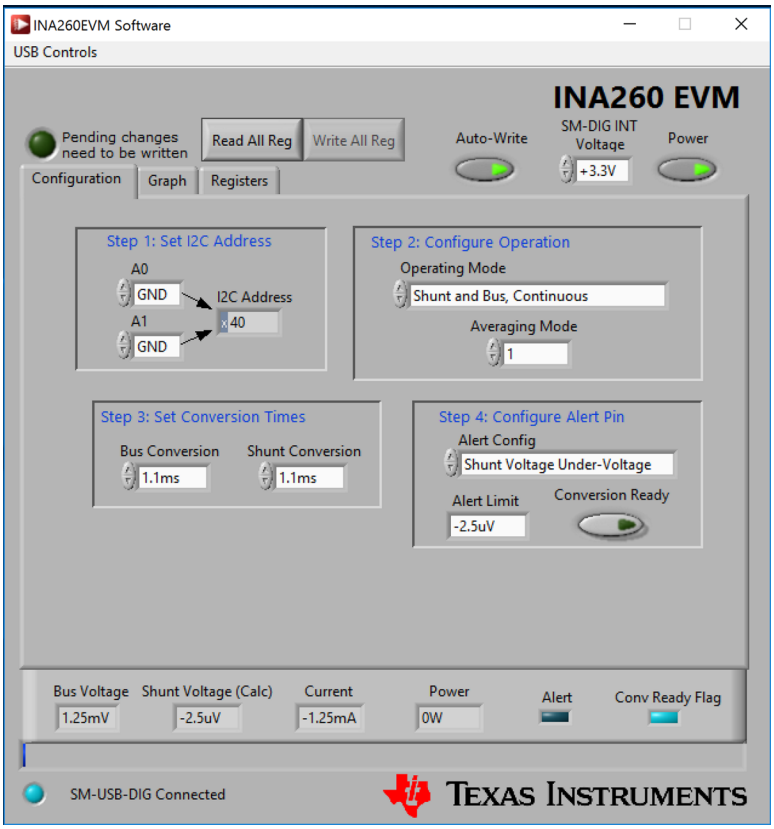


Figure 15. INA260EVM GUI

3.2.2 Test Results

3.2.2.1 Current Accuracy Results

Three separate PCBs are tested for accuracy using the full system solution. Power is supplied to only the low-voltage side of the design, so the INA260 is fully powered through the isolated supply. Measurements are read over the I²C bus using the USB-DIG tool normally provided with the INA260 EVM.

A series of nominal current set points measure across the entire range, with the actual current supplied through the DUT being measured using the Fluke 8846A multimeter. The following tables and charts of results show this measured value, a single sample from the INA260 and an average of five samples.

Table 4. Board 1, Channel 1 Test Results

NOMINAL CURRENT (A)	ACTUAL CURRENT (A)	INA CODE OUTPUT (A)	FIVE-SAMPLE AVG (A)	ERROR	AVG ERROR
0.05	0.05004	0.05125	0.04875	2.418065548%	–2.57793765%
0.1	0.10014	0.1	0.09875	–0.139804274%	–1.388056721%
0.15	0.14991	0.14975	0.15375	–0.106730705%	2.561536922%
0.2	0.20013	0.2	0.20375	–0.064957777%	1.808824264%
0.3	0.30538	0.30425	0.29875	–0.370030781%	–2.171065558%
0.5	0.49917	0.49875	0.49875	–0.084139672%	–0.084139672%
0.75	0.75042	0.74875	0.75	–0.222542043%	–0.055968658%
1	1.00173	1.00125	0.99625	–0.047917103%	–0.547053597%
1.5	1.4982	1.49875	1.50375	0.03671072%	0.370444533%
2	1.99336	1.99	2.01	–0.168559618%	0.834771441%
2.5	2.5027	2.50125	2.50625	–0.057937428%	0.141846805%
3	3.00102	3	2.99875	–0.033988444%	–0.075640949%
4	4.00345	4.00375	4.0075	0.007493537%	0.101162747%
5	5.0007	4.9975	4.99375	–0.063991041%	–0.138980543%
6	5.99888	5.99875	6.0025	–0.002167071%	0.060344598%
7	7.00928	7.00875	7.0075	–0.007561404%	–0.025394905%
8	7.99932	7.99875	8.01375	–0.007125606%	0.180390333%
9	8.99683	8.9975	9.00875	0.007447067%	0.132491111%
10	10.00419	10.0062	10.0025	0.020091582%	–0.016892922%
11	11.02325	11.0263	11.0025	0.027668791%	–0.188238496%
12	11.99947	12.0013	11.995	0.015250674%	–0.037251645%
13	13.03	13.0188	13.05565	–0.085955487%	0.196853415%
14	14.05	14.0412	13.98565	–0.062633452%	–0.458007117%
15	14.98	14.97	14.9988	–0.066755674%	0.125500668%

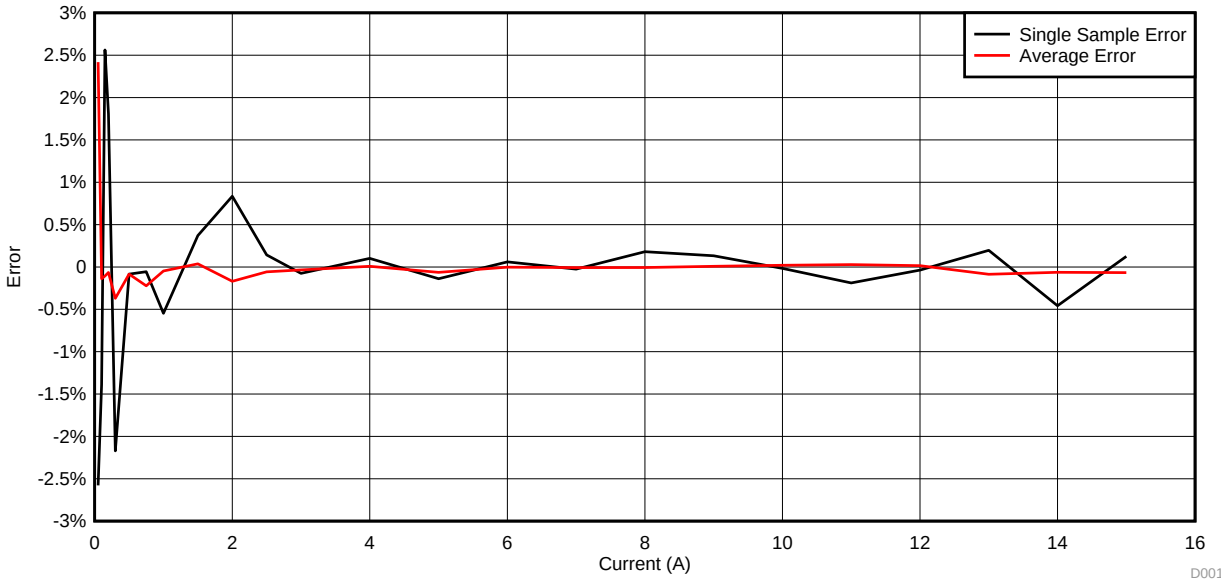


Figure 16. Board 1, Channel 1 Error Chart

Table 5. Board 1, Channel 2 Test Results

NOMINAL CURRENT (A)	ACTUAL CURRENT (A)	INA CODE OUTPUT (A)	FIVE-SAMPLE AVG (A)	ERROR	AVG ERROR
0.05	0.05015	0.0475	0.05125	–5.284147557%	2.193419741%
0.1	0.10501	0.11	0.107	4.751928388%	1.895057614%
0.15	0.15515	0.16	0.15675	3.12600709%	1.031260071%
0.2	0.1999	0.19875	0.19975	–0.575287644%	–0.075037519%
0.3	0.29997	0.2975	0.3	–0.823415675%	0.010001%
0.5	0.50083	0.49875	0.50275	–0.415310584%	0.383363616%
0.75	0.75156	0.7525	0.75325	0.125073181%	0.224865613%
1	1.00267	1.0025	1.0065	–0.016954731%	0.381980113%
1.5	1.50481	1.51	1.50775	0.34489404%	0.195373502%
2	2.00606	2.01375	2.00975	0.383338484%	0.183942654%
2.5	2.48955	2.485	2.4875	–0.182763953%	–0.082344199%
3	3.00027	3.005	3.004	0.157652478%	0.124322144%
4	4.00264	4.0125	4.0085	0.246337417%	0.146403374%
5	5.00504	5.01	5.0095	0.099100107%	0.089110177%
6	6.00234	6.005	6.002	0.04431605%	–0.005664458%
7	6.99897	7.005	7.00625	0.086155534%	0.104015305%
8	8.00402	8.01	8.01025	0.074712457%	0.077835887%
9	8.99625	8.9975	8.99925	0.013894678%	0.033347228%
10	9.99887	10.0025	10	0.036304102%	0.011301277%
11	11.01796	11.0225	11.02352	0.04120545%	0.050463062%
12	11.97164	11.9775	11.98252	0.048949016%	0.09088145%
13	13.01	13.0088	13.00654	–0.009223674%	–0.026594927%
14	13.99	13.9863	13.98802	–0.026447462%	–0.014152966%
15	14.99	14.9938	14.9883	0.025350233%	–0.011340894%

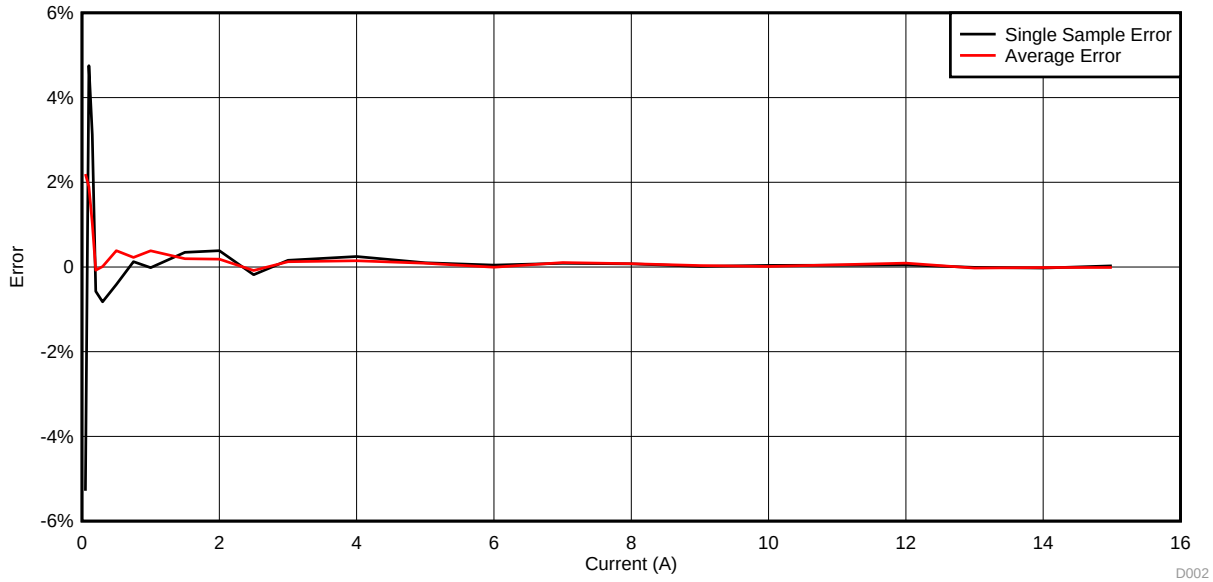


Figure 17. Board 1, Channel 2 Error Chart

Table 6. Board 2, Channel 1 Test Results

NOMINAL CURRENT (A)	ACTUAL CURRENT (A)	INA CODE OUTPUT (A)	FIVE-SAMPLE AVG (A)	ERROR	AVG ERROR
0.05	0.0506	0.05125	0.051	1.28458498%	0.790513834%
0.1	0.10731	0.10625	0.10725	–0.987792377%	–0.055912776%
0.15	0.15222	0.15125	0.15425	–0.63723558%	1.333596111%
0.2	0.20703	0.205	0.2065	–0.980534222%	–0.256001546%
0.3	0.302	0.305	0.303	0.993377483%	0.331125828%
0.5	0.50731	0.51125	0.511	0.776645444%	0.72736591%
0.75	0.74807	0.7475	0.75025	–0.076196078%	0.291416579%
1	0.99914	1	1.002	0.086074024%	0.286246172%
1.5	1.50582	1.5025	1.50475	–0.220477879%	–0.07105763%
2	2.00216	2.00125	2.001	–0.045450913%	–0.057937428%
2.5	2.50022	2.4975	2.49475	–0.108790426%	–0.218780747%
3	2.99744	2.99375	2.9955	–0.12310505%	–0.064721896%
4	4.00928	4.005	4.0075	–0.106752335%	–0.044396999%
5	5.00092	5.0025	4.998	0.031594187%	–0.058389256%
6	5.99972	6.00125	5.99975	0.02550119%	0.000500023%
7	7.01352	7.00875	7.0125	–0.068011498%	–0.014543339%
8	7.99911	8.00125	8.00175	0.026752976%	0.033003672%
9	9.00244	9.0025	9.0035	0.000666486%	0.011774586%
10	9.99924	10	10.00152	0.007600578%	0.022801733%
11	11.03127	11.0412	11.037	0.090016834%	0.051943249%
12	11.98993	11.9938	11.99352	0.032277086%	0.029941793%
13	13.002	13.01	13.01052	0.061528996%	0.06552838%
14	14.004	14.01	14.01076	0.042844901%	0.048271922%
15	14.992	14.99	14.99052	–0.013340448%	–0.009871932%

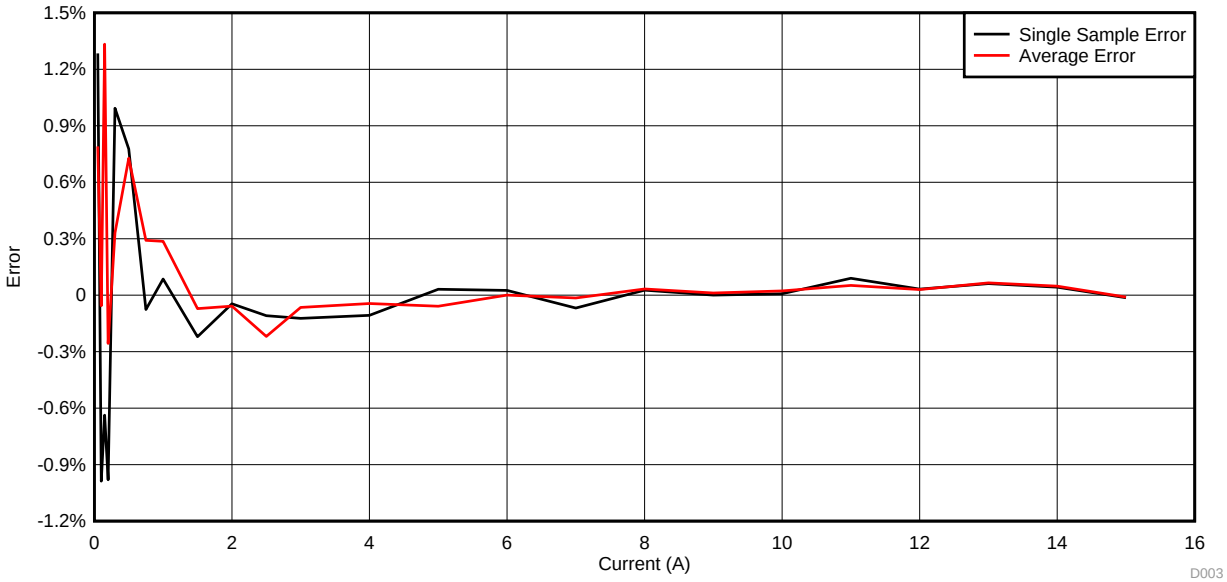


Figure 18. Board 2, Channel 1 Error Chart

Table 7. Board 2, Channel 2 Test Results

NOMINAL CURRENT (A)	ACTUAL CURRENT (A)	INA CODE OUTPUT (A)	FIVE-SAMPLE AVG (A)	ERROR	AVG ERROR
0.05	0.05154	0.05125	0.0515	–0.562669771%	–0.077609624%
0.1	0.10442	0.10375	0.102	–0.641639533%	–2.317563685%
0.15	0.15385	0.1525	0.15175	–0.877478063%	–1.364965876%
0.2	0.20897	0.2075	0.20775	–0.703450256%	–0.583815859%
0.3	0.2995	0.3	0.2985	0.166944908%	–0.333889816%
0.5	0.50002	0.49875	0.49925	–0.25398984%	–0.15399384%
0.75	0.75558	0.755	0.75425	–0.076762222%	–0.176023717%
1	1.00664	1.005	1.006	–0.162918223%	–0.063577843%
1.5	1.50874	1.5075	1.50725	–0.082187786%	–0.098757904%
2	2.00057	1.99875	1.999	–0.090974072%	–0.078477634%
2.5	2.50141	2.50125	2.49975	–0.006396392%	–0.066362572%
3	3.00374	3.0025	3.00225	–0.041281869%	–0.049604826%
4	4.00186	4.00125	4.001	–0.015242912%	–0.021490007%
5	5.00577	5.005	5.005	–0.015382249%	–0.015382249%
6	6.00528	6.00625	6.0055	0.016152453%	0.003663443%
7	7.00199	7.00125	7.002	–0.010568424%	0.000142817%
8	8.00325	8.0025	8.00375	–0.009371193%	0.006247462%
9	9.00578	9.005	9.00675	–0.008661104%	0.01077086%
10	10.00345	10.0038	10.00452	0.003498793%	0.01069631%
11	11.01681	11.02	11.01926	0.02895575%	0.022238742%
12	11.97222	11.9738	11.9743	0.013197218%	0.017373553%
13	13.05	13.045	13.04552	–0.038314176%	–0.034329502%
14	13.99	13.9813	13.98154	–0.062187277%	–0.060471766%
15	14.97	14.955	14.95526	–0.100200401%	–0.098463594%

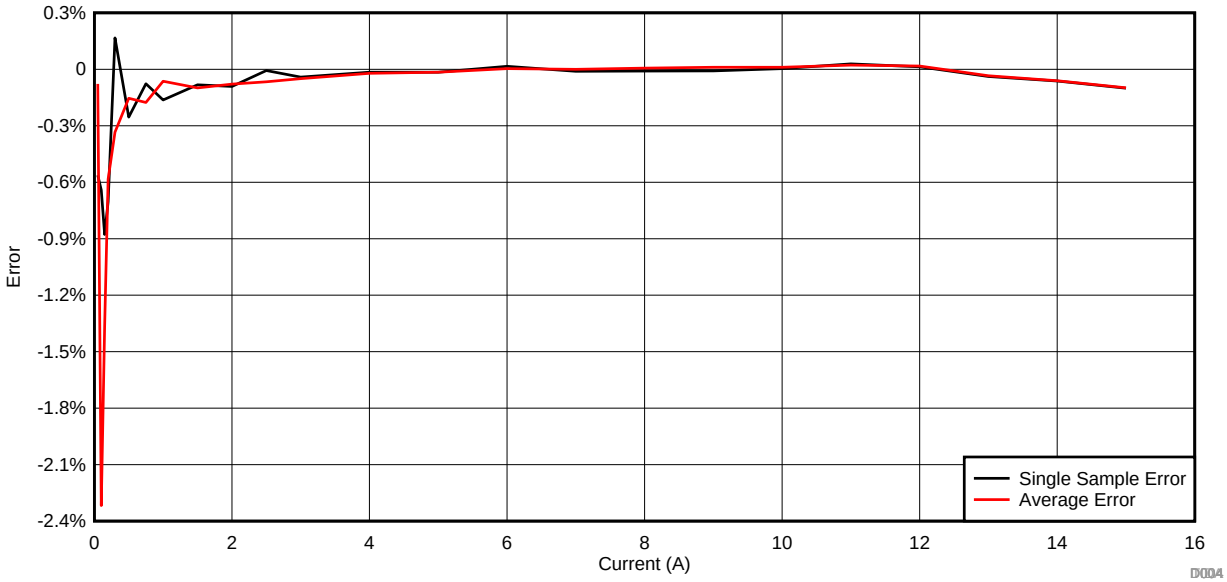


Figure 19. Board 2, Channel 2 Error Chart

Table 8. Board 3, Channel 1 Test Results

NOMINAL CURRENT (A)	ACTUAL CURRENT (A)	INA CODE OUTPUT (A)	FIVE-SAMPLE AVG (A)	ERROR	AVG ERROR
0.05	0.05071	0.05	0.04975	–1.40011832%	–1.893117728%
0.1	0.10164	0.10125	0.10075	–0.383707202%	–0.875639512%
0.15	0.15136	0.15	0.14925	–0.898520085%	–1.394027484%
0.2	0.20693	0.20625	0.2055	–0.328613541%	–0.691054946%
0.3	0.29631	0.295	0.295	–0.442104553%	–0.442104553%
0.5	0.50167	0.50125	0.501	–0.083720374%	–0.13355393%
0.75	0.75772	0.75625	0.75725	–0.194003062%	–0.06202819%
1	1.00887	1.00875	1.00825	–0.011894496%	–0.061454895%
1.5	1.50544	1.50375	1.50475	–0.112259539%	–0.045833776%
2	2.00166	2.00125	2.001	–0.020482999%	–0.032972633%
2.5	2.49807	2.5	2.4975	0.077259644%	–0.022817615%
3	2.9882	2.9875	2.988	–0.023425474%	–0.006692992%
4	4.00374	4.005	4.00425	0.031470575%	0.01273809%
5	5.00164	5.0025	5.00225	0.01719436%	0.012196%
6	6.00355	6.00625	6.00475	0.044973391%	0.019988174%
7	7.00965	7.01125	7.012	0.022825676%	0.033525212%
8	8.02024	8.02125	8.023	0.012593139%	0.034412935%
9	8.99657	9.00125	9.00125	0.052019825%	0.052019825%
10	9.99046	9.995	9.9955	0.045443353%	0.050448128%
11	11.03957	11.04	11.04098	0.003895079%	0.012772237%
12	11.94093	11.9463	11.94728	0.044971372%	0.053178438%
13	12.97	12.9712	12.97046	0.00925212%	0.003546646%
14	13.99	13.985	13.98626	–0.035739814%	–0.026733381%
15	15.01	15.0062	15.007	–0.025316456%	–0.019986676%

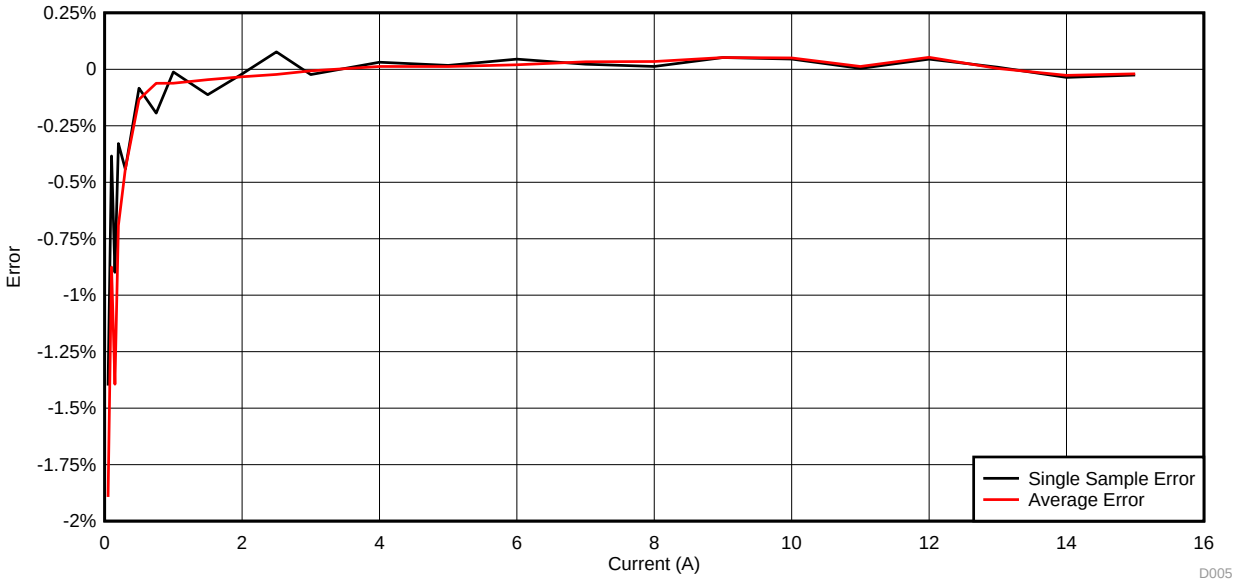


Figure 20. Board 3, Channel 1 Error Chart

Table 9. Board 3, Channel 2 Test Results

NOMINAL CURRENT (A)	ACTUAL CURRENT (A)	INA CODE OUTPUT (A)	FIVE-SAMPLE AVG (A)	ERROR	AVG ERROR
0.05	0.04981	0.0475	0.0515	–4.637622967%	3.392892993%
0.1	0.10408	0.1025	0.10475	–1.518063028%	0.643735588%
0.15	0.14401	0.145	0.146	0.68745226%	1.381848483%
0.2	0.19889	0.195	0.1985	–1.955854995%	–0.19608829%
0.3	0.29405	0.29625	0.2935	0.74817208%	–0.18704302%
0.5	0.49445	0.495	0.495	0.111234705%	0.111234705%
0.75	0.75062	0.7525	0.7505	0.25045962%	–0.015986784%
1	1.00683	1.00125	1.0085	–0.554214714%	0.165867128%
1.5	1.50365	1.5075	1.50375	0.256043627%	0.006650484%
2	2.01541	2.02	2.01525	0.227745223%	–0.007938831%
2.5	2.5154	2.51375	2.514	–0.065595929%	–0.055657152%
3	2.98788	2.9875	2.9895	–0.012718048%	0.054219045%
4	3.9982	4.00625	3.99975	0.201340603%	0.038767445%
5	5.01453	5.01625	5.01625	0.034300323%	0.034300323%
6	6.00705	6.00875	6.00425	0.028300081%	–0.046611898%
7	7.00758	7.01125	7.0115	0.05237186%	0.055939426%
8	7.9984	7.995	7.9995	–0.042508502%	0.013752751%
9	9.04578	9.05	9.0465	0.046651588%	0.007959513%
10	9.98972	9.99125	9.99225	0.015315745%	0.025326035%
11	11.02587	11.0325	11.029	0.060131309%	0.028387783%
12	11.98699	11.9938	11.99052	0.056811593%	0.029448594%
13	13.04	13.0425	13.03878	0.019171779%	–0.009355828%
14	13.98	13.9725	13.97352	–0.053648069%	–0.046351931%
15	15.01	15.0088	15.00804	–0.00799467%	–0.013057961%

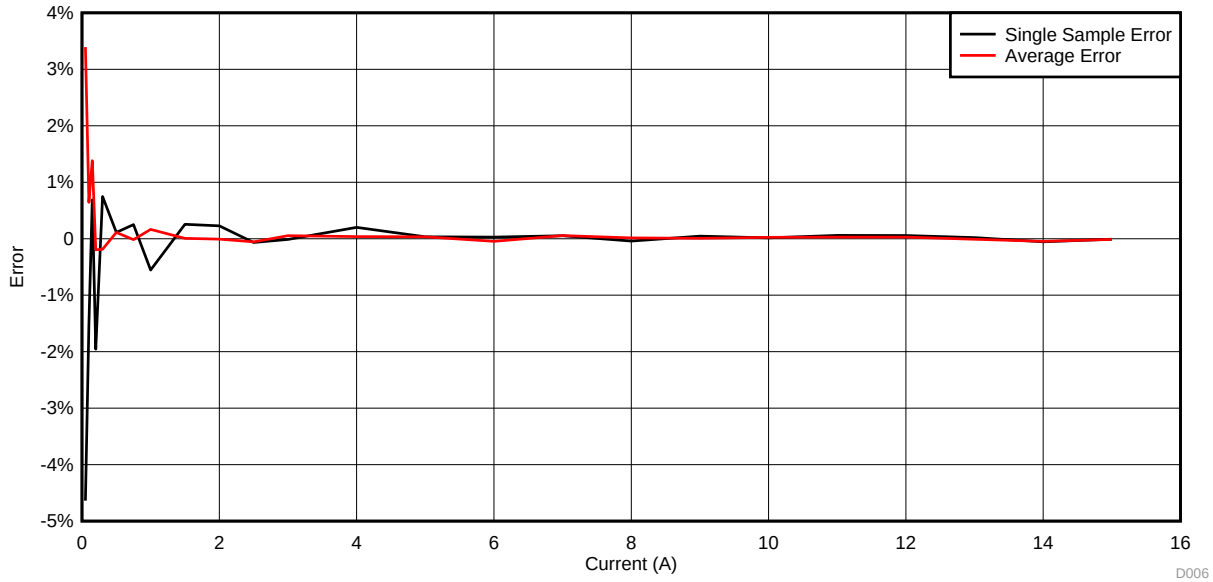


Figure 21. Board 3, Channel 2 Error Chart

3.2.2.2 I²C Bus Data Integrity

Figure 22 and Figure 23 showcase the SDA (blue) and SCL (purple) signals measured on test points located at the high side and low side of the reference design board.

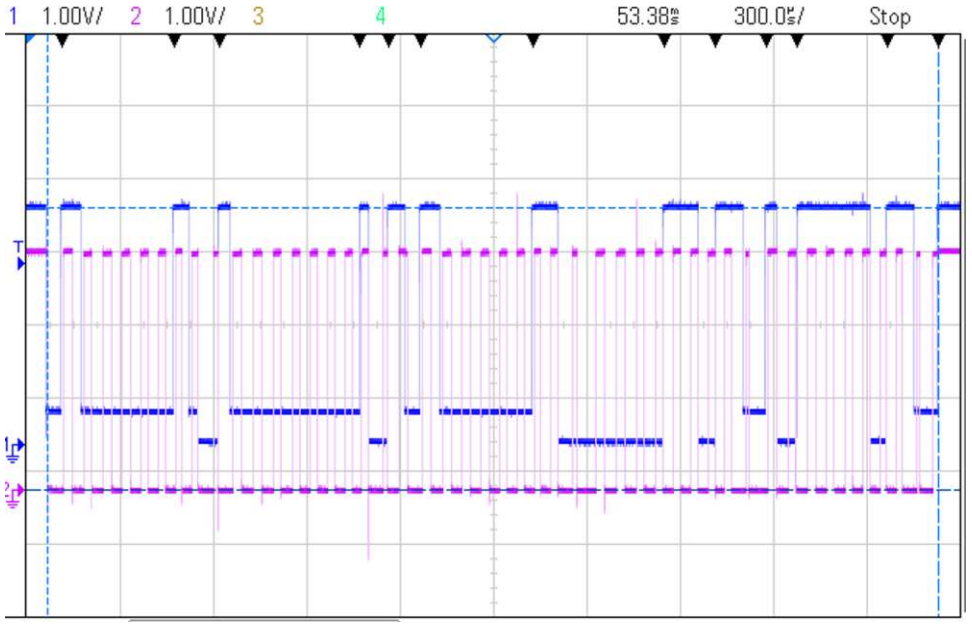


Figure 22. High-Side SDA (Blue) and SCL (Purple) Signals

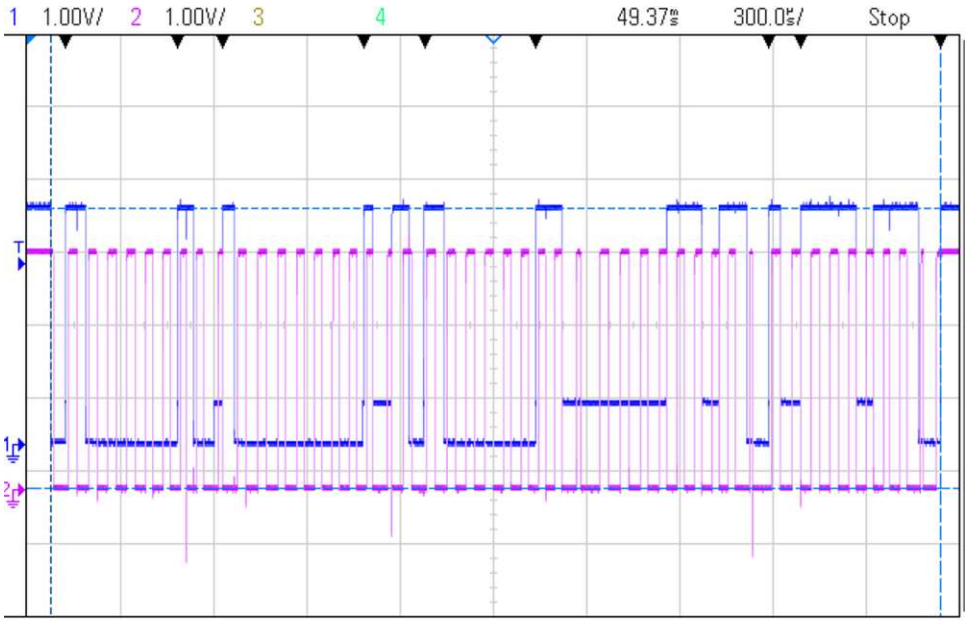


Figure 23. Low-Side SDA (Blue) and SCL (Purple) Signal

3.2.2.2.1 Extended Current Soak Temperature Rise

This reference design is set up to run at 10 V and 15 A (maximum permissible current limit) for an extended period of 10 minutes, and the temperature rise of the INA260 package is recorded using a thermometer.

The peak temperature recorded during this test is 62.2ºC at an ambient temperature of 21.8ºC.

4 Design Files

4.1 Schematics

To download the schematics for each board, see the design files at TIDA-01590.

4.2 Bill of Materials

To download the bill of materials for each board, see the design files at TIDA-01590.

4.3 PCB Layout Recommendations

High-voltage PCB layouts require special consideration. The PCB trace spacing used in this design meet the requirements specified in Table 6-1 of the IPC-2221 standard for external conductors with conformal coating over assembly. The IPC-2221 "Generic Standard on Printed Board Design" specifies spacing requirements for various types of PCB construction, coating, and applications. Consequently, there must be sufficient spacing between the components within the high-voltage portion of the board, which is physically separated from the low-voltage portion of the board by the isolation boundary. The slot through the isolation region serves to increase the creepage rating of the board to be > 11.5 mm.

Another consideration of this layout is the heat production around the INA260 and its internal shunt resistor. Wide 2-oz copper pours connect the high-voltage DC bus terminals (J2-1, J2-2, J3-1, J3-2) to the device IN+ and IN- pins. Many vias are also placed near component inputs and outputs to further facilitate heat dissipation. This ensures heat produced from the 15 A current does not affect the board.

4.3.1 Layout Prints

To download the layout prints for each board see the design files at TIDA-01590.

4.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-01590.

4.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-01590.

4.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-01590.

5 Related Documentation

1. Texas Instruments, *Integrated-Resistor Current Sensors Simplify PCB Design* , TI TechNotes
2. Texas Instruments, *Designing an isolated I²C Bus® interface by using digital isolators* , Analog Applications Journal

5.1 Trademarks

6 About the Authors

BEN GENEREAUX is a systems engineering intern in the Texas Instruments Grid Infrastructure team, focusing on renewable energy. Ben is studying for a bachelor of science in electrical engineering from the University of Miami.

BART BASILE is a systems architect in the Texas Instruments Grid Infrastructure Solutions Team, focusing on renewable energy and EV infrastructure. Bart works across multiple product families and technologies to leverage the best solutions possible for system level application design. Bart received his bachelors of science in electronic engineering from Texas A&M University.

STANI BELL NGOUFACK TCHOUFACK is a applications engineer in the Texas Instruments Grid Infrastructure Solutions Team, focusing on renewable energy. Stani received his bachelor of science in electronics and communication engineering from the Mannheim University of Applied Sciences.

7 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is **intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments**. If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
    1. Keep work area clean and orderly.
    2. Qualified observer(s) must be present anytime circuits are energized.
    3. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
    4. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
    5. Use stable and nonconductive work surface.
    6. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
    1. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
    2. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
    3. After EVM readiness is complete, energize the EVM as intended.

    WARNING: WHILE THE EVM IS ENERGIZED, NEVER TOUCH THE EVM OR ITS ELECTRICAL CIRCUITS AS THEY COULD BE AT HIGH VOLTAGES CAPABLE OF CAUSING ELECTRICAL SHOCK HAZARD.
3. Personal Safety
    1. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265