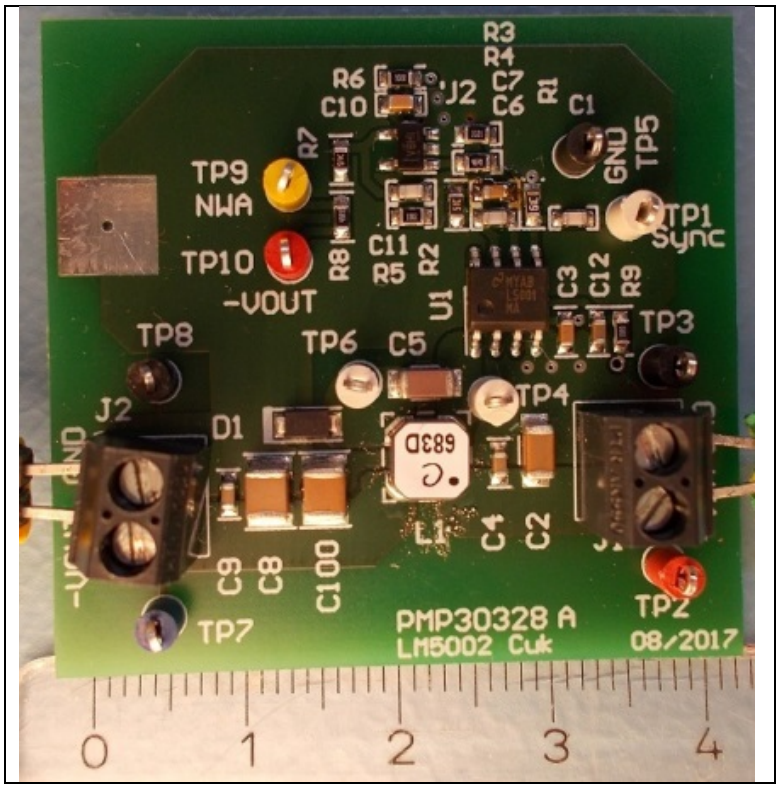
PMP30373RevA Test Results

Topology: **Transission Mode Cuk Converter (= inverting SEPIC)**

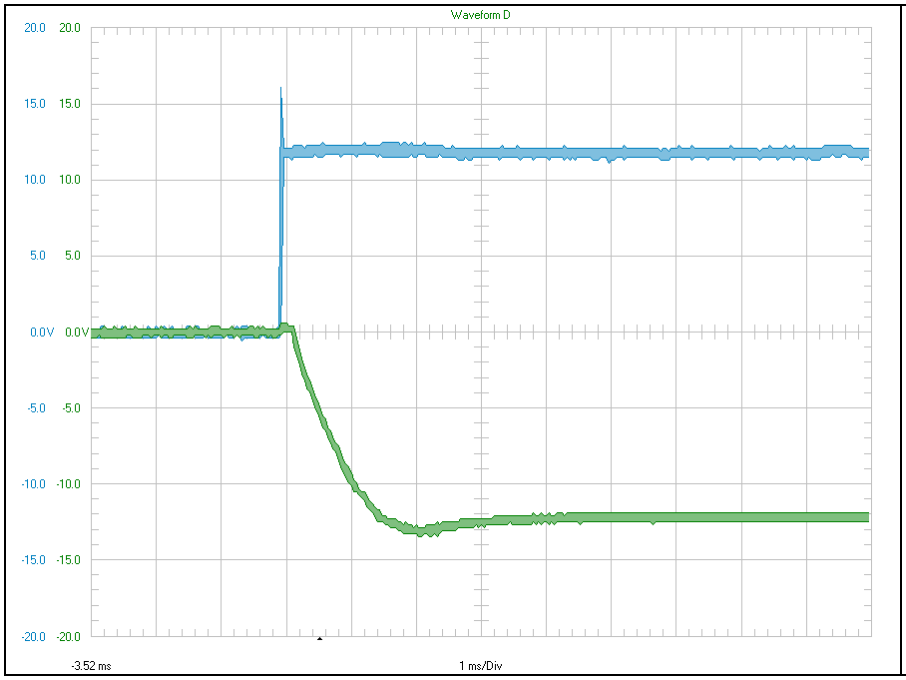
Device: **LM5001 at switching frequency 300kHz**

Unless otherwise mentioned circuit was measured with a resistive load at 200mA output current (with resistive load). This supply is dedicated for sensitive RF or instrumentation circuits.



1 Startup @ Vin 12V / 36V / 60V

The startup waveform is shown in the Figure 1. The input voltage was set to 12V.



Ch1=> input voltage
5V/div

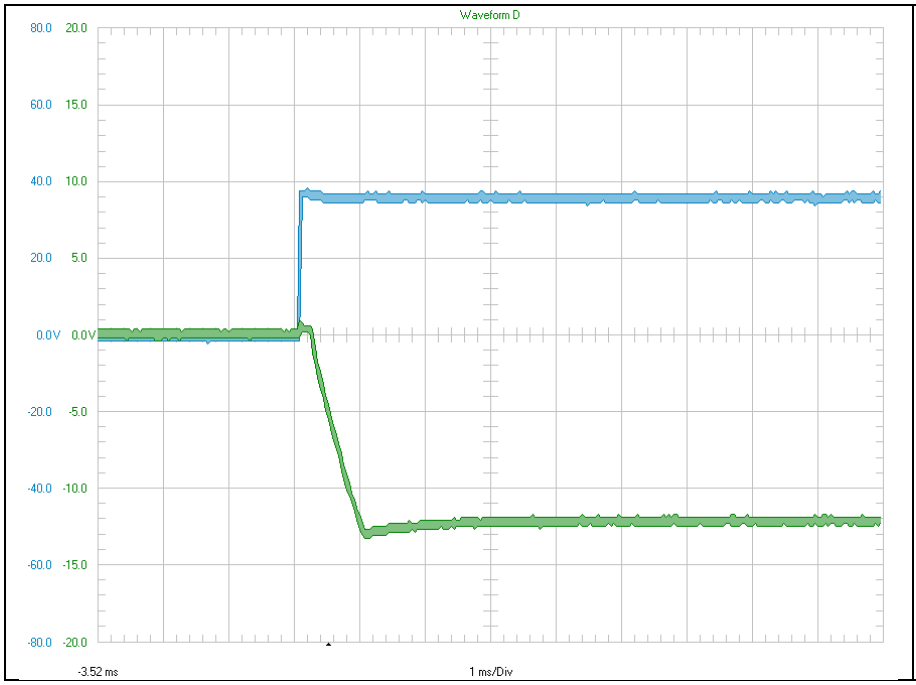
Ch2=> output voltage
5V/div

1ms/div

20MHz bw

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set to 36V.



Ch1=> input voltage
20V/div

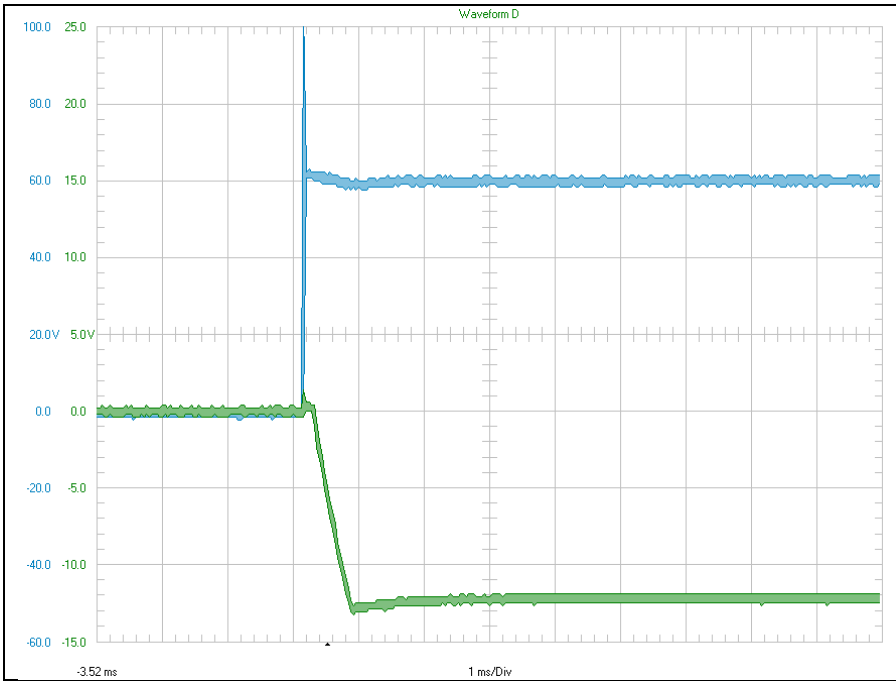
Ch2=> output voltage
5V/div

1ms/div

20MHz bw

Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set to 60V.



Ch1=> input voltage
20V/div

Ch2=> output voltage
5V/div

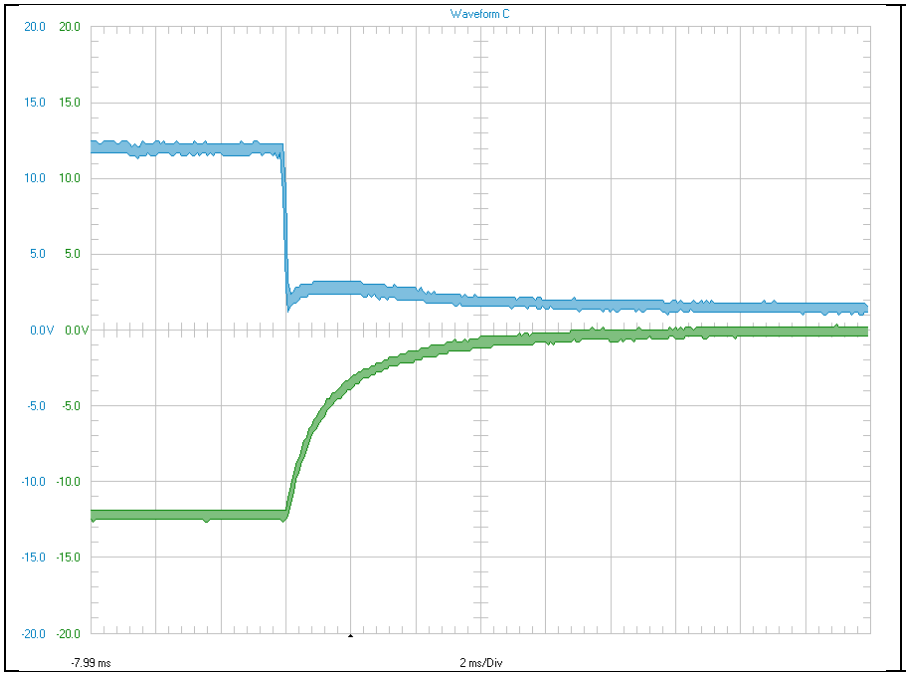
1ms/div

20MHz bw

Figure 3

2 Shutdown @ Vin 12V / 36V / 60V

The shutdown waveform is shown in the Figure 4. The input voltage was set to 12V. The power supply was disconnected.



Ch1=> input voltage
5V/div

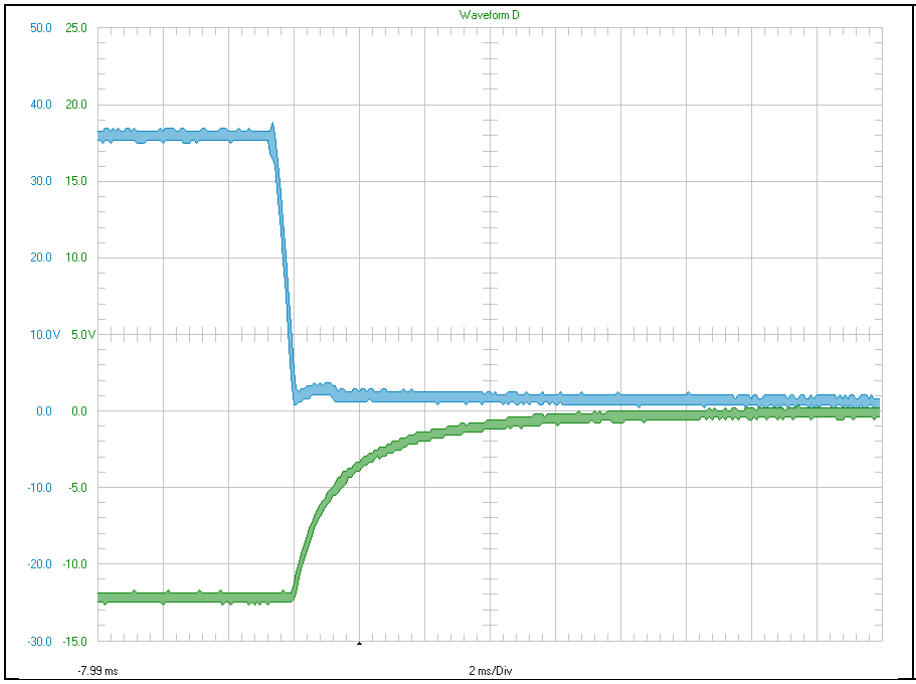
Ch2=> output voltage
5V/div

2ms/div

20MHz bw

Figure 4

The shutdown waveform is shown in the Figure 5. The input voltage was set to 36V. The power supply was disconnected.



Ch1=> input voltage
10V/div

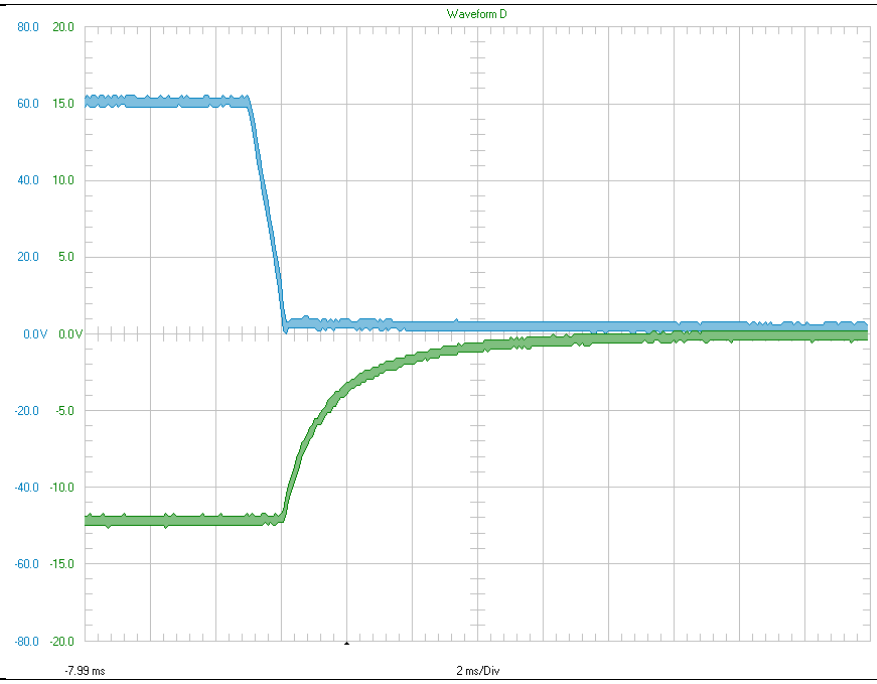
Ch2=> output voltage
5V/div

2ms/div

20MHz bw

Figure 5

The shutdown waveform is shown in the Figure 6. The input voltage was set to 60V. The power supply was disconnected.



Ch1=> input voltage 20V/div

Ch2=> output voltage 5V/div

2ms/div

20MHz bw

Figure 6

3 Efficiency up to 220mA load current

The efficiency is shown in the Figure 7 below. The input voltage was set to 6V / 12V / 36V / 60V. **Maximum load current at 6V input is 140mA** due to max. switch current and max. duty.

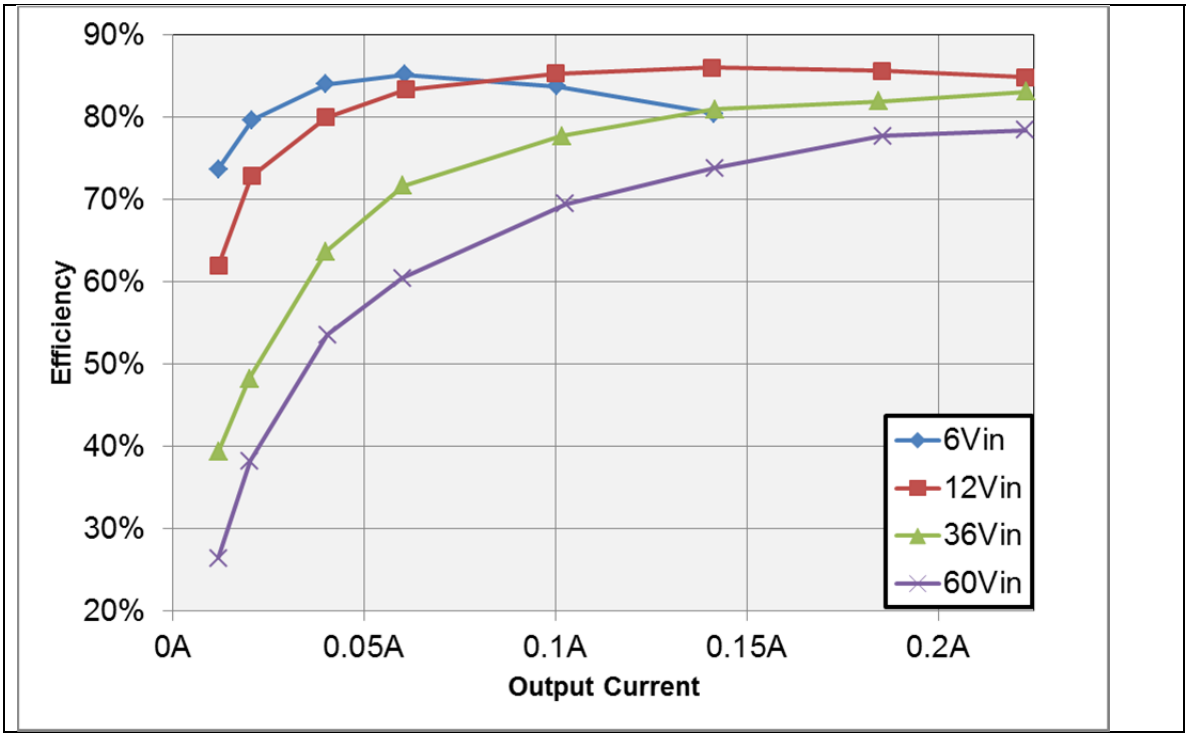


Figure 7

Figure 8 show the losses (Pin - Pout) with input voltage 6V / 12V / 36V / 60V

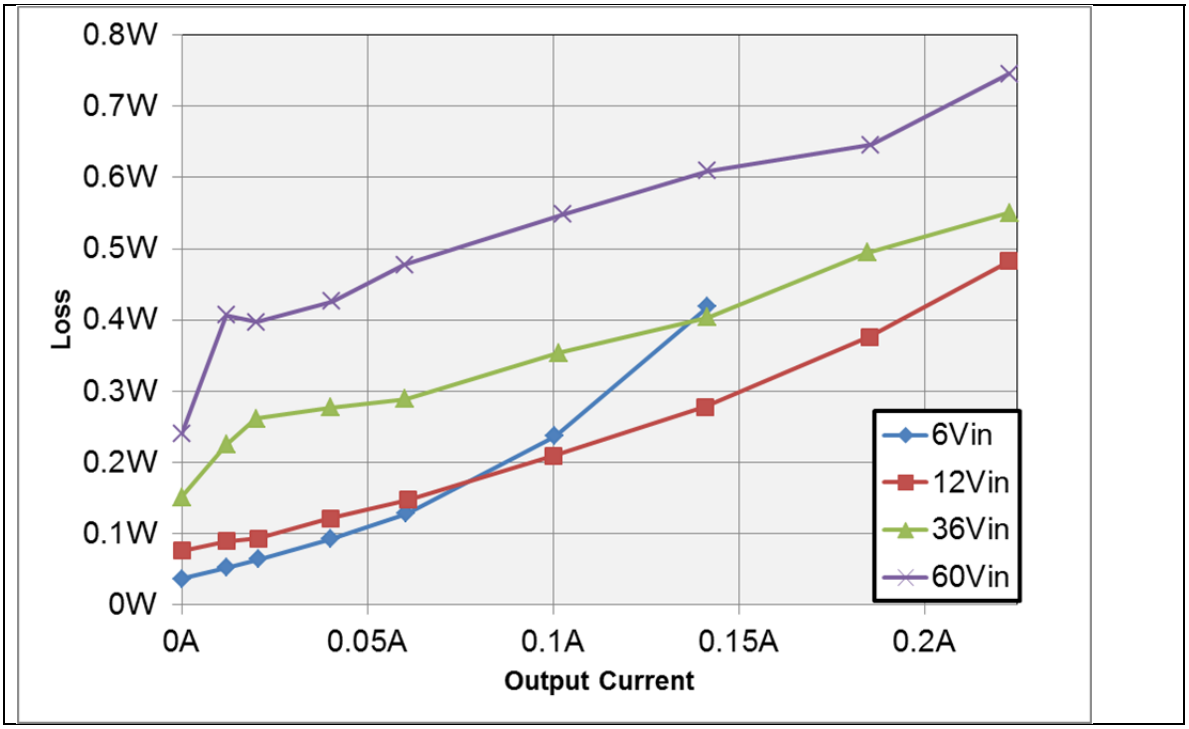


Figure 8

4 Load Regulation

The load regulation of the output is shown in the Figure 9 below.
The input voltage was set to 6V / 12V / 36V / 60V.

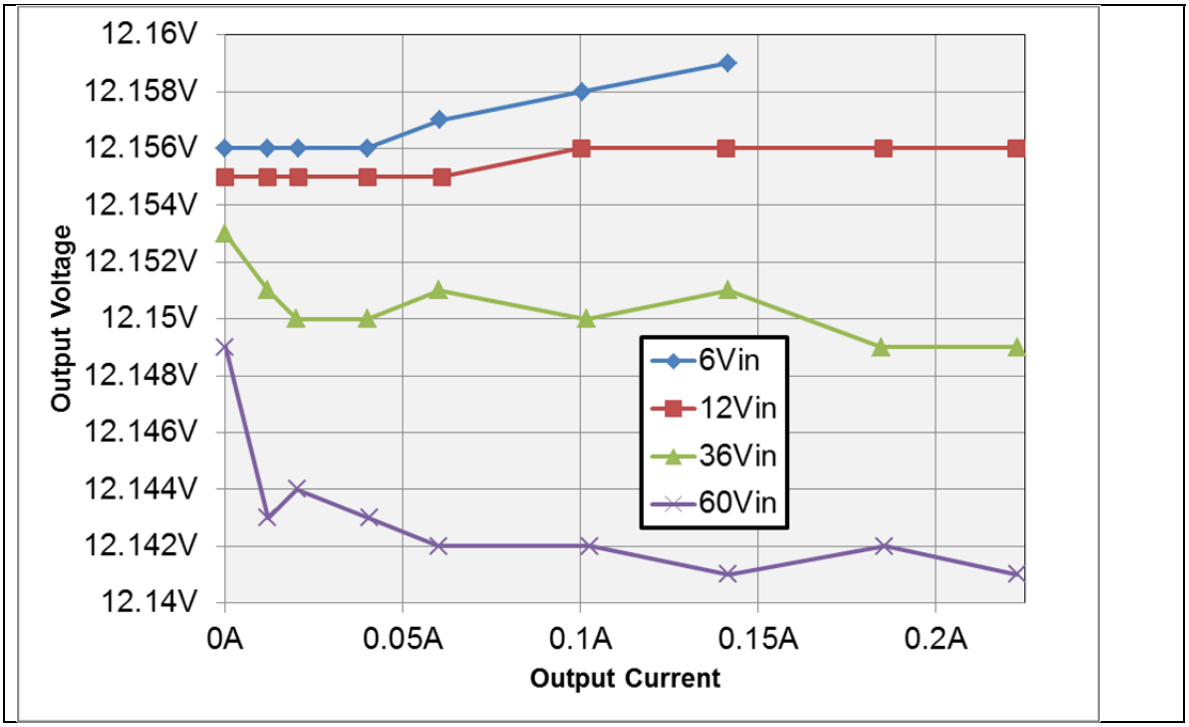


Figure 9

The deviation for load regulation is less than 20mV, means less than 0.2%

5 Line Regulation

The line regulation is shown in Figure 10. The output current was set to full load 200mA.

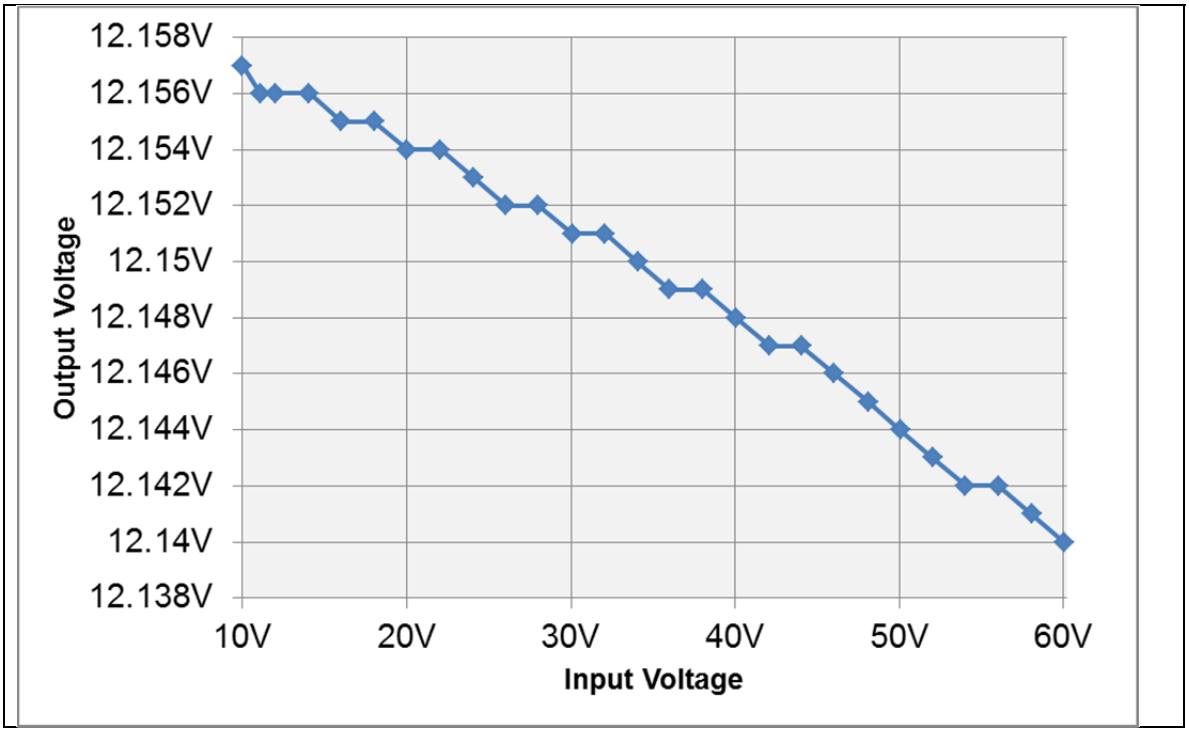


Figure 10

The deviation for line regulation is less than 20mV, means less than 0.2%

With the same setup full load efficiencies and losses were calculated - this is shown in Figure 11:

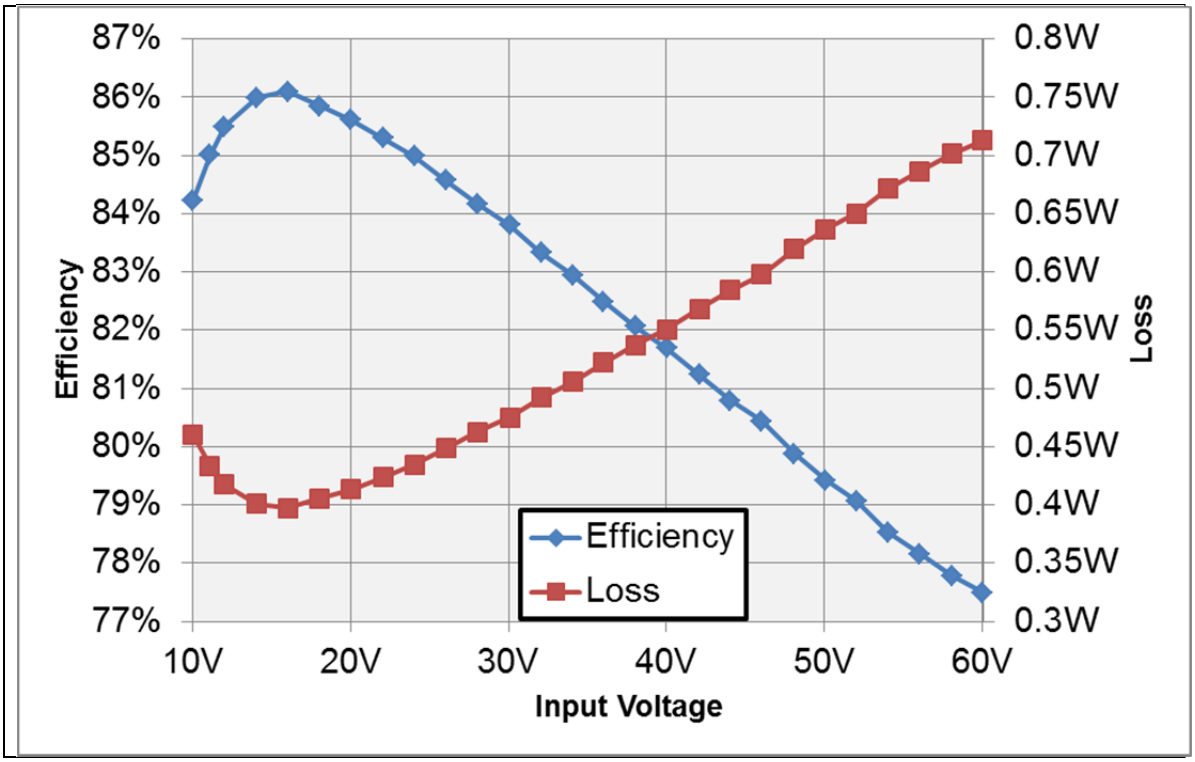
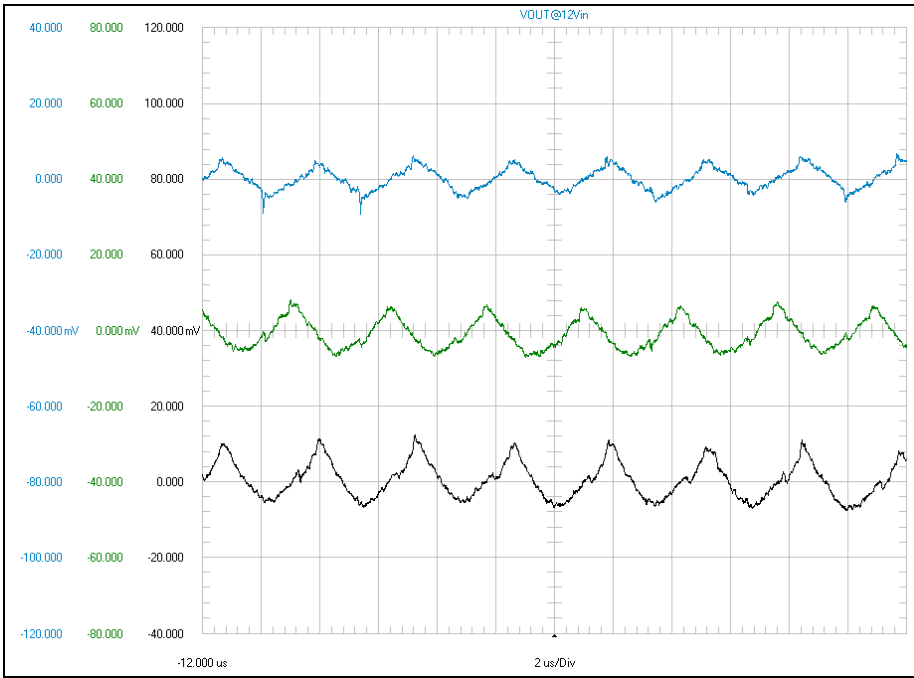


Figure 11

6 Output Ripple Voltage

The output ripple voltage is shown in Figure 12.



Ch1 => output ripple with 12V Vin

Ch2 => output ripple with 36V Vin

Ch3 => output ripple with 60V Vin

20mV/div

AC coupled

20MHz BW

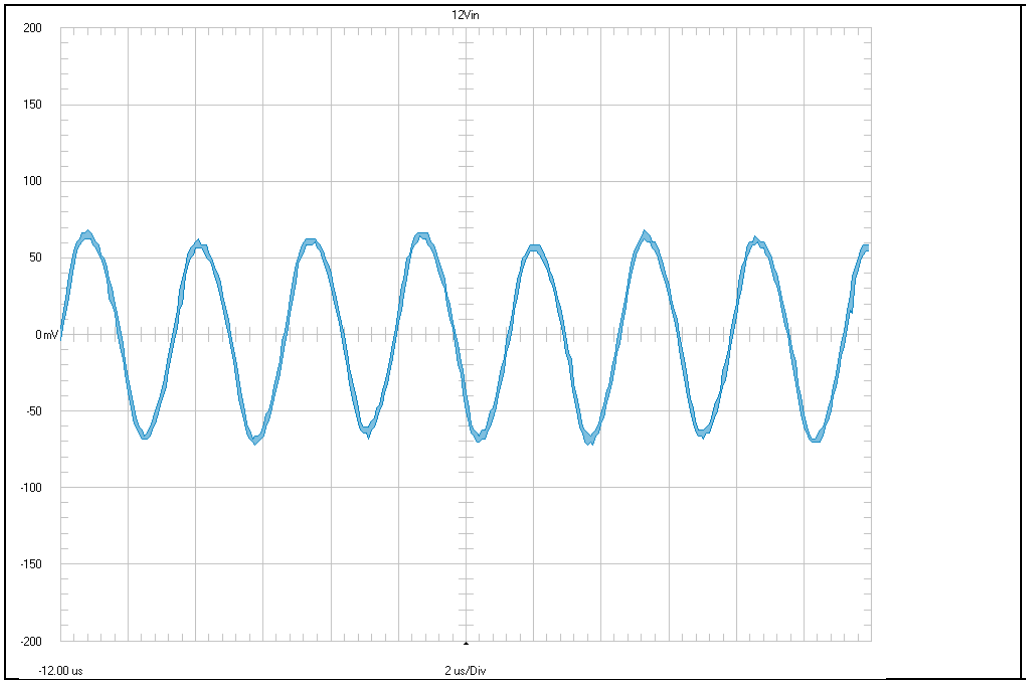
2µs/div

Figure 12

The maximum output ripple is around 20mVpp at 60V input voltage, again less than 0.2% !
Cuk topology provides continuous currents at input AND output, the power stage itself works w/ a filter second order to input and output - this results in low output ripple and low reflected ripple. That's the major benefit compared to inverting Buck Boost, far lower conducted emissions.

7 Input Ripple Voltage

The input ripple voltage at 12V is shown in Figure 13.



Ch1 => input ripple 50mV/div

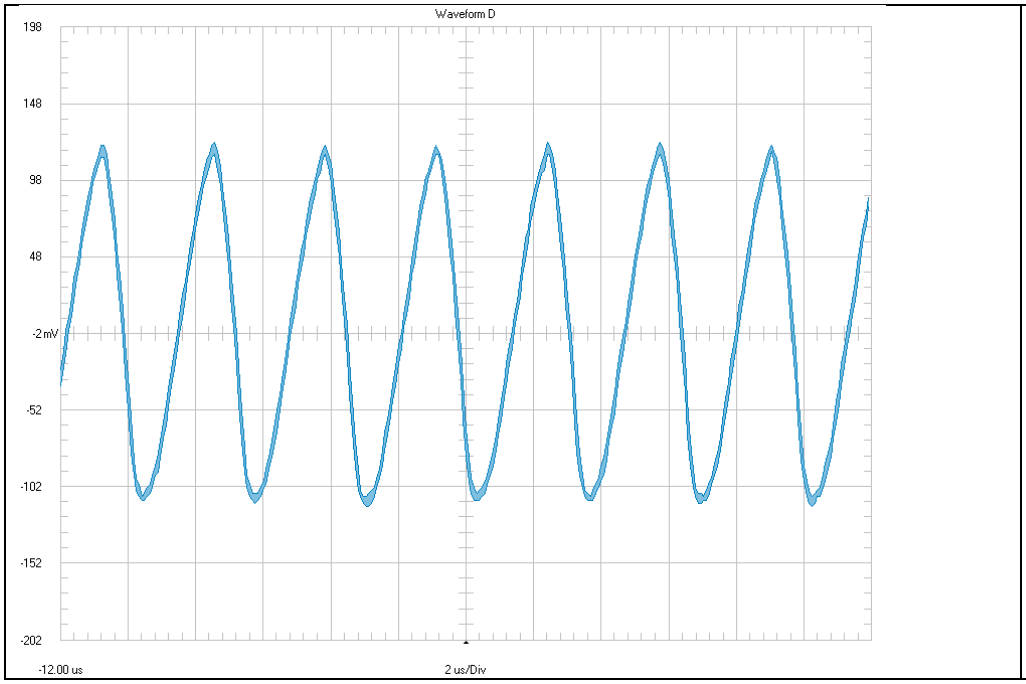
AC coupled

20MHz bw

2µs/div

Figure 13

The input ripple voltage at 36V is shown in Figure 14



Ch1 => input ripple 50mV/div

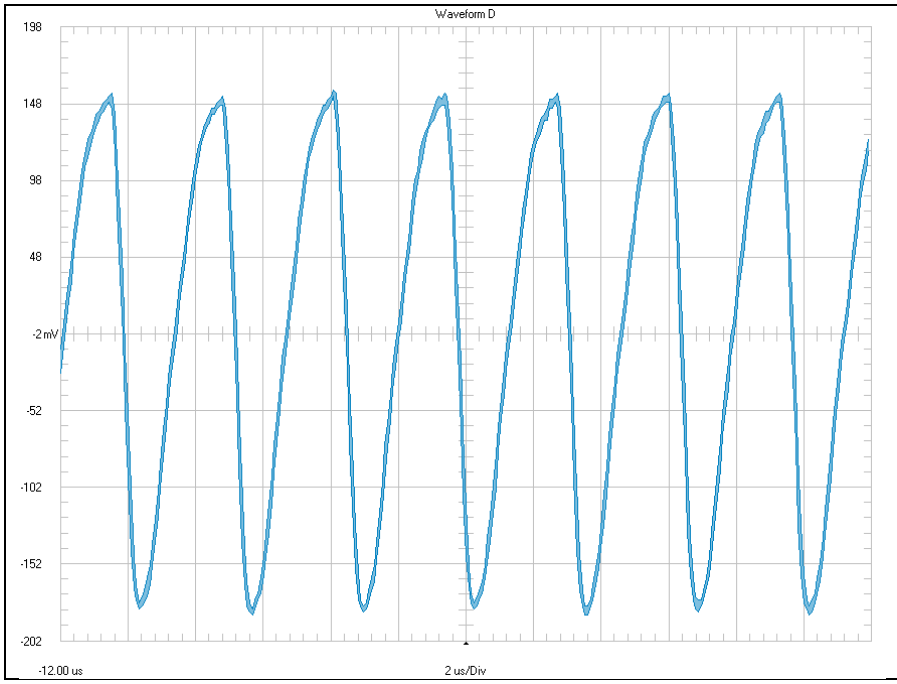
AC coupled

20MHz bw

2µs/div

Figure 14

The input ripple voltage at 60V is shown in Figure 15.



Ch1 => input ripple 50mV/div

AC coupled

20MHz bw

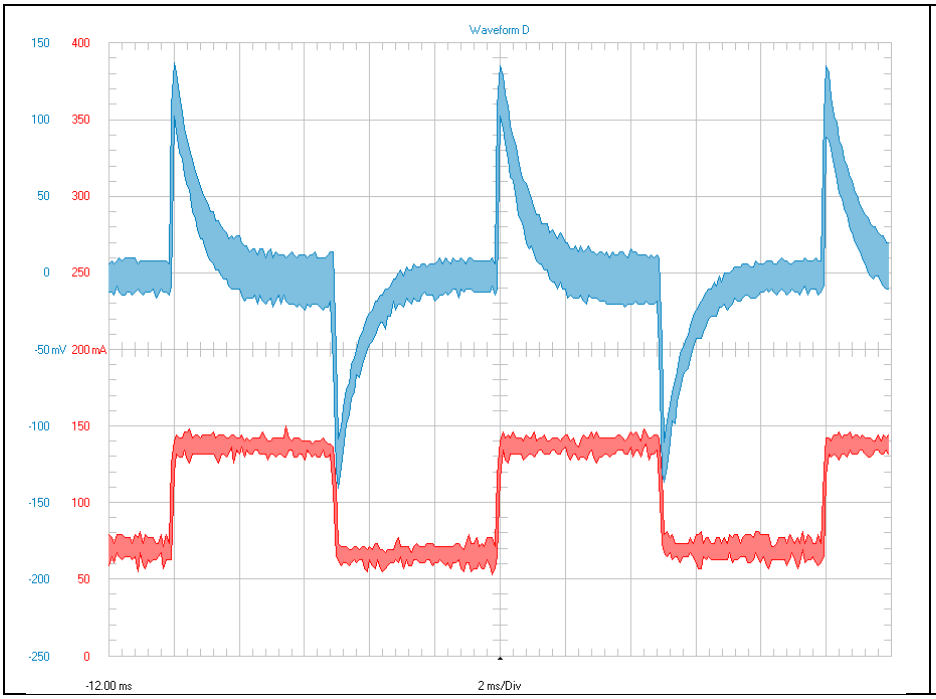
2µs/div

Figure 15

The reflected ripple to input is related to power source impedance, here around 350mVpp almost sinusoidal – means the RF content is far lower than at inverting Buck Boost topology.

8 Load Transients

The Figure 16 shows the response to load transients at 6V input voltage.
The electronic load is switching from 0.070A to 0.14A (100Hz) (electronic load).



Ch1 => output voltage (-VOUT) 50mV/div
AC coupling

20MHz bw

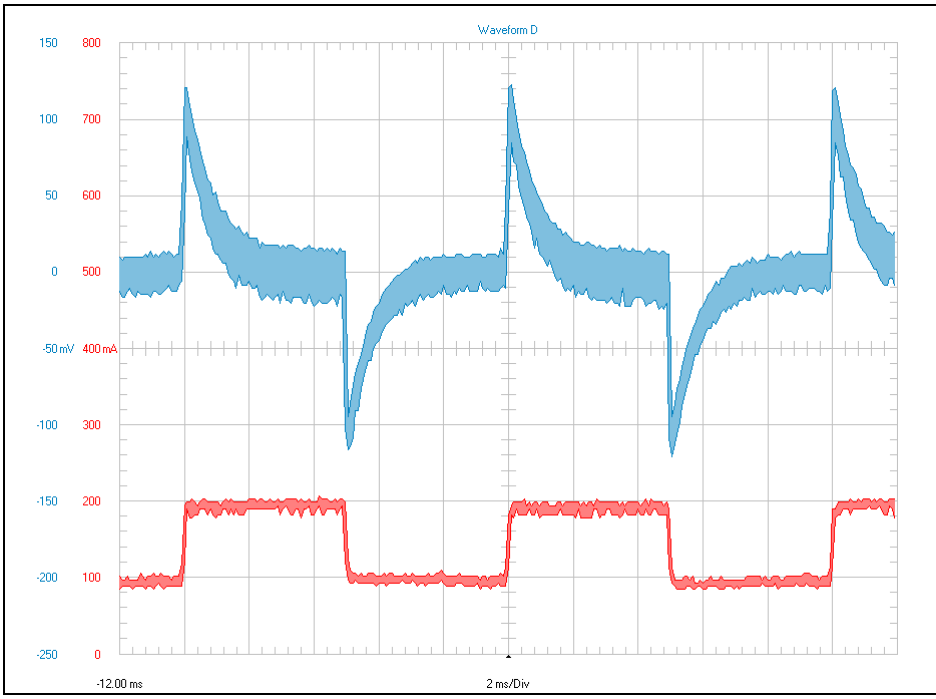
Ch2 => output current 50mA/div

10kHz bw

2ms/div

Figure 16

The Figure 17 shows the response to load transients at 12V input voltage.
The load is switching from 0.1A to 0.2A (100Hz).



Ch1 => output voltage 50mV/div
AC coupling

20MHz bw

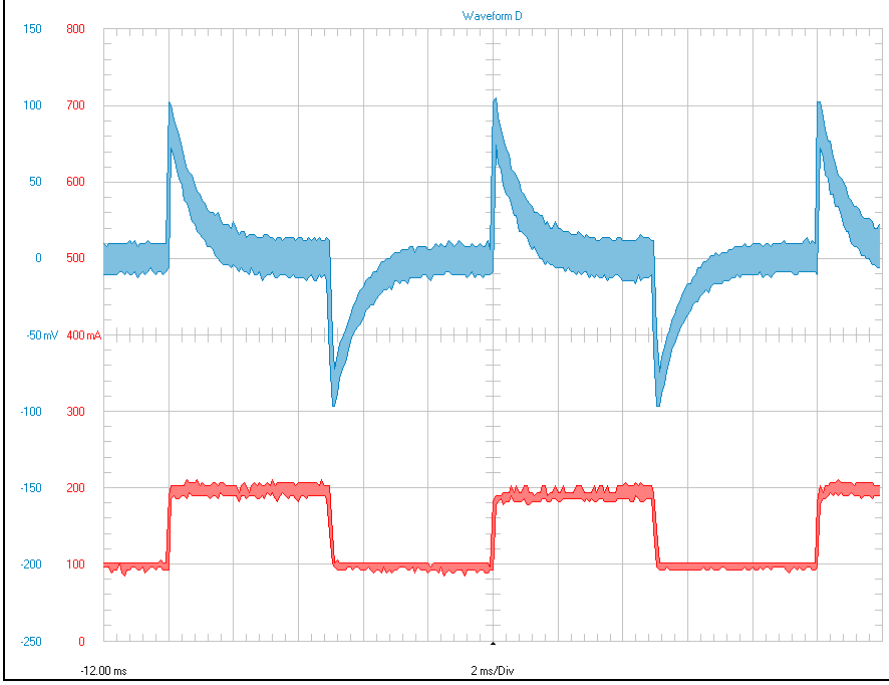
Ch2 => output current 100mA/div

10kHz bw

2ms/div

Figure 17

The Figure 18 shows the response to load transients at 36V input voltage.
The load is switching from 0.1A to 0.2A (100Hz).



Ch1 => output voltage
50mV/div
AC coupling

20MHz bw

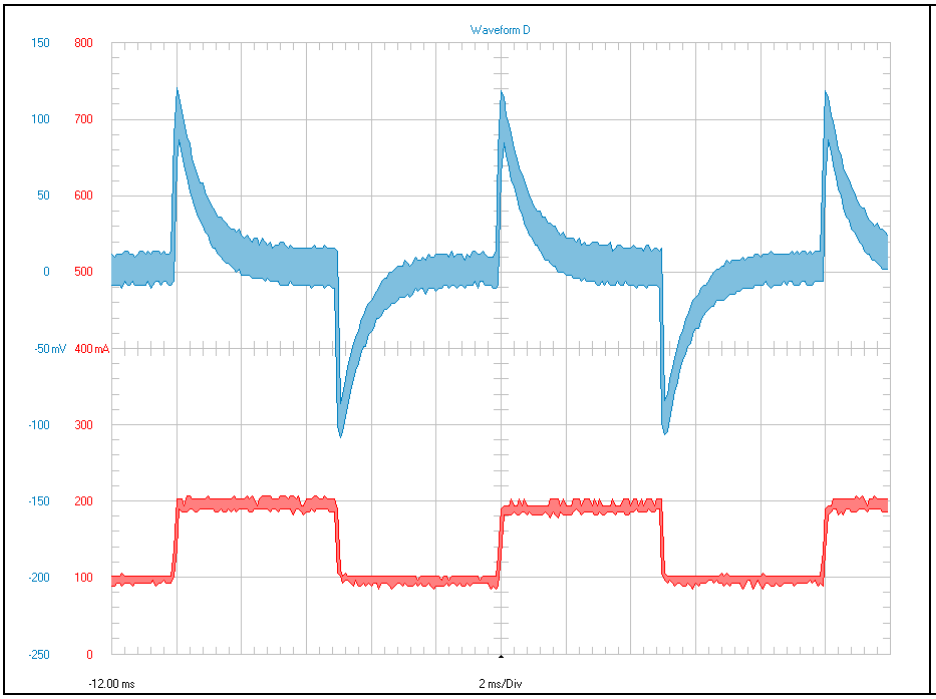
Ch2 => output current
100mA/div

10kHz bw

2ms/div

Figure 18

The Figure 19 shows the response to load transients at 60V input voltage.
The electronic load is switching from 0.1A to 0.2A (100Hz).



Ch1 => output voltage
50mV/div
AC coupling

20MHz bw

Ch2 => output current 100mA/div

10kHz bw

2ms/div

Figure 19

9 Control Loop Frequency Response

Figure 20 shows the loop response for 6Vin. Load is 0.14A.

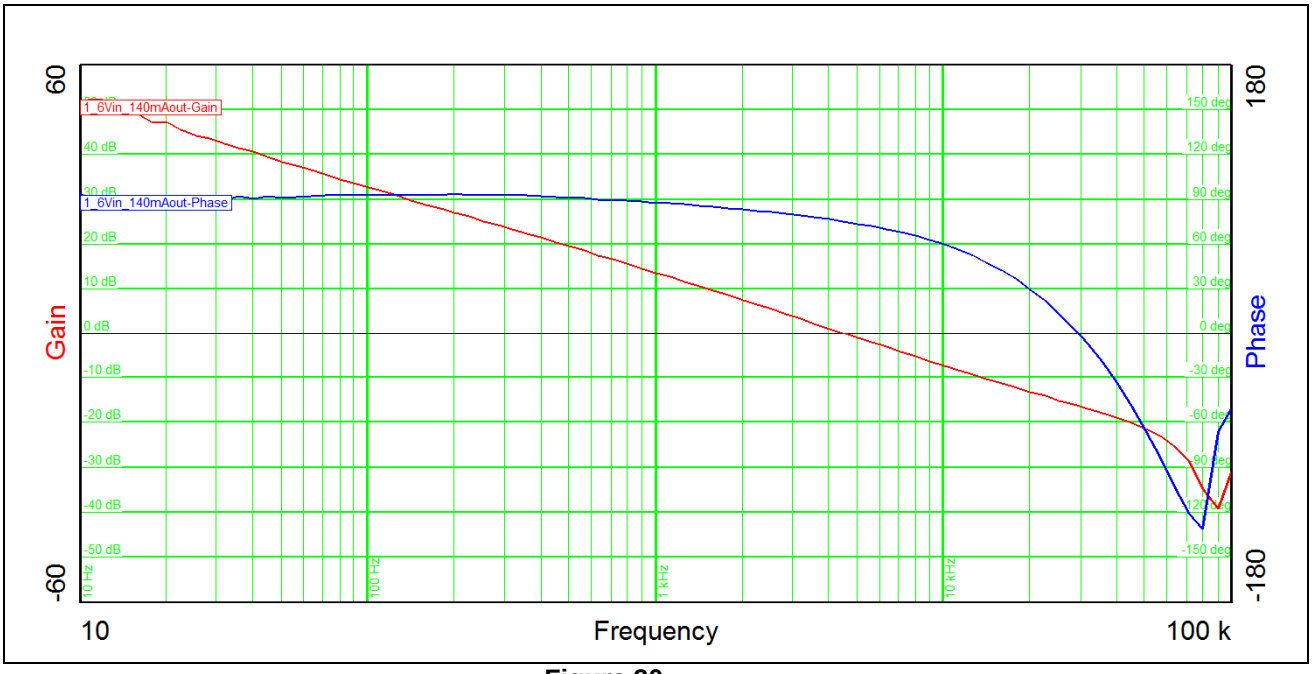


Figure 20

Figure 21 shows the loop response for 12Vin. Load is 0.2A.

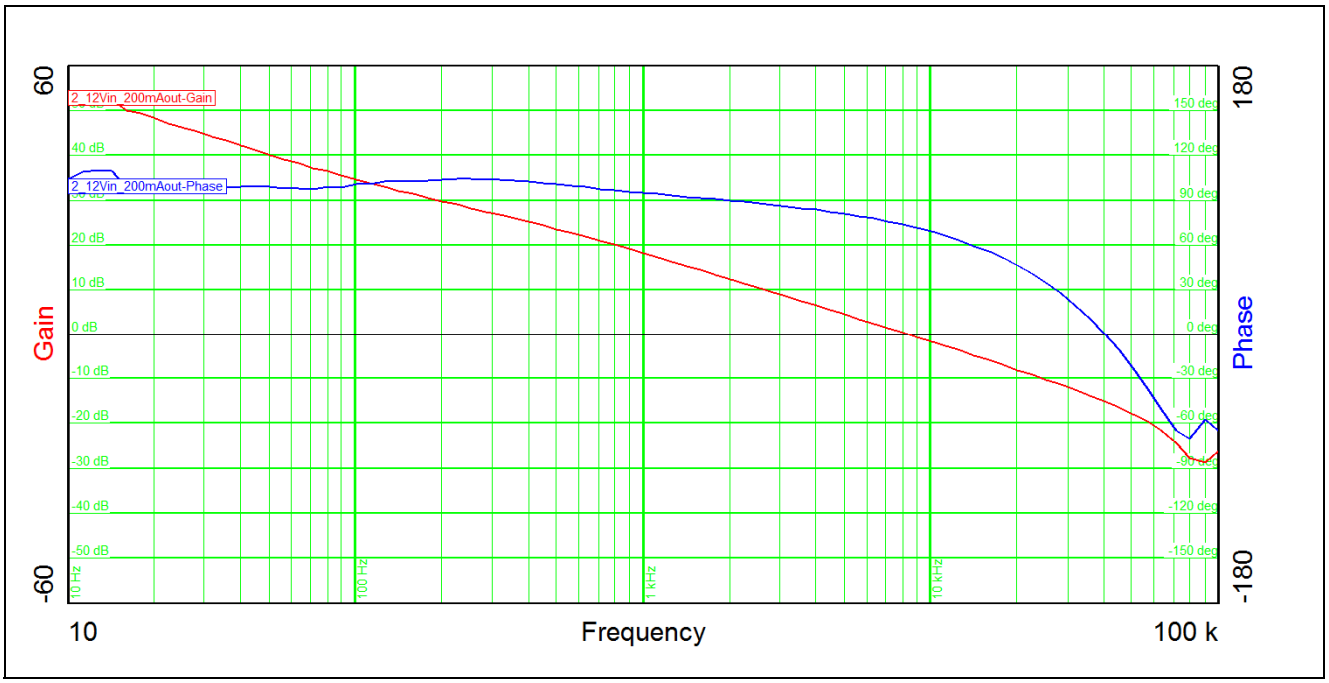


Figure 21

Figure 22 shows the loop response for 36Vin. Load is 0.2A.

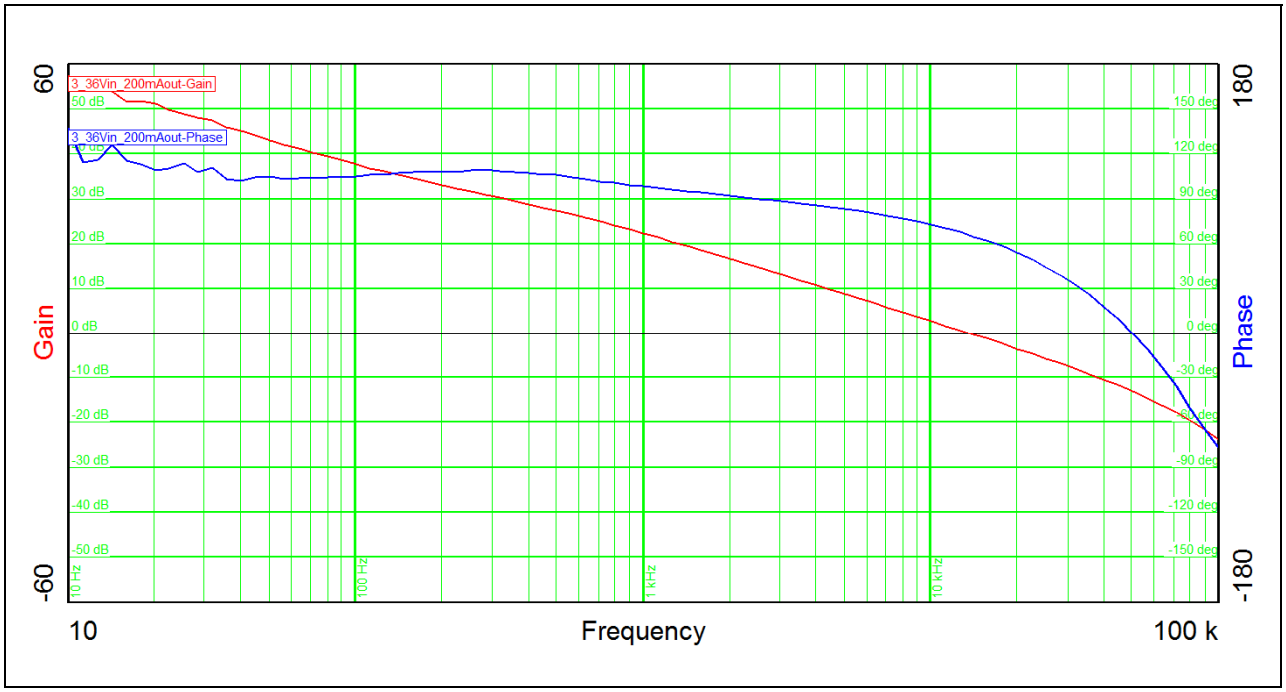


Figure 22

Figure 22 shows the loop response for 60Vin. Load is 0.2A.

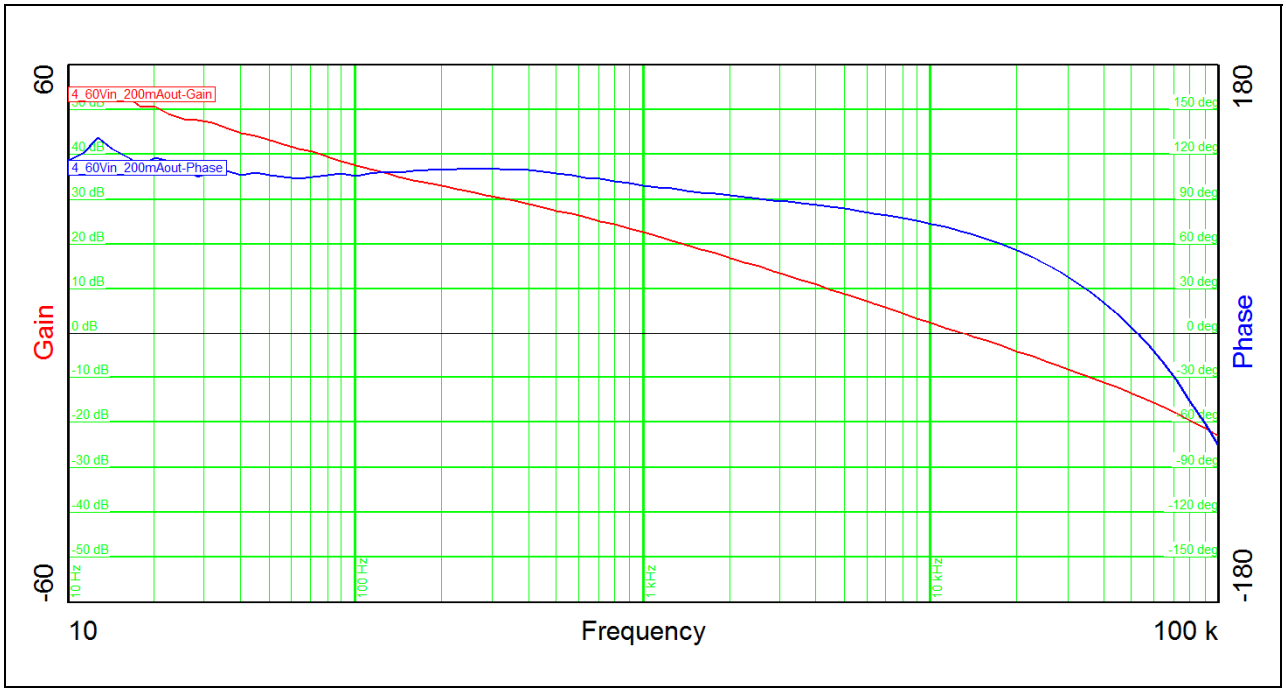


Figure 23

Table 1 summarizes the results of the above measurements

Vin	6V	12V	36V	60V
Bandwidth (kHz)	4.5	8.4	13.7	13.0
Phase margin	75°	72.8°	65.8°	68.3°
slope (20dB/decade)	-1.09	-1.04	-1.05	-1.12
gain margin (dB)	-16.3	-15.1	-13.1	-14.1
slope (20dB/decade)	-0.94	-1.35	-1.38	-1.33
freq (kHz)	29.4	40.4	50.4	52.4

Table 1

The transient response on a 50% load step is around 120mVpk, means the dynamic deviation is only 1%. The Bode plot is optimized for lowest loop bandwidth 4.5kHz at 6V input. Despite some papers describe Cuk compensation as difficult it could be shown that at low magnetizing inductance the results are perfect – a flat phase around +90 degrees and a fine gain slope at -1 (-20dB/decade).

10 Miscellaneous Waveforms

10.1 Switch Node (TP4)

The waveform of the voltage on switch node is shown in Figure 24. Input voltage was set to 12V.

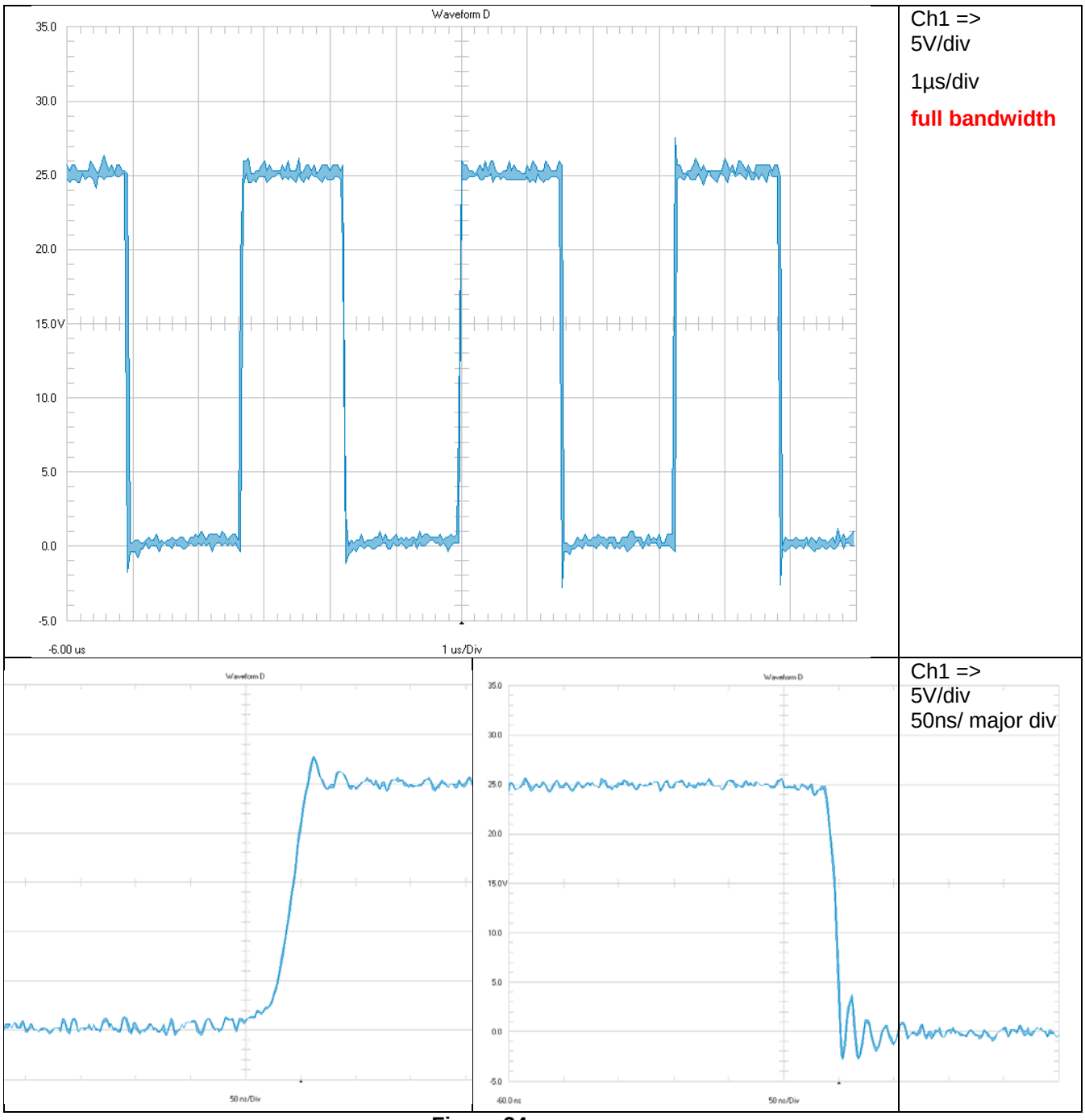


Figure 24

The waveform of the voltage on the switch node is shown in Figure 25. Input voltage was set to 36V.

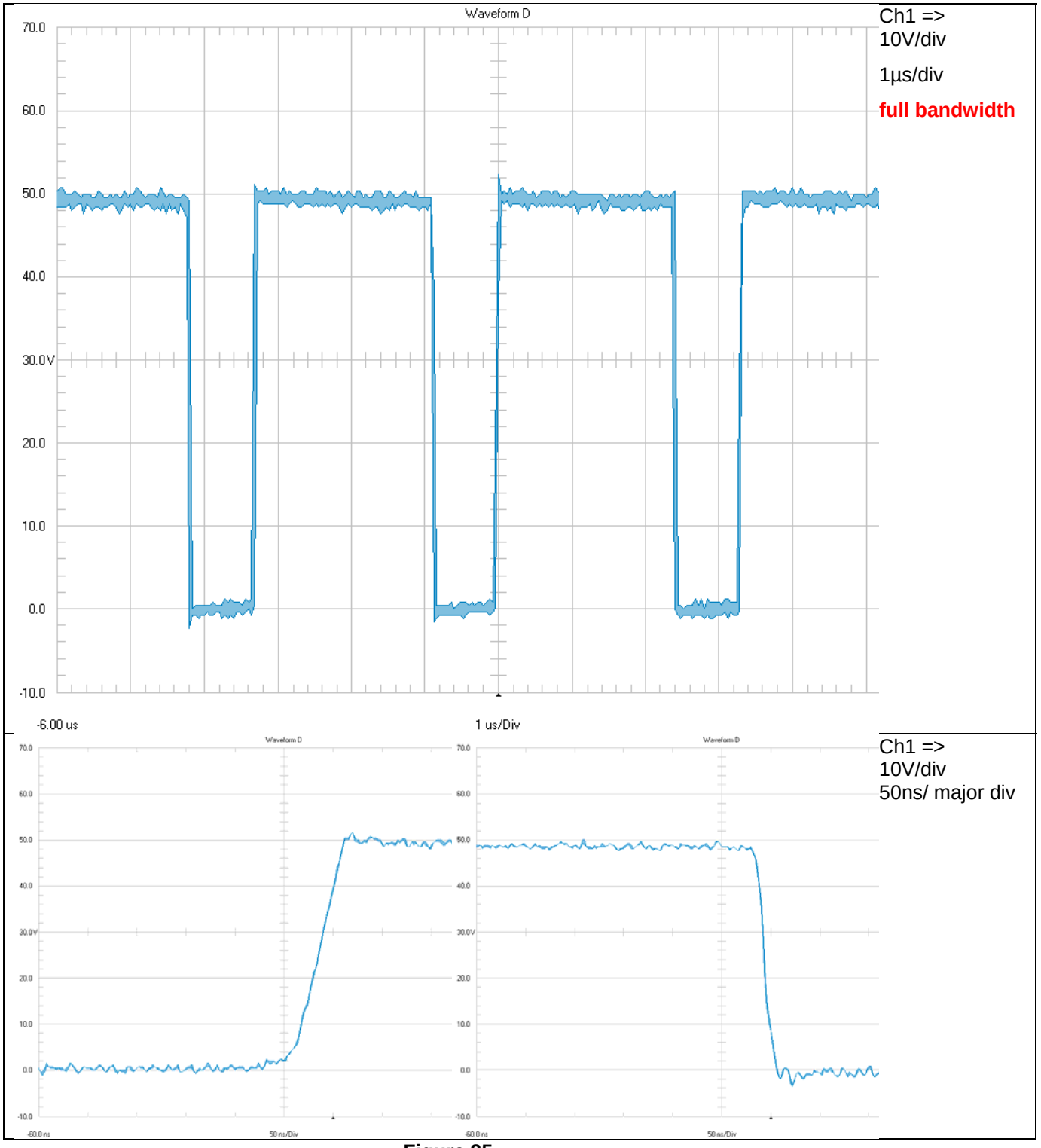


Figure 25

The waveform of the voltage on switch node is shown in Figure 26. Input voltage was set to 60V.

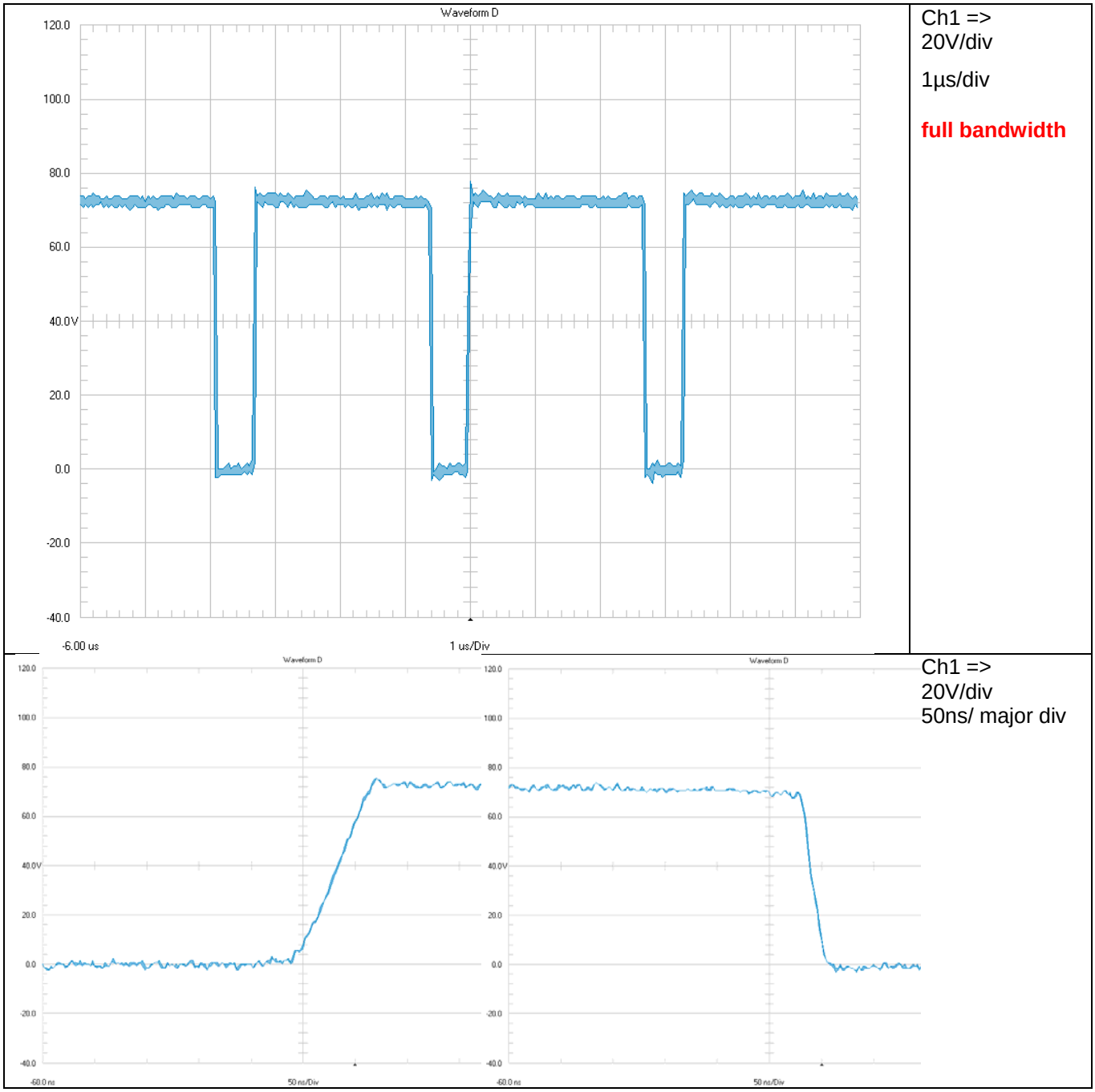


Figure 26

The drain pulse of 72V (input voltage + output voltage) shows perfect switching behavior. Despite a rise time of only 15ns there is almost NO overshoot, NO undershoot, there is NO RF ringing ! Providing a reasonable layout to the CuK topology results in lowest radiated emissions.

10.2 Diode D1 (TP6)

The waveform of the voltage on TP6 to GND is shown in Figure 27. Input voltage was set to 12V.

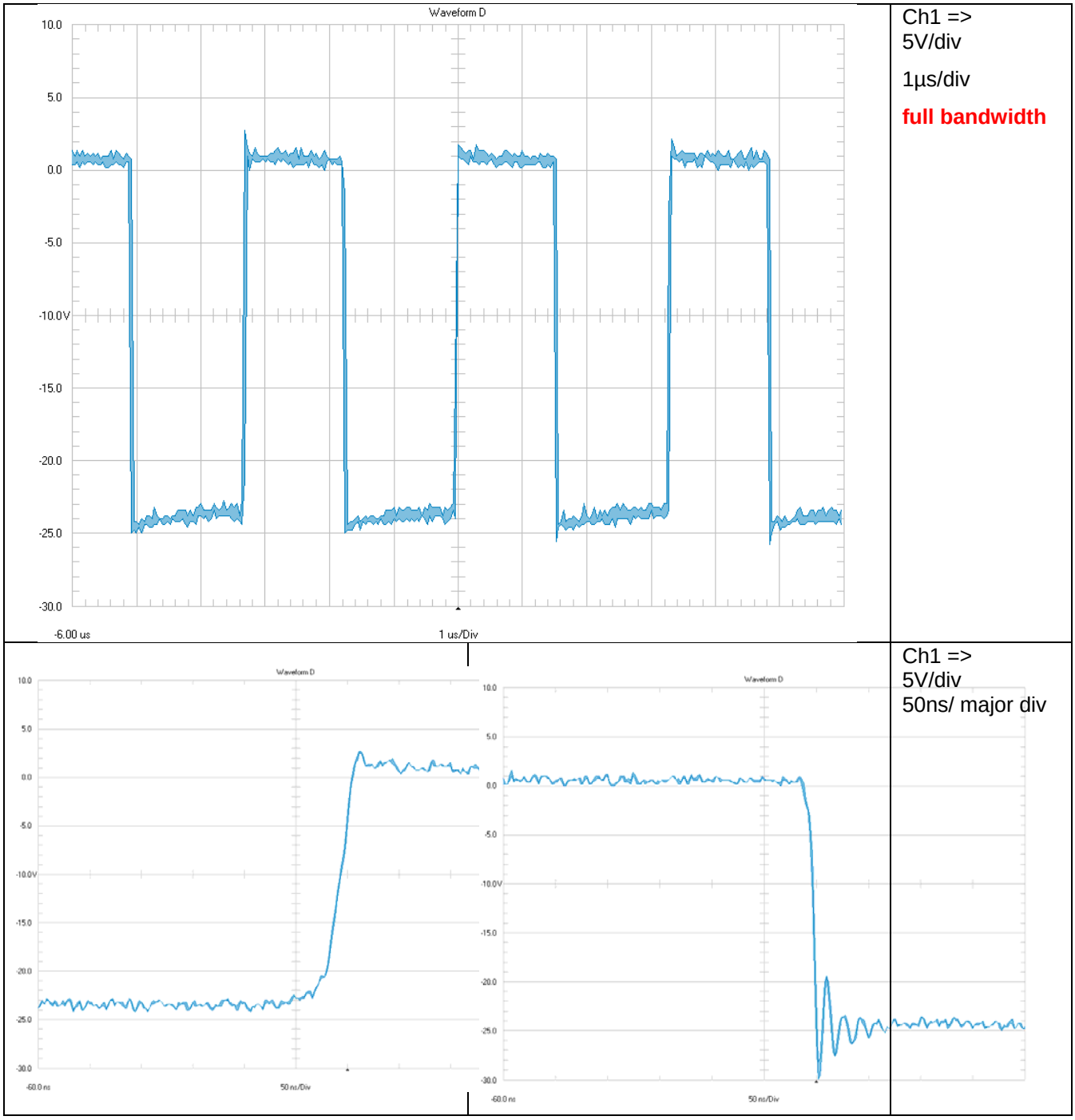


Figure 27

The waveform of the voltage on TP6 to GND is shown in Figure 28. Input voltage was set to 36V.

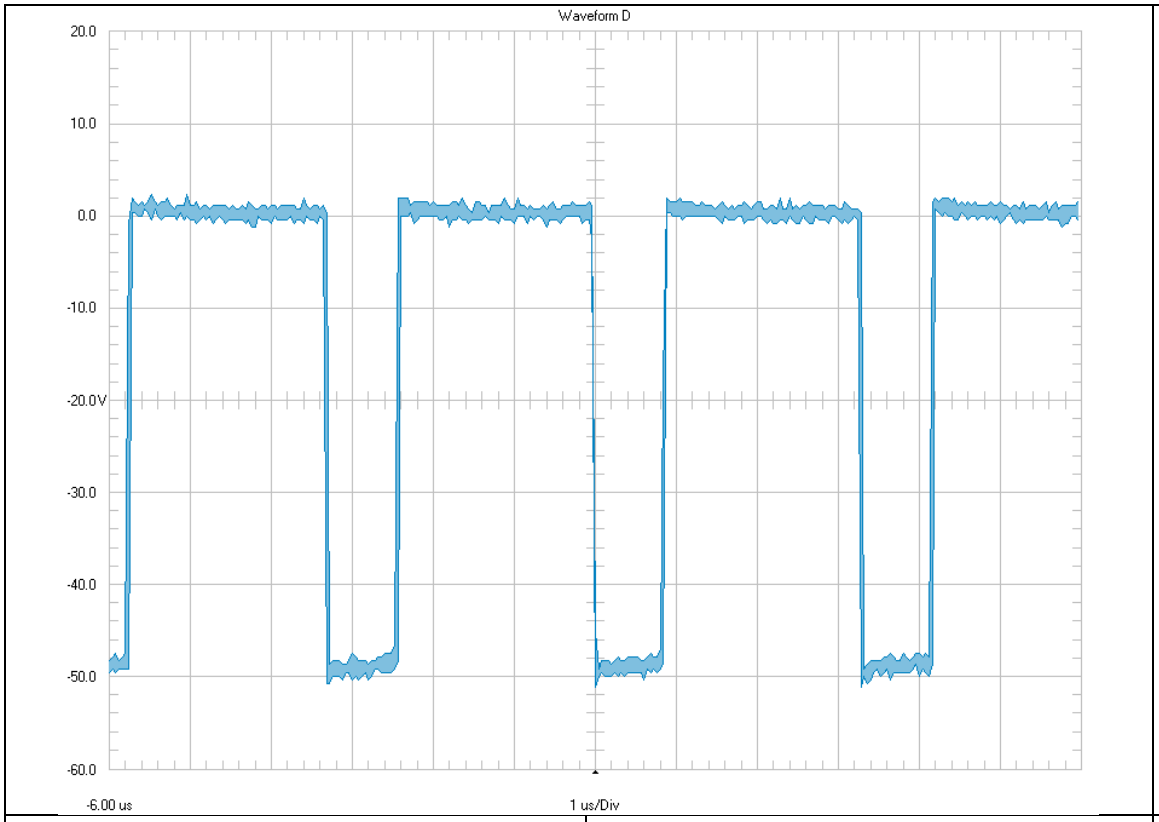


Figure 28

The waveform of the voltage on TP6 to GND is shown in Figure 29. Input voltage was set to 60V.

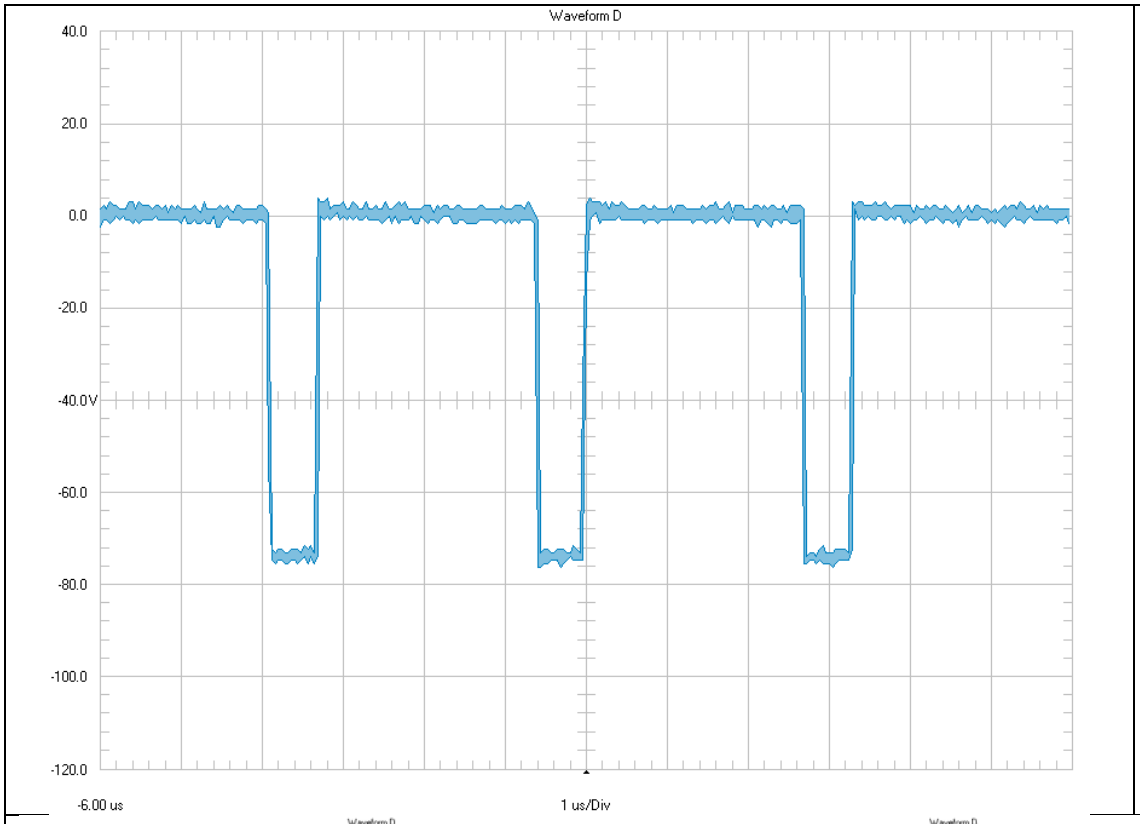


Figure 29

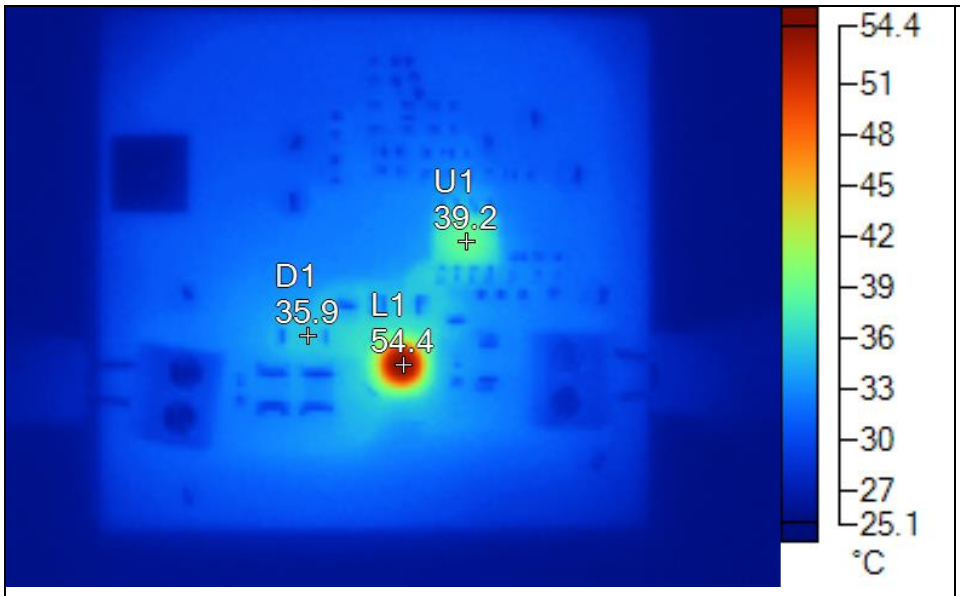
The flying capacitor place in between FET drain and rectifier anode is clamping the diode as well; again no overshoot, no undershoot, no ringing – **overall NO RF distortion !**

Waveforms for Transission Mode, DCM operating:

at 6V input < 30mA load current, at 10V input < 50mA load current
at 24V input <120mA load current, at 36V input <160mA load current
at 48V input <180mA load current, at 60V input <200mA load current (pure DCM)

11 Thermal Image @ Vin 6V /12V / 36V / 60V

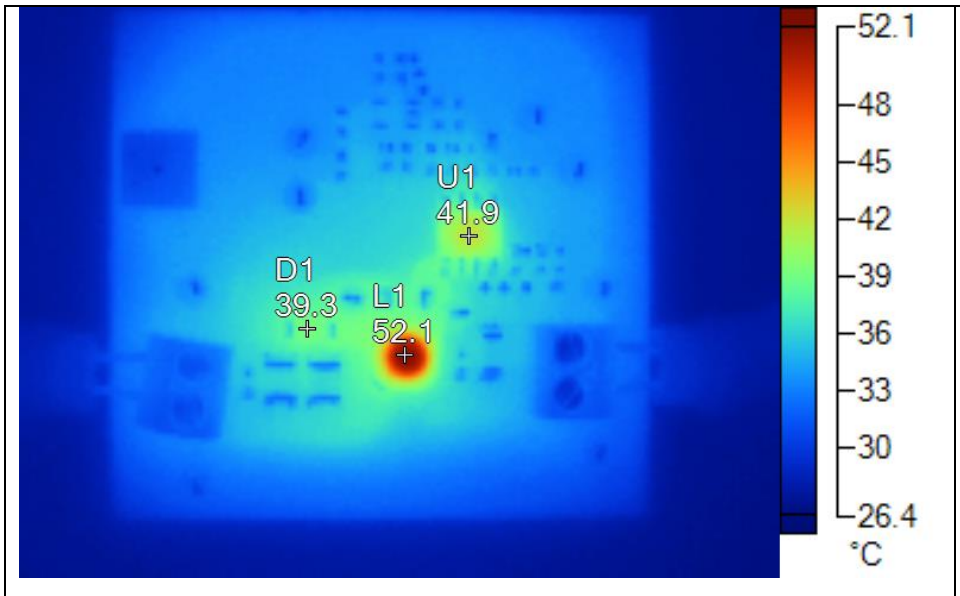
Figure 30 shows the thermal image at 6V input voltage and 140mA output current.



Name	Temperature
L1	54.4°C
U1	39.2°C
D1	35.9°C

Figure 30

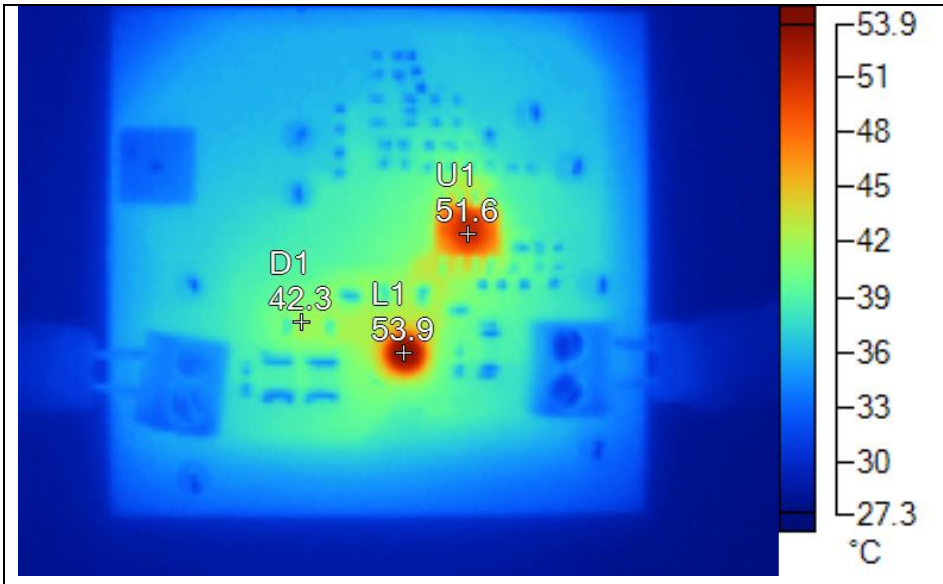
Figure 31 shows the thermal image at 12V input voltage and 200mA output current.



Name	Temperature
L1	52.1°C
U1	41.9°C
D1	39.3°C

Figure 31

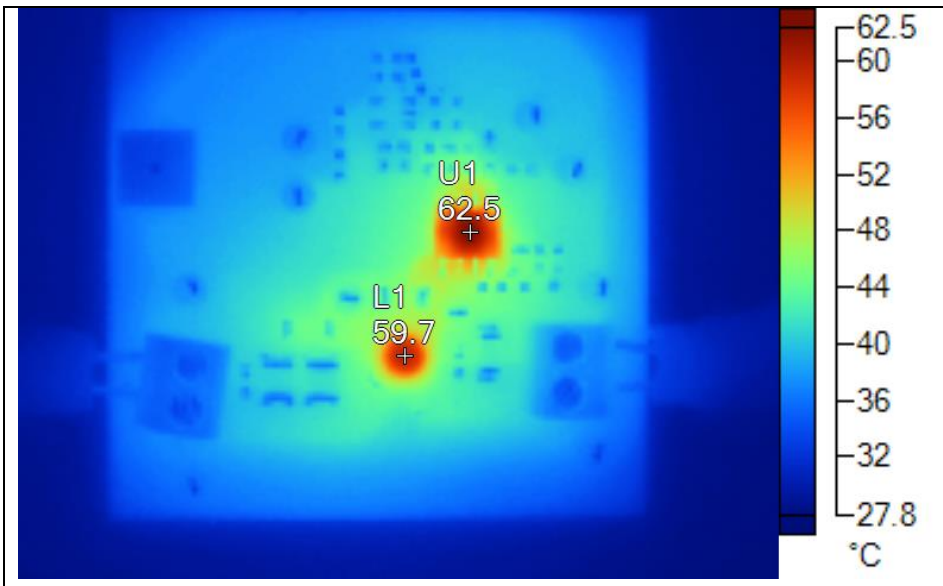
Figure 32 shows the thermal image at 36V input voltage and output current 200mA.



Name	Temperature
L1	53.9°C
U1	51.6°C
D1	42.3°C

Figure 32

Figure 33 shows the thermal image at 60V input voltage and output current 200mA.



Name	Temperature
U1	62.5°C
L1	59.7°C

Figure 33

At high input voltage the losses at internal linear regulator and the switching losses at the internal FET are getting dominant, efficiency drops – but the temperature rise below +40K is still acceptable for industrial temperature range.

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