Design Guide: TIDA-020013
Automotive SPD-SmartGlass™ Driver Reference Design

Description

This reference design details how to drive various forms of electronically-dimmable glass, including SPD-SmartGlass™, from a car battery. This guide illustrates how to make a DC/AC inverter using the LM5155-Q1 boost converter with a charge pump, two UCC27712-Q1 half-bridge drivers, and a TMS320F2807 microcontroller for PWM creation and system monitoring.

Resources

TIDA-020013	Design Folder
LM5155-Q1	Product Folder
UCC27712-Q1	Product Folder
TMS320F28027	Product Folder

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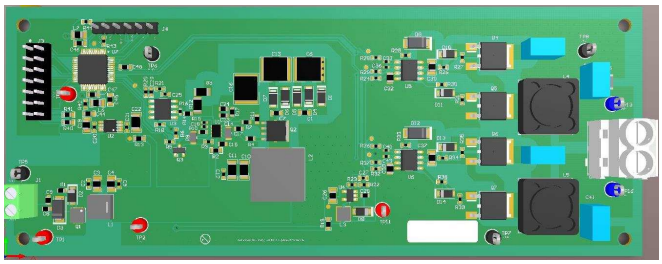
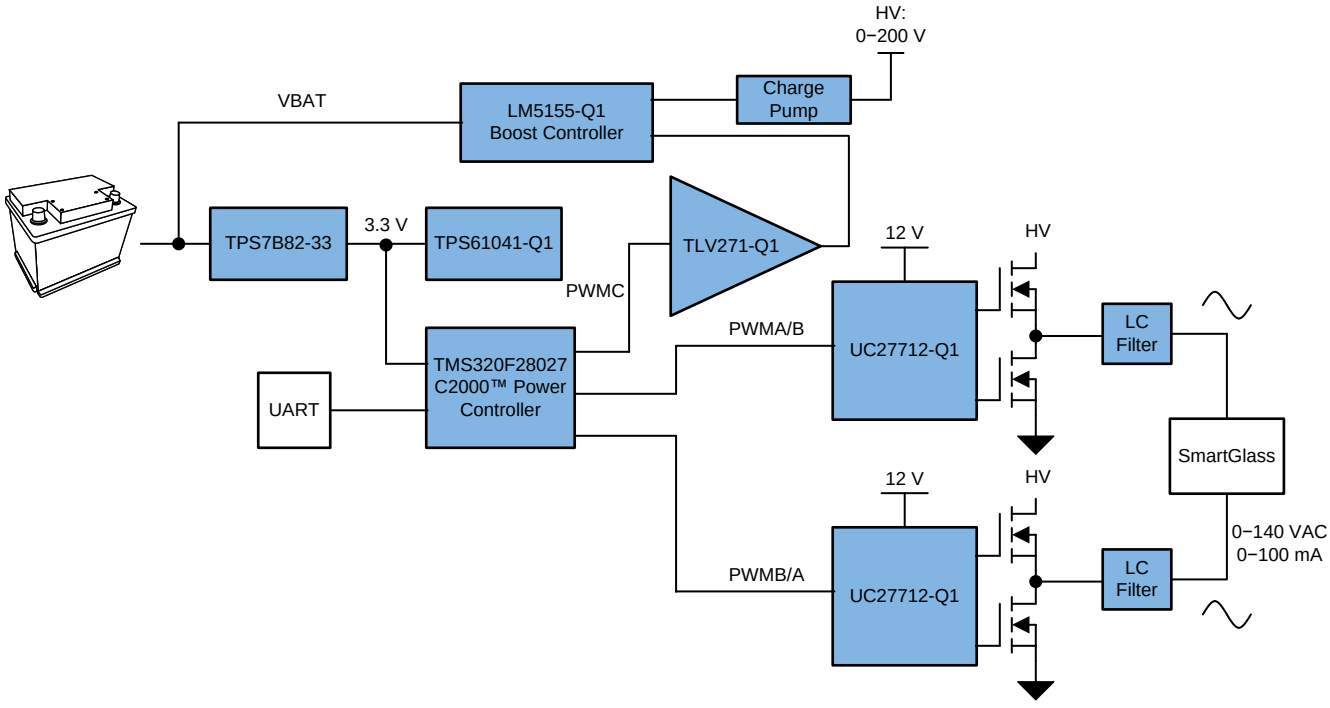
Features

- 120 V_{RMS} AC output
- 100-mA driving capability
- Controllable amplitude for precise adjustments of intermediate amounts of glass dimming

Applications

- DC/AC Inverter





1 System Description

SPD-SmartGlass™ is electrically tintable glass that works by aligning nanoparticles in a film within glass, plastic, acrylic, or chemically strengthened glass. This glazing can be used to block out heat, sunlight, glare, UV and noise. SPD-SmartGlass allows for instant and precise control of the level of light coming into the vehicle, by varying the amplitude of the voltage applied. To drive this dynamic glass a high voltage AC signal is needed to rapidly orient the light-blocking nanoparticles. This design creates the required high voltage AC signal from a typical automotive battery, while using a microcontroller to adjust driving frequency and amplitude to desired levels.

1.1 Key System Specifications

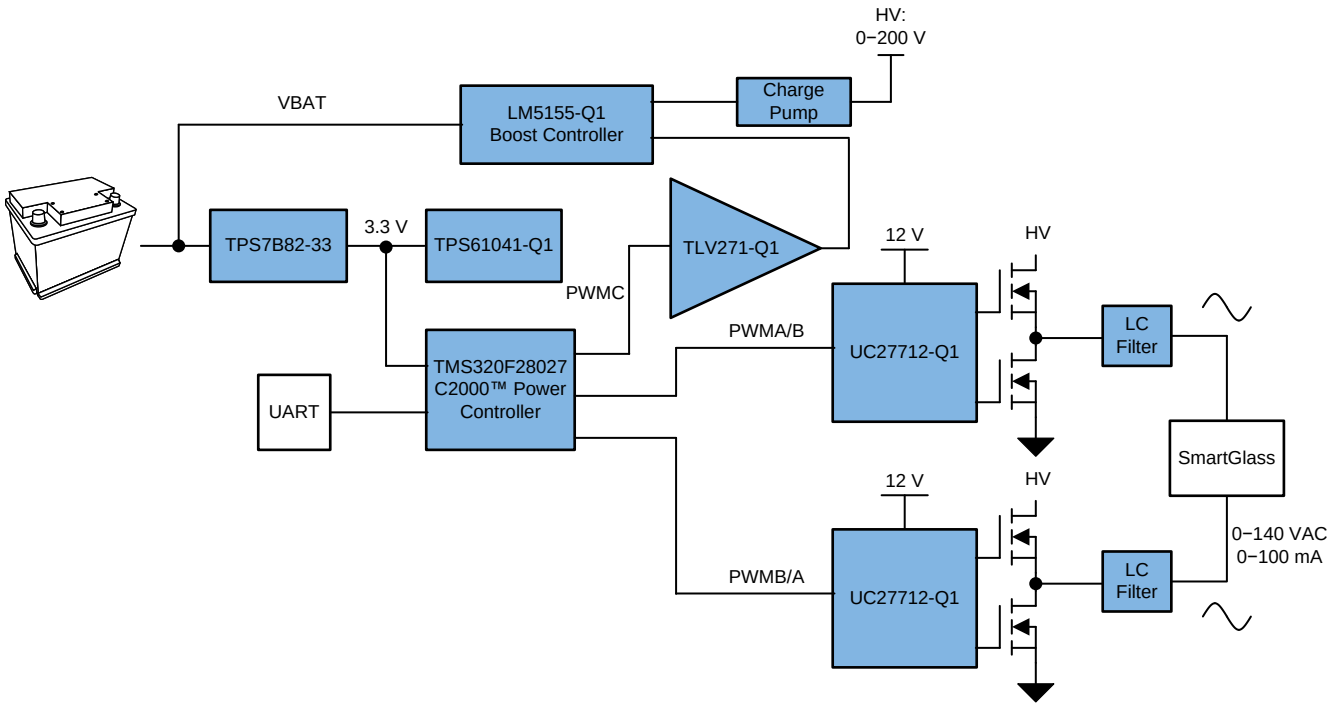
Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	9 V to 18 V	Section 2.3.3.1
Output signal	Pure sine	Section 2.3.4.2
Maximum output voltage	120 VAC	
Maximum output current	70 mA	Section 2.3.3.2
PCB form factor	58.67 mm × 149.86 mm	Section 2.3.1

2 System Overview

2.1 Block Diagram

Figure 1. TIDA-020013 Block Diagram



2.2 Highlighted Products

2.2.1 UCC27712-Q1

The UCC27712 device is a 620-V, high- and low-side gate driver with 1.8-A source, 2.8-A sink current, targeted to drive power MOSFETs or IGBTs. The UCC27712 includes protection features where the outputs are held low when the inputs are left open or when the minimum input pulse width specification is not met. Interlock and deadtime functions prevent both outputs from being turned on simultaneously. In addition, the device accepts a wide range bias supply range from 10 V to 22 V, and offers UVLO protection for both the V_{DD} and HB bias supply. Developed with TI's state of the art high-voltage device technology, the device features robust drive with excellent noise and transient immunity including large negative voltage tolerance on its inputs, high dV/dt tolerance, wide negative transient safe operating area (NTSOA) on the switch node (HS), and interlock. The device consists of one ground-referenced channel (LO) and one floating channel (HO) which is designed for operating with bootstrap or isolated power supplies. The device features fast propagation delays and excellent delay matching between both channels. On the UCC27712, each channel is controlled by its respective input pins, HI and LI.

2.2.2 LM5155-Q1

The LM5155-Q1 device is a wide input range, non-synchronous boost controller that uses peak current mode control. The device can be used in boost, SEPIC, and flyback topologies. The LM5155-Q1 device can start up from a 1-cell battery with a minimum 2.97 V. After start-up, the device can operate down to a 1.5-V input by supplying the BIAS pin from the boost converter output. The internal regulator also supports operation up to 45 V (50 V absolute maximum) for automotive load dump. The switching frequency is dynamically programmable with an external resistor from 100 kHz to 2.2 MHz. Switching at 2.2 MHz minimizes AM band interference and allows for a small solution size and fast transient response. The device features a 1.5-A standard MOSFET driver and a low 100-mV current limit threshold. The device also supports the use of an external V_{CC} supply to improve efficiency. Low operating current and pulse

skipping operation improve efficiency at light loads. The device has built-in protection features such as cycle-by-cycle current limit, overvoltage protection, line UVLO, thermal shutdown, and hiccup mode overload protection which is available in the LM5155-Q1 device option. Additional features include low shutdown I_Q, programmable soft start, programmable slope compensation, precision reference, power good indicator, and external clock synchronization.

2.2.3 TPS7B82-Q1

In automotive battery-connected applications, low quiescent current (I_Q) is important to save power and extend battery lifetime. It is especially necessary to have ultra-low I_Q for always-on systems. The TPS7B82-Q1 is a low-dropout linear regulator designed for up to 40-V VIN applications. With only 2.7-µA typical quiescent current at light load, it is an optimal solution for powering microcontrollers and CAN/LIN transceivers in standby systems. The device features integrated short-circuit and overcurrent protection. This device operates in ambient temperatures from –40°C to 125°C and with junction temperatures from –40°C to 150°C. Additionally, this device uses a thermally conductive package to enable sustained operation despite significant dissipation across the device. Because of these features, the device is well suited as a power supply for various automotive applications.

2.2.4 TMS320F28027

The F2802x Piccolo™ family of microcontrollers provides the power of the C28x core coupled with highly integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code, and also provides a high level of analog integration. An internal voltage regulator allows for single-rail operation. Enhancements have been made to the HRPWM to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0 to 3.3-V fixed full-scale range and supports ratio-metric VREFHI and VREFLO references. The ADC interface has been optimized for low overhead and latency.

2.2.5 TPS61041-Q1

The TPS6104x-Q1 devices are high-frequency boost converters for automotive applications. The devices are ideal for generating output voltages up to 28 V from a pre-regulated low voltage rail, dual-cell NiMH, NiCd, or a single-cell Li-Ion battery, supporting input voltages from 1.8 V to 6 V. The TPS6104x-Q1 devices operate with a switching frequency up to 1 MHz, allowing the use of small external components such as ceramic as well as tantalum output capacitors. Combined with the space-saving, 5-pin SOT-23 package, the TPS6104x-Q1 devices accomplish a small overall solution size. The TPS61041-Q1 device has an internal 400-mA switch current limit, while the TPS61041-Q1 device has a 250-mA switch current limit, offering lower output voltage ripple and allowing the use of a smaller form factor inductor for lower-power applications. The TPS6104x-Q1 devices operate in a pulse frequency modulation (PFM) scheme with constant peak current control. The combination of low quiescent current (28 µA typical) and the optimized control scheme enable operation of the devices at high efficiencies over the entire load current range.

2.2.6 TLV271-Q1

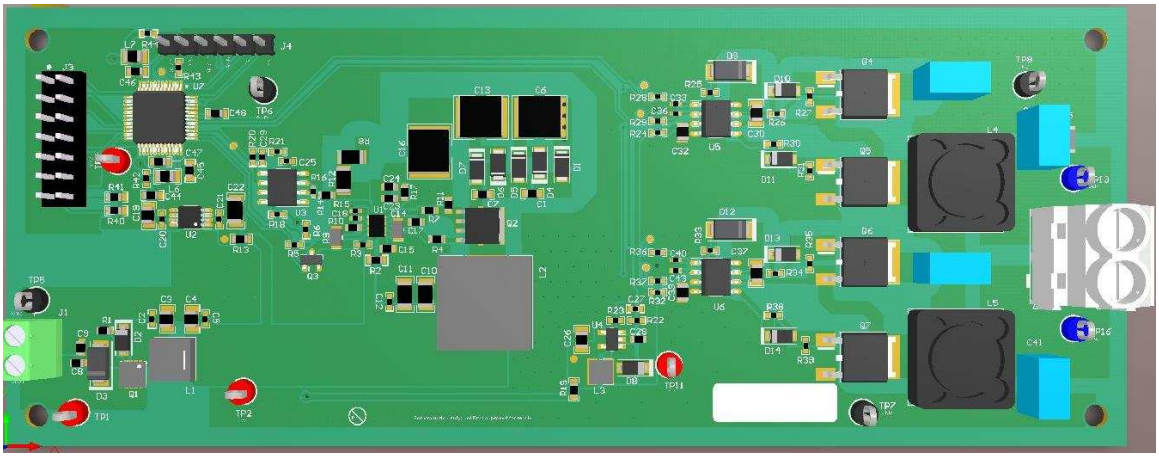
The TLV27x takes the minimum operating supply voltage down to 2.7 V over the extended automotive temperature range while adding the rail-to-rail output swing feature. This makes it an ideal alternative to the TLC27x family for applications where rail-to-rail output swings are essential. The TLV27x also provides 3-MHz bandwidth from only 550 µA. Like the TLC27x, the TLV27x is fully specified for 5-V and ±5-V supplies. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from a variety of rechargeable cells (±8-V supplies down to ±1.35 V). The CMOS inputs enable use in high-impedance sensor interfaces, with the lower voltage operation making an attractive alternative for the TLC27x in battery-powered applications.

2.3 System Design Theory

2.3.1 PCB and Form Factor

This reference design uses a two-layer printed circuit board (PCB) with 1.4-mil copper. All components are placed on the top layer. The PCB in not intended to fit any particular form factor. The PCB has dimensions 58.67 mm × 149.86 mm. The primary object of the design with regards to the PCB is to make a solution that is compact while still providing a way to test the performance of the board. shows a 3D rendering of the board.

Figure 2. Rendered Image of PCB



2.3.2 Input Protection and EMI filter

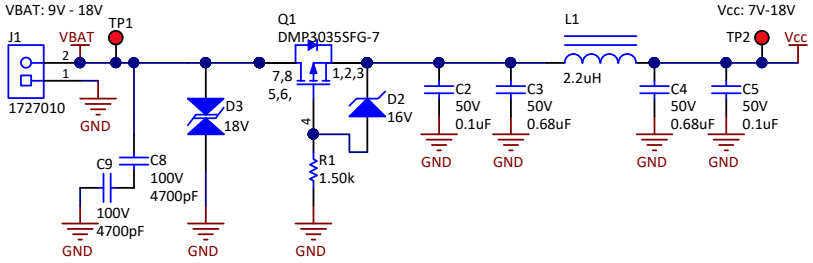
In this reference design, ESD protection is implemented by series capacitors C9 and C19 as Figure 3 shows. Two capacitors in series were used to allow for redundancy in the case of mechanical failure of a single capacitor.

The LM5155-Q1, TPS7B82-Q1, and MOSFET Q1 are connected directly to the battery. Being connected to the battery, transient protection is needed to avoid damaging the ICs. Q1 has the lowest max voltage rating at 30 V. To protect Q1, TVS diode D3 was chosen to clamp the input rail below 30 V during a transient.

For reverse voltage protection, a P-Channel MOSFET Q1, clamping Zener diode D2, and current limiting resistor R1 are used. Resistor R1 is used to limit current flow into the gate of Q1 and Zener diode D2 is used to protect the gate of Q1 and clamp the voltage in the case of a transient. Under normal operation, Q1 is fully saturated acting as a diode. Under a reverse battery condition, the gate-source voltage of Q1 is now negative thus turning off the FET and preventing current flow through the system. A P-channel FET was chosen instead of a diode to reduce power dissipation.

An EMI pi filter is placed at the input of the system to attenuate conducted differential mode noise generated by the system. The filter consists of C2, C3, L1, C4, and C5 as Figure 3 shows. For more details, see *AN-2162 Simple Success With Conducted EMI From DC-DC Converters*.

Figure 3. Input Filter Schematic



2.3.3 LM5155-Q1 Boost Converter, Voltage Tripler, and PWM DAC

To create a high voltage AC signal from a car battery, the DC voltage must first be boosted up to a high voltage DC signal. To maximize the boost range and increase the list of usable MOSFETs, a charge pump was added to the output of the LM5155-Q1. To create an adjustable output voltage a PWM DAC is used to manipulate the feedback current running into the LM5155-Q1.

2.3.3.1 LM5155-Q1 Boost

Table 2 shows the design parameters for the boost converter. Since there is a charge pump attached that will convert current into voltage an inductor is chosen assuming one third the output voltage of the charge pump and three times the current.

Table 2. Design Requirements for Boost Converter

DESIGN PARAMETERS	VALUE
Output voltage	66.7 V
Output current	210 mA
Minimum input voltage	9 V
Switching frequency	2200 kHz

To avoid interference in AM band frequencies the gate of boost converter switches at 2.2 MHz. To achieve a decent level of efficiency when switching at this high frequency a MOSFET with very low input and output capacitance must be chosen.

A MOSFET is placed across the bottom resistor of the UVLO divider. When this MOSFET is conducting the bottom UVLO resistor will be shorted will cause the LM5155-Q1 to enter standby mode. To prevent the LM5155-Q1 from immediately running when power is added to the system, R5 is used to pull the gate up to 3.3 V, forcing the MOSFET to conduct. To enable the LM5155-Q1 the gate of the MOSFET is attached to an open drain output of the TMS320F28027 microcontroller. When this output is pulled low the MOSFET will stop conducting and the LM5155-Q1 will be enabled. See the LM5155-Q1 product page and the *LM5155-Q1 2.2-MHz Wide Input Nonsynchronous Boost, Sepic, Flyback Controller* data sheet for more about the UVLO pin and Standby mode.

The PGOOD pin of the LM5155-Q1 is connected to a C2000™ Microcontroller GPIO for monitoring of the state of the boost converter.

WARNING

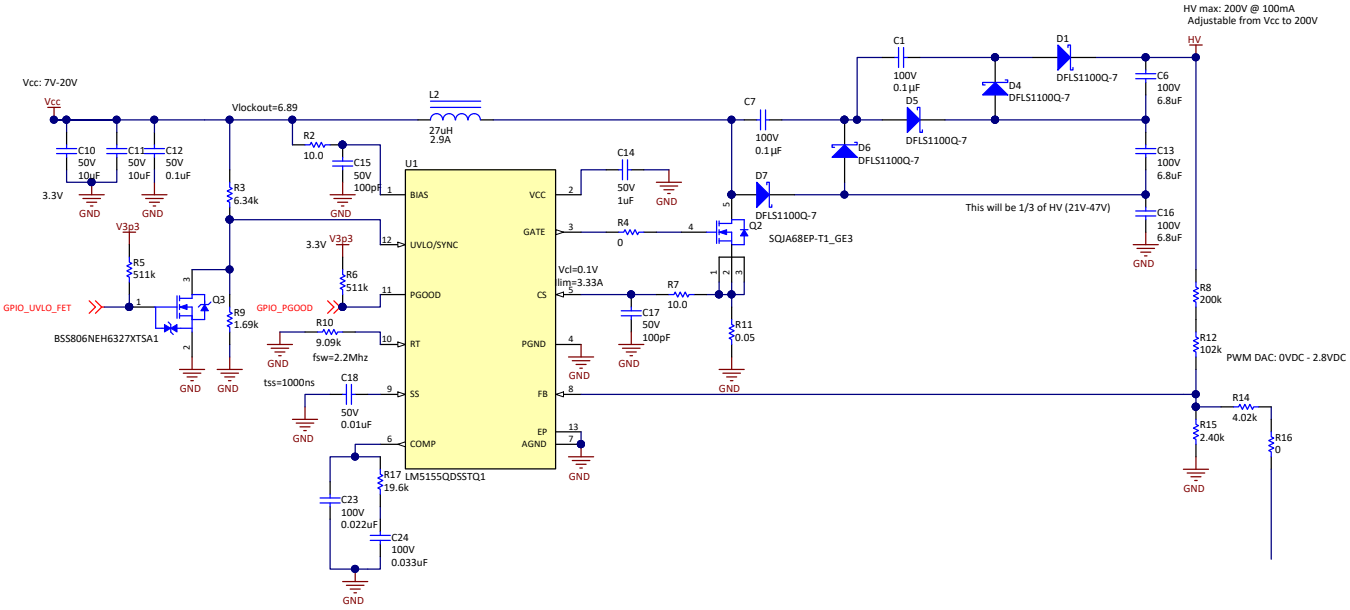
Electric shock is possible when connecting the board to a live wire. A professional is the only person qualified to handle the board.

For safety, TI recommends using isolated test equipment with overvoltage and overcurrent protection.

CAUTION

Do not leave the EVM powered when unattended.

Figure 4. LM5155-Q1 Boost Schematic



2.3.3.2 *Voltage Tripler*

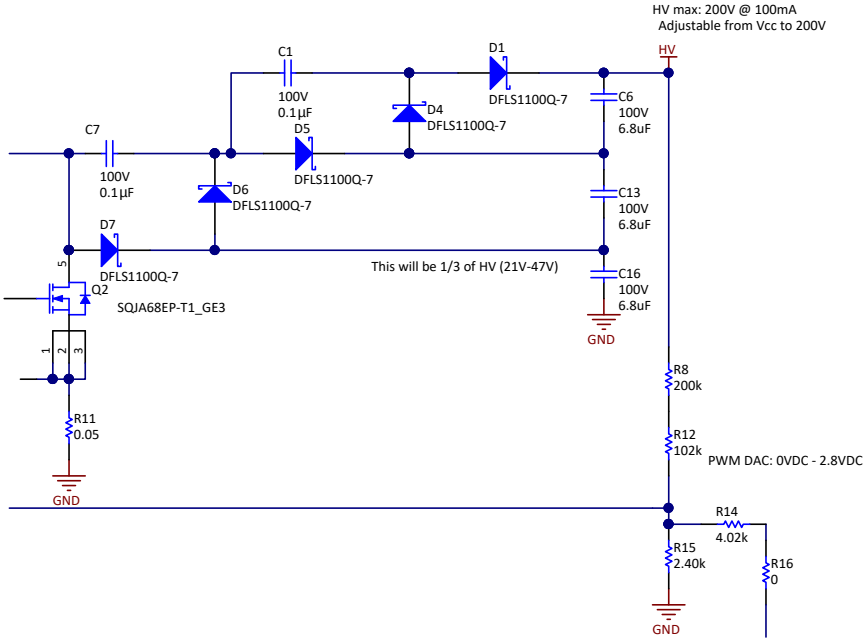
The tripler circuit attached to the LM5155-Q1 converts current into voltage. The tripler circuit reduces the peak current running through the inductor for the same output voltage. This allows the use of a smaller inductor while also having a lower minimum system input voltage. The tripler also allows use of 100 V components while maintaining an output of 200 V. This is because each of the output capacitors only see one third of the output voltage. Since the system is switching at 2.2 MHz and a low gate charge is needed MOSFET selection becomes much easier.

For more information on the functionality of voltage multipliers see Power Tips: Multiply your output voltage. https://e2e.ti.com/blogs_/b/powerhouse/archive/2016/07/20/power-tips-multiply-your-output-voltage

Table 3. Design Requirements for Voltage Tripler

DESIGN PARAMETERS	VALUE
Input Voltage	66.7 V
Output Voltage	200 V
Output Current	70 mA

Figure 5. Voltage Tripler Schematic

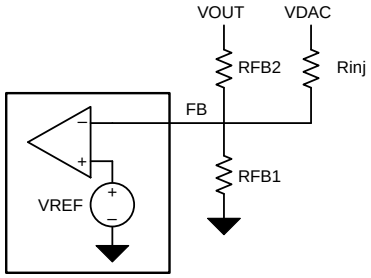


2.3.3.3 PWM DAC

The transparency of *SPD-SmartGlass™* is controlled by the amplitude of the driving signal. To adjust the amplitude of the output sine wave, the LM5155-Q1 boost voltage is adjusted by manipulating the feedback pin of the device with an injection resistor and PWM "DAC" filter. This allows us to sink or source current to the feedback pin and therefore change the output voltage. The DAC voltage to output voltage can be found using the following relationship:

$$\frac{V_{OUT} - V_{REF}}{R_{FB2}} + \frac{V_{DAC} - V_{REF}}{R_{inj}} = \frac{V_{REF}}{R_{FB1}} \quad (1)$$

Figure 6. Injection Circuit

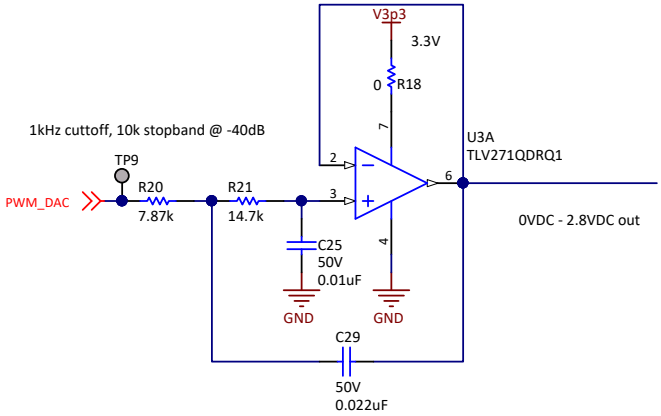


To create an adjustable DC voltage a PWM signal is run through a second order Sallen key low pass filter. The output DC voltage is adjusted by changing the input PWM duty cycle. See Section 3.2 for a graph of PWM duty cycle to output voltage.

Table 4. Design Requirements for PWM DAC

DESIGN PARAMETERS	VALUES
Input PWM Voltage	3.3 V
Output DC Voltage	0 V–2.8 V
Cutoff Frequency (–3 dB)	1 kHz
Stopband Frequency (–40 dB)	10 kHz

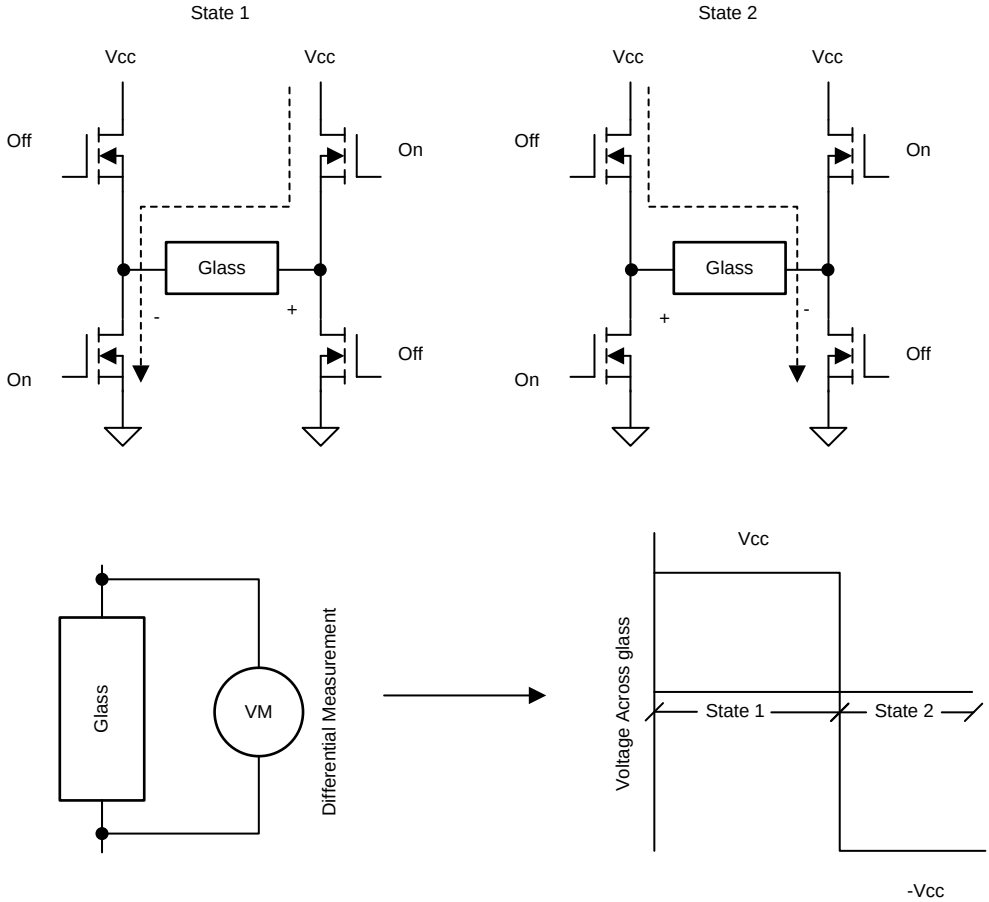
Figure 7. PWM DAC Schematic



2.3.4 UCC27712-Q1 Half-Bridge Drivers and Output Filter

To align the particles inside SmartGlass a bipolar signal must be applied to the glass in order to charge and discharge it. To create this signal without the use of a negative rail the glass is connected in a bridge tied load configuration using UCC27712-Q1 half-bridge drivers. See Figure 8 to see how this works.

Figure 8. Full Bridge Tied Load to Drive SmartGlass



2.3.4.1 Half-Bridge Drivers

Component selection for the gate drivers is crucial. Based on the design requirements in Table 5, the following sections provide guidelines on choosing the correct components for this system.

Table 5. Design Requirements for UCC27712-Q1 Half-Bridge Driver

DESIGN PARAMETERS	VALUE
Input PWM voltage	3.3 V
Input PWM frequency	400 kHz
MOSFET drain voltage	200 V

The bootstrap capacitor must have enough charge to hold the MOSFET gate on during an entire switching period. Using Equation 2, the minimum boost strap capacitor size can be determined, then a capacitor of a slightly larger size to allow some additional headroom is used.

Total charge needed per cycle:

$$Q_{total} = Q_g + \frac{I_{QBS}}{f_{SW}} = 6.85 \times 10^{-9}$$

Ripple voltage on bootstrap capacitance:

$$\Delta V_{boot} = 0.1$$

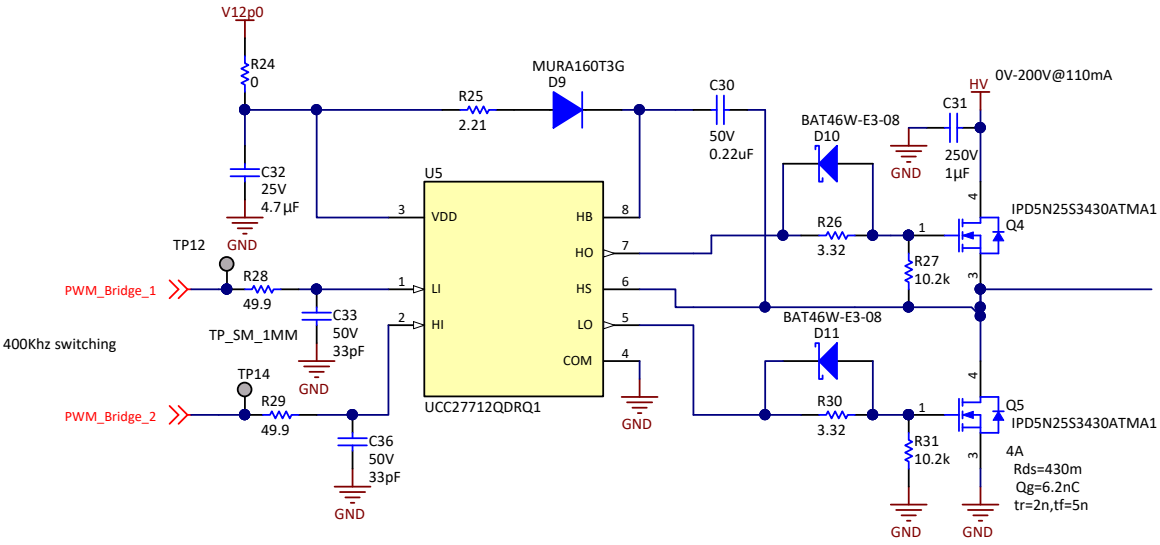
Calculated bootstrap capacitance:

$$C_{boot} = \frac{Q_{total}}{\Delta V_{boot}} = 6.85 \times 10^{-8} \quad (2)$$

Gate drive resistors were added to slow the gate drive, this stops the MOSFET from turning on and off very quickly when voltage in initially applied which ultimately prevents ringing on the output. When turning off the MOSFETs , instead of a path through the gate drive resistor, there is a path through the diodes found in parallel to the resistor. This helps ensure that the MOSFET is turned off quickly. Gate source resistors were added to give a slow path for the bootstrap capacitor to discharge. This is needed so the capacitor does not stay at a high voltage after the system powers down.

To prevent arcing near the high voltage traces, 80-mil trace spacing rules are used in the layout around the MOSFET bridge.

Figure 9. Half-Bridge Driver Schematic



2.3.4.2 LC Filter

For EMI purposes, it may be more ideal to drive the load with a sine wave vs the square wave generated from the half-bridge drivers. To get a sine wave from the given square wave an LC filter is used. To prevent giant inductor peak currents according to the formula below, a higher switching frequency than desired driving frequency may be needed.

shows how an LC filter is used to removed higher frequency components from a signal to keep just the driving frequency.

In addition, a current-limiting resistor is added before the path of the LC filter to minimize the effects of inrush current to protect the high voltage bridge.

Figure 10. LC Filtering Removes Unwanted High Frequency Switching

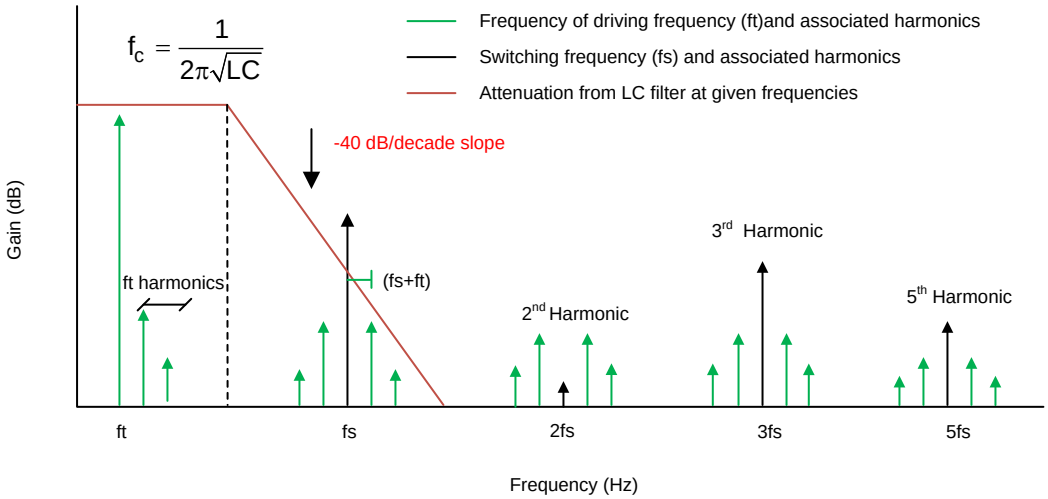
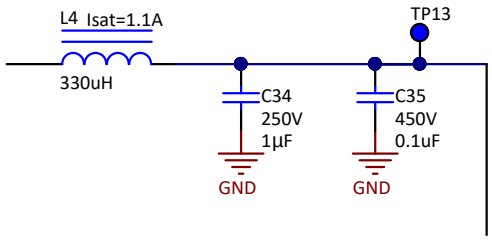


Table 6. Design requirements for LC Filter

DESIGN PARAMETERS	VALUE
Input SPWM voltage	200 V
Cutoff frequency (–3 dB)	8.3 kHz
Attenuation	–40 dB/decade

Figure 11. LC Filtering Schematic



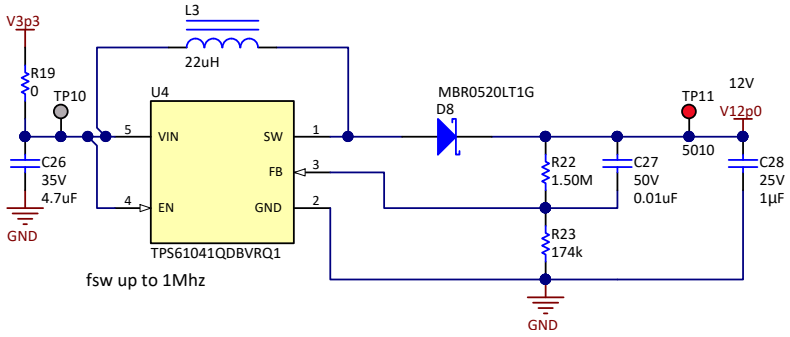
2.3.5 TPS61041-Q1 Boost

The UCC27712 device requires a V_{CC} between 10 V and 20 V, because of this we cannot tie directly to the battery. The TPS61041 is used to boost a 12-V rail from the 3.3-V LDO rail. This method was chosen because it was more efficient and reduced cost compared to buck-boost or buck/LDO solutions off the battery or 200-V rail.

Table 7. Design Requirements for TPS61041-Q1

DESIGN PARAMETERS	VALUE
Input voltage	3.3 V
Output voltage	12 V
Output current	20 mA

Figure 12. TPS61041-Q1 Boost Schematic



2.3.6 TPS7B82-Q1 LDO

The 3.3-V fixed output version of the TPS7B82-Q1 (TPS7B8233-Q1) was used in this reference design. Figure 13 shows the schematic for the LDO used in this reference design.

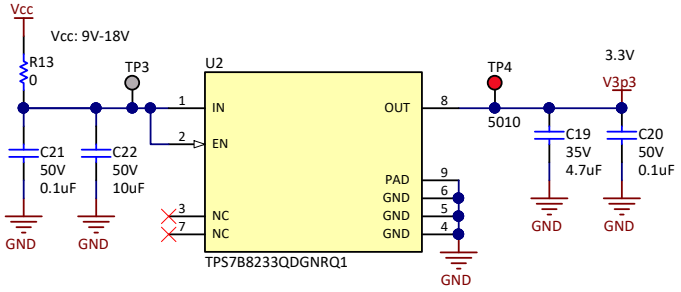
This device only requires input and output capacitors and no additional external components. The components used for the LDO were selected by following the *Detailed Design Procedure* section in the *TPS7B82-Q1 300-mA High-Voltage Ultralow-I_Q Low-Dropout Regulator* data sheet.

See Section 4.3 for the TPS7B82-Q1 layout guidelines in this reference design.

Table 8. Design Requirements for LDO

PARAMETER	VALUE
Input voltage range	6 V to 36 V
Output voltage	3.3 V
Output current	300 mA maximum

Figure 13. LDO Schematic



2.3.7 TMS320F28027 C2000™ Microcontroller

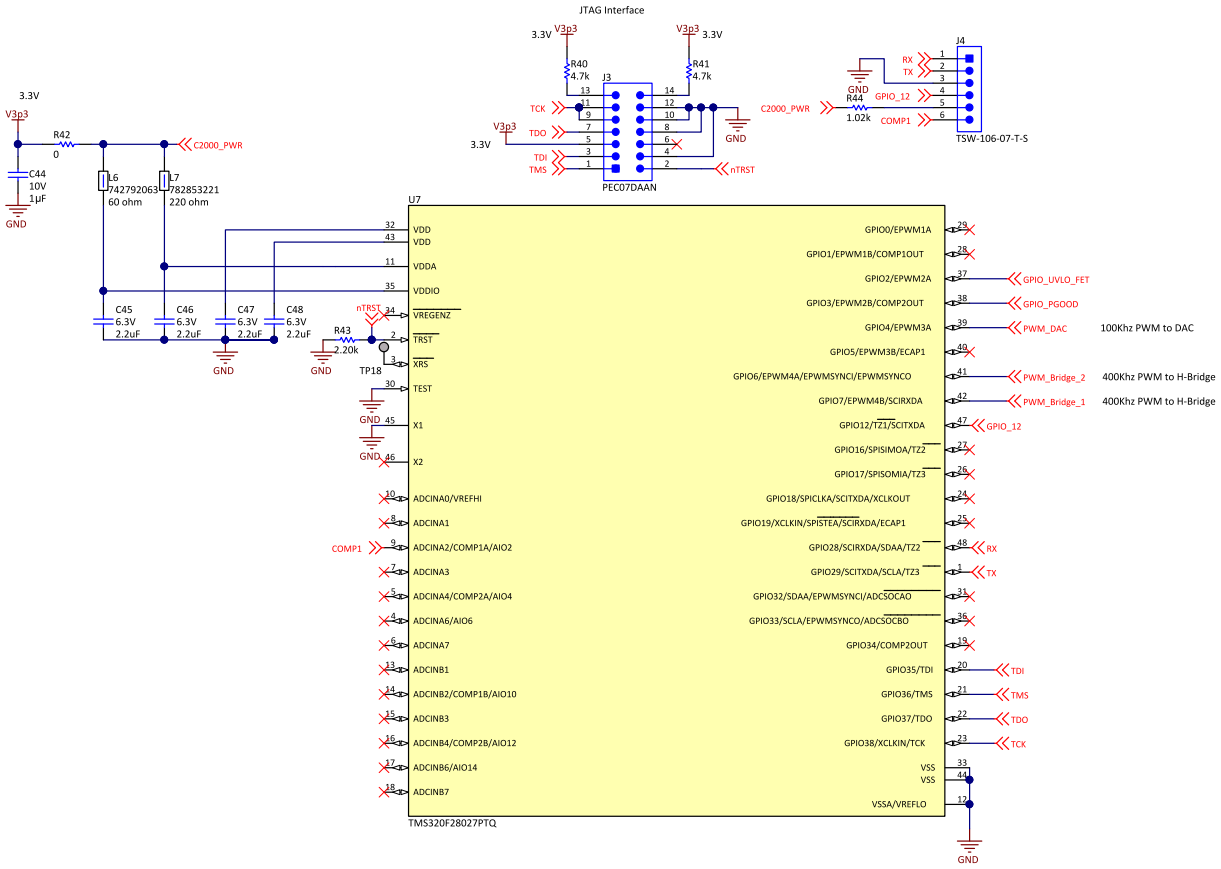
To create multiple adjustable PWM signals and monitor the system, the TMS320F28027 microcontroller is used in this system.

To run the PWM DAC and half-bridge drivers, 3 PWM signals are needed. PWM signals from module 3 are used to create the input signal for the half-bridge drivers. To create a complementary output with the 2 half-bridge drivers, PWM signals 3A and 3B run the opposite MOSFETs on either driver. For example, 3A drives the high-side FET on one driver and the low side FET on the other. The third PWM signal comes from module 3A and is used for the PWM DAC. See PWM DAC section for more information about this.

For system communication, GPIO28 and GPIO29 have been connected to headers. This can be used for SCI, UART, I2C communication. For additional control and monitoring options ADCA2, GPIO12, 3.3 V, and GND are also connected to headers.

To program the microcontroller a 14 pin JTAG header is present on the board. In testing this was programmed using a XDS100 v2.

Figure 14. TMS320F28027 Microcontroller Schematic



3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

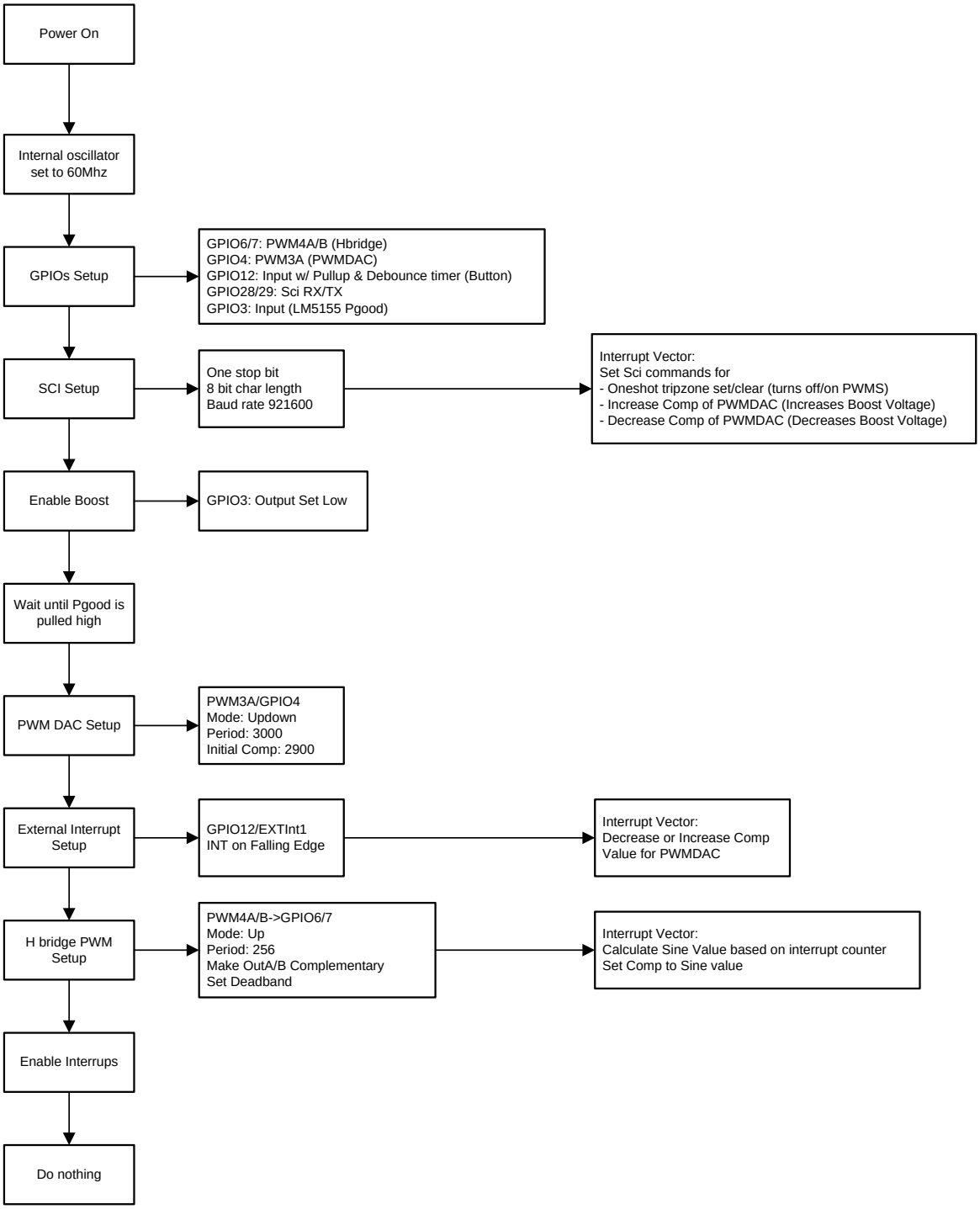
3.1.1 Hardware

A typical automotive battery voltage of 12 V can be applied to this design at jumper J1. The SmartGlass load or simulated load can be connected to the design at jumper J2. For communication and programming of the C2000 for debug, a 14-pin JTAG interface is found on header J3. Additional communication options with the MCU (extra GPIOs and UART/I2C communication) is found on header J4.

3.1.2 Software

Figure 15 is a basic reference for the software flow used to generate the signal to drive the glass.

Figure 15. Software Flow Chart



3.2 Testing and Results

3.2.1 Test Setup

This design was tested with a 38" × 20" panel of SPD-SmartGlass. The electrical requirements are listed in Table 9. The design was tested in parallel to two other reference designs and mounted to panel for demonstration purposes, as Figure 16 shows.

Table 9. Typical Electrical Requirements for SmartGlass

TECHNOLOGY	PEAK VOLTAGE REQUIREMENT	CURRENT (mA/ft^2)
SPD-SmartGlass	120 VAC @ 60 Hz	1.8

Figure 16. Test Setup of SPD-SmartGlass and TIDA-020013 mounted together

3.2.2 Test Results

3.2.2.1 Output Characteristics

The input voltage will impact the total RMS output power possible with the design. **Table 10** provides a reference for the possible output power of the design across the specified automotive battery input voltage range and Figure 17 provides a waveform of the typical sinusoidal output on one side of the half bridge.

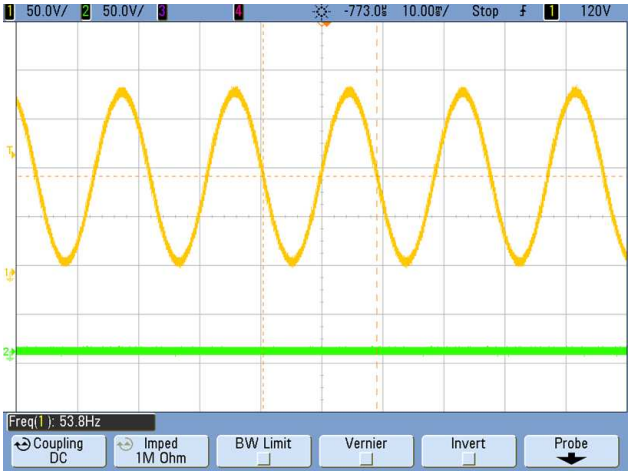
Table 10. Maximum Output Power Rating Across the Input Voltage Range

INPUT VOLTAGE	MAXIMUM RMS CURRENT (mA)	RMS OUTPUT POWER
9	50	7
10	56	7.84
11	66.67	9.3
12	82.35	11.53
13	107.69	15.08

Table 10. Maximum Output Power Rating Across the Input Voltage Range (continued)

INPUT VOLTAGE	MAXIMUM RMS CURRENT (mA)	RMS OUTPUT POWER
14	140	19.6
15	141.14	19.80
16	164.71	23.05
17	200	28
18	208.96	29.25

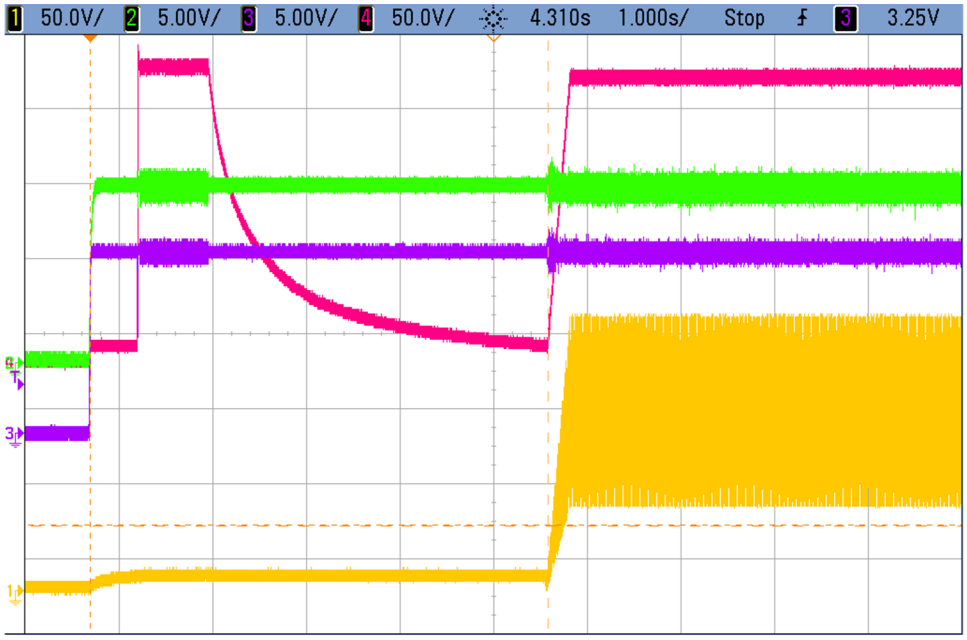
Figure 17. Sinusoidal Waveform Output



3.2.2.2 Complete System Startup

For initial power up of the design, a sequence is configured to allow the LM5155-Q1 boost to reach its maximum voltage. Send a Power Good to the microcontroller, configure the PWM DAC to decay down to a minimum voltage, and then ramp back up once the output stage PWM to generate the sine wave starts. This is done to minimize any potential damage to the output stage FETs from the large inrush current caused by the output stage filter capacitors.

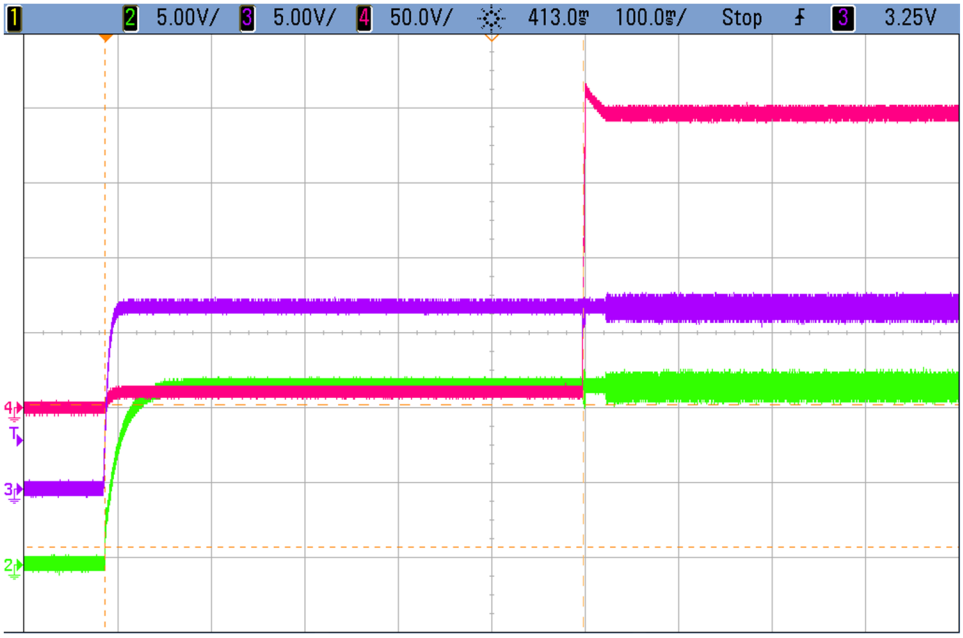
Figure 18. Complete System Startup



3.2.2.3 Boost Startup

A critical part of the design is a stable start up of the LM5155-Q1 device and charge pump to 200 V. Figure 19 provides a capture of this output upon application of 12 V to the design. Additionally, this waveform shows the power up of the TPS61041-Q1, providing a stable 12 V for the output stage gate drivers.

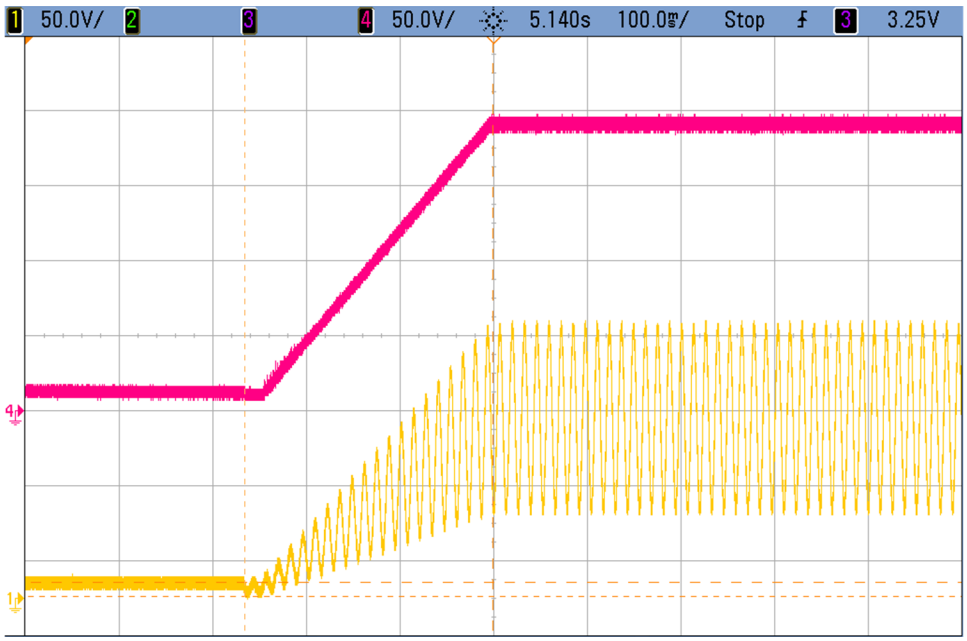
Figure 19. LM5155-Q1 and TPS61041-Q1 Boost Startup



3.2.2.4 Ramp Up of Sinusoid

After the 200-V boost has decayed down to approximately 10 V, the output stage PWM is enable and a sinusoidal waveform is generated. In combination with this, the PWMDAC linearly ramps the LM5155-Q1 output voltage to 200 V, allowing the SPD-Smartglass to be driven to its maximum level of clarity. This ramp also allows for a smooth transition of the glass from the dark to clear state.

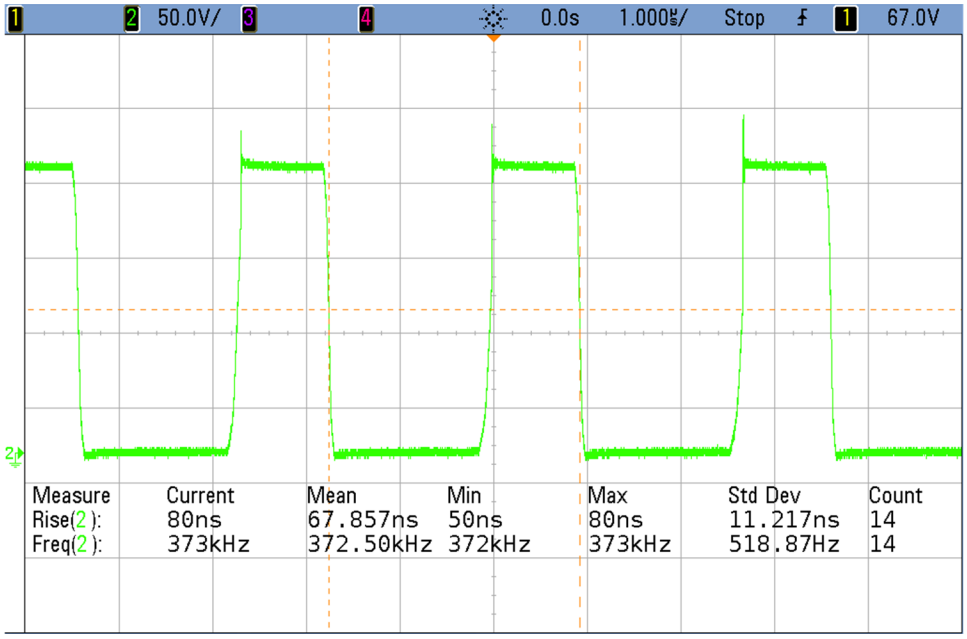
Figure 20. Ramp Up of Output Sinusoid



3.2.2.5 Switch Node

Figure 21 shows an example of the output stage switch node during normal operation.

Figure 21. Performance of the H-bridge as Seen at One of the Switch Nodes



3.2.2.6 PWM DAC Characteristics

provides details on the relationship of duty cycle settings of the PWM to controlling the output voltage of the LM5155-Q1 with the injection circuit.

Table 11. PWM and Duty Cycle Settings in Relation to LM5155-Q1 Output Voltage

DUTY CYCLE (%)	FILTERED PWM OUT (V)	LM5155-Q1 BOOST OUT (V)
80	2.7	10.6
74.5	2.5	23
68.3	2.29	38.5
62	2.07	55.2
55.3	1.86	71.85
49	1.64	88.1
42.8	1.43	104.7
36.1	1.21	121.1
29.8	1	137.5
23.6	0.795	153.8
16.8	0.585	170.3
10.6	0.37	186.5

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-020013.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-020013.

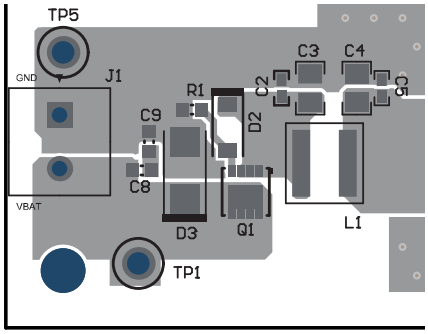
4.3 PCB Layout Recommendations

For PCB layout, follow the guidelines provided in the data sheet for each device. Additional comments about the PCB layout are in the following sections.

4.3.1 Input Filter Protection

Figure 22 shows the top view of the TIDA-020013 board. The two ESD capacitors C8 and C9 are placed in an L-shape to ensure that, in the case of a mechanic fault (the PCB bending), the capacitors will not fail open and will still protect from ESD. The bottom layer of this board is a ground pour but has been removed below the input protection and filtering. This was done intentionally to prevent coupling of input noise onto the ground plane.

Figure 22. Layout of Input Filter



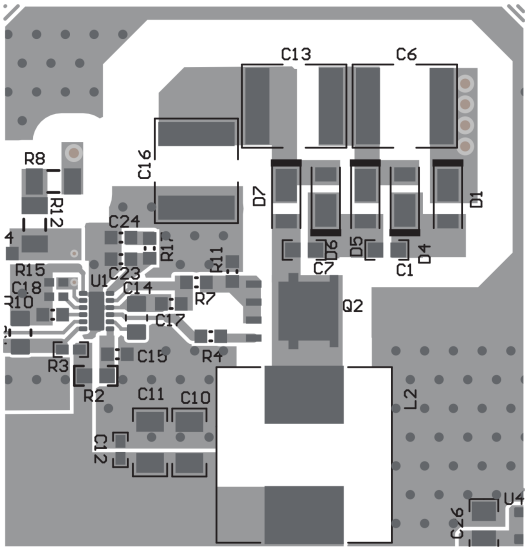
4.3.2 LM5155-Q1 Layout

The LM5155-Q1 is positioned to minimize:

1. The length of the gate drive trace
2. The length of the current sense trace.
3. The two above points should also allow for not crossing of signals
4. Keep the device out of any high di/dt current loops

The ground nodes AGND (analog ground) and PGND (power ground) should be split on separate planes and start connected to the exposed pad of the LM5155-Q1. This helps maximize the impact of ground noise on the system. AGND signals include the RT resistors, SS capacitor, UVLO resistor divider, and FB pins. PGND signals are tied to the CS and COMP pins.

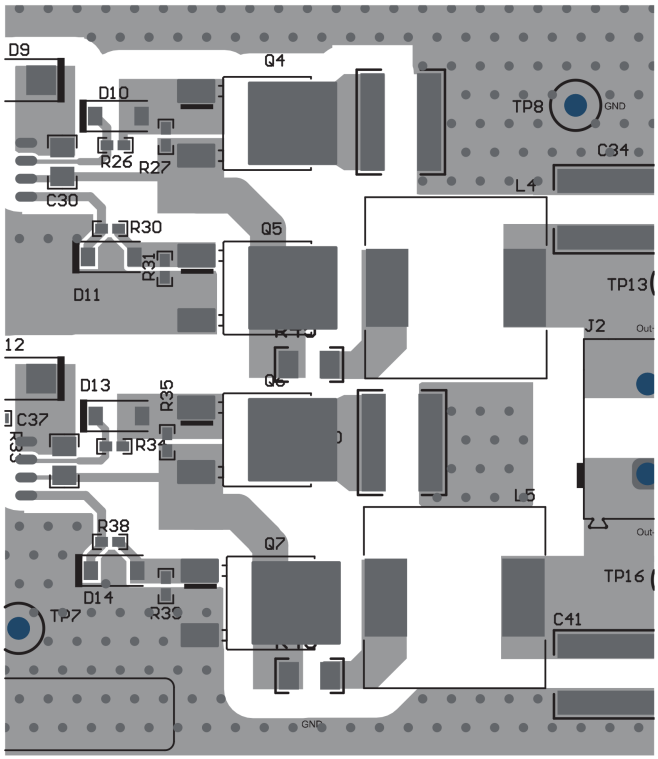
Figure 23. Layout of LM5155-Q1



4.3.3 High-Voltage Layout Blankets and Spacing

To separate high-voltage areas from low voltage areas, schematic blankets are used. Spacing of 80-mil was used in this design and based off the physical spacing of a 1206 capacitor, the smallest standard package that has ratings up to 200 V. This spacing may need to be changed according to system spacing requirements.

Figure 24. Layout of High Voltage Full Bridge



4.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-020013.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-020013.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-020013.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-020013.

5 Software Files

To download the software files, see the design files at TIDA-020013.

6 Related Documentation

1. Texas Instruments, *LM5155-Q1 2.2-MHz Wide Input Nonsynchronous Boost, Sepic, Flyback Controller*
2. Texas Instruments, *UCC27712-Q1 Automotive, 620-V, 1.8-A, 2.8-A High-Side Low-Side Gate Driver with Interlock*
3. Texas Instruments, *TMS320F2807x Piccolo™ Microcontrollers*

6.1 Trademarks

6.2 Third-Party Products Disclaimer

7 About the Author

DAVID SHUMATE worked on this design as a part of the Application Rotation Program at TI, and is now a Field Applications Engineer focusing on Automotive electronics.

MATT SULLIVAN is a systems engineer on the Automotive Body Electronics and Lighting team. He designs and tests reference designs for a wide variety of interior vehicle electronics, including body sensors, overhead console, mirrors, auxiliary power and more. He graduated from the University of Southern California with a B.S.E.E.

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Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://ti.com/customer support for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

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   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non-conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:

   As a precautionary measure, it is always good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.

   a. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   b. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   c. Once EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety
   a. Wear personal protective equipment e.g. latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2018) to A Revision	Page
• Added additional information to *LC Filter* section	11
• Added *Complete System Startup* section	16
• Added additional information to *Boost Startup* section	17
• Changed title of *Boost Startup* image to *LM5155-Q1 and TPS61041-Q1 Boost Startup*	17
• Changed *LM5155-Q1 and TPS61041-Q1 Boost Startup* image	17
• Added *Ramp Up of Sinusoid* section	18
• Added *Switch Node* section	18
• Changed duty cycle value in *PWM and Duty Cycle Settings in Relation to LM5155-Q1 Output Voltage* table	19
• Changed *Layout of LM5155-Q1* image	21
• Changed *Layout of High Voltage Full Bridge* image	21

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