Design Guide: TIDEP-01017

Cascade Imaging Radar Capture Reference Design Using Jacinto™ ADAS Processor

Description

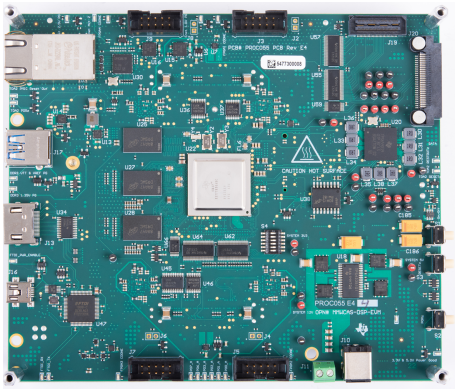
This reference design provides a processing foundation for a cascaded imaging radar system. Cascade radar devices can support front, long-range (LRR) beam-forming applications as well as corner- and side-cascade radar and sensor fusion systems.

This reference design provides qualified developers the design materials to create a functioning software evaluation platform for developing and testing ADAS applications. The design shortens the development time of a base platform supporting multiple automotive radar front end and antenna subsystems.

Resources

TIDEP-01017	Design Folder
TDA2SX	Product Folder
VisionSDK	Tool Folder
TIDEP-01012	Design Folder

TI E2E™ Community — ASK Our E2E™ Experts

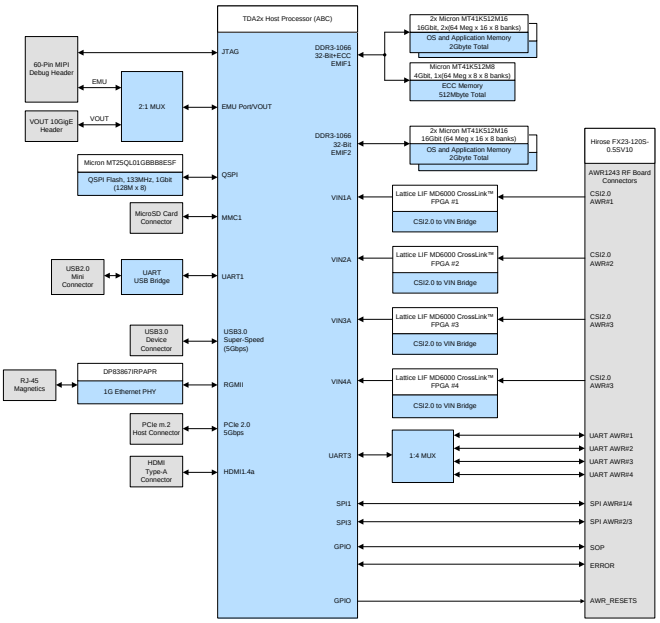


Features

- Compatible with SVTronics AWRx CIR radar antenna reference design
- 4 × Lattice CrossLink™ FPGA-based interfaces (1 each, per AWRx)
- High-performance TDA2x device with 4 radar processing SIMD accelerators (1 EVE per AWRx)
- Ethernet and PCIe connectivity for control and data respectively

Applications

- Long-range radar
- Imaging radar
- Drive assist ECU
- Radar ECU
- Medium and short range radar
- ADAS domain controller



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

Autonomous control of a vehicle provides quality-of-life and safety benefits in addition to making the relatively mundane act of driving safer and less difficult. The quality-of-life features include the ability of a vehicle to park itself, or to determine whether a lane change is possible, and provide features like automatic cruise control—where a vehicle maintains a constant distance with respect to the car ahead of it, essentially, tracking the velocity of the car in front of it. Autonomous braking and collision avoidance are safety features that prevent accidents caused by driver inattention. These features work by observing the area in front of a car and alerting the ADAS subsystems if obstacles are observed that are likely to hit the car. Implementing these technologies requires a variety of sensors to detect obstacles in the environment and track their velocities and positions over time.

1.1 Key System Specifications

This reference design has two sets of specifications because the radar is used as a multi-mode radar. MIMO is the first specification. TX beamforming (TXBF) is the second specification,

Table 1. Key System Specifications

RECOMMENDED OPERATING CONDITIONS	MIN	TYP	MAX
Input voltage (V_{IN})	6 V	12 V	24 V

1.2 Why Cascade Radar?

Frequency-modulated continuous-wave (FMCW) radars allow the accurate measurement of range and relative velocity of obstacles and other vehicles; therefore, radars are useful for autonomous vehicular applications (such as parking assist and lane change assist) and car safety applications (autonomous breaking and collision avoidance). An important advantage of radars over camera and light-detection-and-ranging (LIDAR)-based systems is that radars are relatively immune to environmental conditions (such as the effects of rain, dust, and smoke). FMCW radars can work in complete darkness and also bright daylight (radars are not affected by glare) because they transmit and receive electromagnetic waves. When compared with ultrasound, radars typically have a much longer range and much faster time of transit for their signals.

Despite the many advantages of radar technology, in many cases, automotive manufacturers today still use camera sensors as the primary sensor technology used to make final safety decisions in the system.

The radar sensor is being used as the secondary sensor; meaning, the vehicle system receives the Radar warning, but decides to take an action only upon the camera sensor verification. The main reason is limitation in radar angular resolution. The radar sensors deployed today in most vehicles lack the ability to distinguish between static objects with the same range and same relative velocity.

Today, a typical front radar sensor has about a 5-degree angular resolution that corresponds to the ability of the sensor to distinguish between objects that are 8.5 m apart at 100 m. Objects that are closer than 8.5 m appear as one object. For example, a vehicle stopped in the right lane, might look like a shoulder road street lamp for example, and therefore would be ignored by the safety system.

This is about to change with the introduction of the Imaging Radar solution from Texas Instruments (TI).

The TI Imaging Radar is a four-chip cascade solution, that acts like a single-chip sensor but achieves $20Log10(N_{TX})$ SNR gain in TX beamforming mode and 360/(N*pi) angular resolution (N is the number of virtual antennas in a MIMO configuration).

The TI Imaging Radar solution, we can distinguish between static objects 0.6 degrees apart with all antennae placed in single dimension linearly, and reach a 350-m object detecting range(angular resolution is dependent on the antenna configuration and the number of TX/RX antennae).

This performance enables TI Imaging Radar to become the primary sensor in the vehicle and enhance safety across weather and visibility conditions by providing a high-resolution image for both static and moving objects.

1.3 TI Cascade Radar Design

The TIDEP-01017 provides an easy-to-use, detailed reference design of a base platform, based on the TDA2x, supporting multiple automotive radar front end and antenna sub-systems. This reference design can be used as a starting point to design a standalone sensor for a variety of LRR and imaging radar applications.

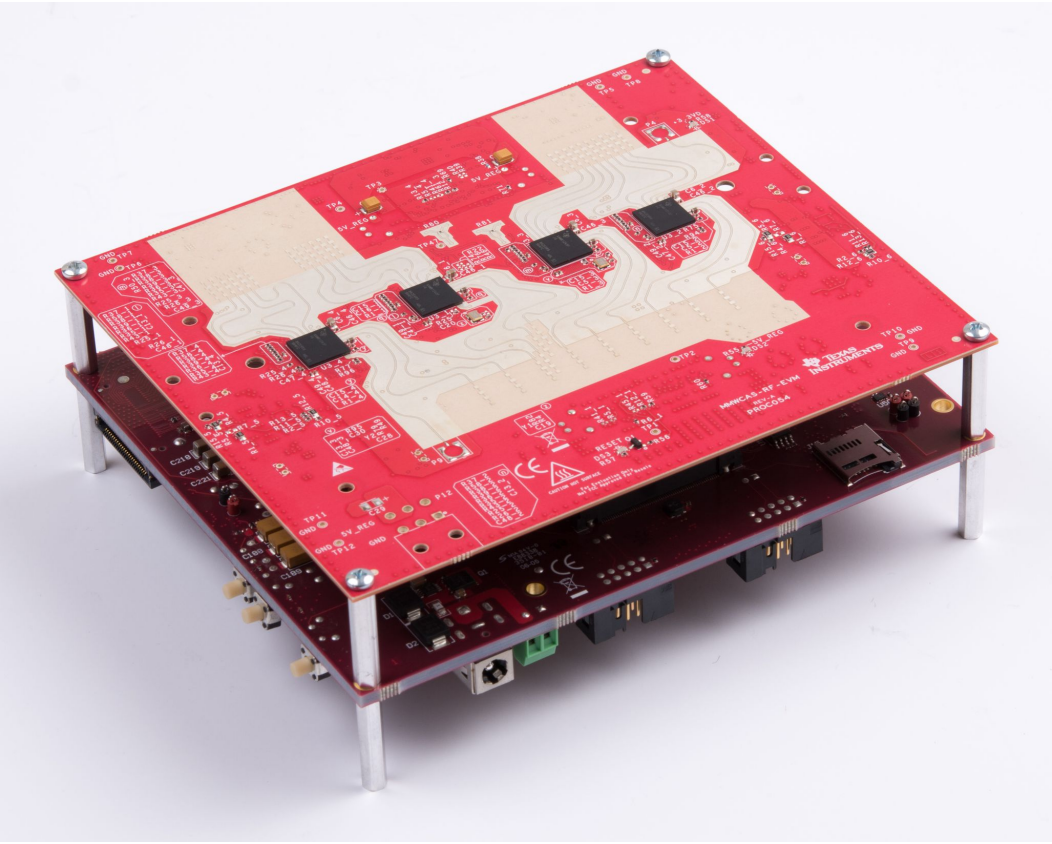
The base platform, or host board, works with the TI Cascade RF reference design, or RF board based on the AWR1243P device.

The flexible chirp and frame timing engine available on the AWR1243P device (similar to other AWR family mmWave sensors) allows the system to function as a multi-mode radar, interleaving beamforming and MIMO configurations on a per-chirp basis. This enables the sensor designer to achieve best range and best angular resolution across the array of Cascaded AWR1243P devices as the scene dynamics requires.

A beamforming antenna across multiple, cascaded, AWR1243P devices provides sensor designers with higher-output power and therefore, lower detectable target RCS or increased range detection, or both. Applications requiring detection of automobile, motorcycle, pedestrian, signage, bridges, and other road-way objects and barriers at or beyond a 350-m range can make use of this mode of operation.

In medium-range applications (150-m ranges), creating MIMO antenna arrays across multiple, cascaded, AWR1243P devices allows the sensor designer to maximize the number of active antennas enabling substantially improved angular resolution. This enables sub-1 degree resolution: true imaging radar capability.

Figure 1. AWR1243P Four-Device Cascade Radar RF Radar Board

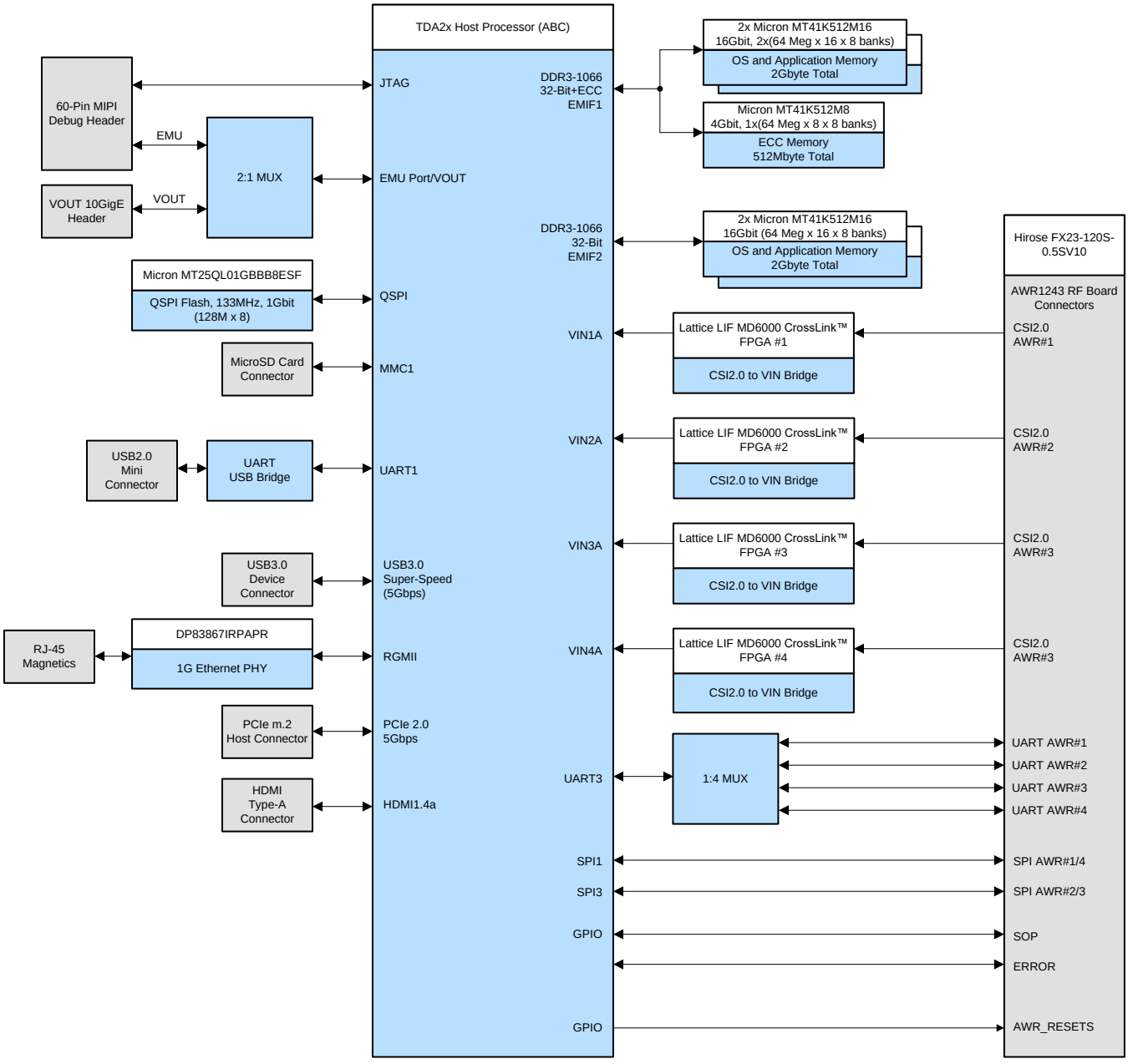


2 System Overview

2.1 Block Diagram

Figure 2 shows the block diagram of the cascade radar host processor board.

Figure 2. Cascade Radar Host Processor Block Diagram



2.2 Design Considerations

2.2.1 Cascade Radar Host Board based on TDA2x Application Processor

This cascade radar host board reference design supports the TDA2x application processor. TI designed the TDA2x System-on-Chip (SoC) as a highly-optimized and scalable family of devices to meet the requirements of leading Advanced Driver Assistance Systems (ADAS). The TDA2x family enables broad ADAS applications in automobiles by integrating an optimal mix of performance, low power and ADAS vision analytics processing that aims to facilitate a more autonomous and collision-free driving experience.

The TDA2x SoC enables sophisticated embedded vision technology in automobiles by broadest range of ADAS applications including front camera, park assist, surround view and sensor fusion on a single architecture

The TDA2x SoC incorporates a heterogeneous, scalable architecture that includes a mix of TI's fixed and floating-point TMS320C66x digital signal processor (DSP) cores, Vision AccelerationPac, Arm® Cortex®-A15 MPCore™ and dual Cortex-M4 processors. The integration of a video accelerator for decoding multiple video streams over an Ethernet AVB network, along with graphics accelerators for rendering virtual views, enable a 3D viewing experience. In addition, the TDA2x SoC also integrates a host of peripherals including multi-camera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN and GigB Ethernet AVB.

The Vision AccelerationPac for this family of products includes multiple embedded vision engines (EVEs) offloading the perception analytics functionality from the application processor while also reducing the power footprint. The Vision AccelerationPac is optimized for perception processing with a 32-bit RISC core for efficient program execution and a vector coprocessor for specialized perception processing.

Additionally, TI provides a complete set of development tools for the Arm, DSP, and EVE coprocessor, including C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a debugging interface for visibility into source code execution.

The TDA2x ADAS processor is qualified according to the AEC-Q100 standard.

2.2.2 Cascade Radar RF Board Based on AWR1243P Sensor

The Cascade Radar RF board is built around the AWR1243P device. The AWR1243P is an integrated single-chip, frequency modulated continuous wave (FMCW) sensor capable of operation in the 76 to 81 GHz frequency band. Built with TI's low-power, 45-nm RFCMOS processor and enabling unprecedented levels of analog and digital integration, the AWR1243P achieves an extremely small form factor. The device has four receivers and three transmitters with a closed-loop phase-locked loop (PLL) for precise and linear chirp synthesis.

Each transmitter includes a programmable 6-bit phase shifter (5.625 degree step) to enable beamforming applications. Each device also includes two 20-GHz local oscillator (LO) output and two 20-GHz LO input paths for sharing the VCO output with neighboring devices. This enables a cost-effective, totally passive, cascaded radar architecture.

The sensor includes a built-in self test (BIST) for RF calibration and safety monitoring. Based on complex baseband architecture, the sensor device supports an IF bandwidth of 15 MHz with reconfigurable output sampling rates in both complex and real sampling modes. Two separate ARM Cortex R4F based processors run the TI provided the radar front-end, calibration, and host processor interface firmware targeting ASIL-B compliance.

2.2.3 TDA2x Reference Design Use Cases and Specifications

The RF board dictates this reference design's use cases and specifications, and has two sets of specifications because the radar is used as a multi-mode radar: MIMO and T TX beamforming (TXBF).

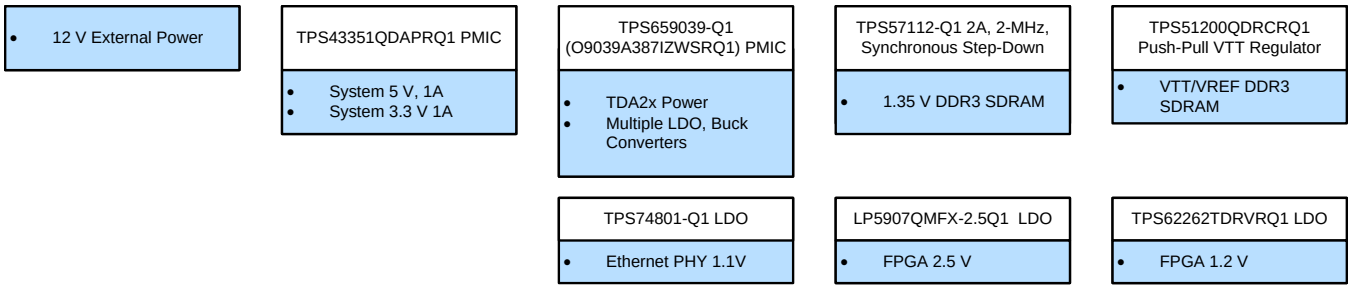
Table 2. Cascade MIMO and Cascade Beamforming specifications

PARAMETER	SPECIFICATIONS (MIMO)	SPECIFICATIONS (TXBF)	DETAILS
Maximum range	150 m	350 m	This represents the maximum distance that the radar can detect an object representing an RCS of approximately 10 m2.
Range resolution	60 cm	150 cm	Range resolution is the ability of a radar system to distinguish between two or more targets on the same bearing but at different ranges. The resolution is configurable, so the provided number is just an example.
Azimuth angle resolution	1.4 degrees	1.4 degrees (with multiple beam steering)	Angle resolution is the ability of a radar system to distinguish between two or more targets with the same range and velocity but different angles. The resolution is equivalent in both applications.
Elevation angle resolution	18 degrees	NA	Elevation angle resolution is only available for MIMO application given the antenna design on the TI cascade RF board.
Maximum velocity	133 kmph	133 kmph	This is the native maximum velocity obtained using a two-dimensional FFT on the frame data. For TDM MIMO case, velocity compensation algorithm is applied to recover the native maximum velocity. This specification will be improved over time by showing how higher-level algorithms can extend the maximum measurable velocity beyond this limit.
Velocity resolution	0.53 kmph	0.53 kmph	This parameter represents the capability of the radar sensor to distinguish between two or more objects at the same range but moving with different velocities.

2.2.4 Power Considerations

Figure 3 shows the various power management devices necessary to provide the various voltage domains necessary for operation of the host board.

Figure 3. Cascade Radar Host Processor Power Block Diagram



In addition, the Cascade RF board accepts 5-V DC, 8-A (max) power through the host board connectors. The primary 5-V system rail shall be converted into the various AWR12x device rails by a pair of LP87524P, quad-channel, monolithic, buck-converters.

Table 3. High-Level System Features of Cascade Radar RF board

	CASCADE RADAR RF BOARD
4 × AWR1243P 76–81GHz radar SoC	Integrated VCO, LO distribution, PA, LNA, ADC, 3 TX and 4 RX ARM MCU R4 Controller
AWR RF PERIPHERALS	
12 × TX, 16 × RX antennas	12 total transmitters across all 4 AWR1243 P devices 16 total receivers across all 4 × AWR1243P devices
Azimuth array	86 element virtual array – enabling 1.4 degree angular resolution
Elevation array	4 element virtual array – enabling 28 degree angular resolution
Embedded antenna	Rogers RO3003 4-element, series-fed, patch antenna
20-GHz LO Star distribution	2 × passive Wilkinson Power dividers fed by the Master AWR12x device LO output to Slave AWR12x devices and Master AWR12x device
AWR DIGITAL PERIPHERALS	
Clock distribution	LMK00804B low-jitter clock distribution
Digital sync distribution	LMK00804B low-jitter clock distribution
CSI2.0 4-lane	600Mbps/Lane, max 2.4Gbps ADC IF data per device
QSPI Flash	16-Mbit QSPI flash for AWR firmware updates
Serial peripherals	SPI, I2C, UART, GPIO
System temperature	TMP112 I2C Temperature Sensors
POWER	
Radar power management IC (PMIC) solution	2 × LP87524P-Q1 Quad-Channel, Integrated FET, Buck Converters and LC filtering solution

2.2.5 Cascade Host System Features

Table 4. High-Level System Features of Cascade Radar Host board

	CASCADE RADAR HOST BOARD
Host processor	TDA2SX ADAS SoC
CPU	Dual-core ARM A15, 1176 MHz
DSP	2 × C66x, 750 MHz
GPU	Dual-core SGX544 GPU, 532 MHz
EVE co-processor	4 × EVE Matrix co-processor, 532 MHz
IVA co-processor	2 × IVA Image co-processor, 532 MHz
Memory	2 × 32-bit, 2GByte, DDR3L-1066 SDRAM (one bank ECC capable)
USB	USB3.0 host and USB2.0 host
CSI2.0	4 × 4-lane CSI2.0, 900Mbps
Video out	24-bit digital video out, HDMI 1.4b
Connectivity	1 Gigabit Ethernet, USB2.0 serial port (TI RTOS/ Linux console)
Data storage	PCIe 2.0 m.2 connector(M-Keyed), 1 Gigabit NOR flash, MicroSD card
Mechanical	160-mm × 140-mm - two automotive rated board to board connectors
Software	TI RTOS with radar SDK packages, TI processors SDK Linux distribution with radar SDK packages, algorithm support via VSDK 3.07

2.2.6 AWR1243P Cascade RF Board Architecture

The AWR1243P Cascade RF board consists of four AWR1243P 77-GHz radar devices and their associated power, clocking, synchronization, LO, and RF circuits.

Each AWR1243P RF, RX, and TX port is routed to its own set of etched, patch antenna. Each AWR1243P on the RF board has a 4-port CSI2.0 transmitter that is used for sending radar data to a host processor CSI2.0 receiver set. The entire AWR1243P configuration, control, and reset lines are made available on two host-interface connectors implemented with Hirose FX32 series connectors.

The AWR1243P devices are separated into master and slave devices classes. AWR1243P #1, the master device, uses the AWR1243P architecture built in LO distribution, clock distribution and frame synchronization distribution to provide 40-MHz clock, 20-GHz LO, and digital frame synchronization to the other three slave devices – AWR1243P #2, #3 and #4. This allows the system to generate and receive coherent FMCW chirps across the 4 AWR1243P device array of transmitters and receivers; enabling beamforming and MIMO operation across the array of devices.

The 20-GHz LO distribution follows the start-network configuration described in the AWR1243 Cascade Radar Application Note, SWRA574A. With the master AWR1243P #1 feeding a network of two Wilkinson power dividers, that provide synchronous LO for the Master and Slave RF PA and mixer subsystems. All clock distribution, synchronization distribution, and LO distribution requirements are documented the *Programming Chirp Parameters in TI Radar Devices* Application Report.

The Cascade RF board accepts 5-V DC, 8-A (max) power through the host board connectors. The primary 5-V system rail can be converted into the various AWR12x device rails by a pair of LP87524P, quad-channel, monolithic, buck-converters.

2.2.7 20-GHz Local Oscillator (LO) Distribution

20-GHz LO distribution to all AWR1243P devices is accomplished through an entirely passive, transmission-line and etched power divider network. By using the dual LO outputs and LO inputs provided on each AWR1243P device, all devices including the master device, receive the same master device generated LO output. This results in all package and die routing delays common across all devices. The PCB designer is left with the task of delay matching only the BGA to BGA delays.

By using both of the 6-dBm (typical) LO output, and minimizing transmission line and power divider losses, no external amplifiers are required to be added to the LO network. Additionally, by outputting 20-GHz LO versus full 77-GHz RF for RF synchronization, the LO PCB link budgets can be more relaxed.

The passive LO distribution network and relaxed link budget results in more PCB design flexibility and a lower overall system cost.

Figure 4 shows the block diagram of the delay matched LO distribution. Figure 5 shows the implemented Wilkinson power dividers in GCPW transmission-line. Fanout from the AWR1243P devices and power dividers is through GCPW lines. The majority of the LO distribution length is carried through an internal Stripline layer.

Figure 4. 20-GHz LO Distribution Block Diagram

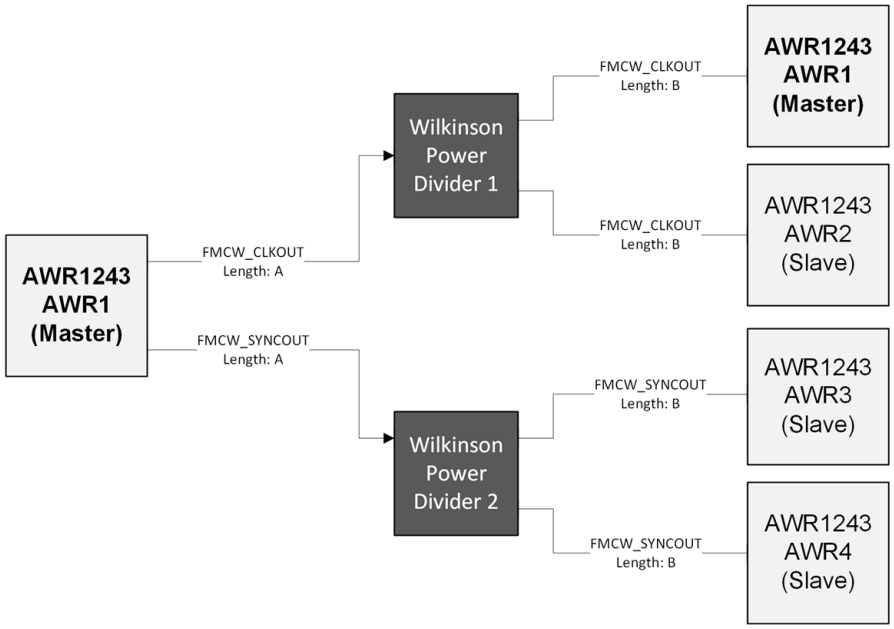
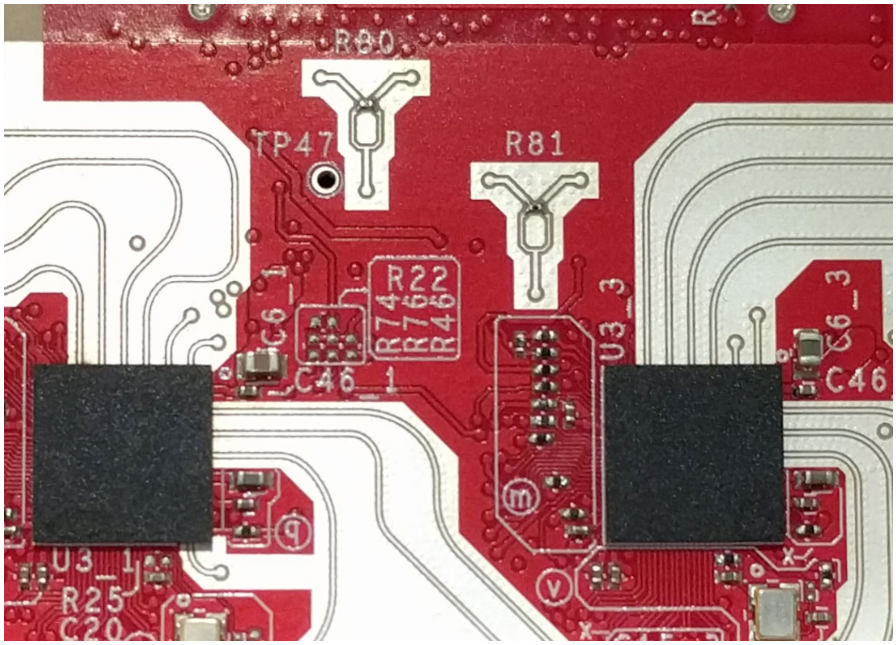


Figure 5. 20-GHz LO Distribution Board Implementation



2.3 Highlighted Products

2.3.1 TDA2SXBTQABCQ1

TI's new TDA2x System-on-Chip (SoC) is a highly optimized and scalable family of devices designed to meet the requirements of leading Advanced Driver Assistance Systems (ADAS). The TDA2x family enables broad ADAS applications in automobiles by integrating an optimal mix of performance, low power and ADAS vision analytics processing that aims to facilitate a more autonomous and collision-free driving experience.

The TDA2x SoC enables sophisticated embedded vision technology in automobiles by broadest range of ADAS applications including front camera, park assist, surround view and sensor fusion on a single architecture.

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Additionally, TI provides a complete set of development tools for the Arm, DSP, and EVE coprocessor, including C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a debugging interface for visibility into source code execution.

2.3.2 TPS43351-Q1

The and TPS43351-Q1 device includes two current-mode synchronous buck controllers designed for the harsh environment in automotive applications. The device is ideal for use in a multi-rail system with low quiescent requirements, because it automatically operates in low-power mode (consuming typically 30 µA) at light loads. The device offers protection features such as thermal, soft-start, and overcurrent protection. During short-circuit conditions of the regulator output, activation of the current-foldback feature can limit the current through the MOSFETs for control of power dissipation. The two independent soft-start inputs allow ramp-up of the output voltage independently during start-up.

The programmable range of the switching frequency is from 150 kHz to 600 kHz, as is the frequency of an external clock to which the devices can synchronize. Additionally, the TPS43351-Q1 device offers frequency-hopping, spread-spectrum operation.

2.3.3 TPS62262-Q1

The TPS6226x-Q1 devices are high-efficiency synchronous step-down dc-dc converters optimized for battery-powered applications. The devices provide up to 600-mA output current from a single Li-Ion cell

and are ideal to power mobile phones and other portable applications.

With a wide input voltage range of 2 V to 6 V, the device supports applications powered by Li-Ion batteries with extended voltage range, two- and three-cell alkaline batteries, 3.3-V and 5-V input voltage rails.

The TPS6226x-Q1 devices operate at 2.25-MHz fixed switching frequency and enter power-save-mode operation at light load currents to maintain high efficiency over the entire load-current range.

The power-save mode is optimized for low output-voltage ripple. For low-noise applications, the devices can be forced into fixed-frequency PWM mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 µA. The TPS6226x-Q1 devices allow the use of small inductors and capacitors to achieve a small solution size.

2.3.4 TPS659039-Q1

The TPS659039-Q1 device is an integrated power-management integrated circuit (PMIC) for automotive applications. The device provides seven configurable step-down converters with up to 6 A of output current for memory, processor core, input-output (I/O), or preregulation of LDOs. One of these configurable step-down converters can be combined with another 3-A regulator to allow up to 9 A of output current. All of the step-down converters can synchronize to an external clock source between 1.7 MHz and 2.7 MHz, or an internal fall back clock at 2.2 MHz. The TPS659039-Q1 device contains six LDO regulators for external use. This LDO regulator can be supplied from either a system supply or a preregulated supply. The power-up and power-down controller is configurable and supports any power-up and power-down sequences (OTP based). The TPS659039-Q1 device includes a 32-kHz RC oscillator to sequence all resources during power up and power down. In cases where a fast start up is needed, a 16-MHz crystal oscillator is also included to quickly generate a stable 32-kHz for the system. All LDOs and SMPS converters can be controlled by the SPI or I^2C interface, or by power request signals. In addition, voltage scaling registers allow transitioning the SMPS to different voltages by SPI, I^2C, or roof and floor control. One dedicated pin in each package can be configured as part of the power-up sequence to control external resources. General-purpose input-output (GPIO) functionality is available and two GPIOs can be configured as part of the power-up sequence to control external resources. Power request signals enable power mode control for power optimization. The device includes a general-purpose (GP) sigma-delta analog-to-digital converter (ADC) with three external input channels. The TPS659039- Q1 device is available in a 13-ball × 13-ball nFBGA package with a 0,8-mm pitch.

2.3.5 TPS57112-Q1

The TPS57112-Q1 device is a full-featured 6-V, 2-A, synchronous step-down current-mode converter with two integrated MOSFETs.

The TPS57112-Q1 device enables small designs by integrating the MOSFETs, implementing current-mode control to reduce external component count, reducing inductor size by enabling up to 2-MHz switching frequency, and minimizing the IC footprint with a small 3-mm × 3-mm thermally enhanced QFN package.

The TPS57112-Q1 device provides accurate regulation for a variety of loads with a ±1% voltage reference (V_{ref}) over temperature.

The integrated 12-mΩ MOSFETs and 515-μA typical supply current maximize efficiency. Using the enable pin to enter the shutdown mode reduces supply current to 5.5 μA, typical.

The internal undervoltage lockout setting is 2.45 V, but programming the threshold with a resistor network on the enable pin can increase the setting. The slow-start pin controls the output-voltage start-up ramp. An open-drain power-good signal indicates when the output is within 93% to 107% of its nominal voltage.

Frequency foldback and thermal shutdown protect the device during an overcurrent condition.

2.3.6 TPS51200-Q1

The TPS51200-Q1 device is a sink and source double-data-rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The TPS51200-Q1 device maintains a fast transient response and only requires a minimum output capacitance of 20 μF. The TPS51200-Q1 device supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, low power DDR3 and DDR4 VTT bus termination.

In addition, the TPS51200-Q1 device provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

The TPS51200-Q1 device is available in the thermally-efficient VSON-10 package, and is rated both green and Pb-free. The device is specified from –40°C to 125°C.

2.3.7 TPS74801-Q1

The TPS74801-Q1 low-dropout (LDO) linear regulator provides an easy-to-use robust power management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. The soft-start is monotonic and well-suited for powering many different types of processors and ASICs. The enable input and power good output allow easy sequencing with external regulators. This complete flexibility permits the user to configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

A precision reference and error amplifier deliver 2% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor greater than or equal to 2.2 μF, and is fully specified from –40°C to 105°C for the DRC package, and from –40°C to 125°C for the RGW package. The TPS74801-Q1 device is offered in a small 3-mm × 3-mm VSON-10 package, yielding a highly compact, total solution size. It is also available in a 5 × 5 QFN-20 for compatibility with the TPS74401.

2.3.8 LP5907-Q1

The LP5907-Q1 is a low-noise LDO that can supply 250 mA of output current. Designed to meet the requirements of RF and analog circuits, the LP5907-Q1 provides low noise, high PSRR, low quiescent current, and low line or load transient response figures. Using new innovative design techniques, the LP5907-Q1 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement.

The device is designed to work with a 1-μF input and a 1-μF output ceramic capacitor (no separate noise bypass capacitor is required).

This device is available with fixed output voltages from 1.2 V to 4.5 V in 25-mV steps. Contact Texas Instruments Sales for specific voltage option needs.

2.3.9 DP83867

The DP83867 device is a robust, low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols. Optimized for ESD protection, the DP83867 exceeds 8-kV IEC 61000-4-2 (direct contact).

The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low latency and provides IEEE 1588 Start of Frame Detection.

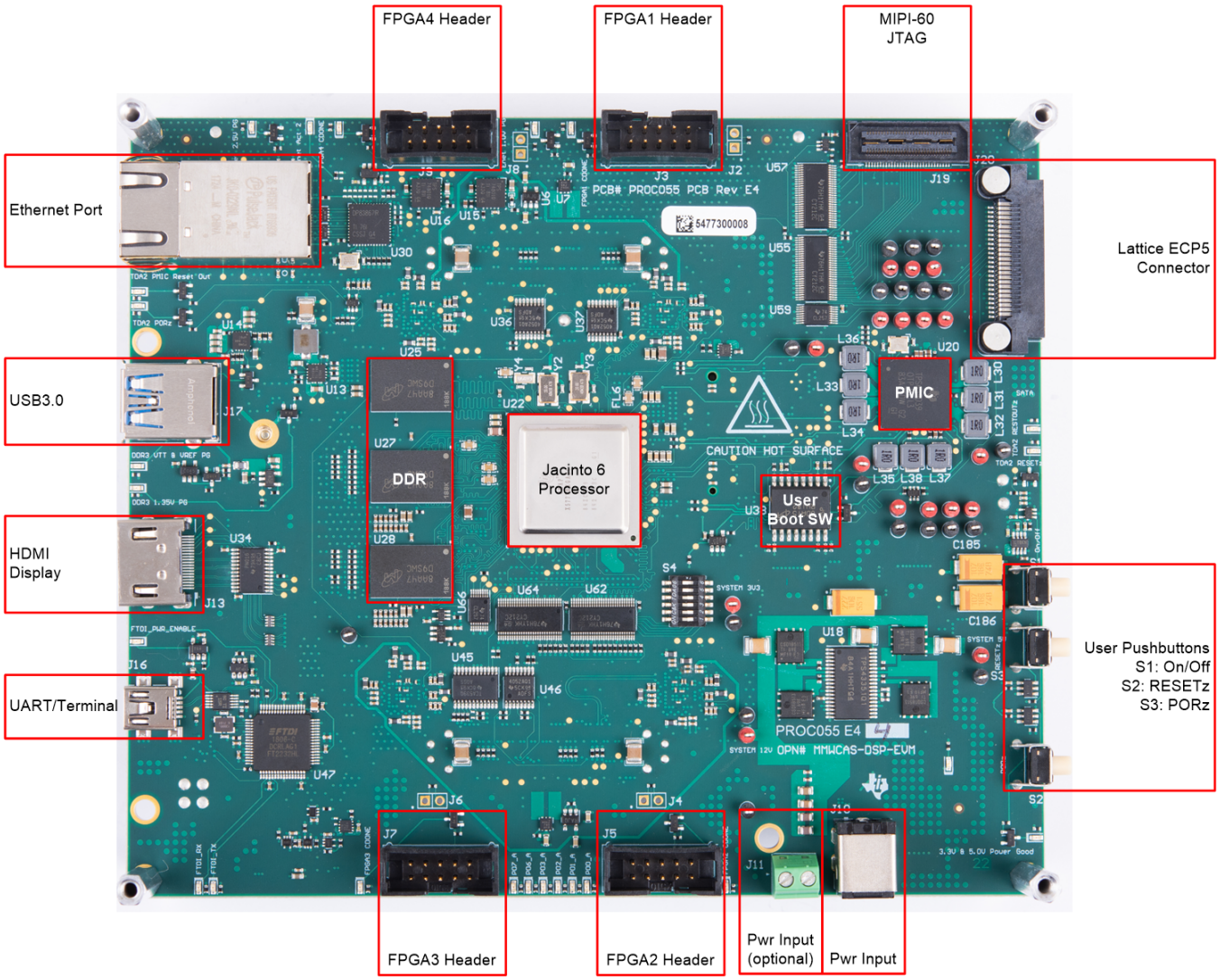
3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

Figure 6 shows the parts on the CPU.

Figure 6. CPU Board – Front



3.1.1.1 Boot Mode

Table 5 lists the supported boot modes. A ‘1’ for the switch configuration indicates ‘ON’, a ‘0’ for the switch configuration indicates ‘OFF’

Table 5. Supported Boot Modes

BOOT MODE	SW1 CONFIGURATION [5:0]
USB boot	010000
UART boot	010011
eMMC boot	111000
eMMC boot partition	111011
SD boot	110000

3.1.1.2 User Pushbuttons

There are three user pushbuttons on the design, as described in Table 6.

Table 6. Pushbutton Table

PUSHBUTTON	DESCRIPTION
S1	Board On/Off. By default button is disabled. Refer to SCH for resistor options.
S2	Generates a PORz reset
S3	Generates a RESETz on SoC

3.1.2 Software

VSDK 3.07 contains algorithms that run on the TDA2x for the Cascade Radar application. The latest VSDK is available at from *Processor SDK for TDAx ADAS SoCs - Linux and TI-RTOS Support*.

3.2 Testing and Results

Multiple test scenarios were setup to explore the capabilities of the Cascade Radar RF design in both MIMO and TX beamforming operation.

All data presented here was collected with the hardware mentioned in Section 3.1.1.

3.2.1 Required Hardware

All data presented here was collected on the AWR1243P Cascade RF board through the TSW14J56-based data capture board. The *Imaging Radar Using Cascaded AWR1243P mmWave Radar* Design Guide contains these same results.

3.2.2 Test Setup

Multiple test scenarios were set up to explore the capabilities of the Cascade Radar RF design in both MIMO and TX beamforming operation.

3.2.2.1 MIMO Test Scenarios

- In-lab Angular Resolution
- Side-by-side Car Detection Resolution
- Side-by-side Car Detection Resolution – MUSIC Application
- Car, Pedestrian and Other Targets Close Range Separation
- Car Contour and Orientation
- Car Door Contour
- Bike Contour and Orientation
- Fence Contour Detection
- Curb Contour Detection
- Manhole Contour Detection
- Height Measurement
- Single-Device vs. Cascade Devices

3.2.2.2 TX Beamforming Test Scenarios

- In-lab Beamforming Control Pattern
- Pedestrian Long-Range Detection
- Car Medium-Range detection
- Car Long-Range Detection

3.2.3 MIMO Test Results

3.2.3.1 In-lab Angular Resolution

A basic azimuth separation test was performed within an anechoic chamber radar test range. Two corner reflectors were placed approximately 8 m from the AWR1243P radar sensor. 1.5 degrees of azimuth separation was applied to the reflectors and the resulting azimuth resolution was measured.

In the current configuration, with 96 virtual array elements in the azimuth axis, and lambda/2 spacing of each element, a best-case 1.4 degree angular resolution is possible. This system measured a 1.5 degree separation, which is in close alignment to the expected.

Figure 7. Two Corner Reflectors Separated by 1.5 Degrees in Azimuth

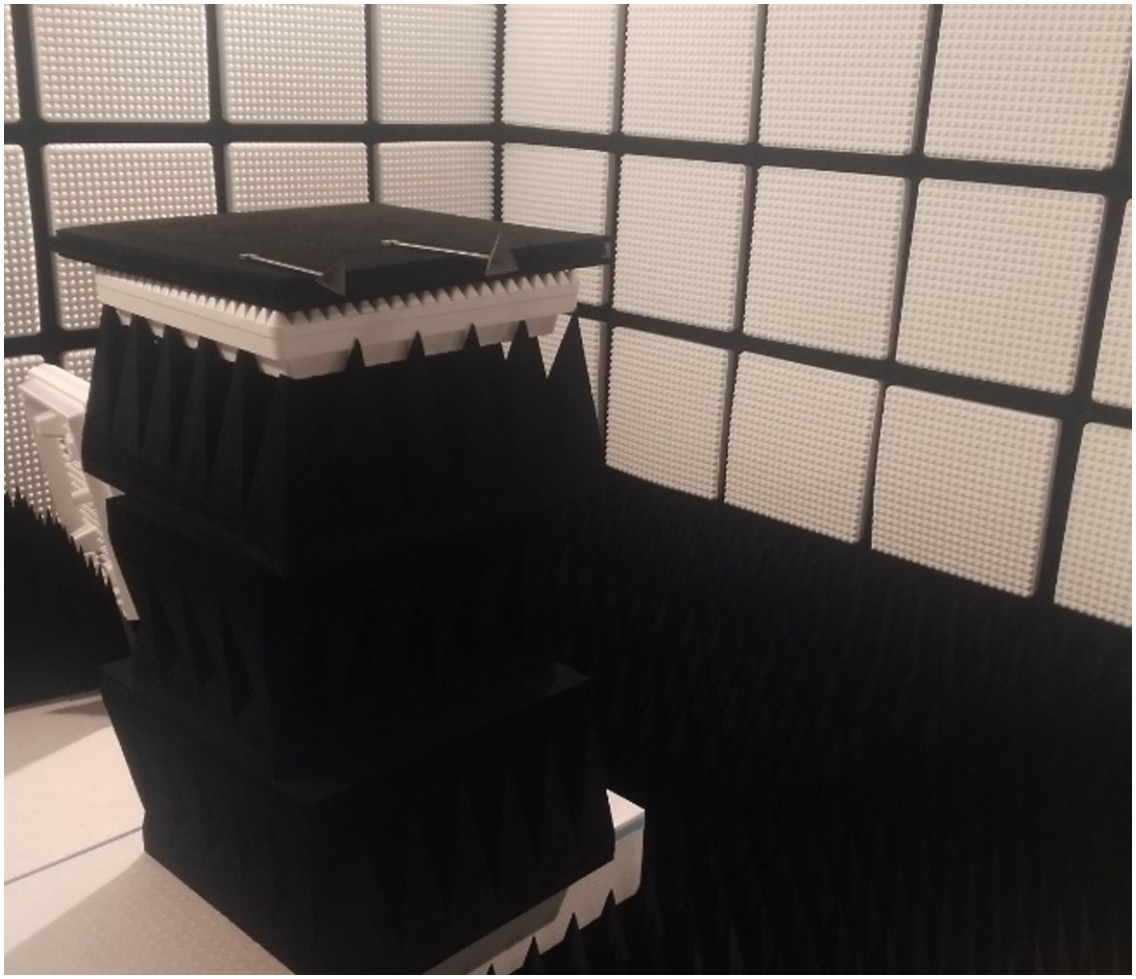
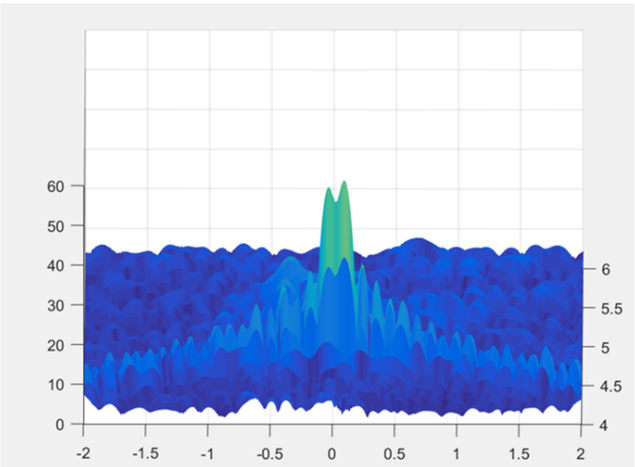
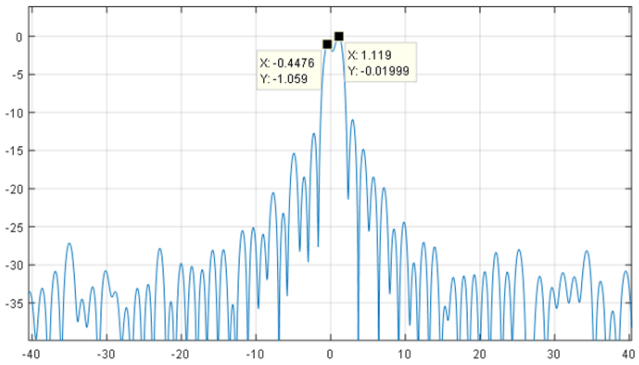


Figure 8. Range-Doppler FFT Plots Showing Detected, Separated Peaks From Both Reflectors





3.2.3.2 Car Angular Resolution Scenario

A test was performed with two cars located at 112 m range from the sensor at varying angular separations, again showing the angular resolution capabilities of the AWR1243P MIMO radar operation.

Figure 9. Two-Car Angular Separation Test Setup

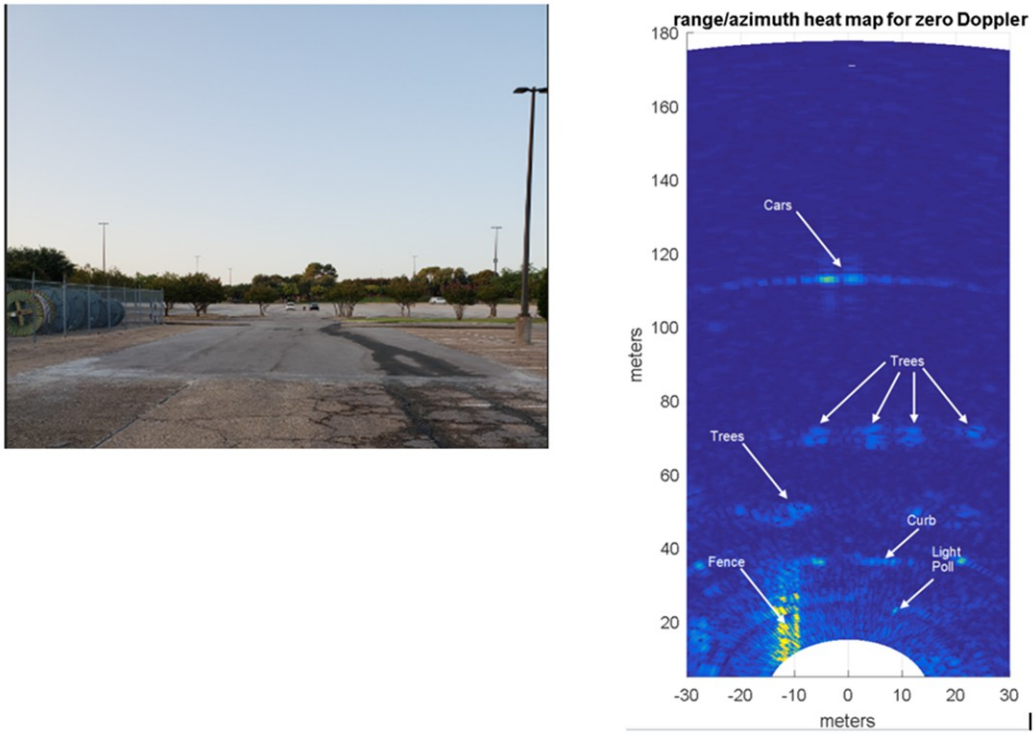
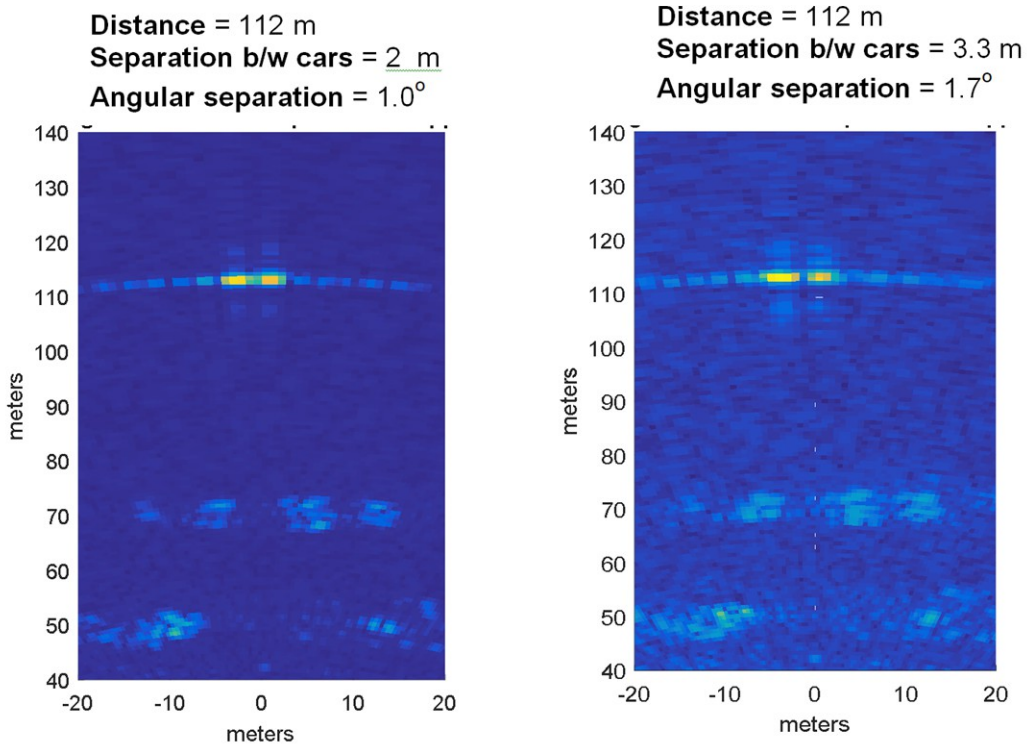


Figure 10. Two-Car Angular Separation Test Results



3.2.3.3 Car, Pedestrian, and Other Targets Close Range Separation

A test was performed showing the AWR1243P MIMO radar is able to separate a person and a bicycle at different lateral distances away from the car. This represents a more challenging scenario due to the pedestrian (or another low RCS object) occupying the same range bin as the high reflecting point from the car (high RCS object).

Figure 11. Bicycle and Person 1.5 m Away From Vehicle

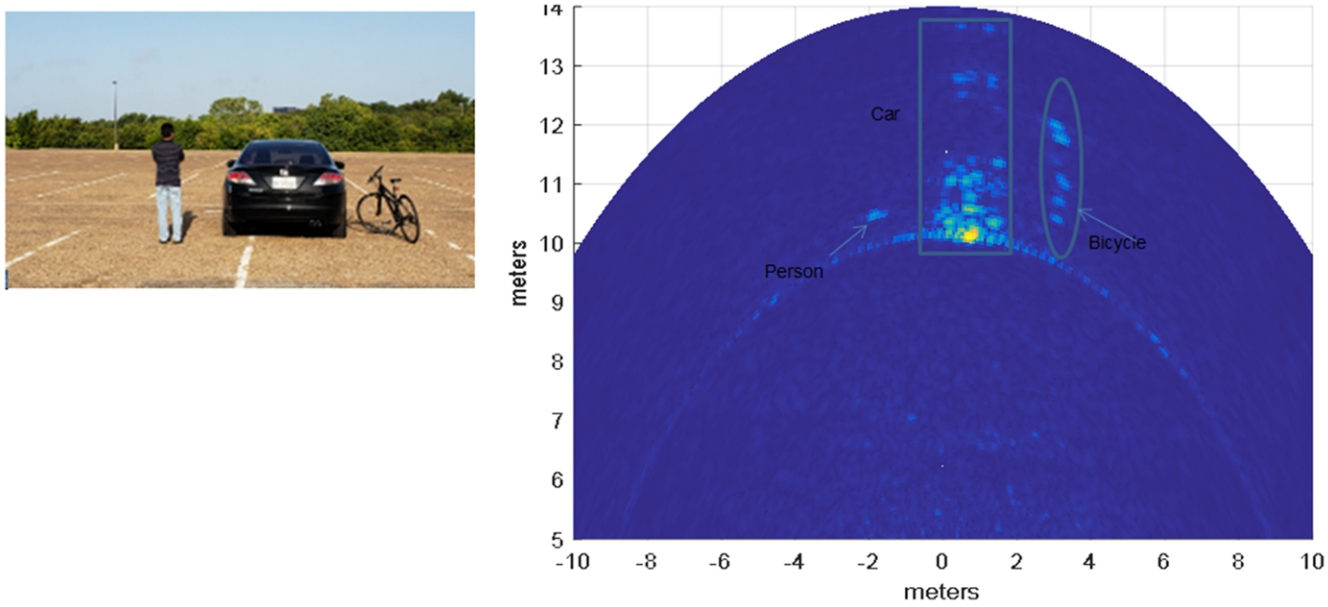
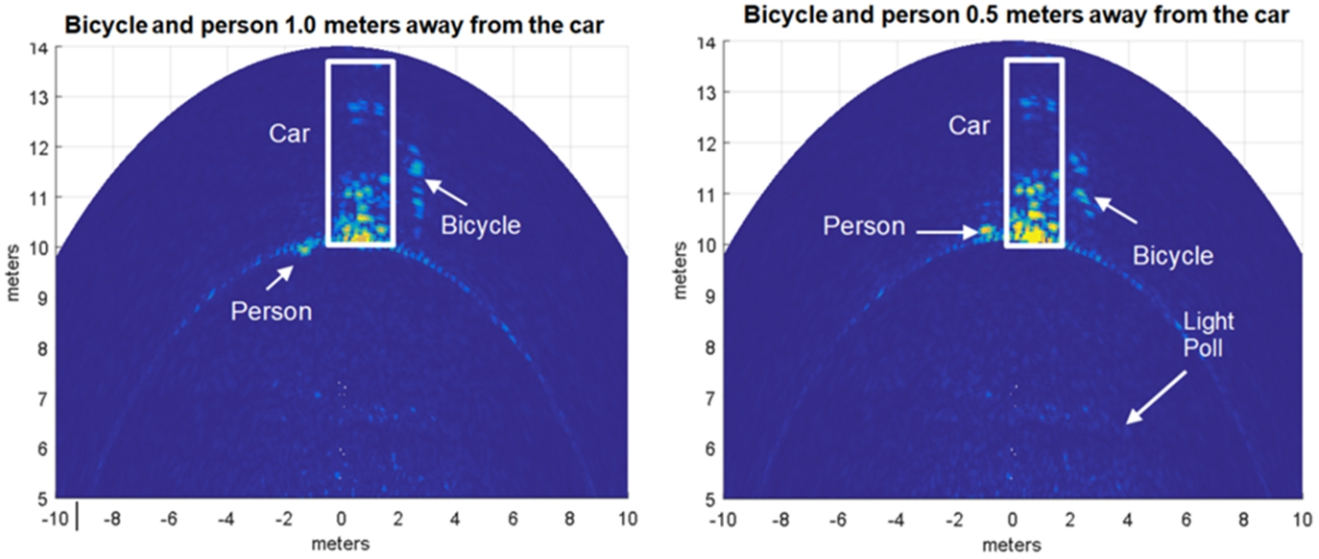


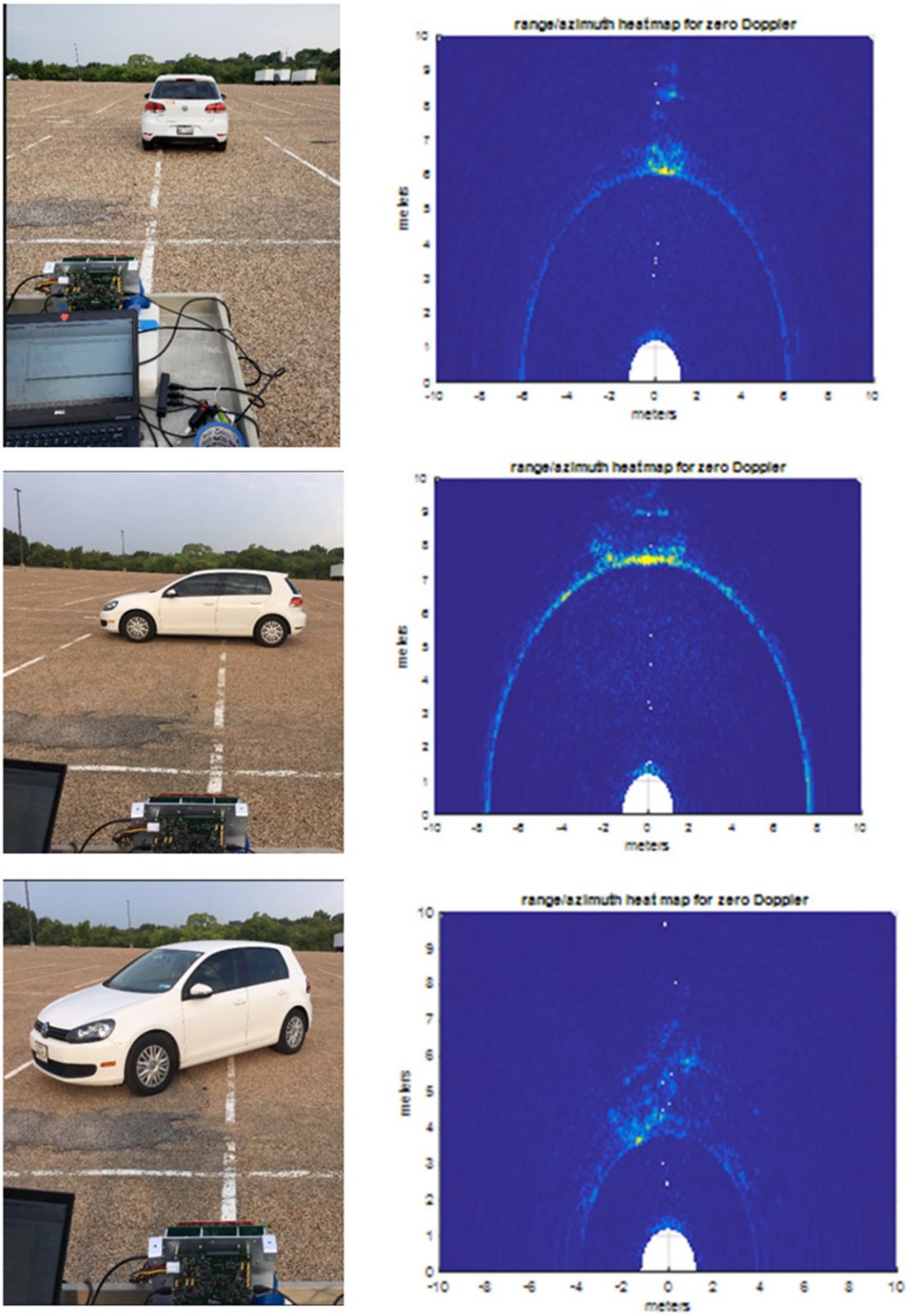
Figure 12. Bicycle and Person 1.0 m (Left) and 0.5 m (Right) Away From Vehicle



3.2.3.4 Car Contour and Orientation

A test was performed showing the AWR1243P MIMO radar detecting the contour and orientation of a car. The azimuth and range resolution allows for the detection of the contour of many vehicle surfaces.

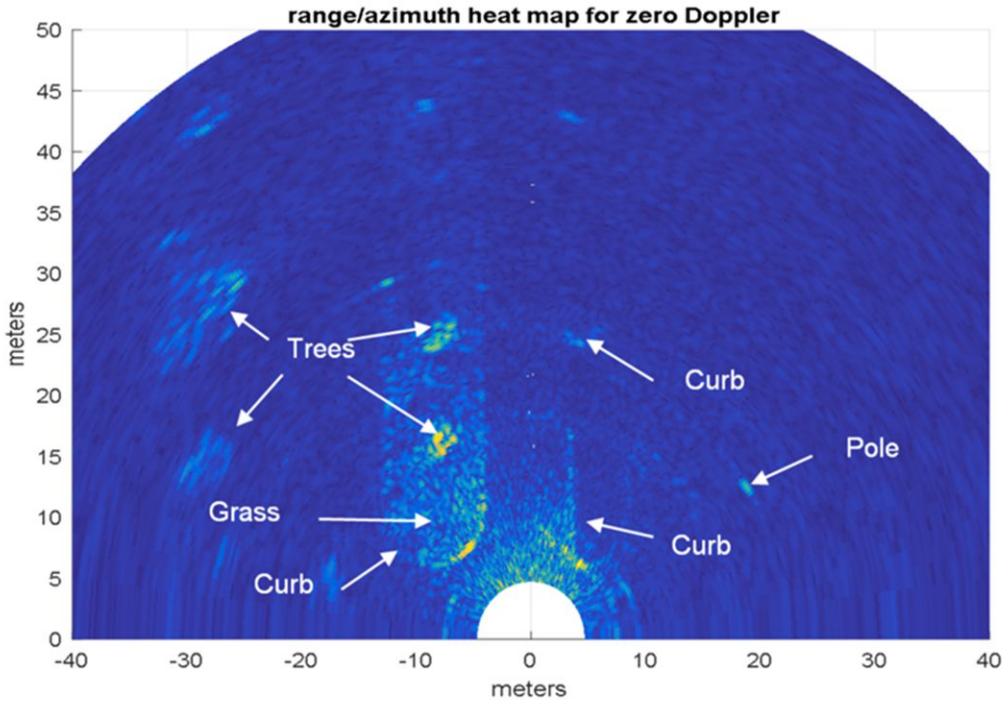
Figure 13. Car at 0 Degrees (Top), 90 Degrees (Middle) and 135 Degrees (Bottom) Orientation and Corresponding Azimuth Range Heatmap



3.2.3.5 Curb Contour Detection

A test was performed showing the AWR1243P MIMO radar detecting the contour and orientation of multiple curbs in a parking lot setting. The azimuth and range resolution allows for the detection of the contour of these shorter driving obstacles.

Figure 14. Parking Lot Curb Scene (Top), and Resulting Azimuth Range Heatmap (Bottom)



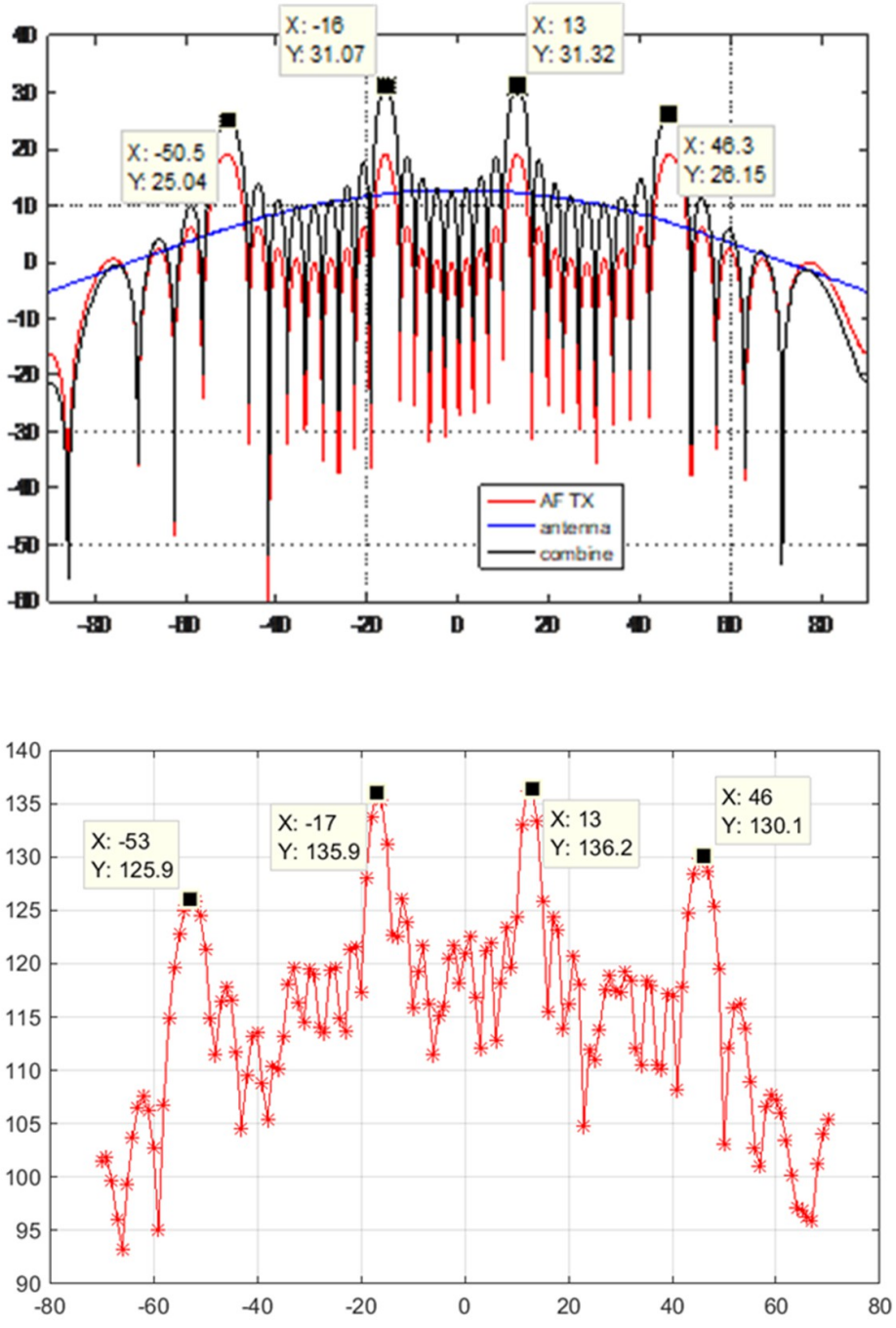
3.2.4 TX Beamforming Results

3.2.4.1 In-lab Beamforming Control Pattern

A basic beam steering test was performed within an anechoic chamber radar test range. A single corner reflector was placed approximately 8 m from the AWR1243P radar sensor. Beamsteering vectors were then programmed into the AWR1243P devices to achieve a 15 degree beam rotation. The resulting target return versus angle graph was then compared against the simulated 15-degree beam rotation pattern.

Close alignment between the simulated and measured system was observed.

Figure 15. Simulated (Top) and Measured (Bottom) 15 Degree Beam Steering Test

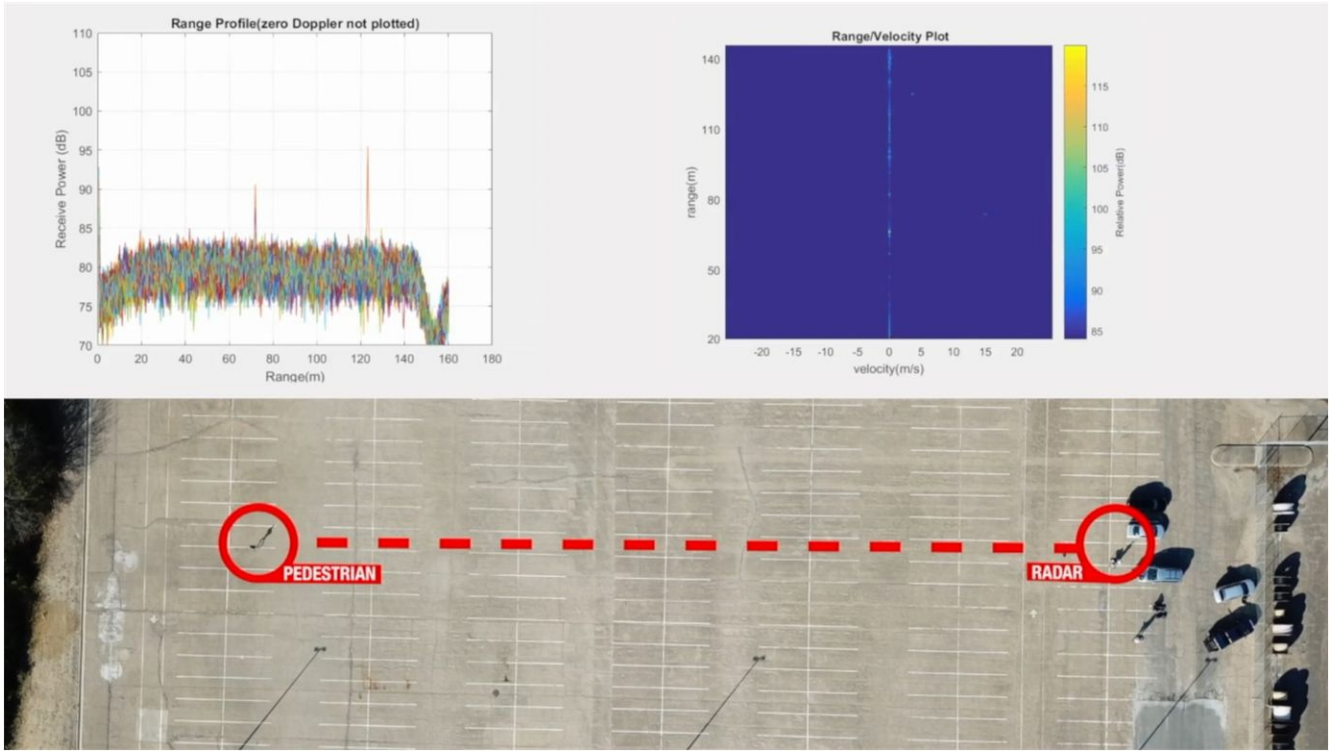


3.2.4.2 Pedestrian Long-Range Detection

In this test a pedestrian jogging from 30 m to 140 m. The AWR1243P Cascade RF board is running in 9-TX beamforming mode.

The range profile shows the pedestrian at 120 m with 20-dB SNR. The Doppler-Range plot is shown to the right. Slight Doppler displacement can be seen corresponding to the pedestrian velocity.

Figure 16. Range Profile (Top Left), and Doppler-Range Plot of a Pedestrian Jogging Away From Radar at 120-m Range

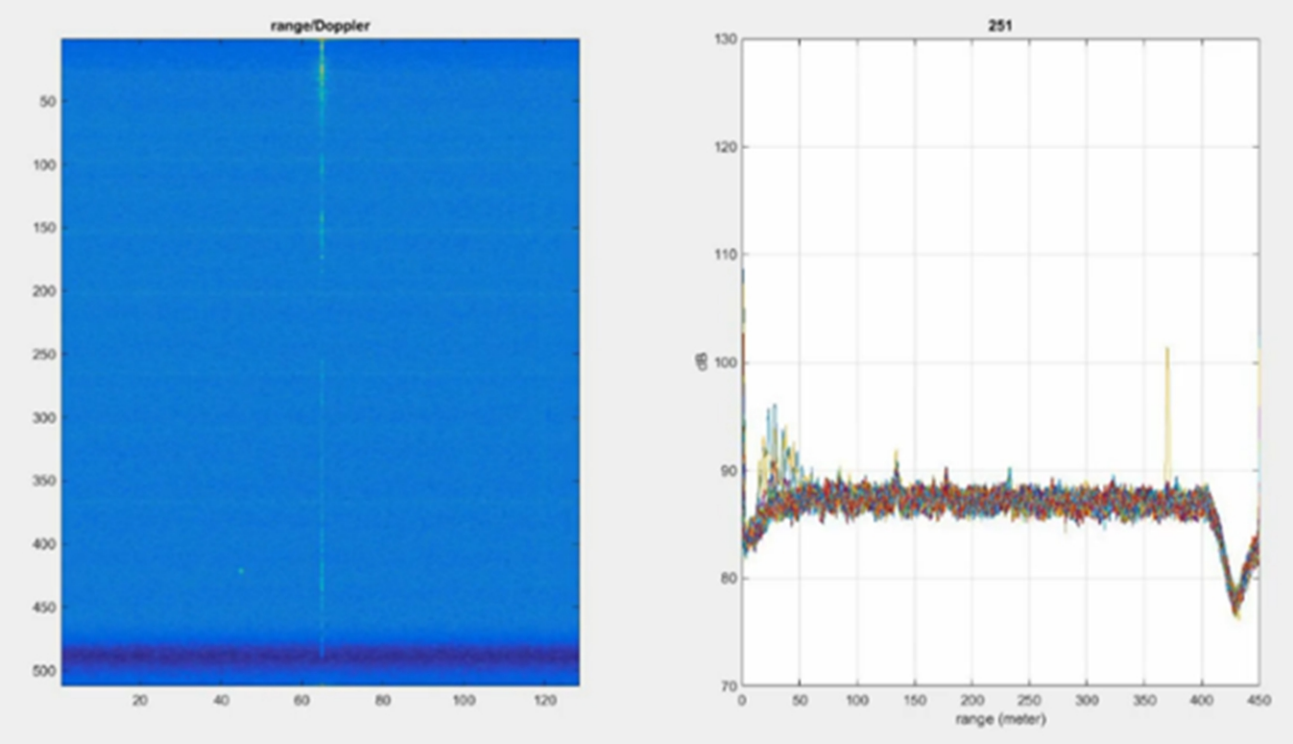


3.2.4.3 Car Long-Range Detection

Similar to the pedestrian long range detection test, this test observes a car at 350-m range. The AWR1243P Cascade RF board is running in 9-TX beamforming mode.

The range profile shows the vehicle at 350 m with 14-dB SNR.

Figure 17. Range Profile (Left), and Doppler-Range Plot of a Vehicle 350-m Range



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDEP-01017.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP-01017.

4.3 Altium Project

To download the Altium Designer® project files, see the design files at TIDEP-01017.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDEP-01017.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDEP-01017.

5 Software Files

VSDK 3.07 contains algorithms that run on the TDA2x for the Cascade Radar application. The latest VSDK is available at from *Processor SDK for TDAx ADAS SoCs - Linux and TI-RTOS Support*.

6 Related Documentation

1. Texas Instruments, *Programming Chirp Parameters in TI Radar Devices Application Report*
2. Texas Instruments, *AWR1243 76-GHz to 81-GHz high-performance automotive MMIC*
3. Texas Instruments, *AWR1243 Cascade Application Report*
4. Texas Instruments, *MMWAVE-STUDIO*

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