Design Guide: TIDA-020060, TIDA-020061

Power over Data Lines Reference Design for 100/1000Base-T1 Automotive Ethernet Applications

Description

This reference design shows an implementation of Power over Data Lines (PoDL) for automotive use cases. The design uses a DP83TG720S-Q1 1000MBit/s single pair Ethernet (SPE) PHY with the option to switch to the DP83TC812S-Q1 SPE PHY for 100MBit/s operation. A coupling and decoupling network is used to couple in and out a maximum power of 50W.

Resources

TIDA-020060, TIDA-020061	Design Folder
DP83TG720S-Q1, DP83TC812S-Q1	Product Folder
LM5157-Q1, LM51571-Q1	Product Folder
LM5158-Q1, LM51581-Q1	Product Folder
TPS1HTC30-Q1	Product Folder

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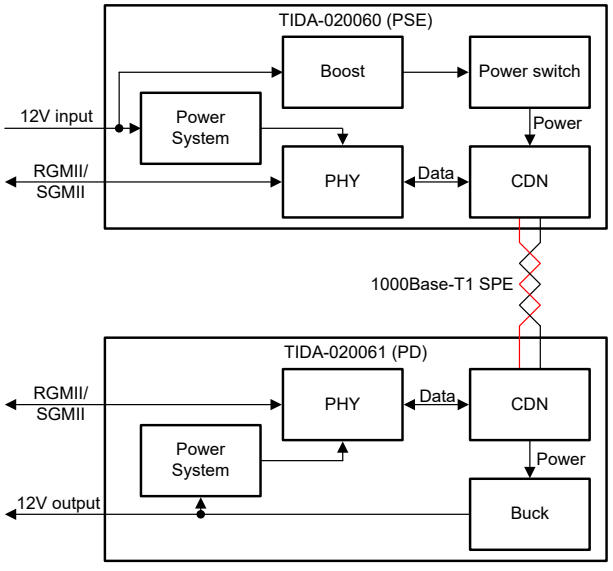
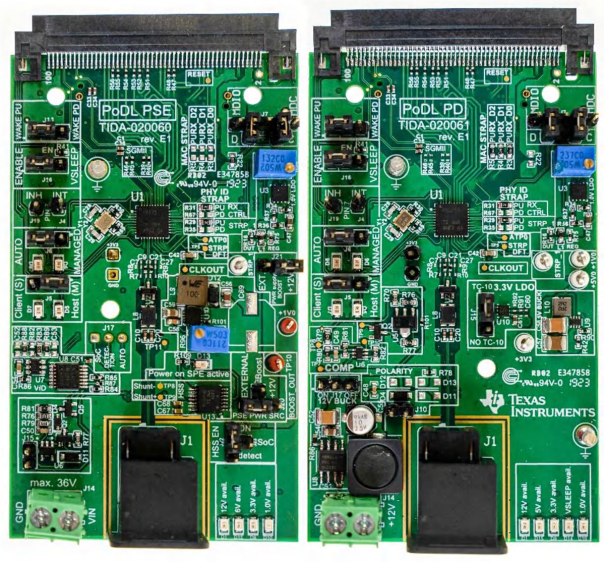
Features

- Capable of 1000Base-T1 automotive Ethernet
- Footprint compatible to TI's latest 100Base-T1 SPE PHY (that is, DP83TC812S-Q1)
- One twisted pair cable used for data and power delivery up to 50W
- Automotive qualified filter network for power coupling and decoupling
- Protection of the powered device (PD) with a high-side switch (HSS)
- Implementation of PoDL according to the automotive market requirements by reducing cost and complexity of the implementation

Applications

- Advanced driver assistance systems (ADAS)
- Radar ECU
- Long range radar
- Radar module without processing
- Mechanically scanning LIDAR
- Rear camera





1 System Description

TIDA-020060: Power sourcing device (PSE) reference design for 100/1000Base-T1 automotive Ethernet

TIDA-020061: Powered device (PD) reference design for 100/1000Base-T1 automotive Ethernet

1.1 Key System Specifications

Table 1-1, Table 1-2, and Table 1-3 show the key parameters of the design.

Table 1-1. System Key Parameters

PARAMETER	CONNECTOR	SPECIFICATION	CONDITION	DETAILS
V_{PoDL}	J1	PoDL voltage on the cable at PSE	—	12V–48V
I_{PoDL}	J1	Maximal PoDL current on the cable	—	1500mA
Bitrate	J1	Communication speed over SPE	—	1000MBit/s
BER	J1	Bit error rate (BER)	Cable length = 15m V_{PoDL}= 48V I_{PoDL}= 1500mA	< 10^{-9}errors/bit

Table 1-2. PSE Key Parameter

PARAMETER	CONNECTOR	SPECIFICATION	CONDITION	DETAILS
V_{ext_IN}	J14	External PoDL input voltage	—	48V max.
I_{ext_IN}	J14	External PoDL input current	—	1500mA max.

Table 1-3. PD Key Parameter

PARAMETER	CONNECTOR	SPECIFICATION	CONDITION	DETAILS
V_{ext_OUT}	J14	Output voltage for external devices	—	12V
I_{ext_OUT}	J14	Output current for external devices	—	1.75A max.

2 System Overview

2.1 System Block Diagram

The system contains two boards, connected via one twisted-pair cable as shown in Figure 2-1 and Figure 2-1.

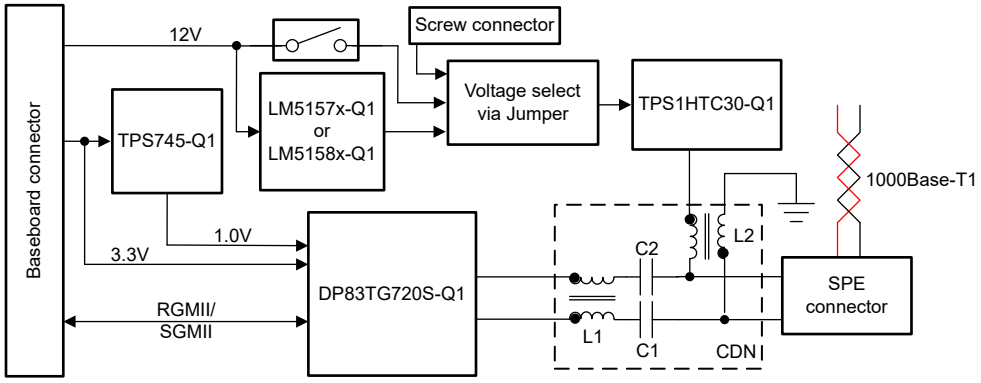


Figure 2-1. TIDA-020060 (PSE) Block Diagram

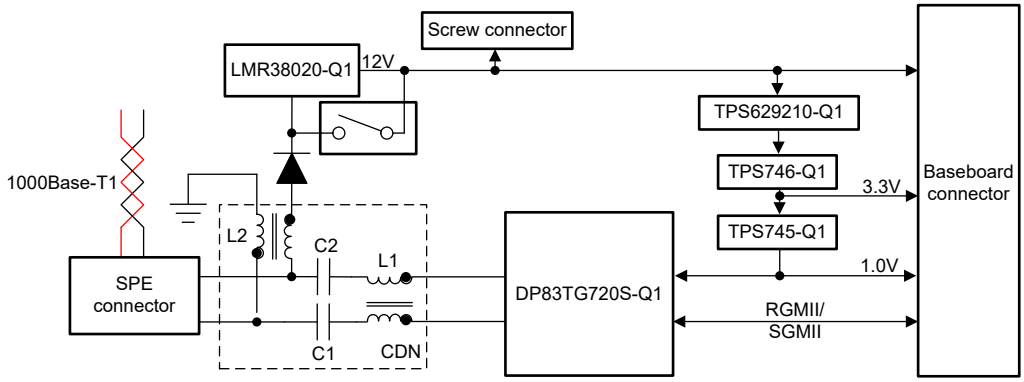


Figure 2-2. TIDA-020061 (PD) Block Diagram

2.2 Design Considerations

This reference design shows the implementation of an Ethernet interface consisting of a single-pair Ethernet (SPE) PHY with the option for powering the design through Power over Data Lines (PoDL). PoDL is standardized in IEEE802.3bu for 100/1000Base-T1. The standard requires mechanisms like detection and classification of the connected device which does not address the automotive requirements of PoDL. In the automotive sector the car OEM defines which ECUs and sensor modules are used in the system and therefore a detection and classification is not required. This assumption is based on the fact that the network does not change over the lifetime of the vehicle. The boards are designed to fulfill the automotive requirements for a cost- and weight-efficient implementation. This PoDL design is not fully compliant to IEEE802.3bu to address the automotive requirements. In general, PoDL can be used in vehicles in all areas where SPE is already used to connect sensors or actuators. The use of PoDL is particularly recommended for supplying devices with low energy requirements, such as radar modules or remote camera modules which are already connected to a domain- or zone controller.

A PoDL system consists of a (power) source and a (power) sink, which are referred to as Power Sourcing Equipment (PSE) and Powered Device (PD). Regardless of the specific application, the implementation of PoDL requires only minor adjustments to both the source and the sink. The coupling decoupling network (CDN) functions as a frequency filter, with the low-frequency component, particularly the DC voltage, directed to the power tree, while the high-frequency components are treated as data transmitted to the PHY. Additional information on this topic is elaborated in Section 3.3. In this topology, the use of the classic fuse is no longer applicable, which is why the integration of a high-side switch (HSS) is strongly recommended to protect the PD from any damage.

2.3 Highlighted Products

This section introduces the key devices in this reference design. For comprehensive details, see the product page and data sheet of each respective device.

2.3.1 DP83RG720S-Q1 (Automotive SPE PHY)

The DP83TG720S-Q1 device is an IEEE 802.3bp and Open Alliance compliant automotive Ethernet physical layer transceiver. The device provides all physical layer functions needed to transmit and receive data over unshielded and shielded single twisted-pair cables. The device provides xMII flexibility with support for RGMII and SGMII MAC interfaces. DP83TG720 is compliant to Open Alliance EMC and interoperable specifications over unshielded twisted cable. DP83TG720 is front print compatible to TI's 100BASE-T1 PHY enabling design scalability with single board for both speeds. This device offers the Diagnostic Tool Kit, with an extensive list of real-time monitoring tools, debug tools and test modes. Within the tool kit is the first integrated electrostatic discharge (ESD) monitoring tool and is capable of counting ESD events on both the xMII and MDI as well as providing real-time monitoring through the use of a programmable interrupt. Additionally, the DP83TG720S-Q1 includes a data generator and checker tool to generate customizable MAC packets and check the errors on incoming packets. This enables system level data path tests and optimizations without dependency on MAC.

2.3.2 TPS1HTC30-Q1 (HSS)

TPS1HTC30-Q1 is a single-channel, smart high-side switch, with integrated NMOS power FET and charge pump, designed to meet the requirements of 24V automotive battery systems. The low R_{ON}(30mΩ) minimizes device power dissipation driving a wide range of output load current up to 6A DC, and the 60V DC operating range improves system robustness.

The device integrates protection features such as thermal shutdown, output clamp, and current limit. These features improve system robustness during fault events such as short circuit. TPS1HTC30-Q1 implements an adjustable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current. The device also provides an accurate load current sense that allows for improved load diagnostics such as overload and open-load detection enabling better predictive maintenance.

TPS1HTC30-Q1 is available in a small 14-pin, 4.40mm × 5.0mm HTSSOP leaded package with 0.65mm pin pitch minimizing the PCB footprint.

2.3.3 LM5157x-Q1 and LM5158x-Q1 (PSE PoDL Boost Converter)

The LM5157x-Q1 device is a wide input range, nonsynchronous boost converter with integrated 50V, 6.5A (LM5157-Q1) or 50V, 4.33A (LM51571-Q1) power switch. The device can be used in boost, SEPIC, and flyback topologies. The device can start up from a single-cell battery with a minimum of 2.9V. The device can operate with the input supply voltage as low as 1.5V if the BIAS pin is greater than 2.9V.

The LM5158x-Q1 device is a wide input range, nonsynchronous boost converter with an integrated 85V, 3.26A (LM5158-Q1) or 85V, 1.63A (LM51581-Q1) power switch. The device can be used in boost, SEPIC, and flyback topologies. The device can start up from a single-cell battery with a minimum of 3.2V and can operate with the input supply voltage as low as 1.5V if the BIAS pin is greater than 3.2V. The BIAS pin operates up to 60V (65V absolute maximum) for automotive load dump. The switching frequency is dynamically programmable from 100kHz to 2.2MHz with an external resistor. Switching at 2.2MHz minimizes AM band interference and allows for a small design size and fast transient response. The device provides a selectable Dual Random Spread Spectrum to help reduce the EMI over a wide frequency range.

2.3.4 LMR38020-Q1 (PD PoDL Buck Converter)

The LMR38020-Q1 synchronous buck converter is designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. The LMR38020-Q1 operates during input voltage dips as low as 4.2V, at nearly 100% duty cycle if needed, making the device an excellent choice for 48V battery automotive applications and MHEV or EV systems.

The LMR38020-Q1 uses precision enable to provide flexibility by enabling a direct connection to the wide input voltage or precise control over device start-up and shutdown. The power-good flag, with built-in filtering and delay, offers a true indication of system status, eliminating the need for an external supervisor. The device incorporates pseudorandom spread spectrum for minimal EMI and switching frequency can be configured between 200kHz and 2.2MHz to avoid noise sensitive frequency bands. In addition, the frequency can be selected for improved efficiency at low operating frequency or smaller design size at high operating frequency.

The device has built-in protection features such as cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation. The LMR38020-Q1 is qualified to automotive AEC-Q100 grade 1 and is available in an 8-pin HSOIC PowerPAD integrated circuit package.

2.3.5 TPS629210-Q1 (PD 5.0V Rail Buck Converter)

The automotive-qualified TPS6292xx-Q1 family of devices are highly-efficient, small, and highly-flexible synchronous step-down DC-DC converters that are easy to use. A wide 3V to 17V input voltage range supports a wide variety of systems powered from either 12V, 5V, or 3.3V supply rails, or single-cell or multicell Li-Ion batteries. The TPS629210-Q1 can be configured to run at either 2.5MHz or 1MHz in a forced PWM mode or a variable frequency (auto PFM) mode. In auto PFM mode, the device automatically transitions to power save mode at light loads to maintain high efficiency. The low 4µA typical quiescent current also provides high efficiency down to the smallest loads. TI's automatic efficiency enhancement (AEE) mode holds a high conversion efficiency through the whole operation range without the need of using different inductors by automatically adjusting the switching frequency based on input and output voltages. In addition to selecting the switching frequency behavior, the MODE/S-CONF input pin can also be used to select between different combinations of external and internal feedback dividers and enabling and disabling the output voltage discharge capability. In the internal feedback configuration, a resistor between the FB/VSET pin and GND can be used to select between 18 different output voltage options.

2.3.6 TPS746-Q1 (PD PHY 3.3V Rail LDO)

The TPS746-Q1 is a 1A, ultra-low-dropout regulator (LDO) with power-good functionality. This device is available in a small 6-pin, 2mm × 2mm WSON package and a small 8-pin, 3mm × 3mm VSON package with wettable flanks to facilitate optical inspection. The TPS746-Q1 consumes low quiescent current and provides fast line and load transient performance.

The TPS746-Q1 is a flexible device for post-regulation by supporting an input voltage range from 1.5V to 6.0V and an externally adjustable output range of 0.55V to 5.5V. The device also features fixed output voltages for powering common voltage rails.

The TPS746-Q1 has a power-good (PG) output that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output can be used for sequencing multiple power supplies in the system.

The TPS746-Q1 is stable with small ceramic output capacitors, allowing for a small overall design size. A precision band-gap and error amplifier provides high accuracy of ±0.85% (max) at 25°C and ±1.5% (max) overtemperature. This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. The TPS746-Q1 has an internal foldback current limit that helps reduce the thermal dissipation during short-circuit events.

2.3.7 TPS745-Q1 (PSE and PD PHY 1.0V Rail LDO)

The TPS745-Q1 is a 500mA ultra-low-dropout regulator (LDO) with power-good functionality. This device is available in a small 6-pin, 2mm × 2mm WSON package and a small 8-pin, 3mm × 3mm VSON package with wettable flanks to facilitate optical inspection. The TPS745-Q1 consumes low quiescent current and provides fast line and load transient performance.

The TPS745-Q1 is a flexible device for post-regulation by supporting an input voltage range from 1.5V to 6.0V and an externally adjustable output range of 0.55V to 5.5V. The device also features fixed output voltages for powering common voltage rails.

The TPS745-Q1 has a power-good (PG) output that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output can be used for sequencing multiple power supplies in the system.

The TPS745-Q1 is stable with small ceramic output capacitors, allowing for a small overall design size. A precision band-gap and error amplifier provides high accuracy of ±0.85% (max) at 25°C and ±1.5% (max) overtemperature. This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. The TPS745-Q1 has an internal foldback current limit that helps reduce the thermal dissipation during short-circuit events.

3 System Design Theory

This section provides details about different sections on the reference design. Figure 3-1 and Figure 3-2 show the location and size of these functional blocks.

3.1 System Design Consideration for TIDA-020060 (PSE)

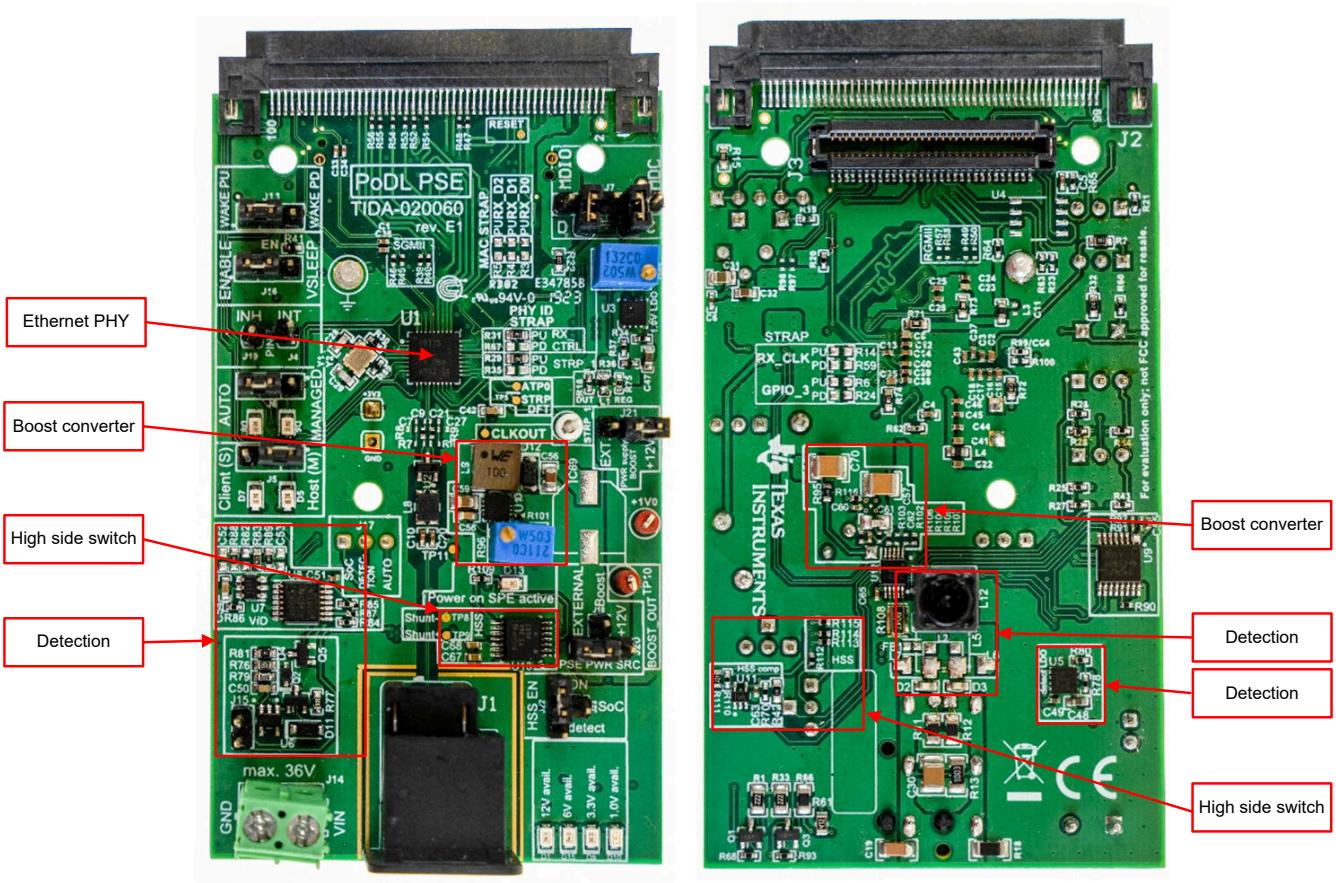


Figure 3-1. TIDA-020060 (PSE) Board Overview

3.1.1 Ethernet PHY

This board supports a broad range of TI's automotive SPE PHYs. The board comes with the DP83TG720S-Q1 populated. This allows for evaluating PoDL for 1000Base-T1. When evaluating 100Base-T1, the PHY can be replaced with the DP83TC812S-Q1.

When replacing the DP83TG720S-Q1 with the DP83TC812S-Q1, remove R72 and R74 and refer to Section 3.1.3. Additionally, see the design requirements and Power Supply Recommendations of the DP83TC812S-Q1 data sheet.

The boards supports both SGMII and RGMII on J2 and only SGMII on J3 to interface to various boards. The board comes with SGMII connected to J2 and J3. If RGMII is required, remove R39, R40, R45, R46 and populate R49, R50, R57, R58.

3.1.2 PHY Power Supply

The DP83TG720S-Q1 is capable of operating with a wide range of IO supply voltages (3.3V, 2.5V, or 1.8V). This board features an IO supply voltage of 3.3V to interface with various baseboards capable of 3.3V IO voltage. The DP83TG720S-Q1 also requires a 1.0V rail. No power supply sequencing is required. Check and follow the *DP83TC811, DP83TG720 Rollover Document* for the latest power supply device recommendation.

3.1.3 PSE Specific PoDL Power Supply

This design includes a boost converter capable of investigating PoDL functionalities in a broad range of use cases. This includes the need for a boost converter family which is able to boost the 12V input voltage up to 48V.

For a final implementation, consider if a boost converter is required or not. Using a boost converter which is optimized for the final application is recommended. When using PoDL to supply low-power applications like a camera or RADAR module, consider using an already available 12V stabilized rail available on the domain, zone controller. In this case, no boost converter is required. This recommendation is based on the fact that the expected power required of the PD is less than 10W. In case more power is needed at the PD, consider using one of the boost converters listed in Table 3-1.

Table 3-1. Recommended PSE PoDL Boost Converter

DEVICE	MAXIMUM OUTPUT VOLTAGE	MAXIMUM OUTPUT CURRENT
TPS55340-Q1	38V	5A
LM5157-Q1	50V	6A
LM51571-Q1	50V	4A

3.2 System Design Consideration for TIDA-020061 (PD)

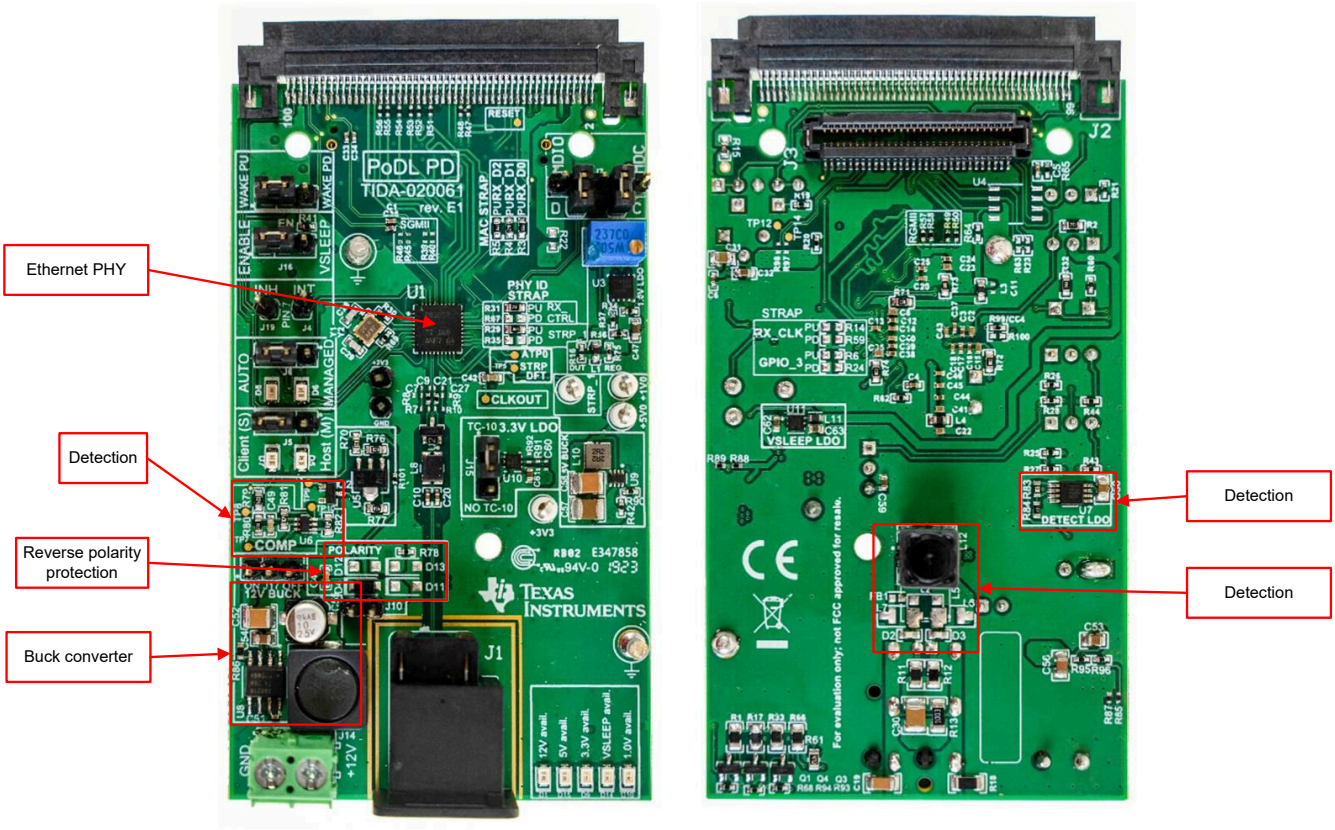


Figure 3-2. TIDA-020061 (PD) board overview

This design includes a buck converter capable of investigating PoDL functionalities in a broad range of use cases. This includes the need for a buck converter family which is able to step down the PoDL voltage down to 12V system voltage rail.

For a final implementation, consider if a buck converter is required or not. Using a buck converter which is optimized for the final application is recommended. In the case where V_{PoDL}= 12V, the output of the CDN can directly be fed into the existing power tree. Consider using one of the buck converters listed in Table 3-2.

Table 3-2. Recommended PD PoDL Buck converter

DEVICE	MAXIMUM INPUT VOLTAGE	MAXIMUM OUTPUT CURRENT
LM63635-Q1	32V	3.25A
LMQ61460-Q1	36V	6A
LM76003-Q1	60V	3.5A

3.3 General Design Consideration for PoDL Coupling Decoupling Network

There are two main factors to consider when selecting a CDN: Ethernet speed and power consumption of the PD. Table 3-3 shows each Ethernet PHY with the corresponding Ethernet standard and data frequency.

Table 3-3. Ethernet Signal Frequencies

Ethernet PHY	IEEE STANDARD	DATA RATE	SYMBOL RATE
—	10Base-T1S	10Mb/s	12.5MHz
DP83TC812-Q1	100Base-T1	100Mb/s	66.6MHz
DP83TC813-Q1			
DP83TC814-Q1			
DP83TG720-Q1	1000Base-T1	1000Mb/s	750MHz

Each PoDL CDN has a maximum current that it can support while maintaining the required impedance based on the saturation characteristics of the components. Inductors do not behave in a flawless manner, the inductors dissipate heat, pass very high frequencies and saturate when too much current is passed through. All components and cables have parasitic capacities and impedances throughout the entire circuit. Knowing the maximum power the PD draws and selecting a CDN solution that can deliver that power for a given PoDL voltage is important. Calculate the maximum power as the worst-case scenario of power consumption on the PD side of the link. Highest power consumption refers to a period where, for example, the radar is chirping and all other remote devices are operating. The user need to select a PoDL network capable of supplying enough current for the PD.

Table 3-4 provides CDN solution suggestions. TI recommends selecting one of the networks based on the desired frequency range, current rating, and temperature.

Table 3-4. CDN Filter Solution for PoDL

VENDOR	CDN FILTER SOLUTION	Ethernet SPEED	COMPONENTS	CURRENT RATING	TEMPERATURE RATING
TDK	2	100Base-T1	CMC: ACT1210L-201-2P-TL00 DMI: PID77S-180M	1350mA	150°C
MuRata	3	1000Base-T1	CMC: DLW32MH101XT2 DMI: LQH32NH3R3J23	425mA	125°C
TDK	4	1000Base-T1	CMC: ACT1210G-800-2P-TL10 DMI: ADL32VHR-3R9M	540mA	150°C
TDK	5	1000Base-T1	CMC: ACT1210G-800-2P-TL10 DMI: ADM70S-2R6	1500mA	150°C

4 Hardware, Software, Testing Requirements, and Test Results

The bit error rate (BER) specifies how many errors per bit occur. For SPE, IEEE requires the $BER < 10^{-10}\frac{error}{bit}$.

The advanced diagnostic features for 100Base-T1 and 1000Base-T1 automotive Ethernet PHYs, specified by OPEN Alliance in TC1 and TC12 are used to make sure this limit is not exceeded. This section describes the test procedure and test results.

4.1 Hardware Requirements

This section describes the fundamental hardware requirements to demonstrate the PoDL functionalities in a minimal setup. The setup allows for investigation of the behavior of the system using different voltage and current levels while transmitting data at full bandwidth.

Table 4-1 lists the required hardware.

Table 4-1. Hardware Required for Minimal Setup

QUANTITY	DEVICE DESCRIPTION	DEVICE NUMBER
1 ×	PoDL PSE board	TIDA-020060
1 ×	PoDL PD board	TIDA-020061
1 ×	TDA4VM SoM board	J721EXSOMXEVM
1 ×	Common processor board for Jacinto 7 processors	J721EXCPXEVM
1 ×	TE Connectivity MATEnet SPE cable	—

4.2 Software Requirements

This section describes the software requirements for the minimal setup. The Software development kit for DRA829 and TDA4VM Jacinto™ processors is used to control and monitor the DUT during testing.

Alternatively, to be able to configure and monitor TI's automotive SPE PHYs, use DIEP. Debug interface for Ethernet PHYs (DIEP) replaces the USB2MDIO tool and includes a range of state-of-the-art debug tools.

4.3 Test Setup

Figure 4-1 shows a block diagram of the test setup.

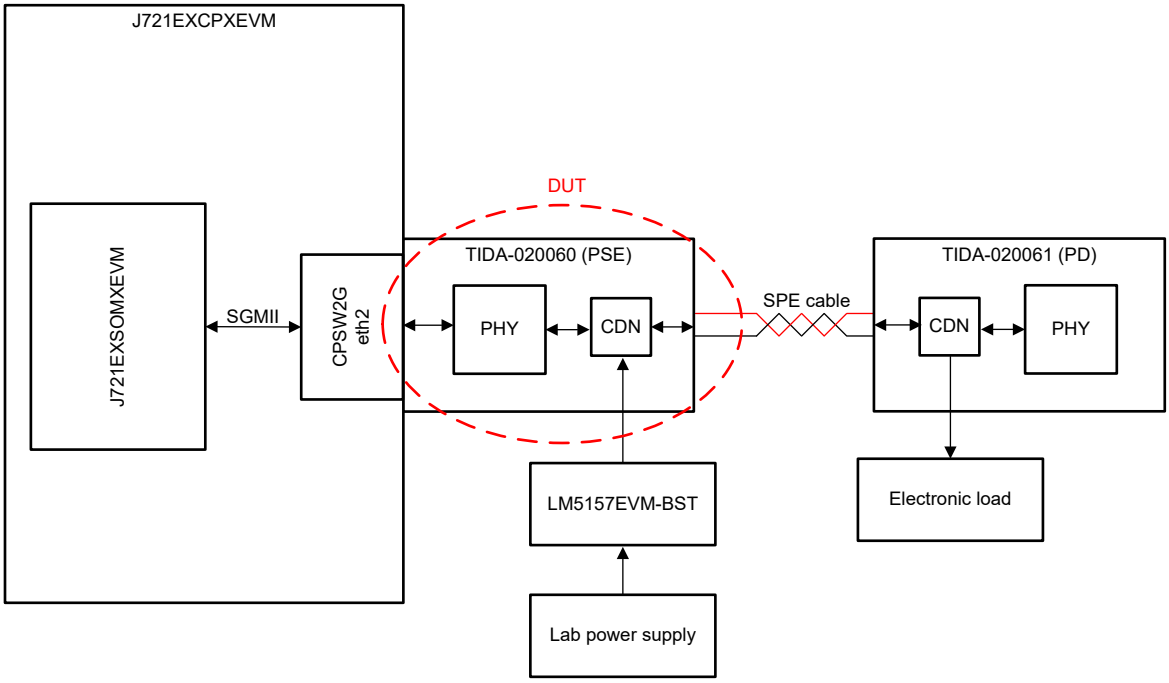


Figure 4-1. Test Setup of SQI Test

Table 4-2 details the test conditions used.

Table 4-2. SQI Test Conditions

TEST CONDITIONS	VALUE
CDN	#2, #3, #4, #5
V_{PoDL}	12V, 24V, 48V
I_{PoDL}	Maximum rated current of CDN, pulsed current profile
Cable length	15m
Temperature	Room temperature
Test duration	10 minutes

This tests evaluates the test parameter SQI. During the test, the PHY continuously measures the mean square error (MSE) of the signal and stores the result in a register. This MSE register of the PHY is logged during the test. After the test is completed, the MSE register log is converted to the signal-to-noise ratio (SNR).

To determine if the test has passed or failed, Table 4-3 is used.

Table 4-3. SNR Limits

SQI VALUE	SNR VALUE	BER FOR AWG NOISE MODEL
SQI = 7	SNR > = 24dB	$BER < 10^{-10}\frac{error}{bit}$ Passing IEEE limit
SQI = 6	24dB > SNR > = 23dB	
SQI = 5	23dB > SNR > = 22dB	
SQI = 4	22dB > SNR > = 21dB	
SQI = 3	21dB > SNR > = 20dB	
SQI = 2	20dB > SNR > = 19dB	$BER > 10^{-10}\frac{error}{bit}$ Failing IEEE limit
SQI = 1	19dB > SNR > = 18dB	
SQI = 0	SNR < 18dB	

4.4 Test Results

This section shows the test results for selected CDN filter solutions.

Table 4-4. Test Results for CDN Filter Solution 2

12V, 680mA	12V, 680mA(1)	24V, 1350mA	24V, 350mA(1)	48V, 1350mA	48V, 205mA(1)
31.6dB	29.8dB	31.6dB	29.8dB	29.8dB	29.8dB
PASS	PASS	PASS	PASS	PASS	PASS

(1) Pulsed current profile

Table 4-5. Test Results for CDN Filter Solution 4

12V, 540mA	12V, 540mA(1)	24V, 540mA	24V, 540mA(1)	48V, 540mA	48V, 540mA(1)
23.8dB	24.6dB	23.8dB	24.6dB	—	24.6dB
PASS	PASS	PASS	PASS	TBD	PASS

(1) Pulsed current profile

Table 4-6. Test Results for CDN Filter Solution 5

12V, 1500mA(1)	24V, 1500mA	48V, 1500mA
23.8dB	23.8dB	23.8dB
PASS	PASS	PASS

(1) 5m cable length due to power losses on a long cable.

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-020060, TIDA-020061.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-020060, TIDA-020061.

5.1.3 PCB Layout Recommendations

Place the DMI as close to the SPE connector as possible.

5.2 Tools and Software

Tools

LM5157EVM-BST	The LM5157EVM-BST evaluation module showcases the features and performance of the LM5157 device as a wide input voltage boost converter with dual random spread spectrum. The standard configuration is designed to provide a regulated output of 12V at 1.6A from an input of 3V to 9V (load derated by half from < 6V input), switching at 2.1MHz.
AWR2544LOPEVM	The AWR2544LOPEVM is an easy-to-use evaluation board for the AWR254x mmWave sensing device, with direct connectivity to the DCA1000EVM. This EVM can be powered via PoDL. Refer to the *AWR2544LOP User's Guide* for the instructions how to use PoDL on this board.

Software

ETHERNET-SW	The Linux™ drivers for Texas Instruments' Ethernet physical layer (PHY) transceivers support communication through the serial management interface (MDC/MDIO) to configure and read PHY registers. The USB-2-MDIO software lets you directly access the registers during debug and prototyping. This tool supports all TI Ethernet PHYs releases of the DIEP GUI installer, packaged with device description files for automatic connection and detection of Ethernet EVMs.
PROCESSOR-SDK-LINUX-J721E	Processor SDK RTOS (PSDK RTOS) can be used together with either Processor SDK Linux (PSDK Linux) or Processor SDK QNX (PSDK QNX) to form a multiprocessor software development platform for TDA4VM and DRA829 SoCs within TI's Jacinto™ platform. The SDK provides a comprehensive set of software tools and components to help users develop and deploy applications on supported J7 SoCs. PSDK RTOS and either PSDK Linux or PSDK QNX can be used together to implement various use cases in robotics, vision, factory and building automation, and automotive ADAS and gateway systems.

5.3 Documentation Support

1. Texas Instruments, *DP83TC811, DP83TG720 Rollover Document Application Note*
2. Texas Instruments, *DP83TG720S-Q1 1000BASE-T1 Automotive Ethernet PHY with SGMII and RGMII Data Sheet*
3. Texas Instruments, *DP83TC812x-Q1 TC-10 Compliant 100BASE-T1 Automotive Ethernet PHY Data Sheet*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

FABIAN BARTH is a highly-skilled systems engineer contributing to the ADAS Systems Engineering Team at Texas Instruments. In this role, he plays a pivotal part in the development of cutting-edge reference designs within the automotive sector. With a wealth of expertise in areas such as single-pair Ethernet, Power over Data Lines, and hardware time synchronization, Fabian brings a depth of knowledge and experience to his responsibilities.

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