Design Guide: TIDA-010938

10-kW, GaN-Based Single-Phase String Inverter With Battery Energy Storage System Reference Design

Description

This reference design provides an overview into the implementation of a GaN-based single-phase string inverter with bidirectional power conversion system for Battery Energy Storage Systems (BESS). The design consists of two string inputs, each able to handle up to 10 photovoltaic (PV) panels in series and one energy storage system port that can handle battery stacks ranging from 50V to 500V. The nominal rated power from string inputs to the BESS is up to 10kW. The configurable DC-AC converter can support up to 4.6kW into a single-phase grid connection at 230V. Digital control of the three power stages is executed on a single C2000™ MCU.

Resources

TIDA-010938	Design Folder
LMG3522R030, TMCS1123, AMC1302	Product Folder
ISOW1044, ISO1412, UCC14131-Q1	Product Folder
ISO7741, ISO7762	Product Folder
OPA4388, INA181	Product Folder
TMDSCNCD280039C	Product Folder

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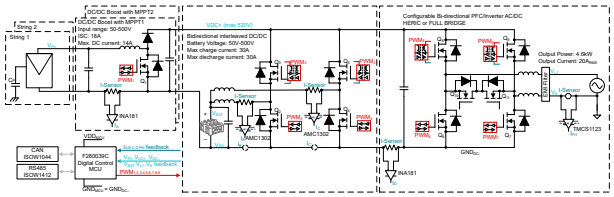
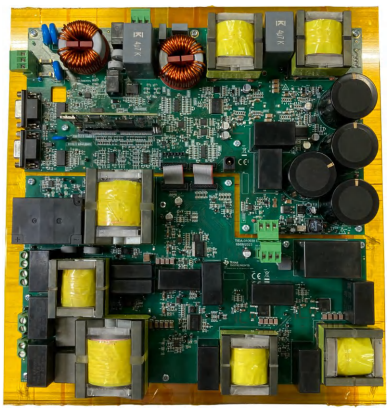
Features

- Bidirectional DC/DC stage configurable for wide battery voltage ranges
- Configurable DC/AC stage (HERIC, H-Bridge Unipolar and Bipolar modulation schemes)
- 2 × power density improvement makes solar inverters lighter and easier to install (2.5kW/L)
- Low total losses (< 2%) harnesses more sun and makes battery energy storage more efficient
- Control of entire board done with a unique MCU
- Cost-optimized with MCU GND referenced to $V_{DC–}$, allows use of non-isolated drive on all GaN devices connected to $V_{DC–}$

Applications

- String inverter
- Power conversion system (PCS)





1 System Description

With an increase in demand for photovoltaic systems, inverters play an important role in facilitating the transition to renewable energy further and making solar energy more accessible for residential purposes. The modularity of string inverters, low cost-per-watt and easy amplification to attain higher power levels makes string inverters a good candidate for the single-phase market. With the additional possibility of energy storage via batteries, hybrid string inverters provide a good outlet to maximize the power utilization of the string input, and also provide an alternate pathway to supply the grid during night or low irradiation scenarios.

Such hybrid string inverters combine PV panel power point tracking with an inverter stage and bidirectional capabilities to include a battery stage, thus increasing the need for higher power density and efficiencies. This is where Gallium Nitrate (GaN) FETs can bring multiple benefits into the picture. Since GaN FETs support high switching frequencies, the GaN FETs allow the EMI filter and heat sink to be smaller, making the system more compact and lighter, thereby increasing the form factor of the design.

This reference design is intended to show an implementation of a two-channel single-phase string inverter with fully bidirectional power flow to combine PV input functionality with BESS supporting a wide range of battery voltages.

The design contains three main stages:

- 2 × PV input with boost converter
- Battery input with bidirectional DC/DC converter
- DC/AC converter

This system consists of two boards that are split by different functionality.

The first board, called DC/DC board, consists of two input boost converters for the individual string inputs and a DC/DC converter associated with the battery stage. The second board, called DC/AC board, consists of DC-link capacitors, DC/AC converter and filtering circuits. All the high-frequency switching components in the design are based on top-side cooled GaN FETs from TI.

Both the boards are mounted above an aluminum heat sink which is connected by means of thermal interface materials to the GaN FETs and additional thermal interface material to the SiC diode. The heat sink in the design is supposed to work in static cooling condition and the size is 324mm × 305mm × 57mm. Overall system dimension is 300mm × 280mm × 48mm, thus leading to a volume of 4 liters and a form factor of 2.5kW/l.

1.1 Key System Specifications

Since this reference design is split into three main stages, the key specifications for each stage is defined individually. Table 1-1 shows the key specifications for the DC/AC converter, Table 1-2 for the boost converter and Table 1-3 for the bidirectional DC/DC converter.

Table 1-1. Key System Specifications: DC/AC Stage

PARAMETER	SPECIFICATION
Maximum | Nominal DC input voltage	520V | 400V
Rated output voltage	230V
Rated output power	4.6kW
Switching frequency	87kHz
Power factor	± Active, ±Reactive
Ambient temperature range	–40 °C to +60 °C
Cooling	Static cooling
Heat sink thermal resistance	0.3 °C/W
Total harmonic distortion (THD)	< 5 %
DC-link capacitance	800µF
DC-link voltage ripple	±23V

Table 1-2. Key System Specifications: DC/DC Boost Stage

PARAMETER	SPECIFICATION
String input voltage	50V to 500V (up to 10 panels per string)
Short circuit current	18A
Nominal DC current	14A | string
Maximum | Nominal DC-link voltage	520V | 400V
Nominal output power	10kW
Switching frequency	130kHz
Ambient temperature range	–40 °C to +60 °C

Table 1-3. Key System Specifications: Bidirectional DC/DC Stage

PARAMETER	SPECIFICATION
Maximum | Nominal DC-link voltage	520V | 400V
Maximum charging | discharging current	30A | 30A
Battery voltage range	50V to 500V
Nominal output power	10kW
Switching frequency	65kHz each leg
Ambient temperature range	–40 °C to +60 °C

CAUTION

Do not leave the design powered when unattended.

WARNING

High voltage! *Accessible high voltages are present on the board.* Electric shock is possible. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

TI considers the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. *When energized, do not touch the design or components connected to the design*.

WARNING

Hot surface! Contact can cause burns. Do not touch!

Some components can reach high temperatures > 55°C when the board is powered on. Do not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

WARNING

TI intends this reference design to be operated in a ***lab environment only and does not consider the design as a finished product*** for general consumer use. The design is intended to be run at ambient room temperature and is not tested for operation under other ambient temperatures.

TI intends this reference design to be used only by ***qualified engineers and technicians*** familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are ***accessible high voltages present on the board*** . The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

1.2 PV Input with Boost Converter

Figure 1-1 shows a block diagram of boost topology. This design consists of two parallel independent string inputs with one common output rail. The input voltage of each string is variable and dependent on various factors such as temperature, number of panels in series, the Maximum Power Point (MPP) operating voltage of the string which is set by the software, etc. Each input is connected to a DC/DC boost stage which boosts the variable string voltage output to a higher and regulated DC-link voltage. The stage is controlling input voltage and current for the strings and implements Maximum Power Point Tracking (MPPT) algorithm for each string. The common DC-link then provides a common bus for connection to the DC/DC bidirectional converter and the DC/AC converter.

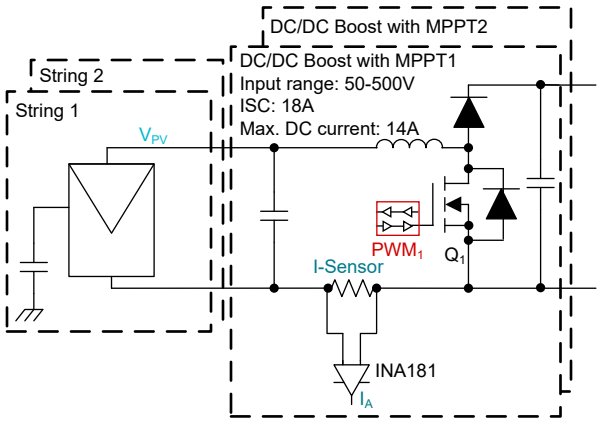


Figure 1-1. Boost Converter Block Diagram

Each string can consist of 2 to 10 panels in series equating to an input voltage of 50V to 500V maximum, considering each panel is nominally 50V rated. With a nominal voltage rating of 350V and 14A input current, the converters are 5kW rated, with an ability to provide a total input power of 10kW.

In this application, the duty-cycle of the boost converter is variable and depends on the input string voltage since the DC-link voltage is kept constant. The GaN FETs are switched at frequencies of 130kHz each.

1.3 Bidirectional DC/DC Converter

Figure 1-2 shows a block diagram of the bidirectional DC/DC converter topology. In non-isolated topologies like that of a string converter, a bidirectional converter can be used to have the possibility of battery energy storage. Bi-directionality is necessary since the DC/DC converter needs to act as a battery charger (buck mode) in one direction and discharge the battery (boost mode) providing a higher and stable output voltage at the DC-link.

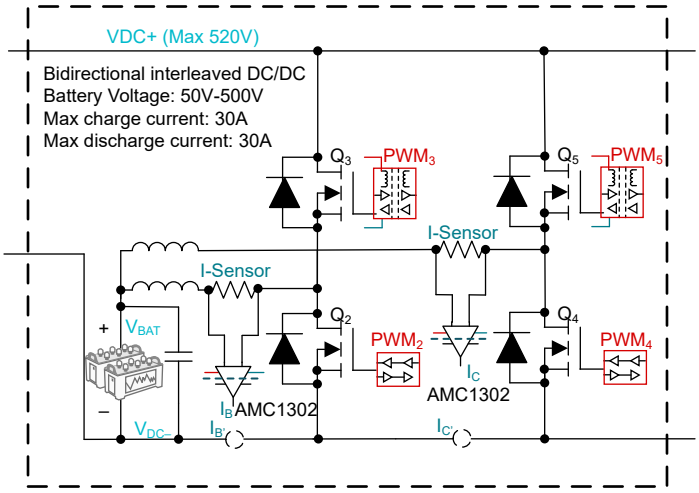


Figure 1-2. Bidirectional DC/DC Converter Block Diagram

In boost mode, since this converter supplies the inverter through the DC-link, the discharge power is limited to 4.6kW, the limitation being the maximum power rating of the inverter stage. Depending on the battery voltage, this value can go up to 30A. In the buck mode as well, there is a possibility to employ a charging current of 30A to reach higher power levels.

With a current value of 30A, just the conduction losses of a single GaN FET alone can be very high (30×30×0.03 = 27W) – which can lead to heating of the GaN device, which in turn increases the conduction losses as the $R_{DS(on)}$ of the GaN FET also increases with temperature.

To reduce this effect of overheating of the devices and increased power losses due to higher conduction and switching losses of the FETs, one plausible design can be interleaving of the branches. A phase difference of 360° / 2 equals 180° is applied between the legs to reduce ripple current as seen in Figure 1-3.

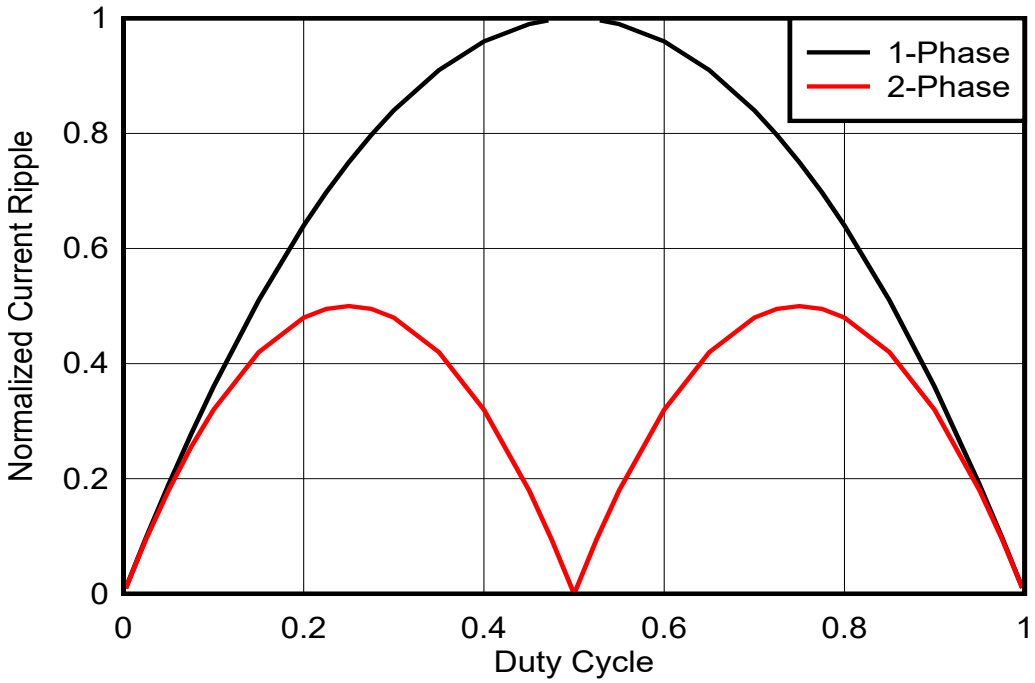


Figure 1-3. Normalized Current Ripple v/s Duty Cycle

Because both the phases of a multiphase design such as this, are tied together at the output node, the inductor currents of each phase are concurrently charging and discharging the output capacitors depending on which phase is active (titled L1 and L2 Current). This charging and discharging produce an overall output current (titled Output Current), which has a lower peak-to-peak value as shown in Figure 1-4.

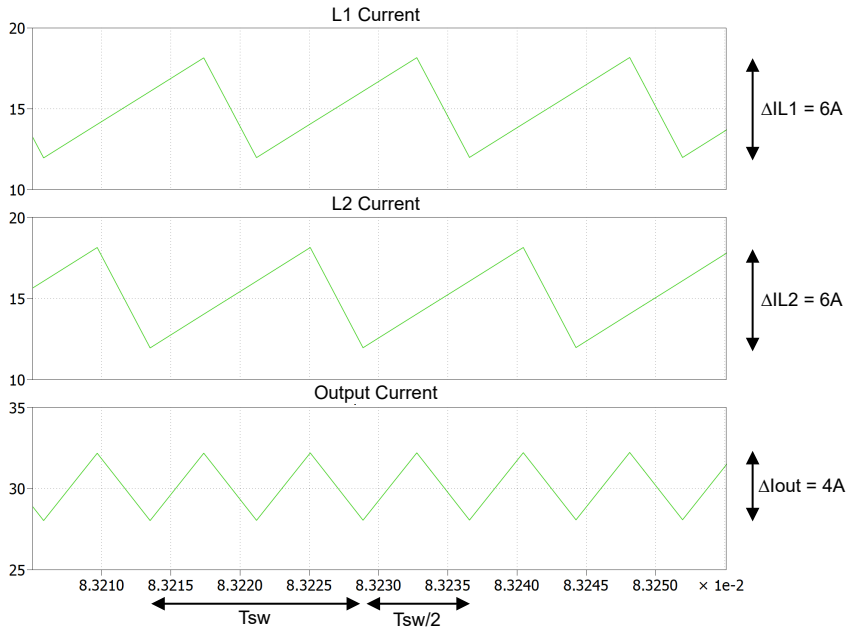


Figure 1-4. Output Current Waveforms

Smaller ripple current or AC current in the output capacitors lowers the overall output voltage ripple which in turn lowers the amount of capacitance needed to keep the output voltage within tolerance. Adding additional phases to a design decreases the RMS input current flowing through the decoupling capacitors thereby reducing the ripple on the input voltage.

Paralleling of the branches also helps in achieving twice the switching frequency across the output EMI filter which helps reduce the size. Symmetric interleaving involves switching the different sections with the same frequency but with interleaving of the phases to control noise output and ripple. The same current is demanded from both the branches leading to twice the output current and the duty-cycle is fixed depending on the battery voltage and the DC-link voltage. Furthermore, a dead time is inserted between the half-bridge FETs to avoid short circuit of current paths, while the switches switch in a complementary fashion. This design is therefore rated to provide a 4.6kW output for boost stage and has a capability to charge the battery nominally up to 10kW at a battery voltage of around 330V. Each interleaved stage is switched at a frequency of 65kHz, resulting in an equivalent output frequency of 130kHz.

1.4 DC/AC Converter

Figure 1-5 shows a block diagram for the DC/AC stage. The inverter stage is bidirectional, enabling power conversion from DC stage to AC stage and vice versa. The topology is constituted by an H-Bridge with each group of diagonal switches operating at high frequency during one half-wave of output voltage. Additional switches placed in parallel to the grid allows an additional voltage-level across the output filter making this power conversion system a three-level topology, thus reducing the switching losses and COSS losses across the FETs. This also enables constant common-mode voltage leading to negligible leakage current since the PV input stage is decoupled from the AC grid in the freewheeling phase.

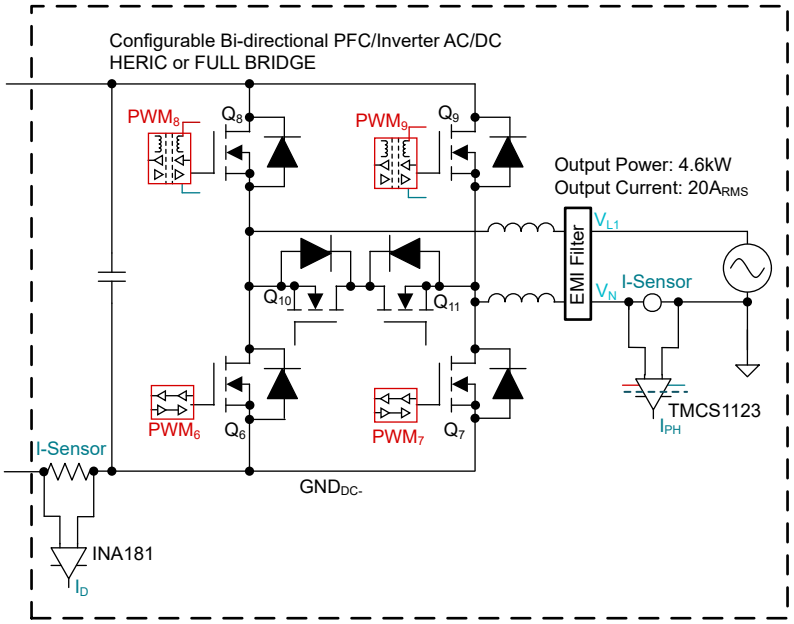


Figure 1-5. DC/AC Converter Block Diagram

This topology is a good choice for transformer-less string inverter applications where there is no isolation available between the AC grid and the PV panels. The common-mode currents are a well-known challenge in PV applications due to PV surfaces exposed over grounded roof or other surfaces in the proximity. The large surface areas can lead to high values of stray capacitance between the PV panel and ground, which can go as high as 200nF / kWp in damp environments or on rainy days, as seen in Figure 1-6. This parasitic capacitance can cause high common-mode current flowing into the system when common-mode voltage of the converters is not well mitigated and can lead to EMI and issues such as grid current distortion.

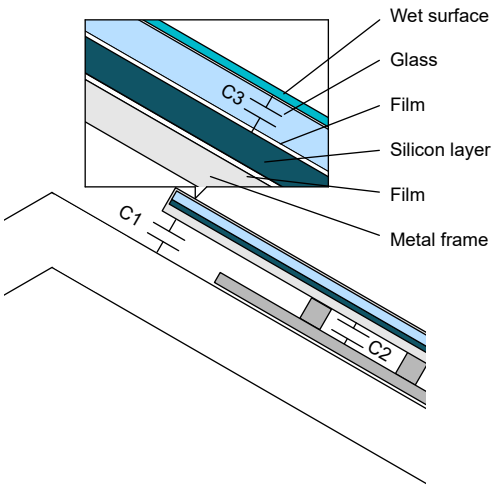


Figure 1-6. PV Panel Parasitic Capacitance

Microinverters containing transformers present high impedance return path for current, however, that is not the same case with cost-sensitive applications such as string inverters. String inverters usually present low impedance paths for return currents, hence leading to very high values of currents as shown in Figure 1-7. The leakage currents to the ground thus constitute an important issue in transformer-less concepts. Special single-phase transformer-less topologies with reduced oscillations can be implemented for such purposes and is later discussed. In addition, the introduction of frame-less panels further contributed to the reduction of such problems.

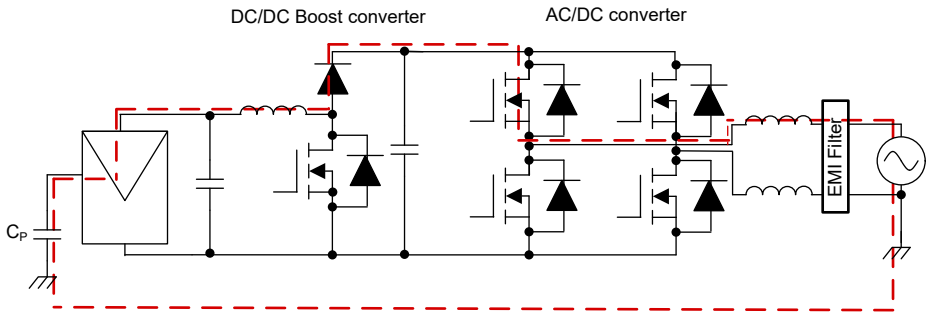


Figure 1-7. Common-Mode Noise

This DC/AC converter stage is operated at a high switching frequency of 87kHz for sinusoidal grid current control, thus allowing the EMI filter design to be compact. With the signle-phase $230V_{RMS}$ grid, an output power of 4.6kW can be achieved with an output current of $20A_{RMS}$. The EMI filter is composed of a boost inductor split between both rails for better common-mode rejection capability, two common-mode chokes, C_x capacitors, and C_y capacitors. The EMI filter has been designed to attenuate both the differential-mode and common-mode noise injected into the grid. Additionally, electrolytic capacitors are present at the DC- link to compensate for the 100Hz power ripple present in such single-phase applications. Note that both of the half-bridges need to have a dead-time to avoid shoot-through. The current in the grid is measured and then controlled by the MCU using Proportional Resonant (PR) controllers. High-accuracy measurement of the current flowing in the Point of Common Coupling (PCC) is required to control active and reactive power. The current control requires the implementation of a Phase Locked Loop (PLL) which is synchronized with the grid voltage frequency. A DC-link voltage control loop is used to control the amplitude of the active current sink or source from the grid.

2 System Design Theory

2.1 Boost Converter

2.1.1 Inductor Design

In any power converter design, the inductor design is the most important part. The four important characteristics pertaining to the inductor design are namely the inductance value, ripple current, saturation current and the DC resistance (DCR).

Normally, the value of inductance can be calculated with Equation 1.

$$L \geq \frac{V_{in} \times (V_{out} - V_{in})}{\Delta i_{L(pk-pk)} \times f_{sw} \times V_{out}} \quad (1)$$

where

- V_{out} is the output voltage of the boost converter
- V_{in} is the input voltage of the boost converter
- f_{sw} is the switching frequency
- i_L is the inductor ripple current

Other way around, the inductor ripple can also be given by Equation 2.

$$\Delta i_{L(pk-pk)} \geq \frac{V_{in} \times (V_{out} - V_{in})}{L \times f_{sw} \times V_{out}} \quad (2)$$

where,

- V_{out} is the output voltage of the boost converter
- V_{in} is the input voltage of the boost converter
- L is the value of inductance
- f_{sw} is the switching frequency

The worst-case duty cycle for a boost converter or a single-phase converter is 50% as seen in Figure 1-3. Hence the inductance value is calculated for the corresponding condition. Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. The saturation current of the inductor must be higher than the calculated peak inductor current.

In a boost regulator, the inductor DC current can be calculated by Equation 3.

$$I_{L-DC} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta} \quad (3)$$

where,

- V_{out} is the output voltage of the boost converter
- I_{out} is the output current of the boost converter
- V_{in} is the input voltage of the boost converter
- η is the power conversion efficiency

Therefore, the inductor peak current is calculated with Equation 4.

$$i_{L-pk} = i_{L-DC} + \frac{\Delta i_{L(pk-pk)}}{2} \quad (4)$$

2.1.2 Rectifier Diode Selection

To further reduce losses in the system, and achieve a high efficiency of the rectification stage, the recommendation is to go with Schottky diode since the Schottky diode has low forward voltage drop and faster recovery time.

The forward current rating needs to be greater than the maximum output current as seen by Equation 5.

$$I_F > I_{out-max} \quad (5)$$

where,

- I_F is the average forward current of the rectifier diode
- $I_{out-max}$ is the maximum output current necessary in the application

Schottky diodes have a much higher peak current rating than average rating. Therefore the higher peak current in the system is not a problem.

The other parameter that need to be checked, is the power dissipation of the diode to keep in check the conduction losses. The diode is able to handle the power dissipation according to Equation 6.

$$P_D = I_F \times V_F \quad (6)$$

where,

- I_F is the average forward current of the rectifier diode
- V_F is the forward voltage of the rectifier diode

In this application, the C6D20065G is used which is a 650V, 20A Silicon Carbide Schottky Diode.

2.1.3 MPPT Operation

The power output from a PV panel depends on a few parameters, such as the irradiation received by the panel, panel voltage, panel temperature, and so forth. Correspondingly, the power output from a string of PV panels, depends on the individual conditions of the PV panels. The power output also varies continuously throughout the day as the conditions affecting the change. Figure 2-1 shows the I-V curve and the P-V curve of a single solar panel. The I-V curve represents the relationship between the panel output current and the output voltage. As the I-V curve in the figure shows, the panel current is at the maximum when the terminals are shorted and is at the lowest when the terminals are open and unloaded.

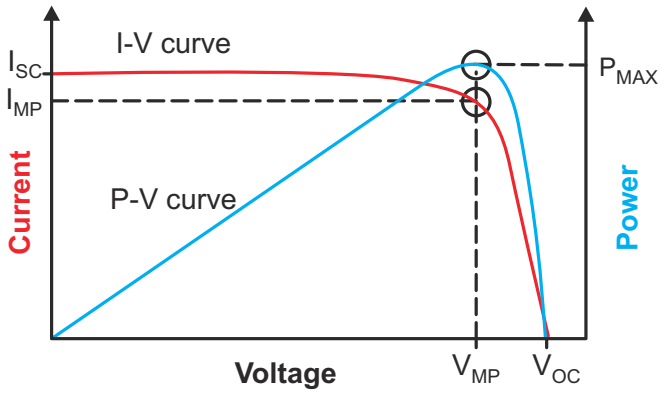


Figure 2-1. Solar Panel Characteristics I-V and P-V Curves

As shown, the maximum power obtained from the panel represented as P_{MAX} at a point when the product of the panel voltage and the panel current is at the maximum. This point is designated as the maximum power point (MPP). Figure 2-2 and Figure 2-3 show examples of how each of the various parameters affect the output power from the solar panel. The graphs also show the variation in the power output of a solar panel as a function of irradiance. Observe in these graphs how the power output from a solar panel increases with the increase in irradiance and decreases with a decrease in irradiance. Also note that the panel voltage at which the MPP occurs also shifts with the change in irradiance. Similar concept can also be applied to a string inverter where the overall string voltage is monitored in addition to the string output current.

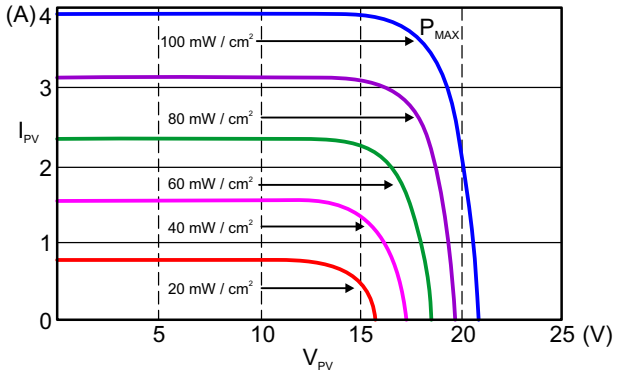


Figure 2-2. Solar Panel Output Power Variation Under Different Irradiation Conditions Graph A

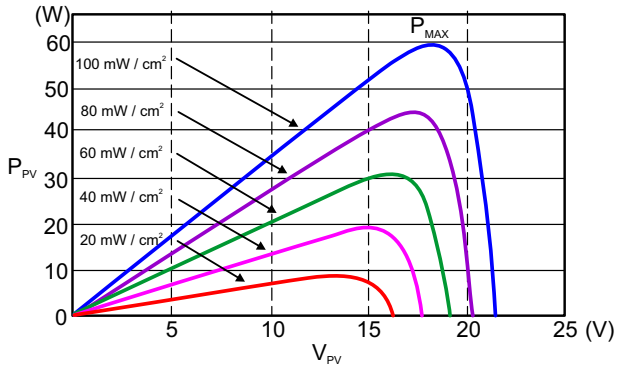


Figure 2-3. Solar Panel Output Power Variation Under Different Irradiation Conditions Graph B

The challenge of automatically identifying the MPP of the panel is typically performed by employing MPPT algorithms in the system. The MPPT algorithm tries to operate the string at the maximum power point and uses a switching power stage to supply the load with the power extracted from the panel. Perturb and Observe (PO) is one of the most popular MPPT algorithms used. The fundamental principle behind this algorithm is simple and easy to implement in a microcontroller based system. The process involves slightly increasing or decreasing (perturbing) the operating voltage of a panel. Perturbing the string voltage is accomplished by changing the duty cycle of the converter. Assuming that the string voltage has been slightly increased and that this leads to an increase in the panel power, then another perturbation in the same direction is performed. If the increase in the string voltage decreases the panel power, then a perturbation in the negative direction is done to slightly lower the string voltage. By performing the perturbations and observing the power output, the system begins to operate close to the MPP of the string with slight oscillations around the MPP. The size of the perturbations determines how close the system is operating to the MPP. Occasionally this algorithm can become stuck in the local maxima instead of the global maxims, but this problem can be solved with minor tweaks to the algorithm. The PO algorithm is easy to implement and effective, and was chosen for this design.

2.2 Bidirectional DC/DC Converter

2.2.1 Inductor Design

In any power converter design, the inductor design is the most important part. The four important characteristics pertaining to the inductor design are namely the inductance value, ripple current, saturation current and the DC resistance (DCR).

Normally, the value of inductance can be calculated with Equation 7

$$L \geq \frac{V_{in} \times (V_{out} - V_{in})}{\Delta i_{L(pk-pk)} \times f_{sw} \times V_{out}} \tag{7}$$

where,

- V_{out} is the output voltage of the boost converter
- V_{in} is the input voltage of the boost converter
- f_{sw} is the switching frequency of the converter
- i_L is the inductor ripple current

Hence, the inductor ripple can also be given by Equation 8

$$\Delta i_{L(pk-pk)} \geq \frac{V_{in} \times (V_{out} - V_{in})}{L \times f_{sw} \times V_{out}} \tag{8}$$

where,

- V_{out} is the output voltage of the boost converter
- V_{in} is the input voltage of the boost converter
- L is the value of inductance

- f_{sw} is the switching frequency

The worst-case duty cycle for a boost converter or a single-phase converter is can be seen from Figure 1-3, to be at 25%. Hence the inductance value is calculated for the corresponding condition. Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. The saturation current of the inductor must be higher than the calculated peak inductor current.

In a boost regulator, the inductor DC current can be calculated by Equation 9

$$I_{L-DC} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta} \tag{9}$$

where,

- V_{out} is the output voltage of the boost converter
- I_{out} is the output current of the boost converter
- V_{in} is the input voltage of the boost converter
- η is the power conversion efficiency

Therefore, the inductor peak current is calculated with Equation 10,

$$i_{L-pk} = i_{L-DC} + \frac{\Delta i_{L(pk-pk)}}{2} \tag{10}$$

where,

$i_{L(pk-pk)}$ is the peak-to-peak inductor current ripple

2.2.2 Low-Voltage Side Capacitor

The low-voltage side capacitor need to filter out the AC ripple component during the buck-mode of operation. The value of capacitance can be calculated with Equation 11

$$C_{LV} = \frac{\Delta i_{out(pk-pk)}}{8 \times f_{sw} \times \Delta V_{out(pk-pk)}} \tag{11}$$

where,

- $i_{out(pk-pk)}$ is the peak-to-peak output current ripple
- f_{sw} is the switching frequency of the converter
- $V_{out(pk-pk)}$ is the peak-to-peak output voltage ripple

2.2.3 High-Voltage Side Capacitor

The high-side capacitor need to filter out the AC ripple component during the boost-mode of operation. The value of capacitance can be calculated with Equation 12

$$C_{HV} = \frac{i_{out(DC-link)} \times D}{n \times f_{sw} \times \Delta V_{out(pk-pk)}} \tag{12}$$

Where,

- $i_{out-DClink}$ is the output DC-link current
- D is the duty cycle
- n is the number of interleaved stages
- f_{sw} is the switching frequency of the converter
- $V_{out(pk-pk)}$ is the peak-to-peak output voltage ripple

2.3 DC/AC Converter

2.3.1 Boost Inductor Design

The inductor plays an important role in system efficiency, current ripple, and overall size. The inductance value is calculated based on the input voltage, output voltage, and worst-case ripple. The inductance value of the DC/AC converter can be calculated with Equation 13.

$$L \geq \frac{V_{DCBus}}{4 \times \Delta I_{pk-pk} \times f_{sw}} \tag{13}$$

where,

- f_{sw} is the switching frequency
- V_{DCBus} is the DC-link voltage
- Ipk-pk is the ripple current

Normally, the recommendation is to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. The saturation current of the inductor must be higher than the calculated peak inductor current.

The inductor peak current is calculated with Equation 14.

$$i_{L-pk} = i_{L-DC} + \frac{\Delta i_{L(pk-pk)}}{2} \tag{14}$$

where,

$i_{L(pk-pk)}$ is the peak-to-peak inductor current ripple

2.3.2 DC-Link Capacitor

DC-link capacitor voltage ripple frequency is double the line frequency. The DC-link capacitor is responsible for removal of this voltage ripple to provide a stable DC-link voltage. The required DC-link capacitance can be calculated as shown in Equation 15.

$$C_{out} \geq \frac{P_{out}}{V_{out} \times 2 \times \pi \times f_g \times V_{ripple}} \tag{15}$$

where,

- V_{out} is the DC-ink nominal voltage
- f_g is the frequency of the grid
- P_{out} is the maximum power
- V_{ripple} is the peak to peak voltage ripple

3 System Overview

3.1 Block Diagram

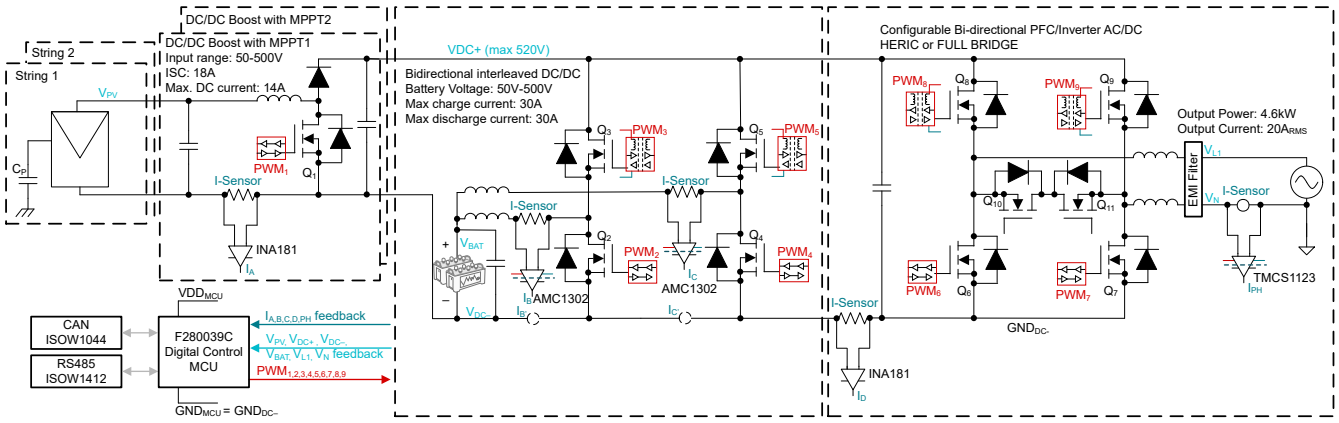


Figure 3-1. TIDA-010938 Block Diagram

3.2 Design Considerations

3.2.1 Boost Converter

The first stage of this reference design is the non-isolated boost converter. This design has two identical channels having a common output rail. By boost converter nature, the output voltage during operation needs to be higher than the input voltage. Considering a string input with up to 10 panels has a voltage range up to 500V, a DC-link voltage of 400V can be chosen with a maximum of 520V. The key parameters can be seen in Table 3-1.

Table 3-1. Boost Converter Specifications

PARAMETER	SPECIFICATION
String input voltage	50V to 500V (up to 10 panels per string)
Nominal DC current	14A | string
Maximum | Nominal DC output voltage	520V | 400V
Nominal output power	5kW
Switching frequency	130kHz

3.2.1.1 High-Frequency FETs

LMG3522R030 is used for this stage. It is the 650V rated 30 mΩ GaN FET with integrated driver and has advanced power management features that include digital temperature reporting and fault detection for overcurrent, short-circuit, overtemperature, VDD UVLO, and high-impedance RDRV pin. The temperature of the GaN FET is reported through a variable duty-cycle PWM output and enables straightforward junction temperature reading at point of interest. An input EMI filter has been designed for differential noise rejection and to stay below the conducted emissions mask. High quality output ceramic capacitors and film capacitor is placed at the DC-link output to handle the current ripple. The inductor used is Bourns 145451. The schematic for one converter stage can be seen in Figure 3-2.

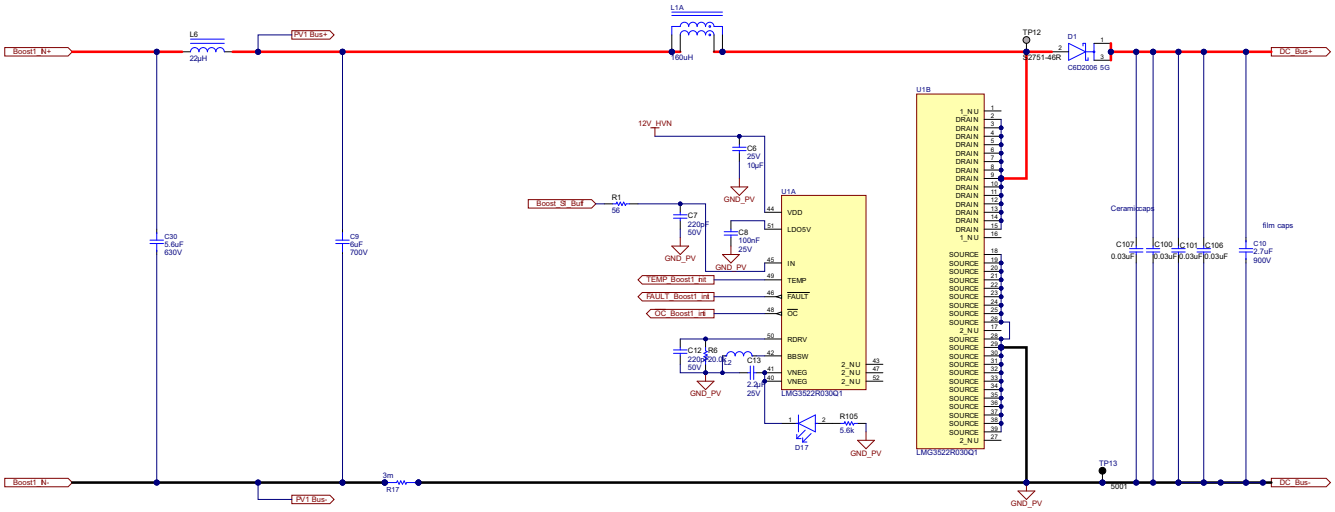


Figure 3-2. Boost Converter Design

The switching frequency is quite high, so it is important to focus on the parasitic inductance and power loop. Reducing the effect of parasitic inductance reduces the voltage spike at the switching node. The routing for the switching node between the GaN, SiC diode, inductor has a very small loop area in the PCB layers and leads to small parasitic inductance and less ringing. Four capacitors in parallel help to reduce Equivalent Series Inductance (ESL) by a factor of four. The power loop between the diode, ceramic capacitors and the GaN is also made as small as possible. The layout for the LMG3522R030 is shown in Figure 3-3, where the switching node is highlighted in yellow and the power loop is marked with arrows. Notice, the SiC diode has a lot of vias underneath as can be seen in the layout. This is done in order to reduce the thermal resistance of the PCB by improving heat dissipation. Both the boost stages are designed to be symmetrical and the schematic and layout are kept as identical as possible.

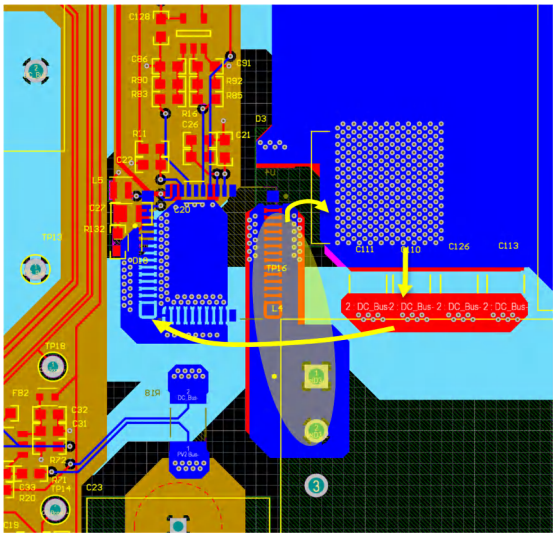


Figure 3-3. Boost Converter Layout

3.2.1.2 Input Voltage and Current Sense

It is important to closely monitor the string input current and voltage to be able to achieve maximum power from each string through MPPT. MPPT is thoroughly described in Section 2.1.3.

To enable MPPT operation, the reference design enables voltage and current measurements of each string input. Since the MCU shares the same ground as the DC Bus- potential, hence there is the possibility to have non-isolated measurements. This enables the use of cost-competitive non-isolated shunt-based current-sensing design using the INA181. INA181 is a bidirectional voltage output current-sense amplifier. The device has

reference voltage input that is used to measure negative current during battery charging. INA181A2 has an internal gain set up to 50V/V and a bandwidth of 210kHz. Sizing the shunt resistor for this design is a trade-off between sensing accuracy and power dissipation. A 3mΩ shunt provides a measurement range of ±22A output inverter but also only generates 0.6W of heat at full load. This can be seen in Figure 3-4.

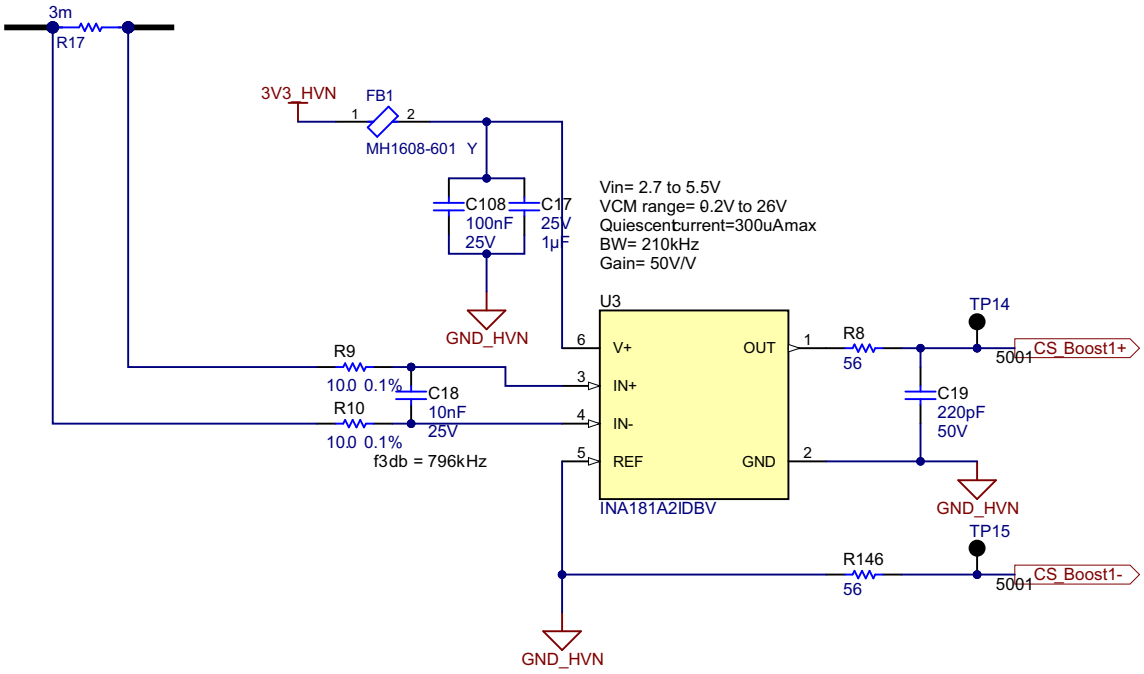


Figure 3-4. Input Current Sense

For the voltage measurement of the boost stages, the OPA2388 is used which is a dual channel operational amplifier. Both the channels are used for both boost stage voltage measurements.

3.2.2 Bidirectional DC/DC Converter

As previously mentioned, the bidirectional DC/DC converter is an interleaved DC/DC converter with the capability to either work as a buck converter when charging the battery or work as a boost converter when charging the DC Bus, hence the DC/AC converter from the battery. The specifications for this stage can be seen in Table 3-2.

Table 3-2. Bidirectional DC/DC Converter Specifications

PARAMETER	SPECIFICATION
Maximum | Nominal DC-link voltage	520V | 400V
Maximum charging | discharging current	30A | 30A
Battery voltage range	50V to 500V
Nominal output power	10kW
Switching frequency	65kHz each leg

3.2.2.1 High-Frequency FETs

Similar to the boost converters, this stage also employees the use of LMG3522R030. A difference in this stage is that the High-side (HS) FETs need isolation from the MCU. The control signal isolation is based on digital isolators ISO7741. The digital isolator is a quad-channel, 3/1 device, and for this device the basic isolation version is used since that is enough for the system. Power to the digital isolator is supplied by the internally generated 5V from the LDO of the LMG3522R030 device. The power supply isolation is based on the UCC14131 which is a high isolation DC/DC power module and provides an isolated 12V supply for the GaN FET from the 12V power supply on the board. LMG3522R030 also has built-in junction temperature reporting. This temperature signal is isolated by using the same digital isolator. The temperature information can be used in the

control MCU to thermally protect the converter when ambient temperature is high. The inductor used is Bourns 145452. The schematic for the same can be seen in Figure 3-5.

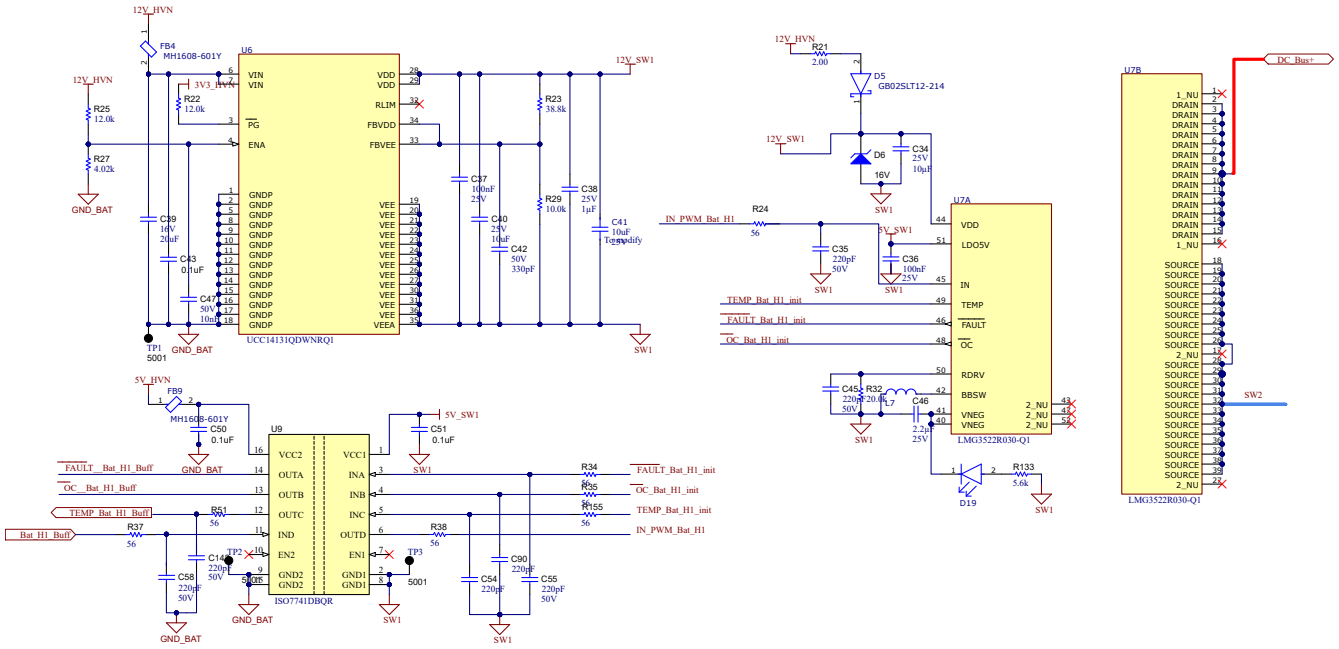


Figure 3-5. High-Side GaN of Bidirectional DC/DC Converter

Since the switching frequency is quite high here as well, it is important to focus on the parasitic inductance and power loop. The routing for the switching node between the HS and LS GaN has a very small loop area in the PCB layers and leads to small parasitic inductance and less ringing. Four capacitors in parallel help to reduce Equivalent Series Inductance (ESL) by a factor of four. The power loop between the GaNs and ceramic capacitors is also made as small as possible. The layout for the above-mentioned loops is shown in Figure 3-6, where the switching node is highlighted in yellow and the power loop is marked with arrows. Both the legs of the bidirectional DC/DC converter are designed to be symmetrical and the schematic and layout are kept as identical as possible.

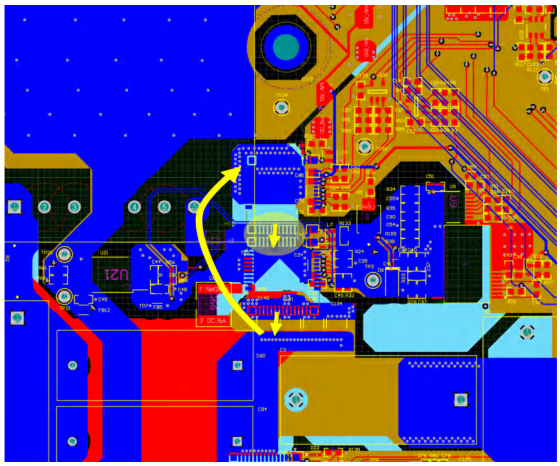


Figure 3-6. Bidirectional DC/DC Converter Layout

3.2.2.2 Current and Voltage Measurement

A big challenge of multi-phase converters is even balancing of the currents between the active phases to avoid thermally stressing any one phase and provide optimal ripple cancellation. Hence it is important to have symmetrical design and layout, similar switching loops, synchronized current sensing for current loop feedback that needs to be fed back to the controller to accurately monitor the phase currents.

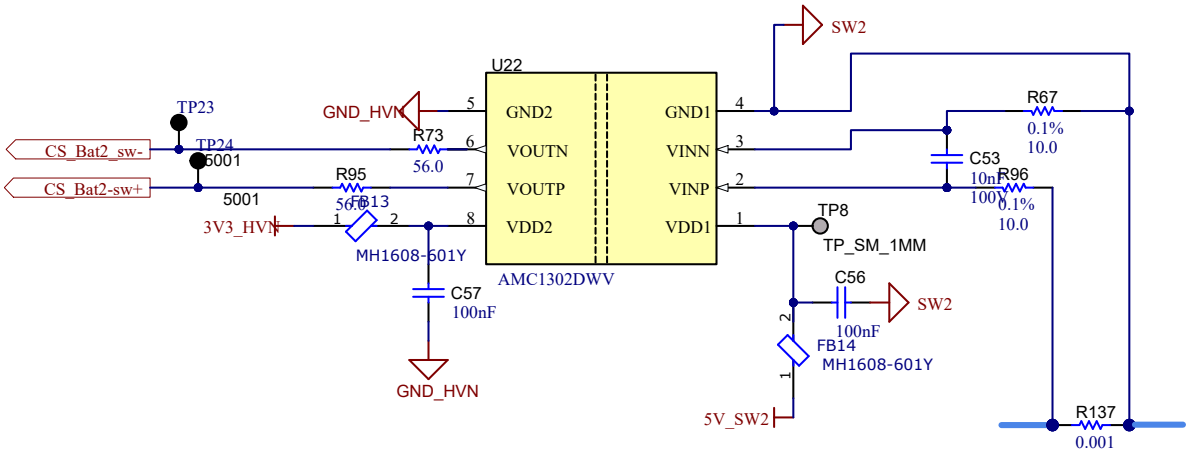


Figure 3-7. Current Sense

The current measurement is done at the respective switching nodes, as seen in Figure 3-7, for each phase with an isolated current amplifier the AMC1302 which is a precision current sensing reinforced isolated amplifier without integrated DC/DC. This IC has ±50mV input voltage range optimized for current measurement with low input impedance. The DC current is passed through a 1mΩ shunt, thus leading to a linear range of the measurement ±50A. The power to the device is supplied by the internally generated 5V from the LDO of the LMG3522R030 device.

For the voltage measurement of the boost stages, the OPA2388 is used which is a dual channel operational amplifier.

3.2.2.3 Input Relay

Since the input terminal of the DC/DC converter is connected to a battery, and as a battery acts more like low-impedance voltage source, there is a possibility of events of overcurrent to the board on startup. Hence a relay with a pre-charge circuit is used to connect and disconnect the circuitry from the battery.

3.2.3 DC/AC Converter

The DC/AC converter is a bidirectional converter, able to operate as both inverter and PFC. The DC/AC converter is a configurable converter, and can be run in the following three different modulation schemes.

- H-Bridge in Unipolar topology
- H-Bridge in Bipolar topology
- HERIC topology

With all pros and cons of the topologies considered, the system can be configured as required with a few tweaks in software and hardware. The specifications of this stage are mentioned in Table 3-3

Table 3-3. DC/AC Converter Specifications

PARAMETER	SPECIFICATION
Maximum | Nominal DC-link voltage	520V | 400V
Rated output voltage	230V
Rated output power	4.6kW
Switching frequency	87kHz
DC-link capacitance	800uF
DC-link voltage ripple	±23V

3.2.3.1 High-Frequency FETs

The LMG3522R030 which is a top-side cooled device, is also used for the AC/DC converter design. This GaN FET has integrated gate-drive and built-in protections. The gate drive speed can be configured by an external resistor. In the current board design, the AC/DC FETs can be divided into two power stages, let's call them Power Stage A and Power Stage B, as seen in Figure 3-8.

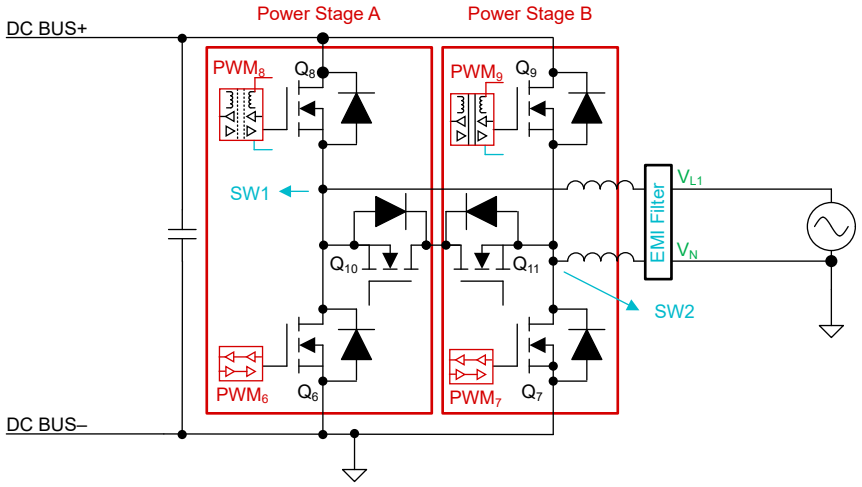


Figure 3-8. Power Stages of DC/AC Converter

In each power stage, there exist two FETs which need isolation from the MCU. The control signal isolation is based on digital isolators ISO7762. The digital isolator is a six-channel, 4/2 device, and for this device the basic isolation version is used since that is enough for the system. Power to the digital isolator is supplied by the internally generated 5V from the LDO of the LMG3522R030 device. The power supply isolation is based on the UCC14131 which is a high isolation DC/DC power module and provides an isolated 12V supply for the GaN FET from the 12V power supply on the board. LMG3522R030 also has built-in junction temperature reporting. This temperature signal is isolated by using the same digital isolator. The temperature information can be used in the control MCU to thermally protect the converter when ambient temperature is high. Each digital isolator takes care of two FET's temperature reporting, Fault/OC signals, and PWM signal. The dead-time between FETs on the same leg is kept to be 140ns to avoid shoot-through. The HS FETs have a configuration similar to that of the Bidirectional DC/DC converter with two FETs sourcing 12V from the magneto and the digital pins for both connected to the same digital isolator.

The switching frequency is quite high, there is importance to focus on the parasitic inductance and power loop. Reducing the effect of parasitic inductance reduces the voltage spike at the switching node. The routing for the switching node between the GaNs on the same switching node and the boost inductor has a very small loop area in the PCB layers and leads to small parasitic inductance and less ringing. The bottom layer is used for the switching nodes, which is kept relatively small but enough to have the approximate current carrying capability. Additionally, for the control circuitry of the switching node, polygons on inner layers 1 and 2 are exploited to extend the switching node and to provide a return path for the signals on top and bottom layer. Three ceramic capacitors in parallel help to reduce Equivalent Series Inductance (ESL) by a factor of three. The power loop between ceramic capacitors and the GaN is also made as small as possible. Both the power stages are designed to be symmetrical and the schematic and layout are kept as identical as possible.

Also important is to have a good DC Bus- or ground connection throughout the board. Also recommended to have a good polygon pour for DC Bus+, AC line and neutral current paths since these are carrying high currents. For signals on the top layer, the recommendation is to have a return layer on the inner layer 1, and for signals routed on the bottom the recommendation is to have a return path through inner layer 2. This helps in preserving the integrity of the signals.

3.2.3.2 Current Measurements

Critical to attaining a closed-loop control system is accurate current measurement of the inverter. The current in the grid is measured by means of a Hall-based current sensor TMCS1123 which allows measurement of the current into the Point of Common Coupling (PCC) with high accuracy. This design allows a reinforced isolation between the grid and the MCU. This current measurement can be seen in Figure 3-9.

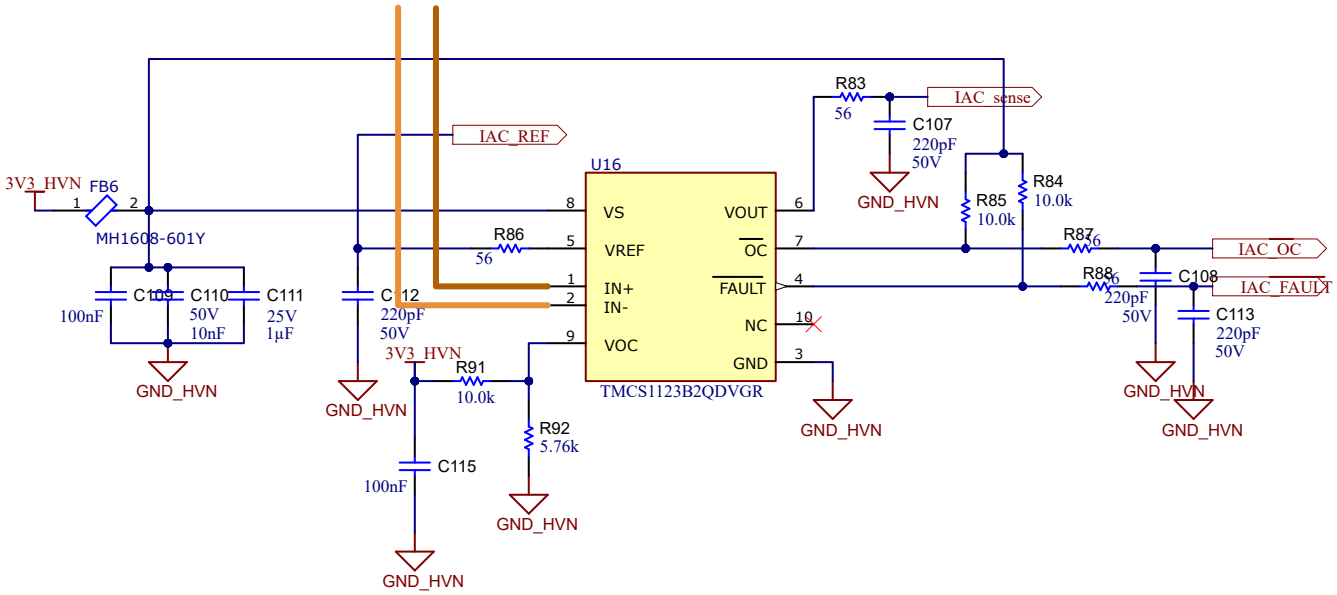


Figure 3-9. AC Current Sense

3.2.3.3 Voltage Measurements

Voltage sensing provision is provided at two points in the inverter signal path to aid in control: before and after the output relay. By enabling measurement on both sides of the relay, the control system can lock into the grid voltage and frequency before connecting, thus preventing any mismatch issues. OPA2388 is used a which is a dual channel operational amplifier. Both the channels are used for the AC voltage measurements. The DC bus voltage is also sensed using another OPA2388 .

3.2.3.4 Auxiliary Power Supply

An auxiliary power supply for the GaN FETs, operation amplifiers, relays, isolated amplifiers, digital circuitry, and so on for the entire system is generated using UCC28710 in buck configuration. The idea is that, on start-up of a string inverter, the input voltage from the strings which appears across the DC bus when reaches a certain value, enables the operation of the UCC28710 buck controller and produces a 12V supply. This is a non-isolated topology, since the MCU also sits on the DC Bus-. The VS sense is set by the resistors R93 and R95 to have an output of 12V. And the current sense is set with the resistors R96, R97 and R98. It is important to keep in mind the peak current and DC current rating of the inductor L13 to have the necessary load current requirements of the circuitry satisfied.

Figure 3-10 shows the power supply schematic.

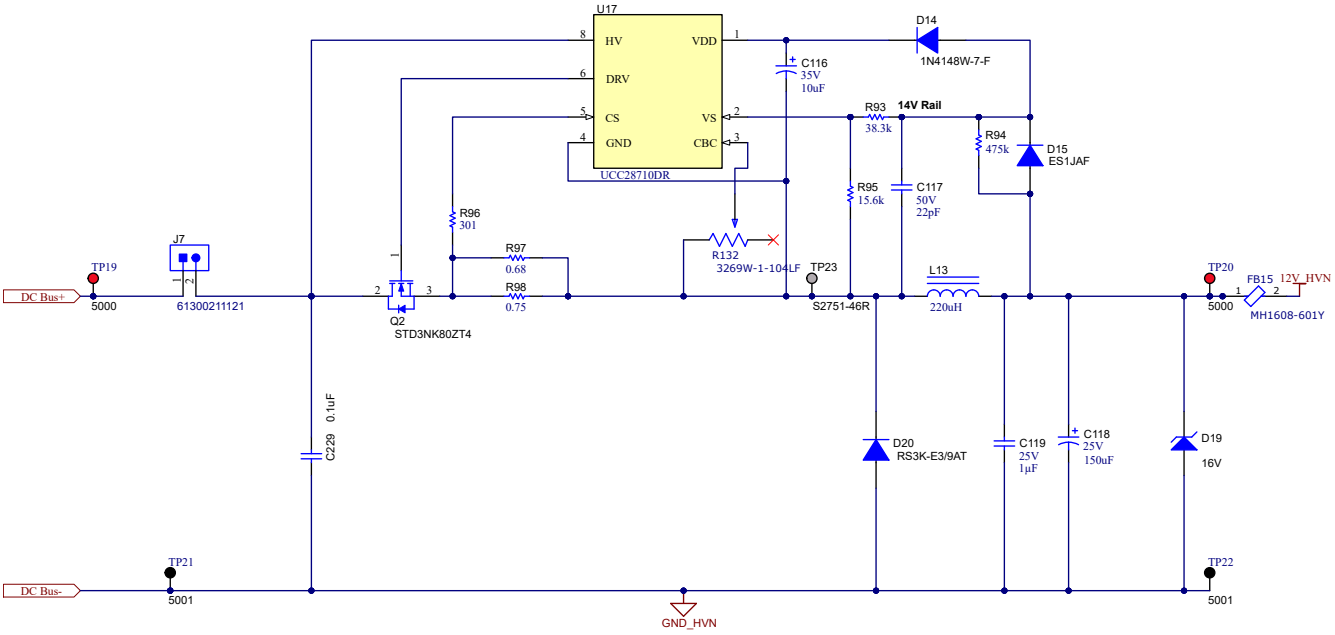


Figure 3-10. Auxiliary Power Supply Design

Furthermore, as required by other components on the board, a buck converter TPS56020 was to convert the 12V rail to a 5V rail and an LDO TLV75533 was used to convert the 5V rail to a 3V3 rail.

3.2.3.5 Passive Components Selection

As Figure 3-11 shows, multiple passive components are present in the DC/AC stage. The theory behind the design of each passive component is described in detail in the following section. The EMI filter design comprises of two boost inductors, two common-mode chokes, and a network of C_X and C_Y safety capacitors.

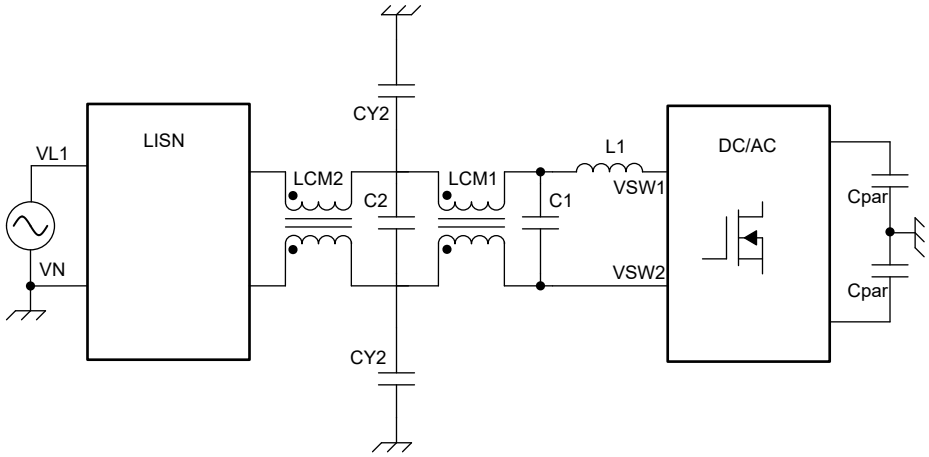


Figure 3-11. Block Diagram DC/AC Filter

- **Boost Inductor Selection**

The design of the boost inductor is essential for finding an optimal EMI filter that results in maximum filter efficiency and minimum filter volume. The primary role of the boost inductor is to filter out the switching frequency harmonics and it is necessary to keep in mind, the calculation of the current ripple and choose material of the core that is able to tolerate the calculated current ripple. The boost inductors are further split to have better common-mode filtering capability and better filtering capacity for the individual switching nodes.

The emission mask for many standards starts at 150kHz; therefore, selecting a switching frequency below 150kHz is always a good design practice. In this design, a switching frequency of 87kHz was selected for the H-Bridge Bipolar and HERIC DC/AC topologies. For H-Bridge in unipolar modulation scheme, by topology

definition, there is a doubling of switching frequency effect at the output EMI filter. Hence, a switching frequency of 43.5kHz was employed. By selecting an operating frequency of 87kHz, the first harmonic does not require significant attenuation but only the successive ones such as the 2nd, 3rd, and so forth. A current ripple factor of 30% was selected for the boost inductor, when having 230V_{AC} output. The inductance value was calculated by using Equation 16.

$$L \geq \frac{520 \ \ V}{4 \times \left(\frac{4600 \ \ W}{230 \ \ V}\right) \times \sqrt{2} \times 0.3 \times 87000 \ \ Hz} \tag{16}$$

An inductance value equal to 176µH was calculated. Bourns 145453 was selected and this is an inductor rated 87µH, 20 $_{RMS}$. The inductor is split in both legs to have better common-mode capability. In general, the boost inductor contributes to the differential and common-mode noise attention.

- **C_X Capacitance Selection**

Class-X (C_X) and Class-Y (C_Y) capacitors are safety-certified capacitors that are usually used in AC line filtering applications which help to minimize the generation of EMI. Furthermore, X capacitors are connected between the line and neutral, to protect against differential mode interference, and Y capacitors are designed to filter out common mode noise. Common mode choke coils have the use of suppression of common mode noise.

C_X are the capacitors connected between line-to-line or line-to-neutral. The aim of these capacitors is to attenuate the differential mode noise injected from the DC/AC into the grid. The value of these capacitors is a trade-off between reactive power provided to the grid and the differential mode attenuation. By default, the reactive power injected into the grid is equal to Equation 17.

$$Q = {V_g}^2 \times 2\pi f_g \times C_X \tag{17}$$

At 10% load, a power factor equal to 0.9 (26°) has been set up as requirement. Thus, leading to limit the quantity of reactive power, given by Equation 18.

$$Q_{max} = 0.1 \times P_{nom} \times tan \ \emptyset \tag{18}$$

The maximum value of capacitance can be calculated from Equation 17and Equation 18 and is equal to 13.5µF. Two C_X capacitors, respectively, with values of 4.7µF each were selected.

- **C_Y Capacitance Selection**

It is necessary to detect small leakage currents (typically 5–30 mA) and disconnect quickly enough (<30 ms) to prevent device damage or electrocution. Certain standards for the leakage current issue mention that PV systems with the transformer-less inverter must discontinue their service if the leakage current value of 100mA can persist up to 0.04s. With the total capacitance of 13.6nF going towards the ground, the leakage current through the Y capacitors can be calculated with Equation 19.

$$I_{Y-Cap} = V \times 2\pi f_g \times C_Y \tag{19}$$

For the grid voltage of 230V_{RMS}, this value comes out to be 0.98 mA < 30 mA, hence the system requirements are met.

- **EMI Filter Design**

The following EMI filter was designed to attenuate both the differential-mode and common-mode noise injected into the grid. The EMI filter can be analyzed in the common-mode and differential-mode domains. From the EMI filter shown in Figure 3-12, it is possible to derive the equivalent common- and differential-mode circuits as shown respectively in parts a) and b), where Lσ represents the leakage inductance of the common-mode choke.

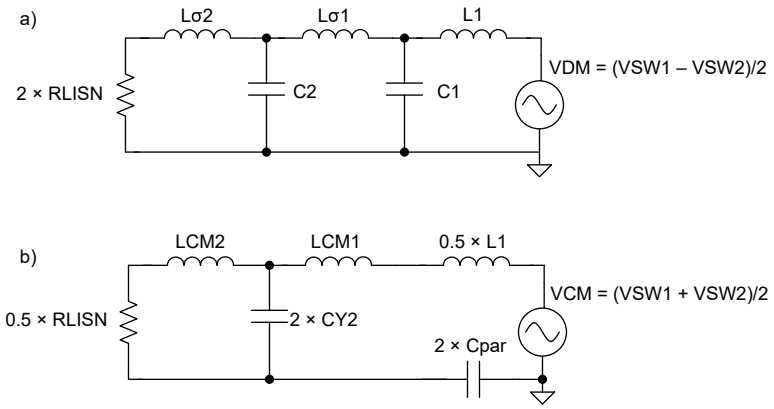


Figure 3-12. EMI Filter Design

- a. Equivalent differential-mode model
- b. Equivalent common-mode model

The first critical frequency to be attenuated is the 174kHz. The 87kHz was not considered because that value is not in the EMI mask.

Table 3-4. Attenuation Required in DM/CM Modes

ATTENUATION	VALUE
Differential-Mode Attenuation at 174kHz	87dB
Common-Mode Attenuation at 174kHz	83dB

An EMI filter with the values listed in Table 3-5 was designed.

Table 3-5. EMI Filter Values

PARAMETER	VALUE
L1	87µH
CX1	4.7µF
Lcm1	Lcm 4mH, Lσ 4µH
CX2	4.7µF
Lcm2	Lcm 4mH, Lσ 4µH
CY2	6.8nF

Two Bourns CMCs (047708) were used in this EMI filter.

- **DC-Link Capacitance**

In single-phase applications, power ripple is present coming from the grid, and can cause voltage ripple on the DC-link. The DC-link capacitor value is calculated using Equation 20.

$$C_{out} \geq \frac{4600\ \ W}{2 \times 400 \times \pi \times 50\ \ Hz \times 46\ \ V} \tag{20}$$

A total capacitance of 800µF was calculated for the 4.6kW, 400V, and 50Hz operating condition. Five of ALH82(1)161DD600 devices was selected for this application. Also note that the ripple current through the electrolytic capacitors can be handled by the model of capacitors used.

3.3 Highlighted Products

3.3.1 TMDSCNCD280039C - TMS320F280039C Evaluation Module C2000™ MCU controlCARD™

The F280039C controlCARD (TMDSCNCD280039C) from Texas Instruments (TI) provides a great way to learn and experiment with F28003x devices. The F28003x devices are members of TI's C2000™ family of microcontrollers (MCUs). This 120-pin controlCARD is intended to provide a well-filtered robust design that is capable of working in most environments.

The controlCARD™ has the following features:

- F280039C Microcontroller – High-performance C2000 microcontroller is located on the controlCARD
- 120-pin HSEC8 Edge Card Interface – Allows for compatibility with all of the 180-pin controlCARD-based application kits and controlCARDs of C2000.
- Built-in Isolated JTAG Emulation – An XDS110 emulator provides a convenient interface to Code Composer Studio™ without additional hardware. Flipping a switch allows an external JTAG emulator to be used.
- Built-in Isolated Power Supply – Passes the 5V supply from the USB Type-C® connector through an isolation barrier. Allows for the controlCARD to be completely powered and operated from the USB Type-C connector. The F280039C is fully isolated from the USB port.
- Automatic Power Supply Switch – The controlCARD automatically switches to external 5V power when present. No additional configuration is required.

For more details on this device, see the TMDSCNCD280039C product page.

3.3.2 LMG3522R030 650-V 30-mΩ GaN FET With Integrated Driver, Protection and Temperature Reporting

The LMG3522R030 GaN FET with integrated driver and protections is targeting switch-mode power converters and enables designers to achieve new levels of power density and efficiency. The LMG3522R030 integrates a silicon driver that enables switching speeds up to 150 V / ns. TI's integrated precision gate bias results in higher switching SOA compared to discrete silicon gate drivers. This integration, combined with TI's low-inductance package, delivers clean switching and minimal ringing in hard-switching power-supply topologies. Adjustable gate drive strength allows control of the slew rate from 20 V / ns to 150 V / ns, which can be used to actively control EMI and optimize switching performance. Advanced power management features include digital temperature reporting and fault detection. The temperature of the GaN FET is reported through a variable duty cycle PWM output, which simplifies managing device loading. Faults reported include overtemperature, overcurrent, and UVLO monitoring.

For more details on this device, see the LMG3522R030 product page.

3.3.3 TMCS1123 - Precision Hall-Effect Current Sensor

The TMCS1123 is a galvanically isolated Hall-effect current sensor with industry leading isolation and accuracy. An output voltage proportional to the input current is provided with excellent linearity and low drift at all sensitivity options. Precision signal conditioning circuitry with built-in drift compensation is capable of less than 1.75% maximum total error over temperature and lifetime with no system level calibration, or less than 1% maximum total error with a one-time room temperature calibration (including both lifetime and temperature drift). AC or DC input current flows through an internal conductor generating a magnetic field measured by integrated on-chip Hall-effect sensors. Coreless construction eliminates the need for magnetic concentrators. Differential Hall sensors reject interference from stray external magnetic fields. Low conductor resistance increases measurable current ranges up to ± 96 A while minimizing power loss and easing thermal dissipation requirements. Insulation capable of withstanding 5000 V_{RMS}, coupled with minimum 8.1-mm creepage and clearance provide up to 1100-VDC reliable lifetime reinforced working voltage. Integrated shielding enables excellent common-mode rejection and transient immunity. Fixed sensitivity allows the TMCS1123 to operate from a single 3-V to 5.5-V power supply, eliminates radiometry errors, and improves supply noise rejection.

For more details on this device, see the TMCS1123 product page.

3.3.4 AMC1302 - Precision, ±50-mV Input, Reinforced Isolated Amplifier

The AMC1302 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to VDE V 0884-11 and UL1577, and supports a working voltage of up to 1.5

kV_{RMS}. The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from hazardous voltages and damage. The input of the AMC1302 is optimized for direct connection to a low-impedance shunt resistor or other low-impedance voltage source with low signal levels. The excellent DC accuracy and low temperature drift supports accurate current control in PFC stages, DC/DC converters, AC-motor and servo drives over the extended industrial temperature range from –40°C to +125°C. The integrated missing-shunt and missing high-side supply detection features simplify system-level design and diagnostics.

For more details on this device, see the AMC1302 product page.

3.3.5 ISO7741 Robust EMC, Quad-channel, 3 Forward, 1 Reverse, Reinforced Digital Isolator

The ISO7741 device is a high-performance, quad-channel digital isolator with 5000 V_{RMS} (DW package) and 3000 V_{RMS} (DBQ package) isolation ratings per UL 1577. The family includes devices with reinforced insulation ratings according to VDE, CSA, TUV, and CQC. The ISO7741B device is designed for applications that require basic insulation ratings only. The ISO774x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier. These devices come with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7740 device has all four channels in the same direction, the ISO7741 device has three forward channels and one reverse-direction channel, and the ISO7742 device has two forward and two reverse-direction channels.

For more details on this device, see the ISO7741 product page.

3.3.6 ISO7762 Robust EMC, Six-Channel, 4 Forward, 2 Reverse, Reinforced Digital Isolator

The ISO7762 device is a high-performance, six-channel digital isolator with 5000-V_{RMS} (DW package) and 3000-V_{RMS} (DBQ package) isolation ratings per UL 1577. The family of devices is also certified according to VDE, CSA, TUV, and CQC. The ISO776x family of devices provides high electromagnetic immunity and low emissions at low-power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic-input and logic-output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier. The ISO776x family of devices is available in all possible pin configurations such that all six channels are in the same direction, or one, two, or three channels are in reverse direction while the remaining channels are in forward direction.

For more details on this device, see the ISO7762 product page.

3.3.7 UCC14131-Q1 Automotive, 1.5-W, 12-V to 15-V V_{IN}, 12-V to 15-V V_{OUT}, High-Density > 5-kV_{RMS} Isolated DC/DC Module

UCC14131-Q1 is an automotive qualified high-isolation voltage DC/DC power module designed to provide power to GaN, IGBT, SiC, or Si gate drivers. The UCC14131-Q1 integrates a transformer and DC/DC controller with a proprietary architecture to achieve high efficiency with very low emissions. The device can provide an isolated 12-V output from a 12-V regulated input for driving GaN and Si MOSFETs; and an isolated 15-V or 18-V output from a 15-V regulated input to bias the driver circuit for SiC MOSFET or IGBTs. The high-accuracy provides better channel enhancement for higher system efficiency without over-stressing the power device gate. The UCC14131-Q1 provides up to 1.5 W (typical) of isolated output power at high efficiency. Requiring a minimum of external components and including on-chip device protection, the module provides extra features such as input undervoltage lockout, overvoltage lockout, output voltage power-good comparators, overtemperature shutdown, soft-start time-out, adjustable isolated positive and negative output voltage, an enable pin, and an open-drain output power-good pin.

For more details on this device, see the UCC14131-Q1 product page.

3.3.8 ISOW1044 Low-Emissions, 5-kV_{RMS} Isolated CAN FD Transceiver With Integrated DC/DC Power

The ISOW1044 device is a galvanically-isolated controller area network (CAN) transceiver with a built-in isolated DC-DC converter that eliminates the need for a separate isolated power supply in space-constrained isolated designs. The low-emissions, isolated DC-DC meets CISPR 32 radiated emissions Class B standard with just two ferrite beads on a simple two-layer PCB. Additional 20-mA output current can be used to power other circuits on

the board. An integrated 10Mbps GPIO channel is available and can help remove an additional digital isolator or optocoupler for diagnostics, LED indication or supply monitoring.

For more details on this device, see the ISOW1044 product page.

3.3.9 ISOW1412 Low-Emissions, 500kbps, Reinforced Isolated RS-485, RS-422 Transceiver With Integrated Power

The ISOW1412 device is a galvanically-isolated RS-485, RS-422 transceiver with a built-in isolated DC-DC converter, that eliminates the need for a separate isolated power supply in space-constrained isolated designs. The low-emissions, isolated DC-DC converter meets CISPR 32 radiated emissions Class B standard with just two ferrite beads on a simple two-layer PCB. Additional 20-mA output current can be used to power other circuits on the board. An integrated 2Mbps GPIO channel helps remove any additional digital isolator or optocoupler for diagnostics, LED indication, or supply monitoring.

For more details on this device, see the ISOW1412 product page.

3.3.10 OPA4388 Quad, 10-MHz, CMOS, Zero-Drift, Zero-Crossover, True RRIO Precision Operational Amplifier

The OPA4388 precision operational amplifier is an ultra-low noise, fast-settling, zero-drift, zero-crossover device that provides rail-to-rail input and output operation. These features and excellent AC performance, combined with only 0.25 µV of offset and 0.005 µV / °C of drift over temperature, makes the OPA4388 a great choice for driving high-precision, analog-to digital converters (ADCs) or buffering the output of high-resolution, digital-to-analog converters (DACs). This design results in excellent performance when driving analog-to-digital converters (ADCs) without degradation of linearity. The OPA388 (single version) is available in the VSSOP-8, SOT23-5, and SOIC-8 packages. The OPA2388 (dual version) is offered in the VSSOP-8 and SO-8 packages. The OPA4388 (quad version) is offered in the TSSOP-14 and SO-14 packages. All versions are specified over the industrial temperature range of –40°C to +125°C.

For more details on this device, see the OPA4388 product page.

3.3.11 OPA2388 Dual, 10-MHz, CMOS, Zero-Drift, Zero-Crossover, True RRIO Precision Operational Amplifier

The OPA2388 is a precision operational amplifier that is an ultra-low noise, fast-settling, zero-drift, zero-crossover device that provides rail-to-rail input and output operation. These features and excellent AC performance, combined with only 0.25 µV of offset and 0.005 µV / °C of drift over temperature, makes the OPA2388 a great choice for driving high-precision, analog-to digital converters (ADCs) or buffering the output of high-resolution, digital-to-analog converters (DACs). This design results in excellent performance when driving analog-to-digital converters (ADCs) without degradation of linearity. The OPA388 (single version) is available in the VSSOP-8, SOT23-5, and SOIC-8 packages. The OPA2388 (dual version) is offered in the VSSOP-8 and SO-8 packages. The OPA4388 (quad version) is offered in the TSSOP-14 and SO-14 packages. All versions are specified over the industrial temperature range of –40°C to +125°C.

For more details on this device, see the OPA2388 product page.

3.3.12 INA181 26-V Bidirectional 350-kHz Current-Sense Amplifier

The INA181 is a current sense amplifier that is designed for cost-optimized applications. This device is a part of a family of bidirectional, current-sense amplifiers (also called current-shunt monitors) that sense voltage drops across current-sense resistors at common-mode voltages from –0.2 V to +26 V, independent of the supply voltage. The INAx181 family integrates a matched resistor gain network in four, fixed-gain device options: 20 V/V, 50 V/V, 100 V/V, or 200 V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift. These devices operate from a single 2.7-V to 5.5-V power supply. The single-channel INA181 draws a maximum supply current of 260 µA; whereas, the dual-channel INA2181 draws a maximum supply current of 500 µA, and the quad-channel INA4181 draws a maximum supply current of 900 µA. The INA181 is available in a 6-pin, SOT-23 package. The INA2181 is available in 10-pin, VSSOP, and WSON packages. The INA4181 is available in a 20- pin, TSSOP package. All device options are specified over the extended operating temperature range of –40°C to +125°C.

For more details on this device, see the INA181 product page.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

The hardware for this reference design is composed of the following:

- 1 TIDA-010938 DC/DC Board
- 1 TIDA-010938 DC/AC Board
- TMDSCNCD280039C control card
- USB Type-C® cable
- USB isolator
- Laptop

The following test equipment is needed to power and evaluate the DUT:

- Isolated 12V, 2A bench style supply for primary board power
- 2 DC supplies (>500V, >30A)
- 1 DC load (>520V, > 30A)
- 1 Bidirectional AC Grid Emulator (> $230V_{RMS}$, $20A_{RMS}$)

4.2 Note

If you have the E1 version of the TIDA-010938 DC/DC and AC/DC boards, please make the following changes, E2 version has all the modifications implemented.

- DC/DC Board
  1. Change C16 to 100nF
  2. Change R144 to 1kΩ
  3. Change C1 to 10µF
  4. Change L18 to (145454)
  5. Remove R148, R160, R161, R162, R163, R164, R165 and R166 resistors and short them.
- AC/DC Board
  1. Change U16 to TMCS1123B1 version
  2. Change relays K1 and K2 to ones with 20A rating
  3. Change Fuses F1 and F2 to ones with 25A rating
  4. Use CMC (047708) for L11 and L12
  5. Add an additional electrolytic capacitor (in addition to C2, C3, C4 and C5) - ALALH82D161DD600
  6. Interchange the nets (see Figure 4-1)
  7. Change R10, R30, R40, R44, R60, and R74 to 56kΩ
  8. Change C13, C26, C51, C41, C42, C59, C71, C96, C86, and C87 to 330pF
  9. Change R93 to 33kΩ
  10. Remove R97, change R98 to 0.1Ω
  11. Change L13 to a power inductor with higher DC and peak current rating (3A)

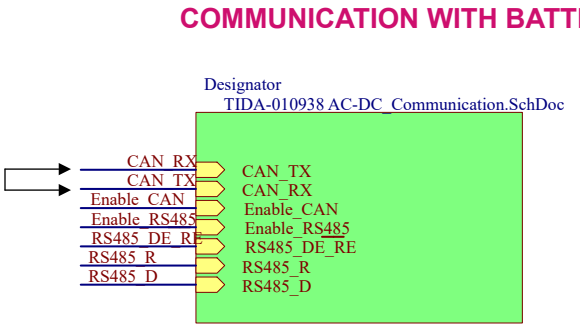


Figure 4-1. Changes in AC/DC Board

4.3 Test Setup

Following is the recommended sequence of tests:

1. DC/DC board with two independent DC power sources on inputs for the boost stages connecting to the DC load on the output
2. DC/DC board with DC power source on input for the bidirectional DC-DC stage connecting to the DC load on the output
3. DC/DC board with DC power source on the output and DC load on input for the bidirectional DC/DC stage
4. DC/AC part with DC power source on input and resistive load on the output
5. DC/AC part with DC power source on input and AC load on the output
6. Both boards together with two independent DC power sources on string inputs and AC load on the output
7. Both boards together with two independent DC power sources on string inputs, DC load on bidirectional DC/DC stage and AC load on the output

Please refer to the software user guide for more information.

4.3.1 Boost Stage

Figure 4-2 shows the connection for the boards. For safety reasons make sure that the proper voltage and current limit is selected on DC power sources. DC load needs to be configured in constant voltage mode with the required voltage and current limits. The DC bus of the DC/DC board is connected to that of the DC/AC board,

and so are the connectors for the control signals. The DC load needs to be configured in constant voltage mode with the DC bus voltage of 520V maximum and appropriate current limitation.

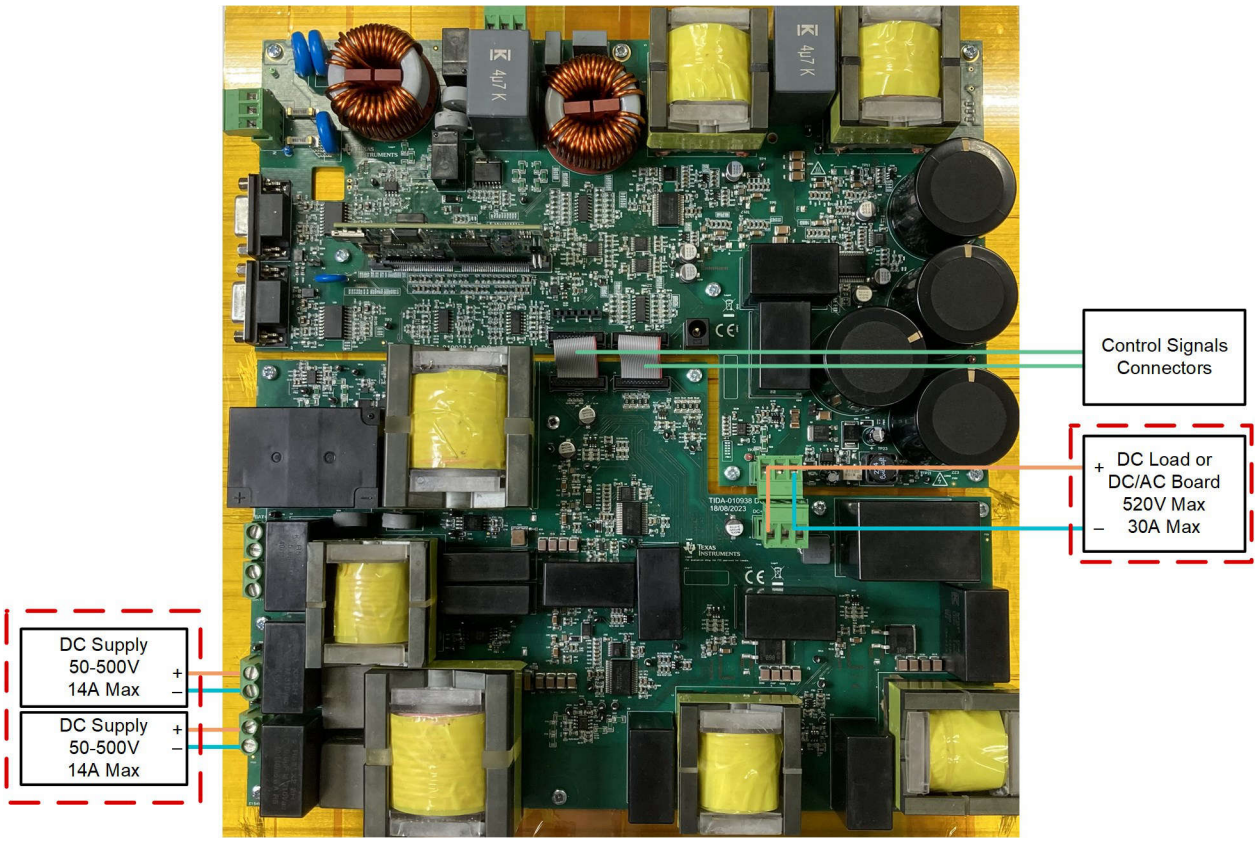


Figure 4-2. Connections for Testing Boost Converter

4.3.2 Bidirectional DC/DC Stage - Buck-Mode

Figure 4-3 shows the connection for the boards. For safety reasons make sure that the proper voltage and current limit is selected on DC power sources. DC load needs to be configured in constant voltage mode with the required voltage and current limits. The DC bus of the DC/DC board is connected to that of DC/AC board, and so are the connectors for the control signals. The DC source needs to be configured in constant-voltage mode with the DC bus voltage of 500V maximum and 30A maximum current.

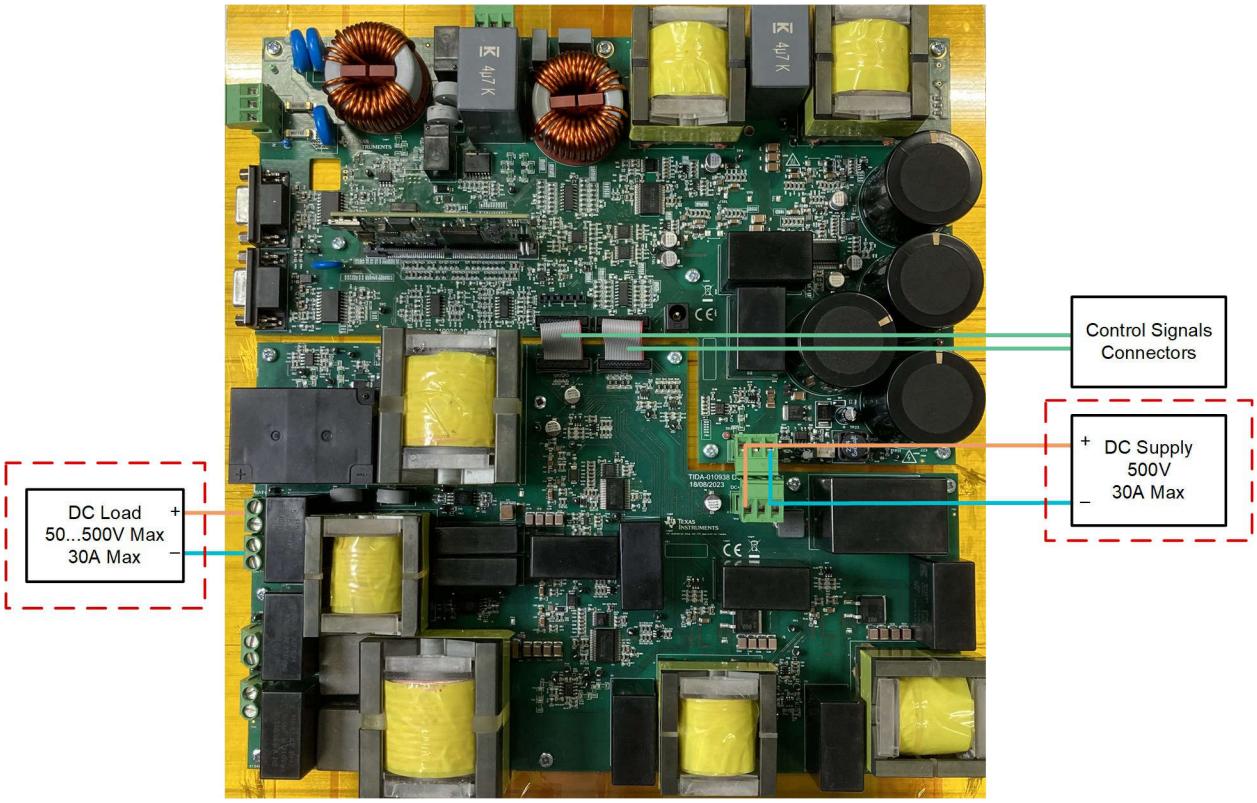


Figure 4-3. Connections for Testing Bidirectional DC-DC in Buck-mode

4.3.3 DC/AC Stage

Note

If you have the E1 version of TIDA-010938 AC/DC board, to run the system in different modulation schemes, please make the following hardware changes:

- **HERIC**

1. Desolder R20, R22, R54, R56, R257, R269 and create a short each.

- **H-Bridge Bipolar**

1. Desolder R22, R56 and create a short each.
2. Desolder R257 and create a short.
3. Desolder R269 and connect R269-2 to R249-2.
4. Desolder R20 and connect R20-2 to R243-2.
5. Desolder R54 and connect R54-2 to R241-2.

- **H-Bridge Unipolar**

1. Desolder R22, R56 and create a short each.
2. Desolder R257, R269 and create a short each.
3. Desolder R35 and connect R35-2 with R249-2.
4. Desolder R69 and connect R69-2 with R245-2.
5. Desolder R20 and connect R20-2 to R243-2.
6. Desolder R54 and connect R54-2 to R241-2.

If you have the E2 version of TIDA-010938 AC/DC board, to run the system in different modulation schemes, please make the following hardware changes:

- **HERIC**

1. Connect Jumpers J22, J23, J24, J25 and J26.

- **H-Bridge Bipolar**

1. Connect Jumpers J4, J5, J13, J21 and J22.

- **H-Bridge Unipolar**

1. Connect Jumpers J4, J5, J13, J14 and J20.

For the changes in software, please follow the software user guide.

Figure 4-4 shows the connection for the boards. For safety reasons make sure that the proper voltage and current limit is selected on DC power source and the AC Grid simulator. DC source needs to be configured in constant voltage mode with the required voltage and current limits. The DC bus of the DC/DC board is connected to that of DC/AC board, and so are the connectors for the control signals. The bidirectional AC Grid Simulator is configured with the approproate voltage, frequency and current settings.

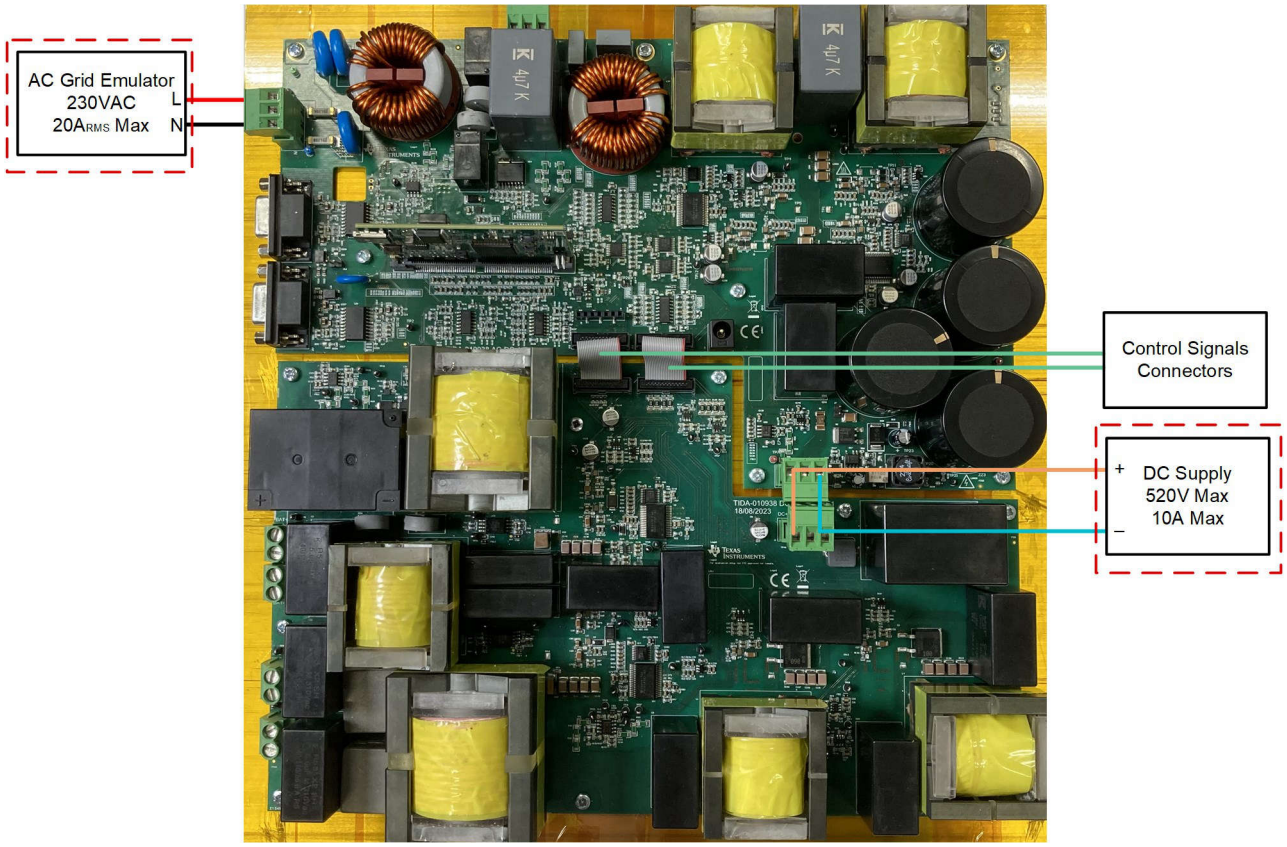


Figure 4-4. Connections for Testing DC/AC

4.4 Test Results

4.4.1 Boost Converter

The voltage of the switching node was measured as shown in Figure 4-5. From the picture, observe the sharp switching edges without overshoot and ringing. A rise-time of around 25ns can be observed.

C4 - Switching node voltage

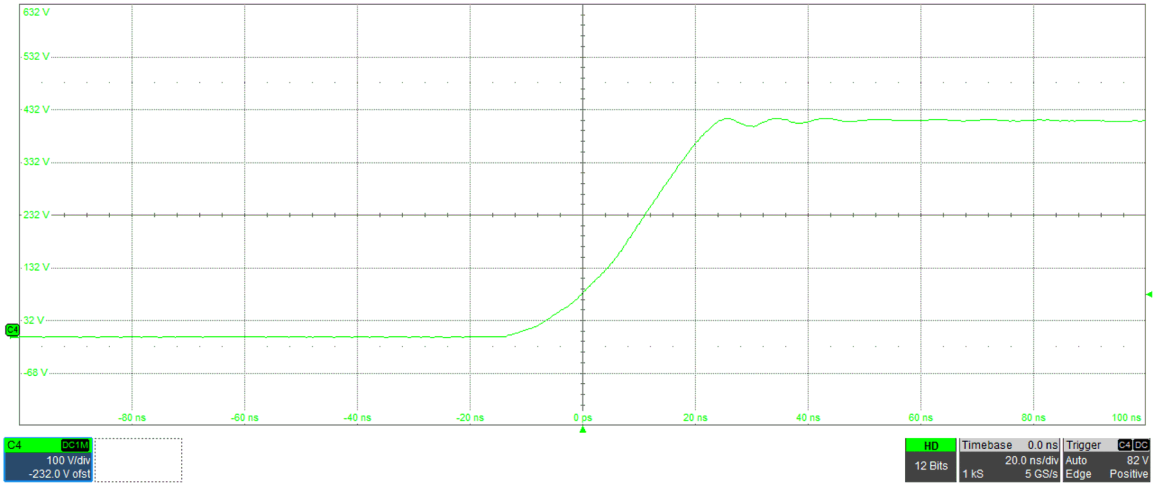


Figure 4-5. Boost Switching Node

Figure 4-6 and Table 4-1 show the efficiency of input DC/DC Boost converter at 400V DC-link output. The input string voltages considered are 50V, 150V, 200V, 250V and 350V. For 200V input, the peak efficiency achieved is 98.9%, where the boost converter demonstrates the worst-case ripple conditions for a duty cycle of 50%. The table shows that the converter achieves both peak and full load efficiency of 99.3% for 350V input.

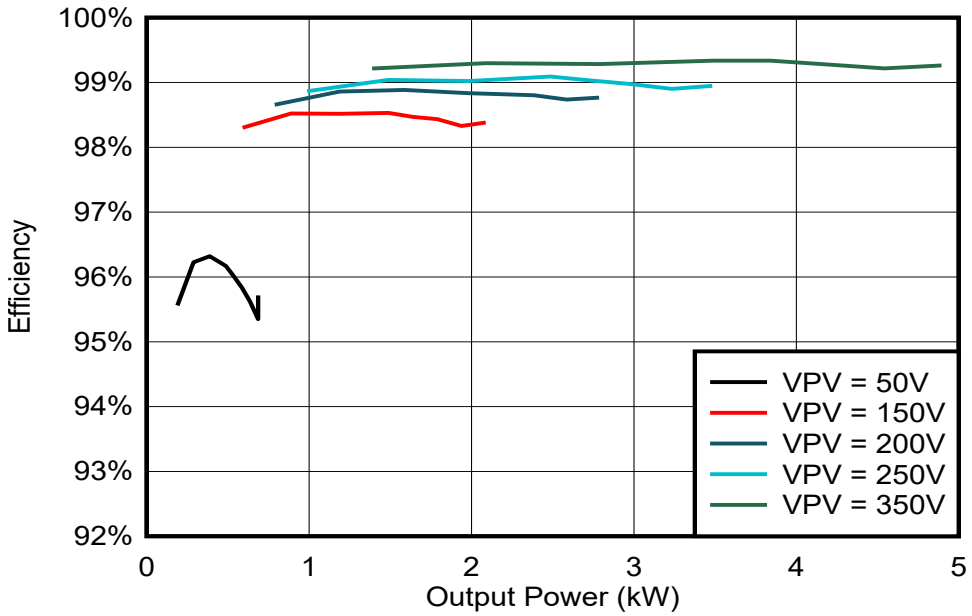


Figure 4-6. Boost Converter Efficiency

Table 4-1. Boost Converter Efficiency

OUTPUT POWER	EFFICIENCY AT V_{PV}=50V	OUTPUT POWER	EFFICIENCY AT V_{PV}=150V	OUTPUT POWER	EFFICIENCY AT V_{IN}=200V	OUTPUT POWER	EFFICIENCY AT V_{IN}=250V	OUTPUT POWER	EFFICIENCY AT V_{IN}=350V
0.2kW	95.6%	0.6kW	98.3%	0.8kW	98.7%	1.0kW	98.9%	1.4kW	99.2%
0.3kW	96.2%	0.9kW	98.5%	1.2kW	98.9%	1.5kW	99.0%	2.1kW	99.3%
0.4kW	96.3%	1.2kW	99.5%	1.6kW	98.9%	2.0kW	99.0%	2.8kW	99.3%
0.5kW	96.2%	1.5kW	98.5%	2.0kW	98.8%	2.5kW	99.1%	3.5kW	99.3%
0.5kW	96.0%	1.6kW	98.5%	2.2kW	98.8%	2.7kW	99.0%	3.8kW	99.3%
0.6kW	95.8%	1.8kW	98.4%	2.4kW	98.8%	3.0kW	99.0%	4.2kW	99.3%

Table 4-1. Boost Converter Efficiency (continued)

OUTPUT POWER	EFFICIENCY AT V_{PV}=50V	OUTPUT POWER	EFFICIENCY AT V_{PV}=150V	OUTPUT POWER	EFFICIENCY AT V_{IN}=200V	OUTPUT POWER	EFFICIENCY AT V_{IN}=250V	OUTPUT POWER	EFFICIENCY AT V_{IN}=350V
0.6kW	95.6%	1.9kW	98.3%	2.6kW	98.7%	3.2kW	98.9%	4.5kW	99.2%
0.7kW	95.4%	2.1kW	98.4%	2.8kW	98.8%	3.5kW	99.0%	4.9kW	99.3%
0.7kW	95.7%								

The GaN junction temperature for the worst-case duty-cycle for the GaN operation (for example, from conversion of PV string input of 50V to the DC-link voltage of 400V can be seen in Figure 4-7. The temperature does not go higher than 68°C.

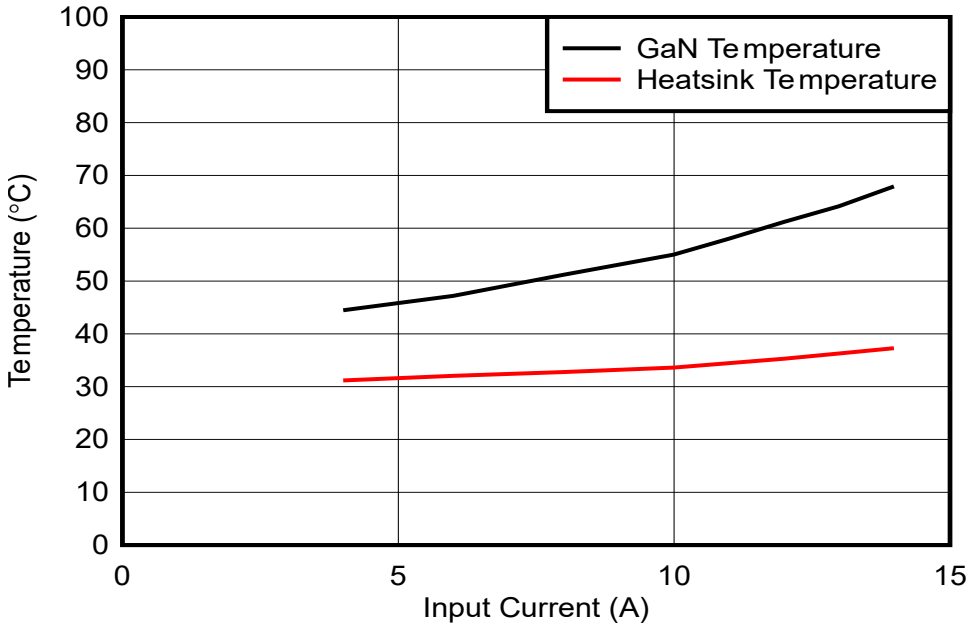


Figure 4-7. GaN v/s Heatsink Temperature for Boost Converter

4.4.2 Bidirectional DC/DC Converter

4.4.2.1 Buck Mode

Figure 4-8 and Table 4-2 show the efficiency of the bidirectional DC/DC converter functioning in buck mode at 400V DC-link output. The input battery voltages considered are 80V, 160V, 240V, and 320V and the table shows that the converter achieves peak efficiencies of 97.9%, 99.0%, 99.2%, and 99.4% respectively.

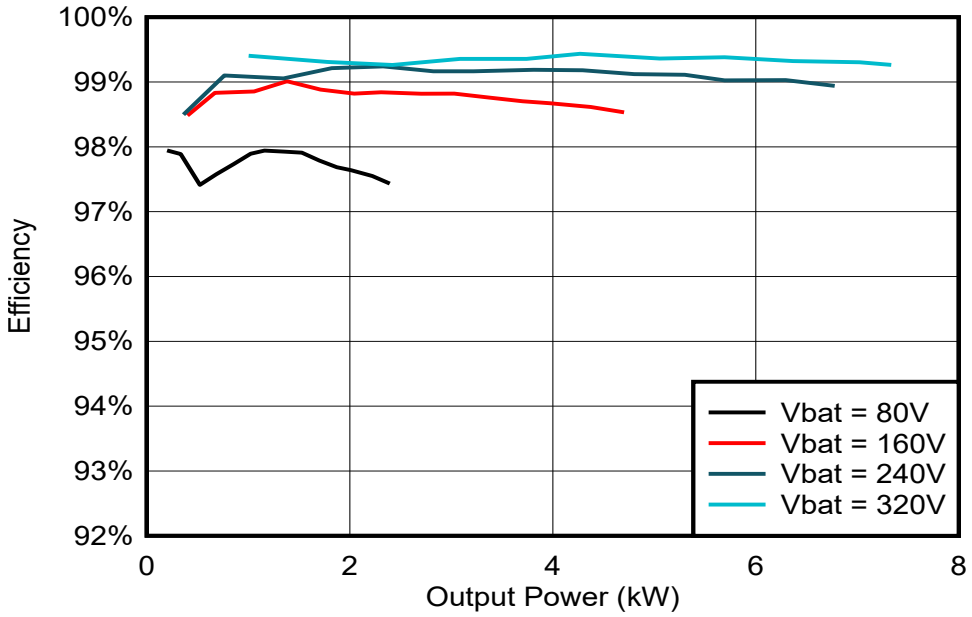


Figure 4-8. Bidirectional DC/DC Efficiency in Buck Mode

Table 4-2. Bidirectional DC/DC Efficiency in Buck Mode

OUTPUT POWER	EFFICIENCY AT VBat=80V	OUTPUT POWER	EFFICIENCY AT VBat=160V	OUTPUT POWER	EFFICIENCY AT VBat=240V	OUTPUT POWER	EFFICIENCY AT VBat=320V
0.2kW	97.9%	0.4kW	98.5%	0.4kW	98.5%	1.0kW	99.4%
0.3kW	97.9%	0.7kW	98.8%	0.8kW	99.1%	1.8kW	99.3%
0.5kW	97.4%	1.1kW	98.9%	1.3kW	99.1%	2.4kW	99.3%
0.7kW	97.6%	1.4kW	99.0%	1.8kW	99.2%	3.1kW	99.4%
0.9kW	97.7%	1.7kW	98.9%	2.3kW	99.2%	3.7kW	99.4%
1.0kW	97.9%	2.0kW	98.8%	2.8kW	99.2%	4.3kW	99.4%
1.2kW	97.9%	2.3kW	98.8%	3.2kW	99.2%	5.1kW	99.4%
1.4kW	97.9%	2.7kW	98.8%	3.8kW	99.2%	5.7kW	99.4%
1.5kW	97.9%	3.0kW	98.8%	4.3kW	99.2%	6.4kW	99.3%
1.7kW	97.8%	3.4kW	98.8%	4.8kW	99.1%	7.0kW	99.3%
1.9kW	97.7%	3.7kW	98.7%	5.3kW	99.1%	7.3kW	99.3%
2.0kW	97.6%	4.0kW	98.7%	5.7kW	99.0%		
2.2kW	97.6%	4.4kW	98.6%	6.3kW	99.0%		
2.4kW	97.4%	4.7kW	98.5%	6.8kW	98.9%		

4.4.2.2 Boost Mode

Figure 4-9 and Table 4-3 show the efficiency of the bidirectional DC/DC converter functioning in boost mode at 400V DC-link output. The input battery voltages considered are 80V, 160V, 240V, and 320V and the table shows that the converter achieves peak efficiencies of 97.7%, 98.8%, 99.3% and 99.5% respectively.

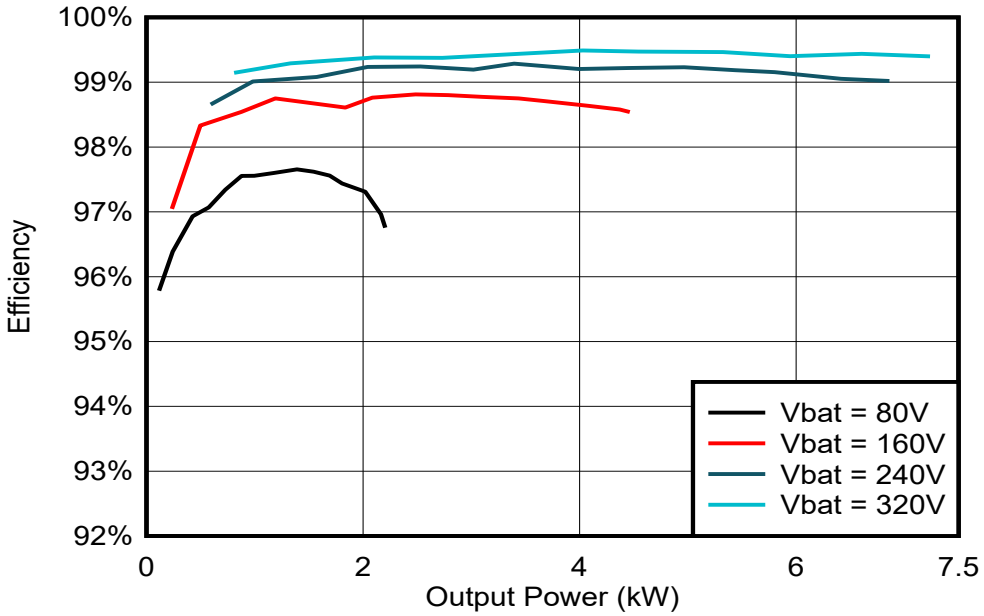


Figure 4-9. Bidirectional DC/DC Efficiency in Boost Mode

Table 4-3. Bidirectional DC/DC Efficiency in Boost Mode

OUTPUT POWER	EFFICIENCY AT VBat=80 V	OUTPUT POWER	EFFICIENCY AT VBat=160 V	OUTPUT POWER	EFFICIENCY AT VBat=240 V	OUTPUT POWER	EFFICIENCY AT VBat=320 V
0.1kW	95.6%	0.2kW	97.0%	0.6kW	98.7%	0.8kW	99.1%
0.2kW	96.4%	0.5kW	98.3%	1.0kW	99.0%	1.3kW	99.3%
0.4kW	97.0%	0.9kW	98.5%	1.6kW	99.1%	2.1kW	99.4%
0.6kW	97.1%	1.2kW	98.8%	2.0kW	99.2%	2.7kW	99.4%
0.7kW	97.3%	1.8kW	98.6%	2.5kW	99.2%	3.4kW	99.4%
0.9kW	97.6%	2.1kW	98.8%	3.0kW	99.2%	4.0kW	99.5%
1.0kW	97.6%	2.5kW	98.8%	3.4kW	99.3%	4.5kW	99.5%
1.2kW	97.6%	2.8kW	98.8%	4.0kW	99.2%	5.3kW	99.5%
1.4kW	97.7%	3.1kW	98.8%	4.4kW	99.2%	5.9kW	99.4%
1.5kW	97.6%	3.4kW	98.8%	5.0kW	99.2%	6.6kW	99.4%
1.7kW	97.6%	3.7kW	98.7%	5.4kW	99.2%	7.2kW	99.4%
1.8kW	97.4%	4.1kW	98.6%	5.8kW	99.2%		
2.0kW	97.3%	4.4kW	98.6%	6.4kW	99.1%		
2.2kW	97.0%	4.5kW	98.5%	6.9kW	99.0%		
2.4kW	96.8%						

The results for the boost mode are similar to that of buck mode, however the losses at low power are higher, hence the efficiency is lower. This is due to the boosting operation, and higher losses of the GaN FET when boosting up to a higher voltage.

Figure 4-10 shows the voltage of the switching node of one of the legs during operation of the converter in Boost mode. From the picture, observe the sharp switching edges without overshoot and ringing. A rise-time of around 30ns can be observed.

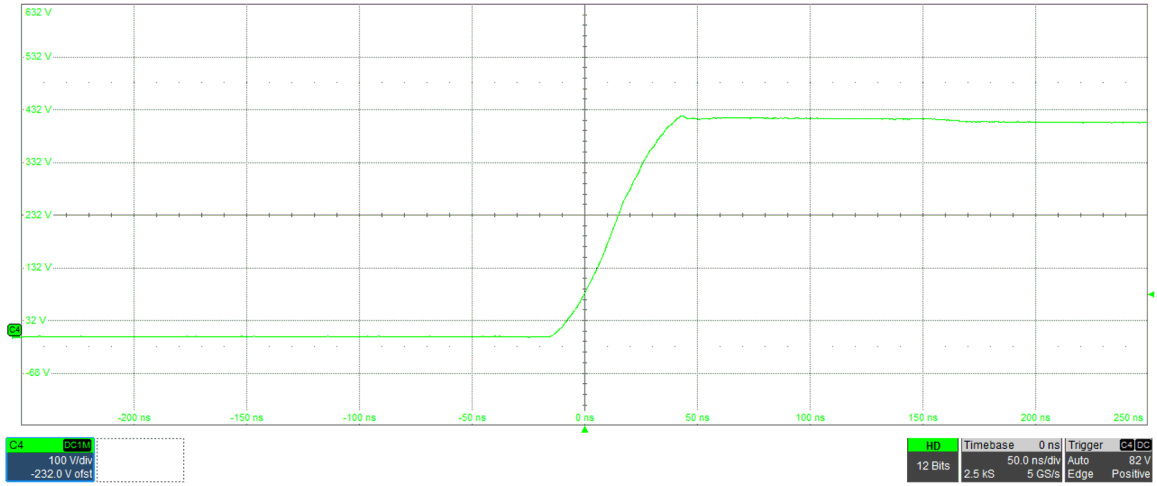


Figure 4-10. Bidirectional DC/DC Switching Node in Boost Mode

The GaN junction temperature for the can be seen in Figure 4-11. The other GaNs have a similar temperature profile. This operation corresponds to a conversion of VBat of 240V to a DC-link voltage of 400V. The temperature does not go higher than 70°C.

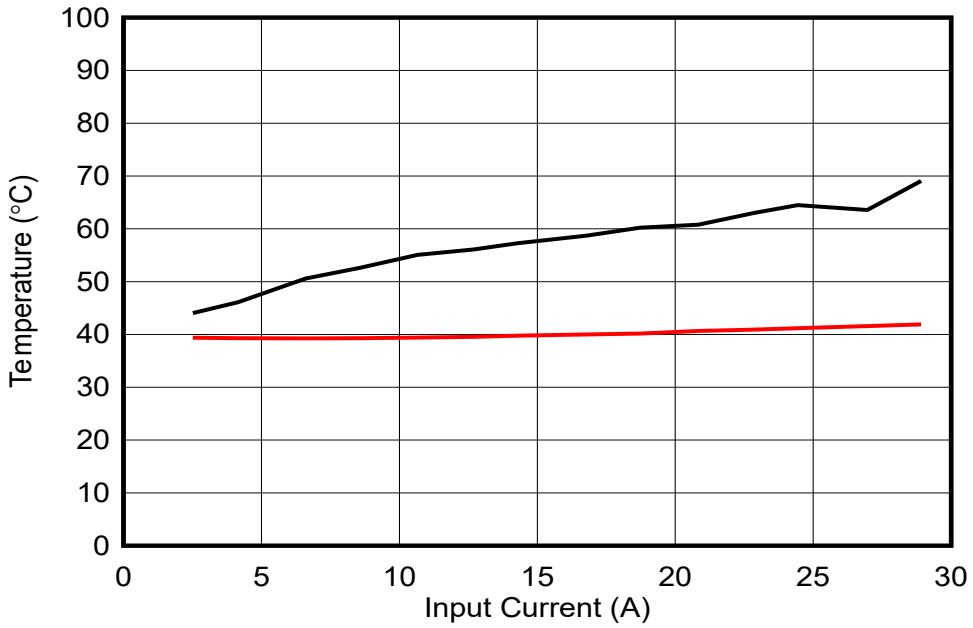


Figure 4-11. GaN v/s Heatsink Temperature for Bidirectional DC/DC Converter

4.4.3 DC/AC Converter

In Figure 4-12, around 4.4kW output power was sourced from 400V DC-link to 230VAC. The line voltage is present in yellow and the line current in pink color respectively. Notice that no important current ripple is injected into the resistor. The figure also shows the DC-link power ripple present at 100Hz in green color.

C1 - Output voltage, C2 - Output current, C4 - DC bus voltage

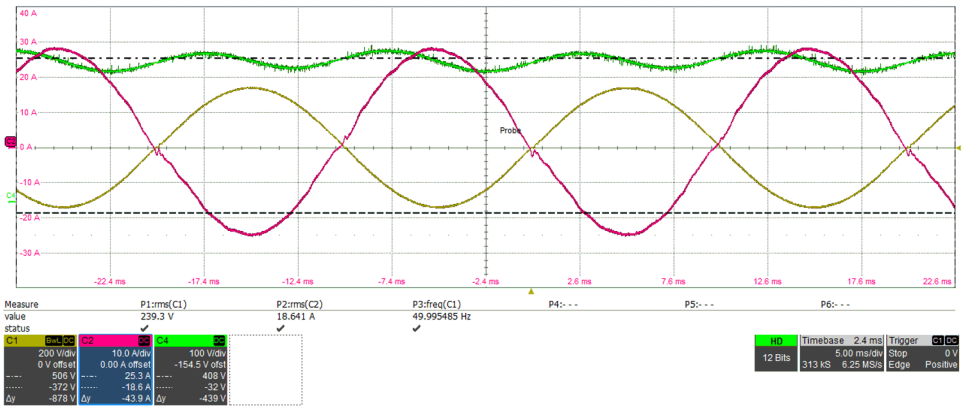


Figure 4-12. DC/AC Line Voltage, Line Current and DC Bus Voltage

Figure 4-13 and Table 4-4 show the overall efficiency converting from DC Bus to 230V_{AC} output. The results are discussed for comparison of all three modulation schemes, H-Bridge in unipolar, H-Bridge in bipolar and HERIC modes.

The table shows that the reference design in H-Brideg Unipolar mode achieves a η_{peak} = 98.4% at approximately 2.4kW and 400V input, $\eta_{full\text{-}load}$ of 98.2% and η_{CEC} = *98.3%* .

The table shows that the reference design in H-Brideg Bipolar mode achieves a η_{peak} = 98.1% at approximately 2.8kW and 400V input, $\eta_{full\text{-}load}$ of 97.9% and η_{CEC} = *97.8%*.

The table shows that the reference design in HERIC mode achieves η_{peak} = 98.5% at approximately 2.4kW and 400V input, $\eta_{full\text{-}load}$ of 98.2% and η_{CEC} = *98.4%.*

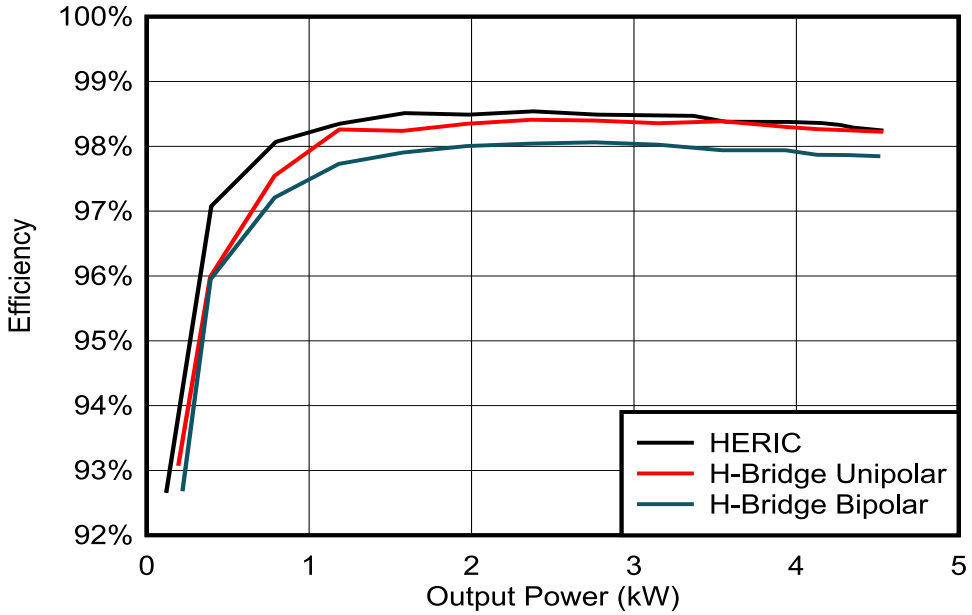


Figure 4-13. DC/AC Efficiency Comparison

Table 4-4. DC/AC Efficiency

OUTPUT POWER	EFFICIENCY FOR H-BRIDGE UNIPOLAR	OUTPUT POWER	EFFICIENCY FOR H-BRIDGE BIPOLAR	OUTPUT POWER	EFFICIENCY FOR HERIC
0.2kW	93.1%	0.2kW	92.7%	0.1kW	92.7%
0.4kW	96.0%	0.4kW	95.9%	0.4kW	97.1%
0.8kW	97.5%	0.8kW	97.2%	0.8kW	98.1%
1.2kW	98.3%	1.2kW	97.7%	1.2kW	98.3%

Table 4-4. DC/AC Efficiency (continued)

OUTPUT POWER	EFFICIENCY FOR H-BRIDGE UNIPOLAR	OUTPUT POWER	EFFICIENCY FOR H-BRIDGE BIPOLAR	OUTPUT POWER	EFFICIENCY FOR HERIC
1.6kW	98.2%	1.6kW	97.9%	1.2kW	98.4%
2.0kW	98.3%	2.0kW	98.0%	1.6kW	98.5%
2.4kW	98.4%	2.4kW	98.0%	2.0kW	98.5%
2.8kW	98.4%	2.8kW	98.1%	2.4kW	98.5%
3.2kW	98.4%	3.2kW	98.0%	2.8kW	98.5%
3.5kW	98.4%	3.5kW	97.9%	3.2kW	98.5%
3.9kW	98.3%	3.9kW	97.9%	3.4kW	98.5%
4.1kW	98.3%	4.1kW	97.9%	3.6kW	98.4%
4.3kW	98.2%	4.3kW	97.9%	4.0kW	98.4%
4.5kW	98.2%	4.5kW	97.8%	4.2kW	98.4%
				4.3kW	98.3%
				4.5kW	98.2%

Furthermore, the voltage of the switching node of the H-Bridge with Unipolar modulation scheme was measured as shown in Figure 4-14. Observe from the image that no important overvoltage was detected even when the switching was at 60kV / µs. A rise-time of around 6ns can be observed.

C1 - Line voltage, C2 - Line current, C3 - DC bus voltage, C4 - Switching node voltage

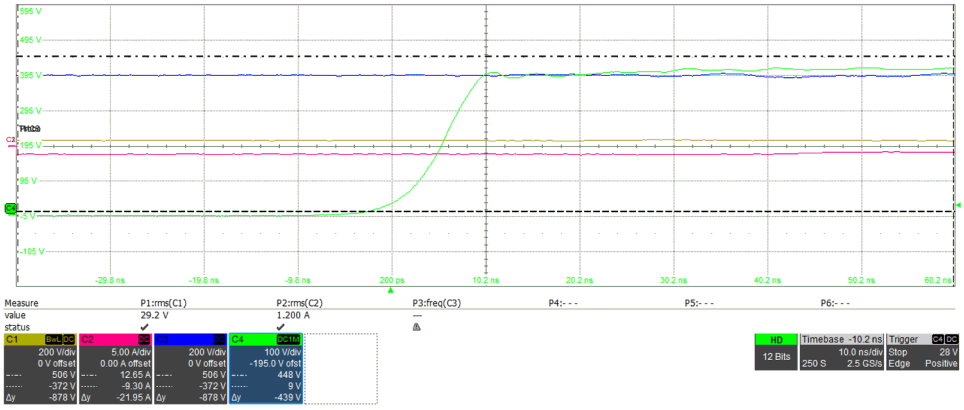


Figure 4-14. DC/AC Switching Node in H-Bridge Unipolar

The voltage of the switching node of the H-Bridge with Bipolar modulation scheme was measured as shown in Figure 4-15. Observe from the image that no important overvoltage was detected even when the switching was at 60 kV / µs. A rise-time of around 6.5ns can be observed.

C1 - Line voltage, C2 - Line current, C3 - DC bus voltage, C4 - Switching node voltage

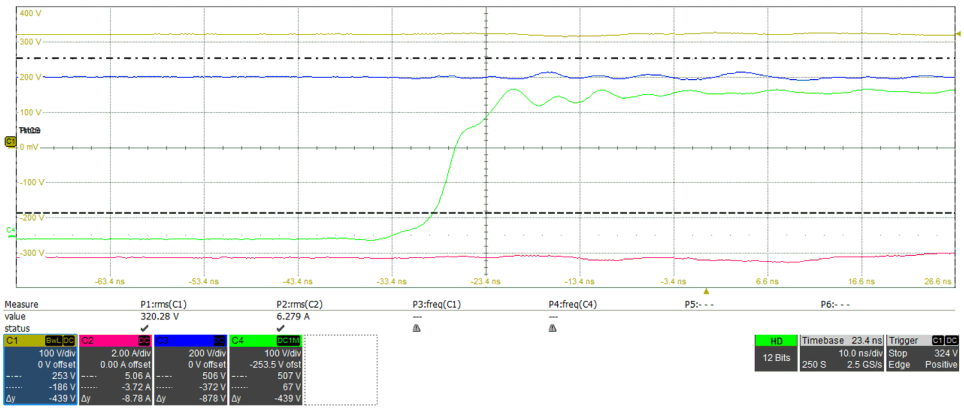


Figure 4-15. DC/AC Switching Node in H-Bridge Bipolar

The voltage of the switching node of the HERIC molulation scheme was measured as shown in Figure 4-16. From topology point of view, in HERIC mode, due to additional zero-voltage states in positive and negative half-cycles, the voltage across the FETs is also halved. So, we can see the switching node voltage rises from 200V to 400V. The other switching node in this scenario can be from 0V to 200V.

C1 - Line voltage, C2 - Line current, C3 - Switching node voltage, C4 -DC bus voltage

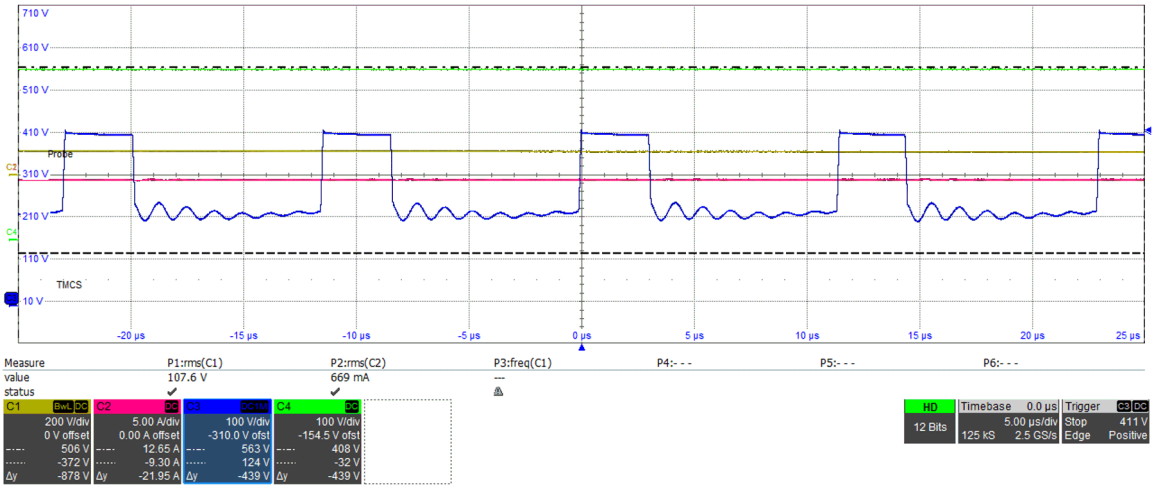


Figure 4-16. DC/AC Switching Node in HERIC

The Total Harmonic Distortion (THD) profiles for the corresponding modulation schemes can also be seen in Figure 4-17.

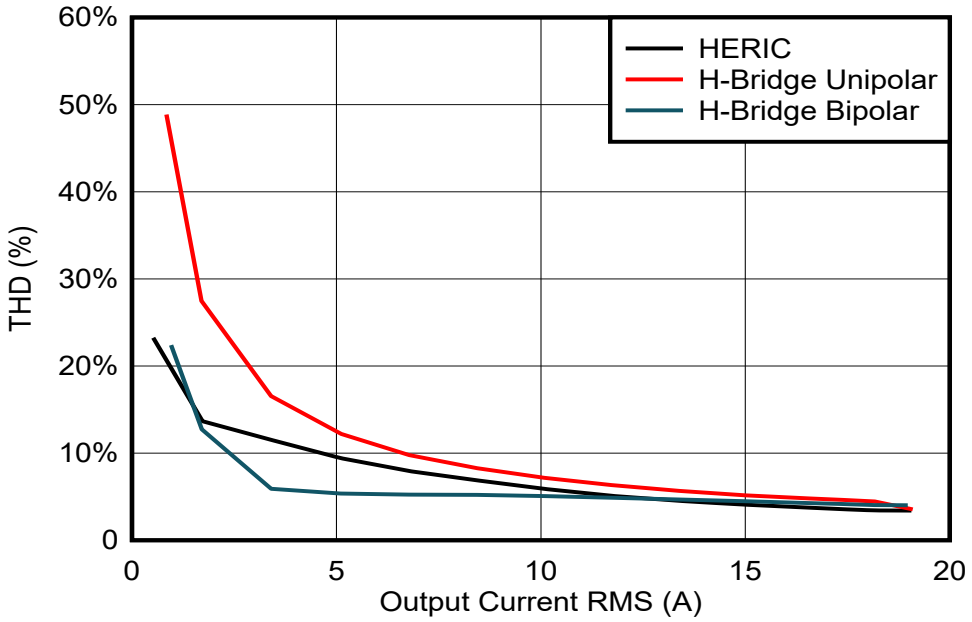


Figure 4-17. Total Harmonic Distortion for DC/AC

Furthermore, the junction temperature of the GaN FETs for the unipolar topology can be seen in Figure 4-18. The other H-Bridge GaNs have a similar temperature profile. This operation corresponds to a conversion of a DC-link voltage of 400V to 230V grid. It can be seen that the temperature does not go higher than 54°C.

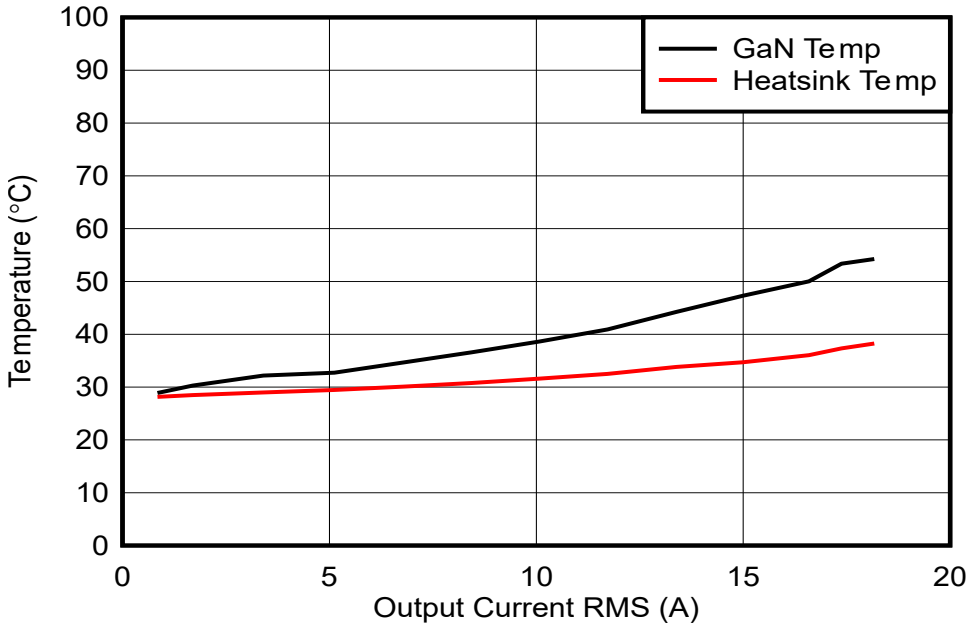


Figure 4-18. GaN v/s Heatsink Temperature for H-Bridge Unipolar

The junction temperature of the GaN FETs for the bipolar topology can be seen in Figure 4-19. The other H-Bridge GaNs have a similar temperature profile. This operation corresponds to a conversion of a DC-link voltage of 400V to 230V grid. It can be seen that the temperature does not go higher than 70°C.

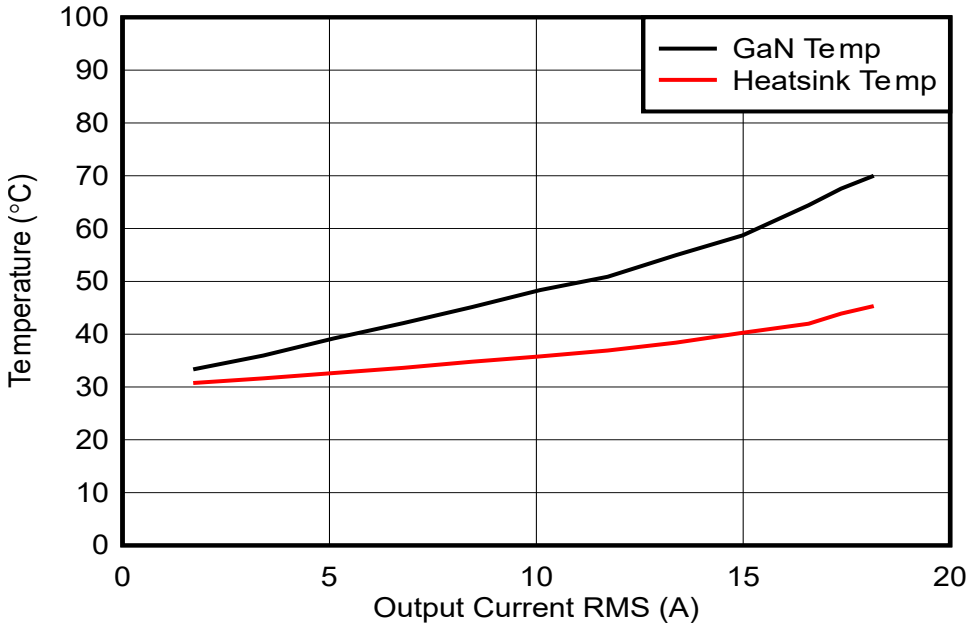


Figure 4-19. GaN v/s Heatsink Temperature for H-Bridge Bipolar

The junction temperature of the GaN FETs for the HERIC topology can be seen in Figure 4-20. The other H-Bridge GaNs have a similar temperature profile. This operation corresponds to a conversion of a DC-link voltage of 400V to 230V grid. The temperature does not go higher than 54°C.

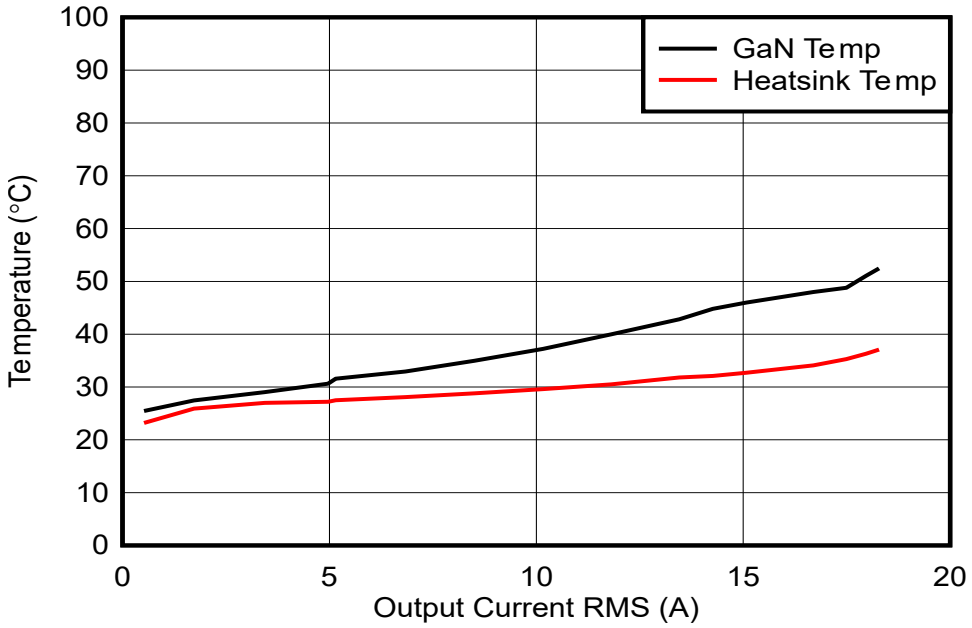


Figure 4-20. GaN v/s Heatsink Temperature for HERIC

In summary, both H-Bridge in unipolar modulation and HERIC are 3-level topologies which leads to lower switching losses across the FETs, compared to H-Bridge in bipolar modulation which is a 2-level topology. HERIC and H-Bridge in bipolar modulation have better common-mode rejection capabilities. Unipolar offers high common-mode voltage and for a transformer-less system such as the string inverter, this can lead to high leakage current. However, the unipolar is run at half the switching frequency and has doubled frequency at the output for a comparable EMI filter design. Hence, there are multiple points to consider when comparing the three topologies.

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010938.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010938.

5.2 Tools and Software

Tools

TMDSCNCD280039C	TMS320F280039C evaluation module C2000™ MCU controlCARD™

Software

Code Composer Studio™	Integrated development environment (IDE)

5.3 Documentation Support

1. Texas Instruments, *TMS320F280039C controlCARD Information Guide* user's guide

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7 Revision History

Changes from Revision * (April 2024) to Revision A (August 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed *7.2-kW* to *10-kW* in document title	1
• Updated Description topic to reflect different input voltage ranges on string input and battery port and updated power rating of BESS stage to 10kW nominal and AC/DC stage to 4.6kW	1
• Changed *7.2-kW* to *10-kW* in document title	1
• Changed power density to 2.5kW/L	1
• Updated board dimensions and added power density of the design	2
• Updated Key Specifications of each converter stage	3
• Added *PV Input with Boost Converter* topic	4
• Added *Bidirectional DC/DC Converter* topic	5
• Added *DC/AC Converter* topic	7
• Added *System Design Theory* topic	9
• Updated *System Overview* section to reflect latest board specifications	14
• Updated sections to reflect updated testing requirements	27
• Updated section to add test results for Bidirectional DC/DC converters in boost mode and DC/AC converter	31

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