Design Guide: TIDA-011011

Isolated Gate Driver Board With Isolated Bias Supply for 3.3kV SiC-FET Reference Design

Description

This reference design provides a template for implementing gate drive designs for field effect transistors (FETs) rated up to 3.3kV. By utilizing single-channel isolated pre-drivers with split outputs, multiple variants of power FETs can be driven while maintaining high current sink and source capability. The performance of the driving design is further enhanced by incorporating a DC/DC isolated bias supply with controlled output rail voltages, enabling lower $R_{DS(on)}$ operation.

Resources

TIDA-011011	Design Folder
UCC35131-Q1	Product Folder
UCC218915-Q1	Product Folder

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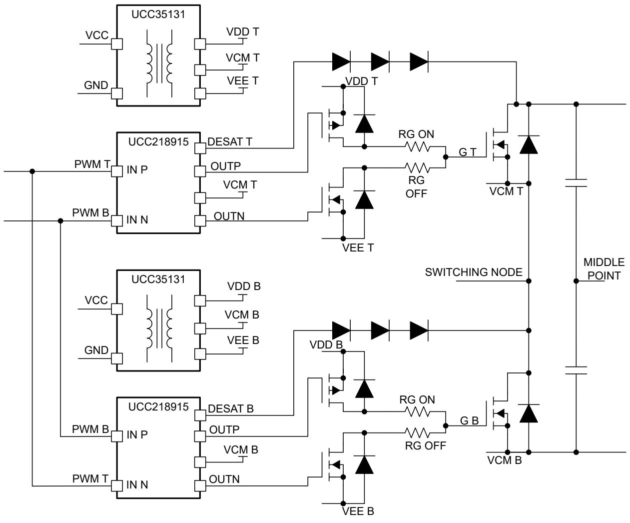
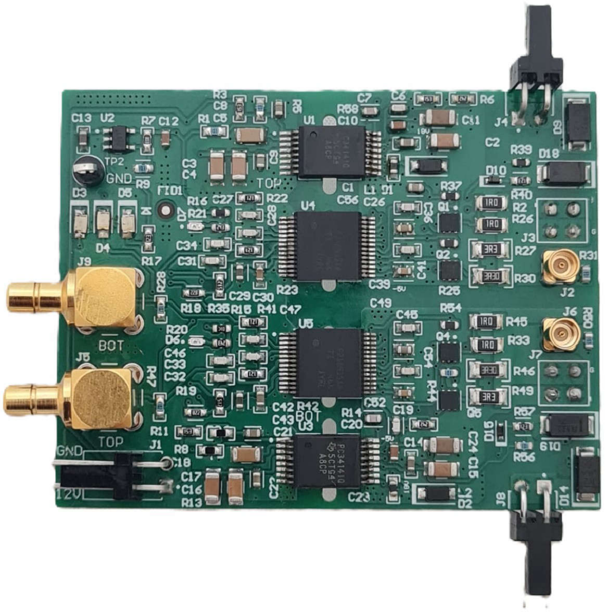
Features

- Gate driver design for FETs rated with voltage up to 3.3kV
- Pre-drivers with split output designs
- Controlled gate driver voltage rails

Applications

- Central inverter
- Power conversion system (PCS)
- Solid state transformer





1 System Description

Modern power conversion systems are experiencing a significant trend towards higher operating voltages, as exemplified in applications such as solid-state transformers used in data centers, energy storage systems (ESS), and solar applications. Concurrently, system currents are also increasing substantially, thus requiring high driving currents from the gate driver. As system voltages rise, power devices must be designed with correspondingly higher breakdown voltages. This evolution necessitates gate drivers and DC-DC isolated power supplies capable of withstanding these elevated isolation voltage requirements.

This reference design addresses these challenges by incorporating devices rated to withstand RMS operating voltages up to $1050V_{RMS}$. This capability enables the control of FETs rated up to 3.3kV when the MCU is referenced to the midpoint of the DC link, providing a robust design for high-voltage power conversion applications.

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the schematic representation of the circuit implemented inside the reference design board. This board is composed of two gate driver units (UCC218915), plus two isolated power supplies (UCC35131).

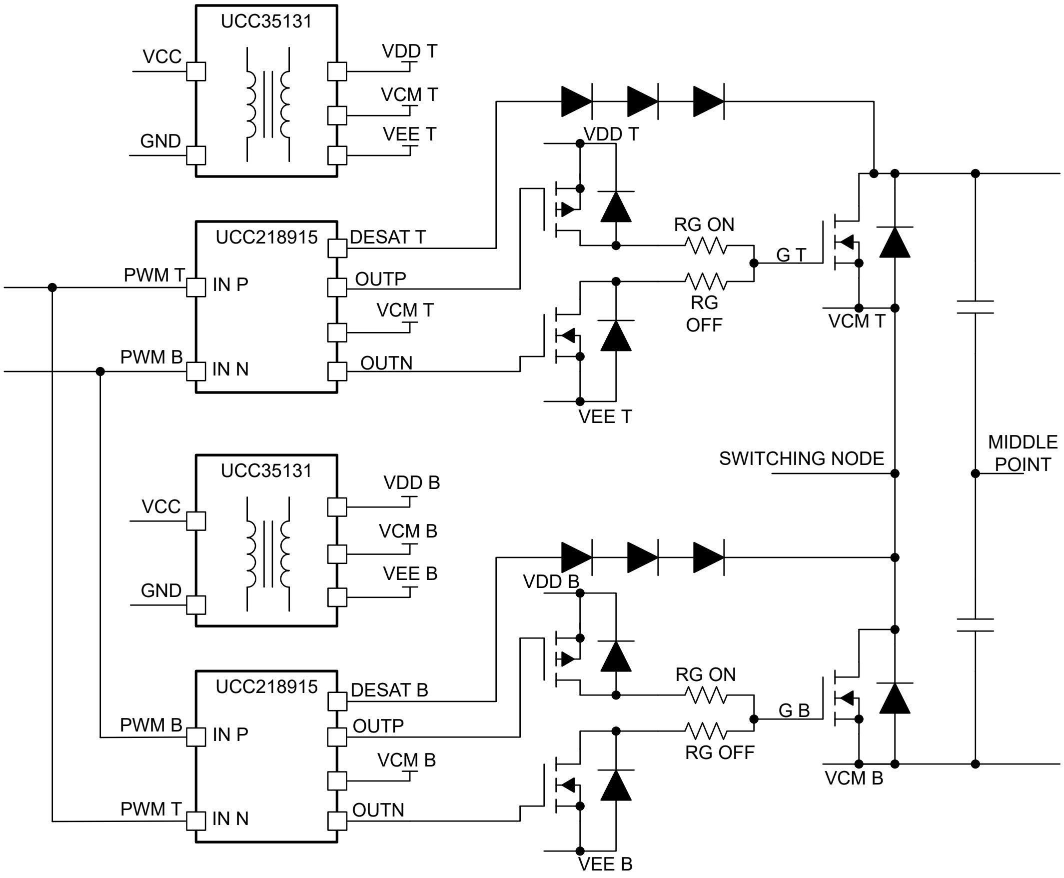


Figure 2-1. Block Diagram of the Reference Design

2.2 Design Considerations

This reference design features a gate driver board that controls two power silicon carbide FETs through two external PWM signals. The design is specifically intended for driving the FETs within two Silicon Carbide (SiC) power modules:

- G4H22MT33GB4 module contains FETs rated at 3.3kV with 2.2mΩ on-resistance,
- G4H11MT23BH4 module features FETs rated at 2.3kV with 1.1mΩ on-resistance.

2.3 Highlighted Products

2.3.1 UCC35131-Q1

The UCC35131-Q1 is an automotive-qualified high-isolation voltage DC/DC power module designed to provide power to IGBT, SiC, Si, and GaN isolated gate drivers and UIR sensors. The proprietary integrated transformer, flip-chip package, and advanced control architectures of the device achieve high power density and low noise. This device is capable of delivering 2.0W typical output power at 85°C ambient temperature. The highly accurate dual-output voltages, easily set by resistor dividers, enable low on-resistance, fast and reliable switching for SiC, IGBT, and GaN devices. The low-latency feedback control reduces the output capacitance for fast load transient and supports dynamic voltage programming. The wide input voltage and adjustable VIN UVLO supports both wide battery voltage of electric vehicles and regulated input rails. The device is operational from 5.5V to 20V VIN, and can withstand VIN overvoltage transient up to 28V. The integrated protection features, fault-report Power Good pin, and enable function increase system robustness and save external components. The SOIC package with 8.2mm creepage and clearance distance provides high-isolation capability.

2.3.2 UCC218915-Q1

The UCC218915-Q1 is a galvanically-isolated single channel pre-driver designed for SiC MOSFETs and IGBTs up to 1500V DC operating voltage with advanced protection features, best-in-class dynamic performance, and robustness. The UCC218915-Q1 has dual 2.8A outputs for directly driving an external buffer NMOS/PMOS pair. The input side is isolated from the output side with SiO_2 isolation technology, supporting up to $1.06kV_{RMS}$ working voltage, $10kV_{PK}$ surge immunity with longer than 40-years isolation barrier life, as well as providing low part-to-part skew, and > 200V/ns common mode noise immunity (CMTI). The UCC218915-Q1 includes state-of-the-art protection features, such as fast overcurrent and short-circuit detection, controlled soft shutdown after a fault, fault reporting, active Miller clamp, active short circuit input on the high-voltage side, and input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness.

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware Requirements

The device under test (DUT) in this design is set up and operated in several pieces:

- One TIDA-011011 gate driver board
- One Power Module together with the heat sink
- One Power Board which works as connection means between the power module and the gate driver card
- TMDSCNCD28P55X control card
- TMDSHSECDOCK
- USB isolator
- Power adapter with 12V output and 3A rating
- Laptop
- Oscilloscope, current and voltage probes

3.2 Test Setup

Figure 3-1 shows the connections for testing.

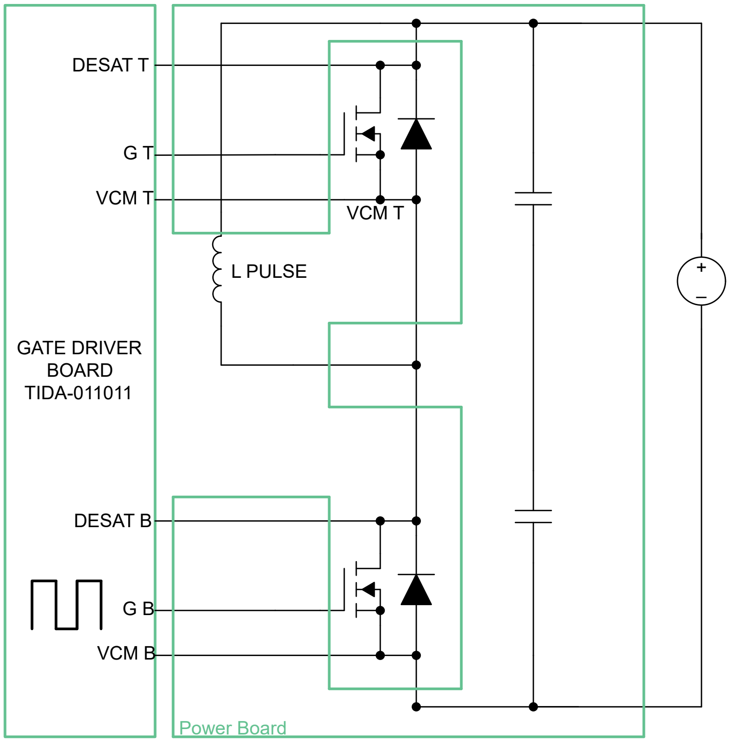


Figure 3-1. Connections for Testing the Reference Design Gate Driver Board

3.3 Test Results

Double pulse testing was performed using a power module (part number: G4H11MT23BH4). The module incorporates two power FETs, each rated at 2.3kV with 1.1mΩ on-resistance. The module operates with nominal gate voltages of +18V and –5V.

The double pulse test characterizes two critical switching transients: turn-on and turn-off behavior of the power FETs. Testing was conducted using 2.5Ω gate resistors for both turn-on and turn-off transitions, with the resulting waveforms presented in the following figures.

Figure 3-2, Figure 3-3, and Figure 3-4 demonstrate the turn-off transient characteristics under test conditions of 1.5kV DC link voltage and 400A drain current. Analysis of the voltage transients reveals a common-mode transient immunity (CMTI) measurement of approximately 40nV/ns.

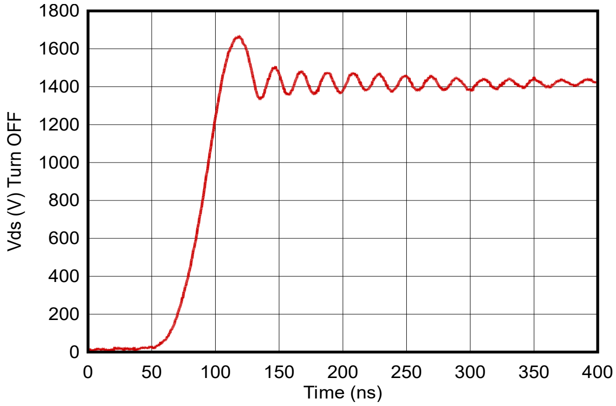


Figure 3-2. Turn OFF Drain Source Voltage Switching Waveform (2.5Ω)

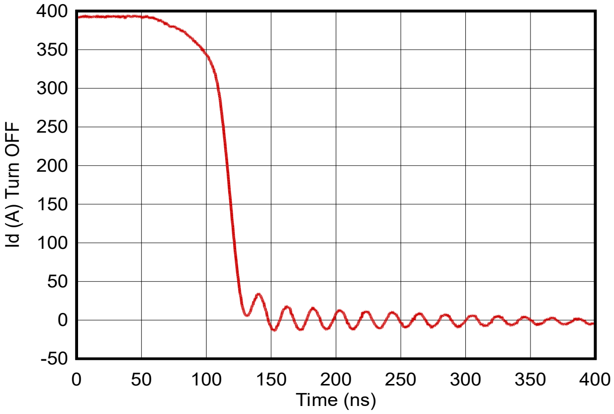


Figure 3-3. Turn OFF Drain Current Waveform (2.5Ω)

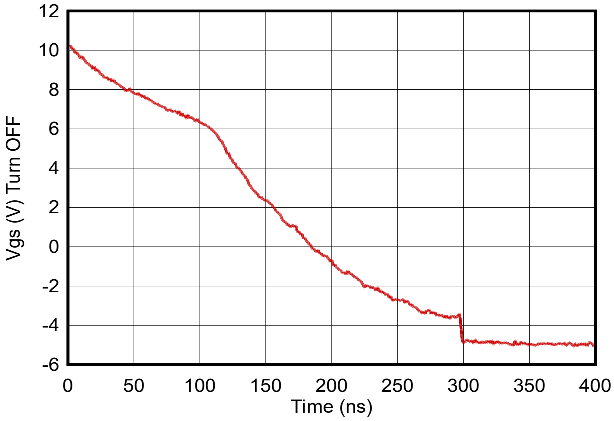


Figure 3-4. Turn OFF Gate Source Voltage Waveform (2.5Ω)

Figure 3-5, Figure 3-6, and Figure 3-7 present the turn-on transient waveforms measured under test conditions of 1.5kV DC link voltage and 320A switching node current. Analysis of the voltage transients indicates a common-mode transient immunity (CMTI) of approximately 50V/ns during the turn-on switching event.

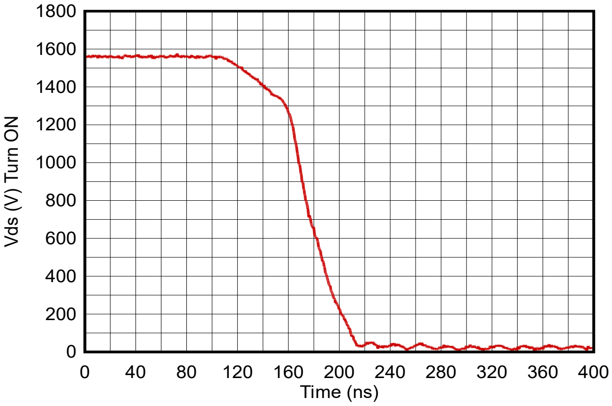


Figure 3-5. Turn On Drain Source Voltage Measurement Waveform (2.5Ω)

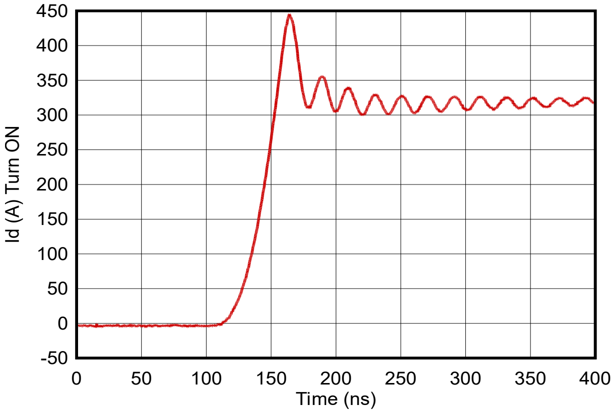


Figure 3-6. Turn On Drain Current Measurement Waveform (2.5Ω)

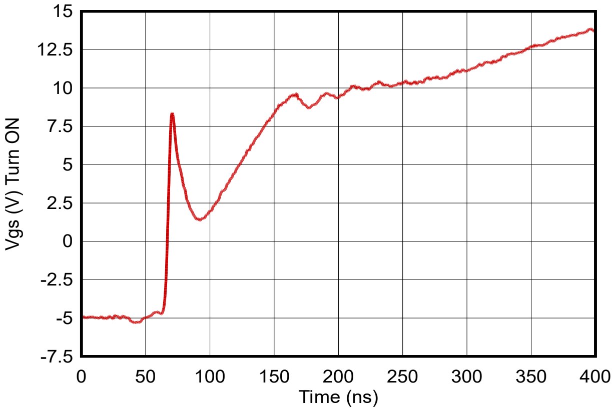


Figure 3-7. Turn On Gate to Source Voltage Measurement Waveform (2.5Ω)

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-011011.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-011011.

4.2 Tools

UCC35131-Q1-CALC	Design calculator tool to generate external BOM based on system requirement

4.3 Documentation Support

1. Texas Instruments, *UCC35131-Q1 Automotive 2.0W, 12V VIN, High-Density, > 5kV$_{RMS}$, Isolated DC/DC Module Datasheet*
2. Texas Instruments, *UCC218915-Q1 Single Channel Isolated Pre-Driver for SiC/IGBT with Active Protection for Automotive Applications Datasheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

RICCARDO RUFFO received the Ph.D. degree in Electric, Electronics and Communication Engineering from Politecnico di Torino, Turin, Italy in 2019. He is currently working at Texas Instruments Germany as System Engineer in the area of Solar Energy within the Energy Infrastructure Team. His main work includes EV charging, inductive wireless power transfer, photovoltaic, renewable energy, and energy storage applications.

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