Design Guide: TIPA-010000

Power Delivery Architecture for AMD® Ultrascale+™ MPSoC Proof of Concept

Description

This design guide proposes power tree concept reference designs surrounding an Advanced Micro Devices® (AMD) Ultrascale+™ Multi-Processor System-on-Chip (MPSoC) Field-Programmable Gate Array (FPGA). The power trees leverage newer TI modules and MagPack™ technology to minimize size on constrained boards while maintaining competitive efficiency, performance, and cost.

Resources

TIPA-010000	Design Folder
TPSM8F7420	Product Folder
TPSM843B22	Product Folder
TPSM82816	Product Folder
TPSM8287A15M	Product Folder

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Features

- Common input voltage (12V and 5V) power trees
- Compact power trees achieves down to 159mm^2 total size
- Leverages MagPack™ technology and TI's newest power modules
- Up to 90% efficiency

Applications

- Radar
- Electronic warfare
- Seeker front end

1 System Description

The AMD UltraScale+™ MPSoC FPGA family consists of multiple part numbers, each with different current consumptions, which changes the TI power tree or power design network (PDN) recommendation. This design guide provides voltage regulator module (VRM) recommendation look up tables (LUT) to help designers select an alternative TI device at a variety of current levels that enhances size and efficiency. The MPSoC FPGA family achieves high-performance, real-time data processing in a compact, low-power package that integrates either a Dual-core or Quad-Core Arm™ Cortex™-A53 into the chip. MPSoC FPGAs allow the designer to replace multiple discrete chips with a single-die approach to save on board footprint and power consumption.

Texas Instruments' wide portfolio of DC-DC switching regulators, sequencers, and DDR memory Power Management Integrated Circuits (PMIC) provide Aerospace and Defense (A&D) power designers a range of devices to leverage while meeting Size, Weight, Power, and cost (SWaP-c) constraints and making system-level trade-offs. A&D power supplies require size-constrained designs in small form factors, which provide high efficiency to avoid complex heat-sink design. TI's MagPack™ technology and newer modules incorporate the inductor within the package to reduce design time and to save space on the board, while increasing efficiency.

2 System Overview

The Ultrascale+ MPSoC PDNs in this design guide come from either a 12V or 5V intermediate power rail to the FPGA point of load (PoL). The TI PDNs are based upon the Ultrascale+ MPSoC FPGA XCZU9EG-2FFVB1156E using the minimum rail power consolidation. The design calculates the currents using the AMD power estimation calculator or PDM. The TI PDN utilizes the Power Design Manager (PDM) tool with the assumptions made listed in Section 2.1.

The XCZU9EG-2FFVB1156E is used on the Ultrascale+ MPSoC evaluation board (ZCU102). The PDN implemented on that evaluation board implements the full power management approach and is not consolidated to a minimum rail approach that is necessary to implement in some highly compact A&D end applications. The evaluation board serves as a baseline to the TI suggested PDNs and not a direct comparison between two minimum rail PDNs.

Although there are designs that can leverage PMICs, LDOs, and a multi-stage power tree, these are not in the scope of these proof-of-concept designs. The designs in this design guide showcase fixed-frequency TI modules that can synchronize to a system clock, DDR PMICs, and sequencers in a single-stage DC-DC power tree configuration. These designs serve as a starting point estimate for small form factor power tree designs that remain highly efficient.

2.1 Assumptions on FPGA Utilization

The PDM tool can export all of the information associated within the PDM GUI into a .pwr output file. The associated PDM output file is found in the Design Folder on TI.com (see the *Resources* section). The following assumptions are used to calculate the maximum current levels found in the PDNs:

- Clock: 320MHz
- Logic: 70% utilization (LUTs and registers)
  - LUTs evenly distributed as logic, shift registers, and distributed RAM
- Block RAM: 100% utilization (RAM18DP + RAM36SDP_ECC)
- Ultra RAM: 100% utilization (URAM288_ECC)
- DSP: 100% utilization with pre-add ON
- GTH: see the PDM output file
- I/O: assuming a maximum of 4A for I/O
- Hard IP blocks: see PDM output file
- PS: see the PDM output file
- Network on Chip (NoC), DDR Memory Controller (DDRMC): see the PDM output file

2.2 Block Diagrams

Figure 2-1 illustrates a 12V input PDN implementing industrial-rated, fixed-frequency TI modules, including options for sequencers, and powering LPDDR4 or DDR4 memory that is a common peripheral around the UltraScale+™ MPSoC family.

Up to seven VCCO rails can vary from 1V to 3.3V with different current levels. For this analysis, 4A was assumed for each VCCO. The VCCO provides the power for the output drivers of the MPSoC FPGA, and usage of each rail is driven by which peripherals the design implements to interface with these output drivers.

The TPSM8F7420 is a quad-output module that works well for the variable implementation of the VCCO rails. The quad output allows the designer to implement all seven VCCO rails with one extra channel to spare for another rail, such as the VMCTAVCC. If any of the other VCCO rails goes unused, the additional TPSM8F7420 outputs can be used without increasing the power design network size.

Note that the circled numbers in Figure 2-1 are the order in which the rails are sequenced according to the PDM tool. The 2nd rail to be sequenced is the VCCINT_VCU rail when using an EV device and is omitted from this example because the example uses an EG device.

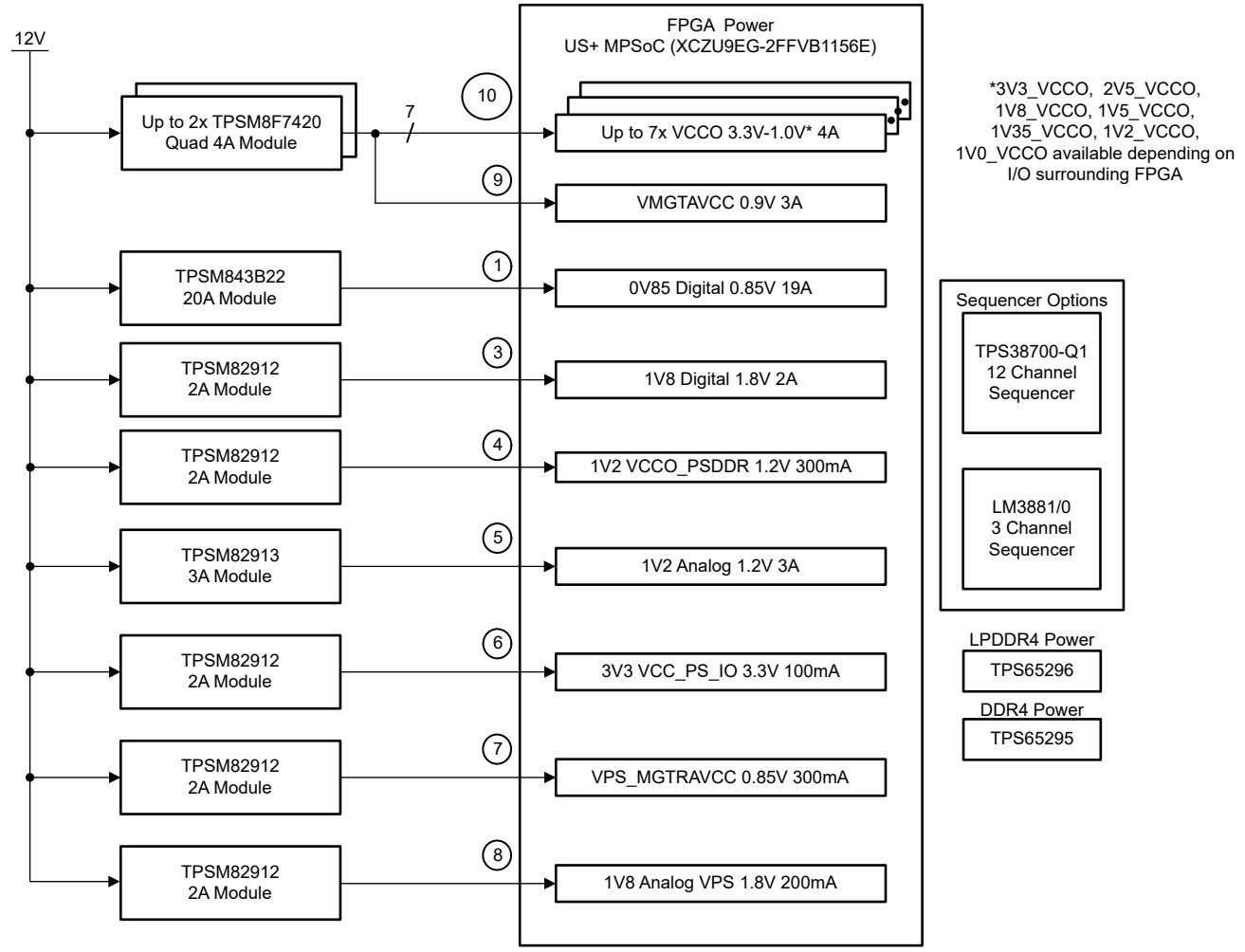

Figure 2-1. 12V Input Voltage to FPGA PoL PDN (TI Modules, Sequencing, and DDR Power)

Figure 2-2 illustrates a 5V input PDN using industrial-rated, fixed-frequency TI modules, including options for sequencers, and powering LPDDR4 or DDR4 memory that is a common peripheral around the UltraScale+™ MPSoC family.

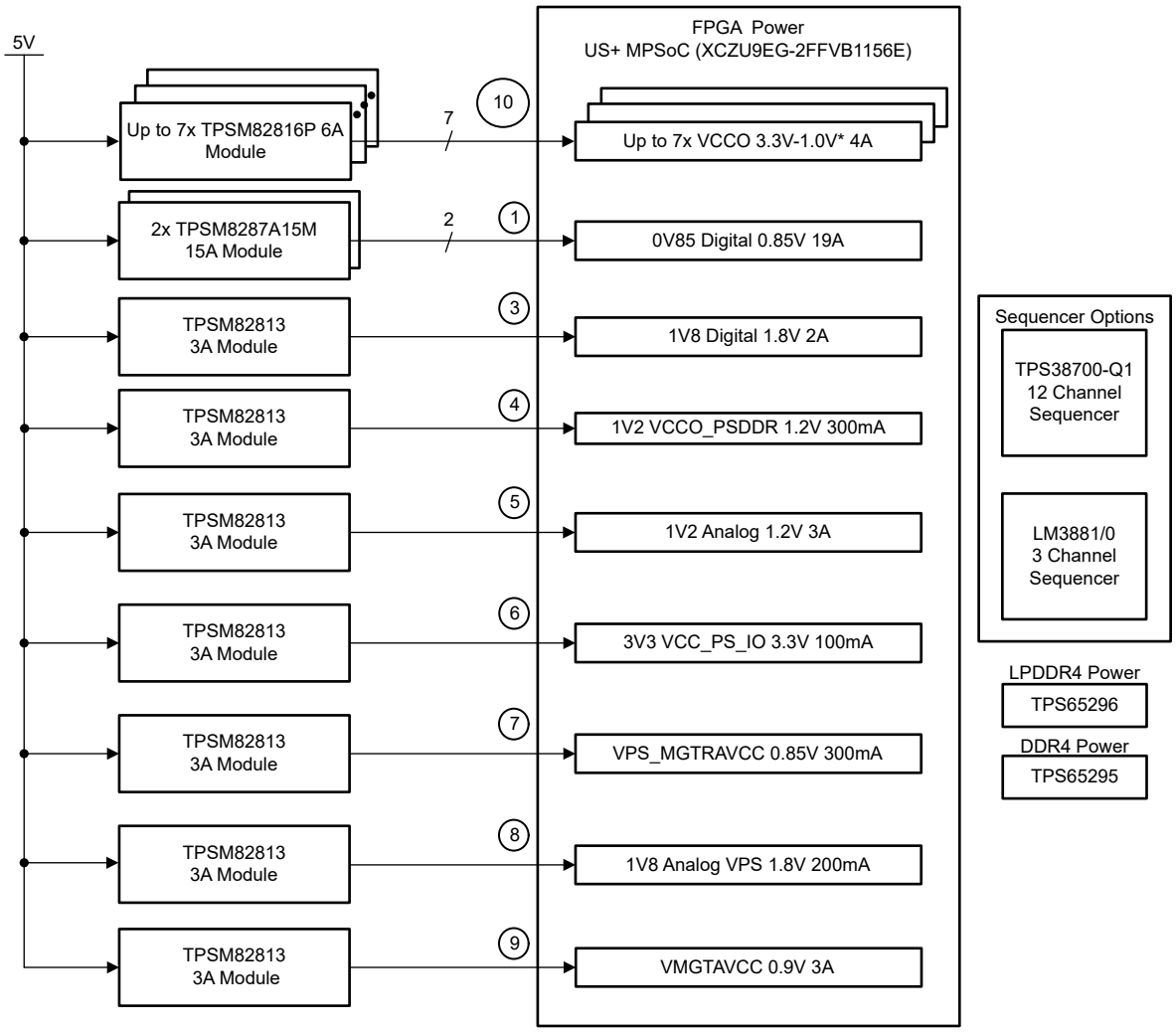

Figure 2-2. 5V Input Voltage to FPGA PoL PDN (TI Modules, Sequencing, and DDR Power)

2.3 Design Considerations

Designing for FPGA PDNs requires flexibility between choosing devices that can handle the expected currents for each power rail and balancing between efficiency, size, and cost. Control architectures are also of importance when selecting a VRM. TI's modules use either fixed-frequency or constant on-time (COT) control architectures that both come with tradeoffs. Fixed-frequency devices can sync the VRM switching frequency to an external clock. However, COT control devices, in general, have faster transient responses and smaller footprints compared to fixed-frequency devices (see the *Fixed-frequency DCS-Control: Fast transient response with clock synchronization* Analog Design Journal for more information).

The need for design flexibility comes from changes in current levels or an increased need for efficiency at the expense of regulator size. Current levels can change based upon power estimation tool modifications throughout the course of the component level design (that is, FPGA utilizations changing, FPGA device change, and so forth). Additionally, derating the VRM current to increase efficiency becomes necessary for the component to reduce power dissipation and temperature rise.

The following alternative VRM recommendation LUTs provide references to the devices enhanced for size and efficiency where cost is less of a priority for a current range of up to 300A. These LUTs can be utilized for alternative device selection if:

- Current levels are higher or lower than assumed in the PDNs in this design guide
- Current derating is applied to the design to increase efficiency
- PDN can leverage either COT or fixed-frequency control

Table 2-1 provides the TI part numbers for a range of currents (up to 300A) for both COT and fixed-frequency control regulator architectures, assuming a 12V input. The table showcases the newest TI modules. In absence of a module, an integrated-MOSFET converter or a controller and power stage option are provided. The table also highlights, in orange, TI devices capable of a –55°C to 125°C temperature range, rather than the standard industrial temperature range of –40°C to 125°C.

Table 2-1. Alternative TI VRMs Supporting 12V Input Voltage

CURRENT	CONSTANT ON TIME (COT) (FAST TRANSIENT RESPONSE, SMALL SIZE, RIPPLE ACCEPTABLE)	FIXED FREQUENCY (EXCELLENT RIPPLE PERFORMANCE FOR SENSITIVE RAILS)
200A–300A	TPS53689T + (8 ×) CSD965200	N/A
140A–200A	(4 ×) TPS546E25	N/A
100A–140A	(3 ×) TPS546E25, (4 ×) TPS546C25 (alt)	(2x) TPSM8D6C24 (up to 140A) / (4x) TPS546D24S (up to 160A) (alt)
50A–100A	(2 ×) TPS546E25, (3 ×) TPS546C25 (alt)	
35A–50A	TPS546E25, (2 ×) TPS546C25 (alt)	TPSM8D6B24, (1× to 2 ×) TPS546D24S (alt)
24A–35A	TPS546C25	TPSM8S6C24
18A–24A		TPSM8F7620
6A–20A	TPS548B23	TPSM843B22, TPSM843A26, TPSM843A22
4A–6A	TPS54J061	TPSM82916, TPSM8F7420 (alt), TPSM8F7620 (alt)
3A–4A		TPSM8F7420, TPS543421 (alt)
2A–3A	TPSM82903	TPSM82913
1A–2A	TPSM82902	TPSM82912, TPS62912 (alt)
0A–1A	TPSM82901	
–55°C to 125°C Temperature Rating Available		

Table 2-2 provides the TI part numbers for a range of currents (up to 300A) for both COT and fixed-frequency control regulator architectures assuming a 5V input. The table showcases the newest TI modules. In absence of a module, an integrated-MOSFET converter or controller and power stage option are provided. The table also highlights, in orange, TI device ratings capable of a –55°C to 125°C temperature range rather than the standard industrial temperature range of –40°C to 125°C. The automotive grade devices in the table are in bold text.

Table 2-2. Alternative TI VRMs Supporting 5V Input Voltage

CURRENT	COT	FIXED FREQUENCY
200A–300A	TPS53689T + (8 ×) CSD965200	(6 ×)**TPS62893-Q1**
50A–200A	(4 ×) TPS546E25	(2 × to 6 ×) TPSM8287B30
15A–50A	TPS546E25, (2 ×), TPS546C25 (alt)	(1 × to 4 ×)TPSM8287A15M
6A–15A	TPS548B23	TPSM8287A15M
4A–6A	TPSM82866A, TPSM82866C	TPSM82816
3A–4A	TPSM82866A	TPSM82810
2A–3A	TPSM828303	TPSM82813
1A–2A	TPSM828302	TPSM82813, **TPS62442(-Q1) (Dual out)**
0A–1A	TPSM828301	TPSM82813, **TPS62442(-Q1)**
–55°C to 125°C Temperature Rating Available	Available in MagPack™ Packages: TPSM82830x family, TPSM8281x family, TPSM8286xx family, and TPSM8287Bxx family	
Automotive (-Q1) Rating Available		

3 System Design Theory

This section shows how the TI PDNs compare to the evaluation board from AMD for the power rails using the XCZU9EG-2FFVB1156E FPGA as a baseline.

Table 3-1 shows the size of the existing power rail regulator device size including inductors and estimated rail efficiencies when looking at efficiency curves in the corresponding device datasheets.

The total power rail component size accounts for the power regulators, external FETs, and inductors upon inspection of the schematic of the evaluation board. The total power rail size does not account for the decoupling capacitor size. The rail efficiency estimates assume a switching frequency of 600kHz, which is a common switching frequency among the datasheets evaluated and the total estimated power loss is 22W. The supply names in the table correspond to the supply name of the evaluation board and the supply names of the PDM tool, respectively.

Table 3-1. ZCU102 AMD® Evaluation Board for UltraScale+™ MPSoC

SUPPLY NAME	VOLTAGE (V)	CURRENT (A)	TOTAL POWER RAIL COMPONENT SIZE (MM²)	RAIL EFFICIENCY ESTIMATE
VCCINT (0V85_VCCINT)	0.85	40	325	84%
VCCBRAM (0V85_VCC_RAM_IO)	0.85	6	63	80%
VCCAUX (1V8 (Digital))	1.8	3	54	89%
VCC1V2 (1V2_VCCO (Digital))	1.2	2	91	85%
VCC3V3 (3V3_VCCO (Digital))	3.3	5	84	92%
VADJ_FMC (1V8_VCCO (Digital))	1.8	10	65	92%
MGTAVCC (0V9 (Analog))	0.9	6	143	88%
MGTAVTT (1V2 (Analog))	1.2	6	143	90%
MGTVCCAUX (1V8 (Analog))	1.8	1	22	55%
VCCPSINTFP (0V85_PSFP (Digital))	0.85	10	84	89%
VCCPSINTLP (0V85_PSLP (Digital))	0.85	2	59	83%
VCCPSAUX (1V8_LPD (Digital))	1.81	0.5	22	55%
VCCPSPLL (1V2_PSPLL (Analog))	1.2	0.2	22	36%
MGTRAVCC (0V85_PS_GTR)	0.85	0.4	22	26%
MGTRAVTT (1V8_PS_GTR)	1.81	0.1	22	55%
DDR4_DIMM_VDDQ (1V2_VCCO_PSDDR)	1.2	6	84	83%
VCCOPS (1V8_VCCO_PS_IO)	1.8	4	84	89%
VCCOPS3 (1V8_VCCO_PS_IO)	1.81	0.3	22	55%
VCCPSDDRPLL (1V8_PSDDR_PLL)	1.81	0.1	22	55%
		Totals	**1,434mm²**	**85%**

Table 3-2 and Table 3-3 show the TI PDNs for 12V and 5V input, respectively. The same names from the AMD power estimation tool are used to identify each FPGA power rail in the minimum rail configuration. The total power rail component size does not account for the decoupling capacitor size. The current levels are calculated using the *AMD Power Design Manager*. Although, the 1V35_VCCO rail can be utilized with the UltraScale+™ MPSoC, this rail is not included in the analysis in the table since the rail is primarily used for I/O banks interfacing with low-power DDR3L memory and has a small impact on overall efficiency and size of the power tree.

Table 3-2. 12V Input Voltage to FPGA PoL PDN (Device Size and Rail Efficiency Estimates)

PDM SUPPLY NAME	VOLTAGE (V)	CURRENT (A)	TI PART NUMBER	DEVICE SIZE (MM²)	RAIL EFFICIENCY ESTIMATE
3V3_VCCO	3.3	4	2 × TPSM8F7420 (6 of 8 output)	168	93%
2V5_VCCO	2.5	4			90%
1V8_VCCO	1.8	4			88%
1V5_VCCO	1.5	4			86%
1V2_VCCO	1.2	4			84%
1V0_VCCO	1	4			82%
0V85 Digital	0.85	19	TPSM843B22	48.75	80%
1V8 Digital	1.8	2	TPSM82912	24.75	86%
1V2 VCCO_PSDDR	1.2	0.3	TPSM82912	24.75	78%
1V2 Analog	1.2	3	TPSM8F7420 (7 of 8 output)	N/A	85%
3V3 VCC_PS_IO	3.3	0.1	TPSM82912	24.75	69%
VPS_MGTRAVCC	0.85	0.3	TPSM82912	24.75	71%
1V8 Analog VPS	1.8	0.2	TPSM82912	24.75	75%
VMGTAVCC	0.9	3	TPSM8F7420 (8 of 8 output)	N/A	81%
			Totals	**292mm²**	**85.6 %**

For the 12V input PDN, the total estimated power loss is 12W. The efficiencies were estimated using the datasheet efficiency curves at a 1MHz switching frequency. The six outputs of the TPSM8F7240 quad module can handle the VCCO rails with the additional two outputs free to cover the 1V2 analog and the VMGTAVCC power rails with slightly higher efficiency and smaller size footprint than if two TPSM82913 3A modules (24.75mm² each) are used.

Table 3-3. 5V Input Voltage to FPGA PoL PDN (Device Size and Rail Efficiency Estimates)

PDM SUPPLY NAME	VOLTAGE (V)	CURRENT (A)	TI PART NUMBER	DEVICE SIZE (MM²)	RAIL EFFICIENCY ESTIMATE
3V3_VCCO	3.3	4	6 × TPSM82816	45	95%
2V5_VCCO	2.5	4			94%
1V8_VCCO	1.8	4			92%
1V5_VCCO	1.5	4			90%
1V2_VCCO	1.2	4			89%
1V0_VCCO	1	4			87%
0V85 Digital	0.85	19	2 × TPSM8287A15M	61.2	87%
1V8 Digital	1.8	2	TPSM82813	7.5	90%
1V2 VCCO_PSDDR	1.2	0.3	TPSM82813	7.5	83%
1V2 Analog	1.2	3	TPSM82813	7.5	84%
3V3 VCC_PS_IO	3.3	0.1	TPSM82813	7.5	78%
VPS_MGTRAVCC	0.85	0.3	TPSM82813	7.5	78%
1V8 Analog VPS	1.8	0.2	TPSM82813	7.5	80%
VMGTAVCC	0.9	3	TPSM82813	7.5	79%
			Totals	**159mm²**	**89.7%**

For the 5V input PDN, the total estimated power loss is 8.4W. The efficiencies are estimated using the datasheet efficiency curves at a 1.8MHz switching frequency, except for the 0V85 digital rail where a 1.5MHz switching frequency is utilized. The 0V85 digital power rail has two TPSM8287A15M stacked in parallel and two more can be stacked to slightly increase the rails efficiency to 90%. TPSM82813 and TPSM82816 are MagPack power modules that reduce the volume of the package by about 49% and about 22% compared to the alternative power module package option.

Table 3-4 shows a summary of the PDNs presented in this proof of concept design.

Table 3-4. Summary of FPGA PoL PDNs

PDN	SIZE ESTIMATE	EFFICIENCY ESTIMATE	POWER LOSS ESTIMATE
UltraScale+™ MPSoC Eval Board	1,434mm²	85%	22W
12V Input TI PDN*	292mm²	85.6 %	12W
5V Input TI PDN*	159mm²	89.7%	8.4W
*Both the 12V and 5V TI PDNs use simplified power architectures that deliver less total output power than the Eval Board.			

4 Design and Documentation Support

4.1 Documentation Support

1. Texas Instruments, *MagPack technology: Four benefits of new power modules that can help you pack more power in less space* Technical Article
2. Texas Instruments, *Fixed-frequency DCS-Control: Fast transient response with clock synchronization* Analog Design Journal
3. Texas Instruments, *Power for your embedded systems*
4. AMD, *AMD Power Design Manager*

4.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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