Design Guide: TIDA-010988

Eight-Channel V and I Combined Analog Input Module with Single Supply Reference Design

Description

The TIDA-010988 is an eight-channel analog input module with 2-terminal inputs for industrial automation applications. Each channel supports software-selectable voltage range of 0V to 10V and ±10V, as well as current range of 4mA to 20mA, ±20mA. The design implements a high-density isolated analog input module powered from either a single 24V field supply or 5V USB. By using the ADS125H18 chip-select forwarding feature, the design implements a shared SPI architecture that reduces the required digital isolation channel count. The system is designed to achieve over temperature system absolute accuracy error better than 0.1% for voltage input and 0.2% for current input.

Resources

TIDA-010988	Design Folder
ADS125H18	Product Folder
MSPM0G5117	Product Folder
TXE8116	Product Folder
ISO6441	Product Folder
LM5180	Product Folder
UCC33420	Product Folder
TPS7A2050	Product Folder
TLV709A33	Product Folder

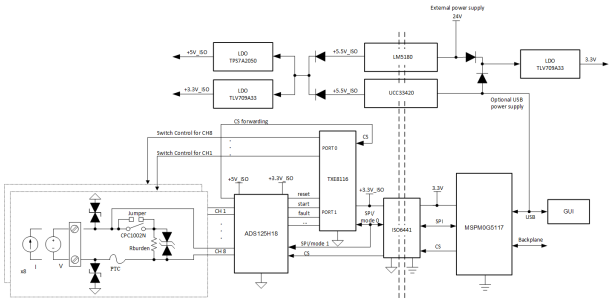
Features

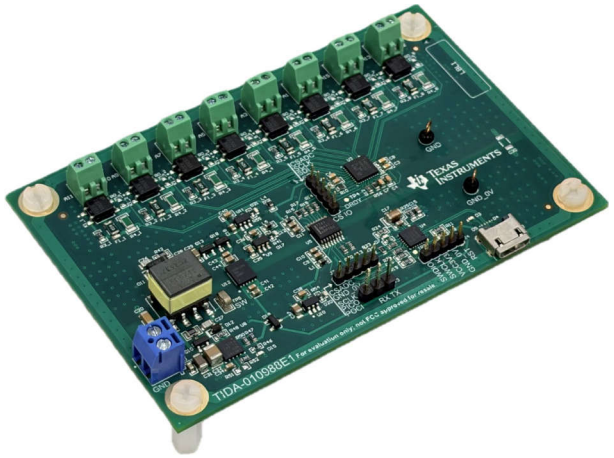
- Eight identical 2-terminal analog input channels
- Per-channel support for voltage (0V to 10V, ±10V) and current (4mA to 20mA, ±20mA) input
- Photo-MOS based voltage and current switching with open-wire detection on each channel
- Integrated PTC, TVS, and Zener diodes input protection for robust industrial interfaces
- Single 24V supply or 5V USB supply for evaluation
- System absolute accuracy error:
  - Over temperature (–40°C to 125°C), Voltage: <0.1%, Current: <0.2%
  - Room temperature (25°C), Voltage: <0.05%, Current: <0.15%

Applications

- Analog input modules
- Mixed module (AI,AO,DI,DO)

Ask our TI E2E™ support experts





1 System Description

This reference design implements an 8-channel isolated analog input module with 2-terminal inputs and per-channel voltage and the ability to configure the current. A single 24V field supply or 5V USB powers the module. The system is built around the ADS125H18 precision delta-sigma ADC, the MSPM0G5117 MCU, the LM5180 isolated power supply, the ISO6441 digital isolator, and the TXE8116 I/O expander. The design is designed for compact industrial analog input modules that require a balance among channel density, isolation, power, and PCB area.

Each channel front end combines PTCs, TVS diodes, and clamp devices to improve robustness against surge and sustained overvoltage, while the TXE8116 provides per-channel mode selection between voltage and current. Supported input types include 0V to 10V and ±10V voltage inputs, and 4mA to 20mA and ±20mA current inputs. Signals within these supported ranges are directly measurable once the channel input mode is selected without additional range switching.

The reference design is intended to support system level absolute accuracy error better than 0.1% for voltage input and better than 0.2% for current input over the –40°C to 125°C temperature range, including the impact of the protection network. Under room temperature conditions, the design achieves better than 0.05% accuracy error for voltage input and better than 0.15% accuracy error for current input.

The design uses a single digital isolator together with the ADS125H18 chip-select forwarding function to reduce the isolated digital interface requirement. The ADC forwards chip-select signals to the isolated-side I/O expander used for input mode control. This arrangement allows the MCU to manage ADC conversions, per-channel mode control, and diagnostics through a single isolated SPI plus a small number of additional control lines. This approach reduces the number of isolated channels, external components, and MCU SPI resources, helping improve channel density and minimize overall module size while maintaining full isolation and functionality.

The USB interface provides an auxiliary power option and a direct connection to a host PC GUI for operating mode configuration and real-time data visualization during evaluation. In addition, a backplane interface allows the module to be integrated into PLC and DCS systems or evaluated as a standalone analog input card.

1.1 Key System Specifications

Parameter	Specification	Details
Number of analog input channels	8	
Power supply options	24V field supply or 5V USB	Section 3.1
Channel configuration	Per-channel software-selectable voltage or current input mode	Section 3.2.2
Supported voltage input ranges	0V to 10V, ±10V	
Supported current input ranges	4mA to 20mA, ±20mA	
Open-wire detection	Available on each channel	
ADC resolution	24-bit	
System absolute accuracy error (25°C)	Voltage: <0.05%	Section 4.2.3.3
	Current: <0.15%	
System absolute accuracy error (-40°C to 125°C)	Voltage: <0.1%	
	Current: <0.2%	
Input impedance	Voltage mode: Approximately 2.2MΩ	
	Current mode: Approximately 249Ω	
Target applications	PLC/DCS analog input modules and industrial analog data acquisition systems	

2 System Overview

2.1 Block Diagram

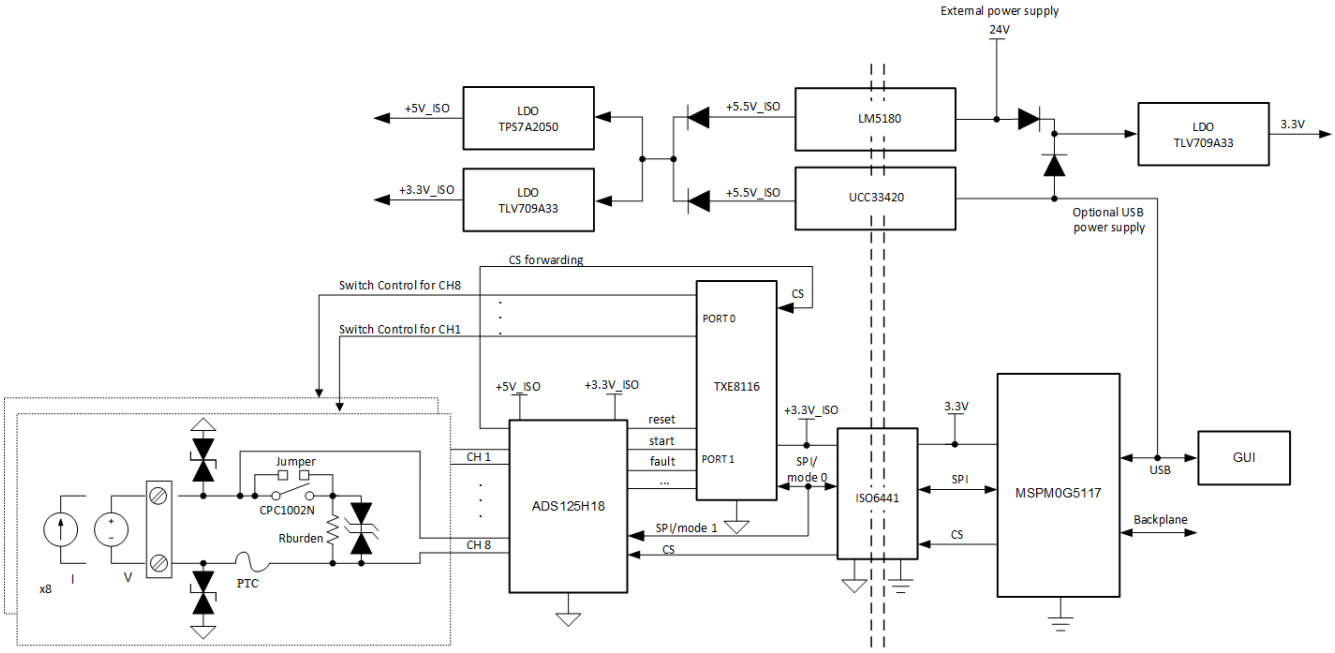


Figure 2-1. System Block Diagram of TIDA-010988

2.2 Design Considerations

Industrial analog input modules often require a common hardware platform that supports both voltage and current signals while maintaining channel density, isolation, and low cost. This design addresses that need with eight identical 2-terminal input channels. Each channel uses the same pair of field terminals for either voltage or current measurement, reducing connector count and simplifying field wiring compared with input structures that require separate terminals or dedicated channel variants.

The signal chain is built around the ADS125H18 ADC, which multiplexes the eight field inputs on the isolated side. Input protection is included to improve robustness against surge, fault, and miswiring conditions commonly found in industrial environments. Transient clamps and a PTC help protect the input stage, while the switchable shunt path allows current measurement to be enabled only when required. The switching approach prevents unnecessary loading when the channel is configured for voltage input.

To reduce isolator channel count, the design uses the ADS125H18 chip-select forwarding function so that the SPI bus can be shared with the isolated-side I/O expander used for channel switch control. The shared SPI architecture simplifies the isolated digital interface while maintaining per-channel configurability.

The power path supports both 24V and 5V. External power is used for the isolated field side during normal operation, while optional USB power can be used for evaluation and GUI-based testing. Separate rails are generated for the isolated analog and digital circuitry to support the ADC and switch-control functions.

2.3 Highlighted Products

2.3.1 ADS125H18

The ADS125H18 is a high-performance, 24-bit multiplexed delta-sigma (ΔΣ) ADC for precision multi-channel data acquisition in industrial systems. The device integrates an input multiplexer, a precision voltage reference, diagnostic features, and resistor-divider inputs that support up to 20V common-mode signals, which reduces external component count in high-channel-density analog input modules.

The ADS125H18 supports a CS (chip-select) forwarding feature, in which an ADC GPIO can be used to control the CS pin of a secondary device. The CS forwarding feature allows the ADC to assist in managing SPI

transactions with external companion devices. As a result, the number of signals that must cross the isolation barrier is reduced, avoiding additional dedicated isolator channels for separate chip-select signals.

In this design, the ADS125H18 serves as the main data converter for the 8-channel analog input front end. The integrated multiplexer, flexible conversion modes, high common-mode input capability through the resistor-divider inputs, and diagnostic capability make the ADS125H18 an excellent choice for PLC and DCS analog input modules that require accurate measurement, efficient channel scanning, and compact implementation over the –40°C to 125°C temperature range.

2.3.2 MSPM0G5117

The MSPM0G5117 is a 32-bit Arm Cortex-M0+ microcontroller designed for embedded control and mixed-signal industrial applications. The MSPM0G5117 integrates on-chip memory, analog peripherals, timers, communication interfaces, and a USB 2.0 full-speed interface, providing a compact control device for measurement and system-management functions.

In this design, the MSPM0G5117 manages ADC communication, channel configuration, diagnostics, and host-interface functions. The high level of integration and low-power operation make the device a good fit for compact analog input modules that require both real-time control and flexible system connectivity.

The TI MSPM0 MCU platform offers a range of package options and on-chip memory sizes to support different system requirements.

2.3.3 TXE8116

The TXE8116 is a 16-bit SPI I/O expander that provides additional general-purpose digital I/O in systems with limited MCU pin availability. The device supports a wide operating-voltage range and integrates features such as programmable pull resistors, interrupt capability, and configurable output modes.

In this design, the TXE8116 is used to control per-channel front-end switching for voltage and current mode selection, along with other discrete control functions. By offloading these signals from the MCU, the device helps reduce controller pin-count requirements and simplifies PCB routing in the isolated analog input module.

2.3.4 ISO6441

The ISO6441 is a reinforced, quad-channel digital isolator that provides galvanic isolation for three forward and one reverse unidirectional channels. The device uses a silicon-dioxide (SiO_2) insulation barrier to achieve high isolation ratings and high common-mode transient immunity, improving robustness in noisy industrial environments.

In this design, the ISO6441 provides galvanic isolation for the digital communication path between the controller and the isolated analog input domain. Combined with the shared SPI architecture, the ISO6441 helps reduce isolated channel count and external components while maintaining robust isolated communication.

2.3.5 LM5180

The LM5180 is a primary-side regulated flyback converter with an integrated high-voltage power switch, designed to generate isolated or non-isolated power rails from a wide input-voltage range. Primary-side regulation eliminates the need for an optocoupler or secondary-side feedback circuitry, enabling a compact and reliable isolated power design.

In this design, the LM5180 is used to generate isolated power rails for the analog front end and related circuitry. The wide input-voltage capability supports industrial modules powered from a 24V field supply.

2.3.6 UCC33420

The UCC33420 is an isolated DC/DC converter module that integrates a transformer driver, power switches, and rectification. This device is designed to deliver regulated output power across an integrated high-voltage isolation barrier with minimal external components, which can be used as an isolated power option when the board is powered from 5V USB.

2.3.7 TPS7A2050

The TPS7A2050 is a low-dropout (LDO) linear regulator that provides a fixed 5.0V output with high PSRR and low output noise over a wide input-voltage range. The device offers low quiescent current and good transient response, enabling efficient post-regulation of switching converters or supply rails that feed precision analog and mixed-signal circuitry.

Integrated current limit and thermal-shutdown protection enhance system reliability which makes the TPS7A2050 an excellent choice for generating clean 5V rails for ADCs.

2.3.8 TLV709A33

The TLV709A33 is a low-quiescent-current, fixed 3.3V LDO regulator designed for space-constrained and cost-sensitive applications. The TLV709A33 offers good line and load regulation, low dropout voltage, and stable operation with small ceramic output capacitors.

3 System Design Theory

This section explains the system design architecture and how the key subsystems are implemented and interact with each other.

3.1 Power Supply

The power tree is divided into non-isolated and isolated sections separated by a galvanic isolation barrier. In this design, isolated power is generated either from the 24V field supply using the LM5180 flyback converter or from the 5V USB input using the UCC33420 isolated DC/DC module. The digital isolator provides digital communication across the isolation barrier.

3.1.1 24V Input Power Path

When powered from the 24V input at J5, the input stage provides protection and filtering before the isolated converter. D14 provides reverse-current protection, D16 clamps input transients, and C31, C32, and C33 provide input decoupling and bulk energy storage.

The conditioned 24V rail powers the LM5180 flyback converter (U8). Together with T1, D11, and C28/C29, this stage generates the isolated 5V5_ISO_OUT rail. The converter uses primary-side regulation, eliminating the need for an optocoupler and simplifying the isolated power design. The UVLO network is configured for approximately 9.5V turn-on and 6.5V turn-off, with an approximately 9ms soft start.

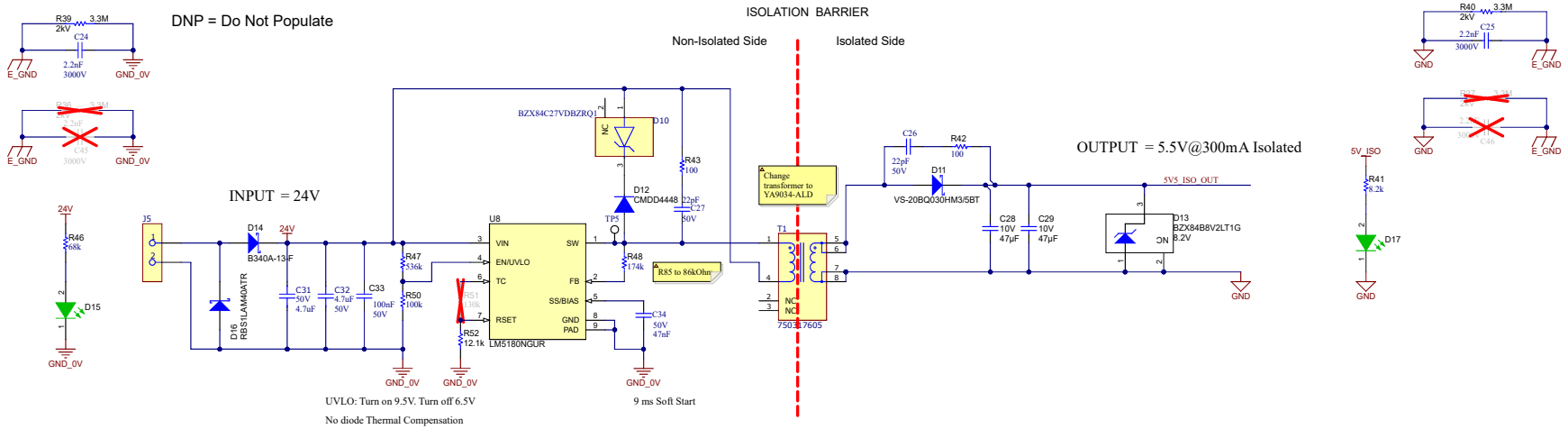


Figure 3-1. Schematic of 24V Input Power Path

For additional details on this circuit, see *Design 1* in the *Typical Applications* section in the LM5180 datasheet.

3.1.2 USB Power Path

For evaluation and bench testing, the board can also be powered from the 5V USB input. In this mode, VUSB powers the UCC33420 isolated DC/DC module (U12), which generates the isolated 5V5_ISO_USB rail.

C41 and C42 provide input decoupling, while C43 and C44 filter the isolated output and support load transients. In the current configuration, this path provides approximately 1.5W of isolated output power.

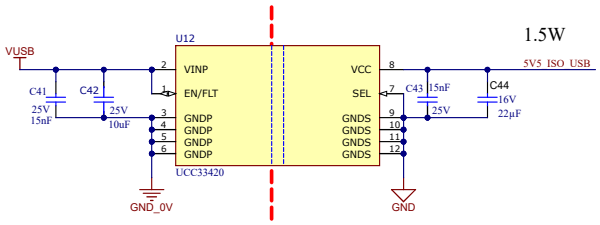


Figure 3-2. Schematic of USB Power Path

3.1.3 Non-isolated MCU Power

On the non-isolated side, the MCU and local digital circuitry are powered from VCC_3V3, generated by U10 (TLV709A33). A diode OR-ing network at D19 selects the source that feeds U10 and prevents back-feeding between the 24V-derived supply path and VUSB. C37 and C38 provide local input and output decoupling. This rail powers the MSPM0G5117 and other non-isolated digital circuitry.

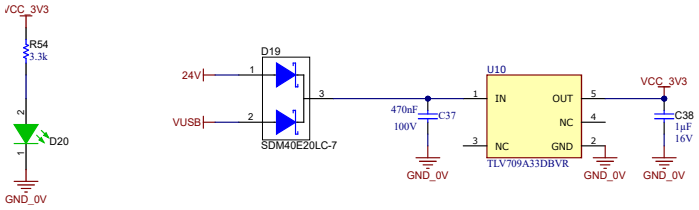


Figure 3-3. Schematic of Non-isolated MCU Power

3.1.4 Isolated ADC and Peripheral Power

The isolated measurement domain is powered from a common isolated 5.5V bus formed by diode OR-ing 5V5_ISO_OUT and 5V5_ISO_USB through D18. This diode OR-ing arrangement allows either isolated source to power the field-side circuitry while preventing reverse current between the two sources.

This bus feeds two post-regulated rails:

1. 5V_ISO, generated by U9 (TPS7A2050), provides a low-noise supply for the precision analog circuitry, including the ADS125H18. C35 and C36 provide local decoupling.
2. 3V3_ISO, generated by U11 (TLV709A33), powers the isolated-side digital and control circuitry. C18 and C40 provide local decoupling.

Together, these rails provide a clean isolated supply for the measurement subsystem while keeping the MCU and host-side circuitry on the non-isolated side of the isolation barrier.

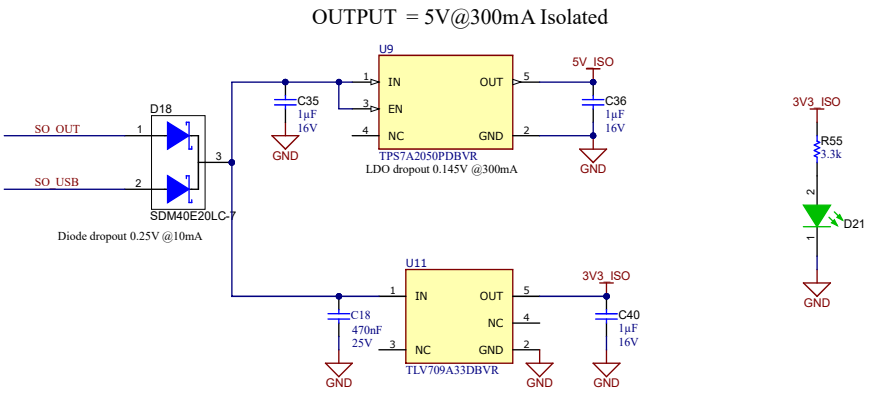


Figure 3-4. Schematic of Isolated ADC and Peripherals Power

3.2 Analog Input Ports

The design includes eight identical 2-terminal analog input channels. Each channel uses a single pair of field terminals and supports either ±10V differential voltage input or ±20mA differential current input. Mode selection is implemented per channel by a Photo-MOS switch, allowing software configuration without rewiring. This 2-terminal input architecture reduces connector count and supports compact high-density analog input modules.

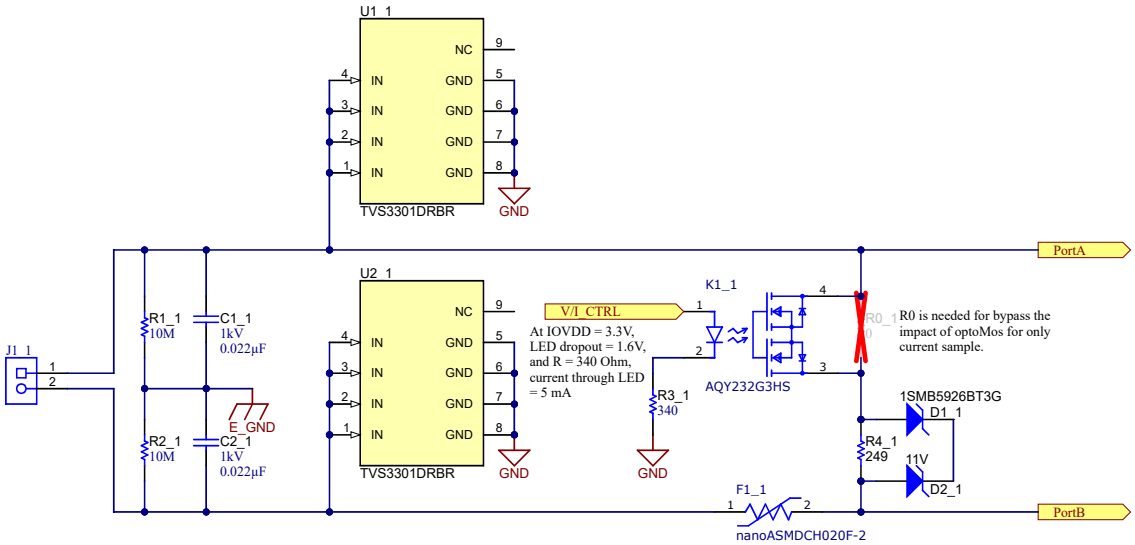


Figure 3-5. Schematic of Analog Input Front End

3.2.1 Analog Input Port and Protection

Each channel is connected through a 2-position input terminal. At the front end, the input includes an EMI network referenced to E_GND and a transient protection stage referenced to the isolated analog ground. R1, R2, C1, and C2 form the input EMI network. The high-value resistors provide a discharge path for the line-to-earth capacitors and prevent charge buildup on floating field wiring while adding negligible loading.

The capacitors provide a high-frequency return path to E_GND, improving EMI performance on long cables.

Transient protection is implemented by U1 and U2 using TVS3301 devices. These clamp surge and ESD events at the input and protect the downstream switching and measurement circuitry.

3.2.2 Voltage and Current Mode Selection

Each channel supports voltage or current measurement through the Photo-MOS switch K1. The isolated-side digital control circuitry drives the switch through the V/I_CTRL signal.

When K1 is turned on, the current measurement path is connected and the channel operates in current mode.

When K1 is turned off, the current path is disconnected and the channel operates as a high-impedance differential voltage input.

R3 sets the LED drive current for the Photo-MOS input from the 3.3V control signal. R0 is an optional 0Ω bypass location that can reduce the effect of the Photo-MOS on-resistance in current mode. In the default implementation, R0 is left unpopulated.

3.2.3 Current Measurement Path

In current mode, the input current flows through the protected current measurement path. R4 is the shunt resistor that converts input current into a differential voltage for the ADC. For a ±20mA input range, the 249Ω shunt produces approximately ±4.98V across the measurement resistor, which is within the ADC input range.

F1 is a resettable fuse placed in series with the current path to improve fault robustness under miswiring or sustained overcurrent conditions. D1 and D2 are bidirectional clamp diodes connected across the shunt path to limit excessive voltage stress during overload events.

3.2.4 Voltage Measurement Path

In voltage mode, K1 disconnects the current measurement branch, including F1, D1, D2, and R4, from the input path. The channel then operates as a differential voltage input for the ±10V range.

In this mode, the input signal is applied to the ADC through only the front-end protection and EMI network. The TVS devices continue to provide transient protection, while the RC network referenced to E_GND maintains EMI performance.

3.2.5 Channel Configuration

All eight channels use the same input topology and are independently controlled. Each channel has a V/I_CTRL signal, enabling software selection between voltage and current input modes on a per-channel basis. This approach provides a flexible analog input interface while keeping the front-end circuitry simple and robust.

3.3 Digital Control and Data Acquisition Subsystem

This section describes the digital subsystem used to control the ADC, acquire conversion data, and manage per-channel voltage and current mode selection. The design is partitioned into a non-isolated controller domain (GND_0V) and an isolated measurement domain (GND) separated by the isolation barrier.

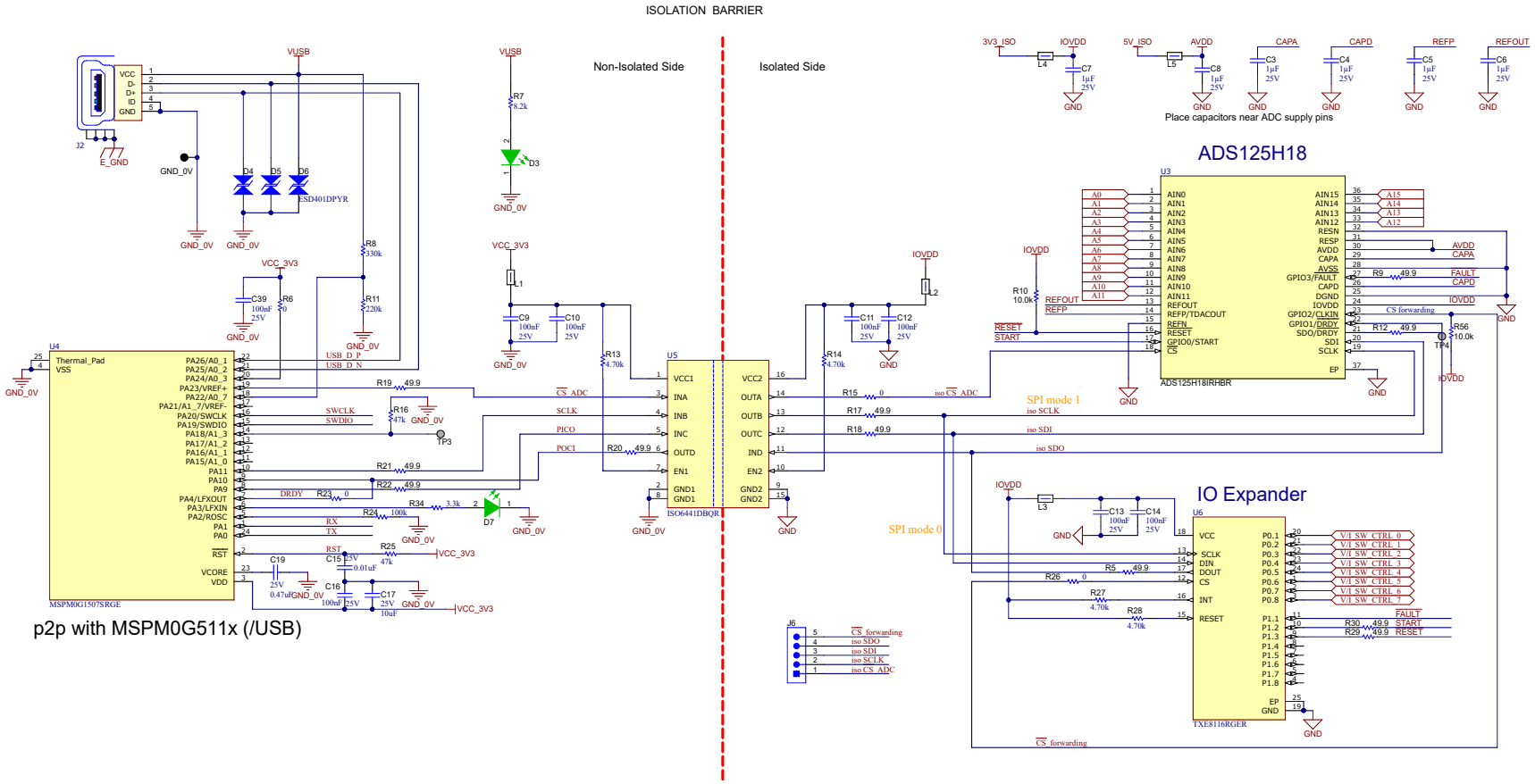


Figure 3-6. Schematic of Digital Control and Data Acquisition Subsystem

3.3.1 Microcontroller Platform

The reference design supports two pin-to-pin compatible MCU options: MSPM0G5117 and MSPM0G1507. The MSPM0G5117 is the primary option and provides USB connectivity for evaluation, configuration, and data capture. The MSPM0G1507 offers a lower-cost option for designs that do not require USB connectivity.

For the USB-enabled implementation, the USB connector is routed to the MCU through protection and support circuitry. D4–D6 provide ESD protection on the USB lines, and resistor dividers are used for VBUS detection and related USB support functions. A 0Ω option, R6, supports assembly selection for the USB-capable variant. The MCU also provides local debug and service interfaces.

3.3.2 Precision ADC

The ADS125H18 precision ADC (U3) is the core of the isolated measurement domain and provides the analog input interface and conversion engine for the eight input channels. The ADC is powered from the isolated rails, with local decoupling placed close to the AVDD, IOVDD, CAPA, CAPD, REFP, and REFOUT pins to reduce supply impedance and support low-noise operation.

The ADC communicates through SPI and also provides control and status signals, including START, RESET, DRDY, and FAULT. These signals are used by the controller and isolated-side support logic to manage conversion sequencing and monitor device status.

GPIO2 is used for the chip-select forwarding function. A pull-up resistor (R56) is added to this node to use a defined logic level during power-up and other idle conditions. Although the pull-up is not strictly required, R56 helps prevent unintended communication to a downstream device before the device is intentionally selected.

3.3.3 Shared SPI Bus and Chip-Select Forwarding

The design uses the ADS125H18 chip-select forwarding function to share one SPI between the ADC and the I/O expander. The chip-select forwarding function is using an ADC GPIO to control the chip-select (CS) pin of a secondary serial peripheral. The chip-select forwarding function allows the ADC to assist in managing SPI communication with external companion devices. As a result, the number of signals that must cross the isolation barrier is reduced, avoiding additional dedicated isolator channels for separate chip-select signals.

The ADC operates in SPI mode 1, while the I/O expander operates in SPI mode 0. The MCU switches SPI mode as needed and communicates with both devices through the same isolated SPI bus by using the ADC forwarding path, while preserving deterministic device selection.

Series resistors (49.9Ω) are used on the digital interface lines to provide source termination and improve signal integrity. The series resistors help damp ringing and overshoot on fast edges and reduce EMI, especially on signals crossing the isolation barrier or routed over longer traces. Place these resistors close to the signal driver.

3.3.4 I/O Expander

An SPI-based I/O expander, TXE8116 (U6), provides the additional isolated-side digital control signals required by the system. The primary function is to generate the eight V/I_SW_CTRL outputs used for per-channel voltage and current mode selection in the analog front end. The TXE8116 also supports ADC-related control and monitoring functions such as START, RESET, and FAULT handling.

Local decoupling capacitors are placed near the expander supply pins to reduce digital supply noise in the isolated domain.

3.3.5 Optional External Reference

The design includes an optional external precision voltage reference, REF6025 (U7), to improve accuracy and temperature drift performance. When the external reference option is populated, the reference drives the ADC reference input and is locally filtered to maintain a low-noise reference node. This option can improve reference accuracy and temperature drift performance compared with relying only on the ADC internal reference path.

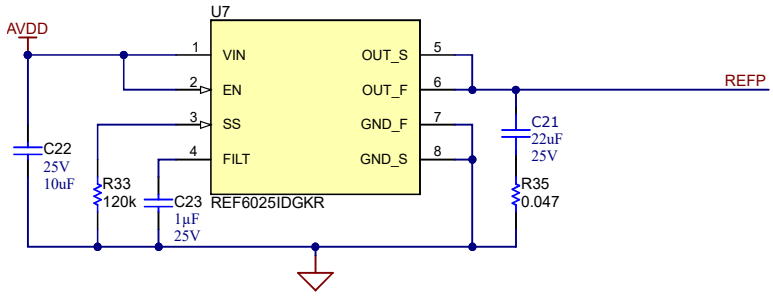


Figure 3-7. Schematic of Optional External Reference

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

4.1.1 PCB Overview

Figure 4-1 and Figure 4-2 show the top and bottom views of the TIDA-010988 PCB.

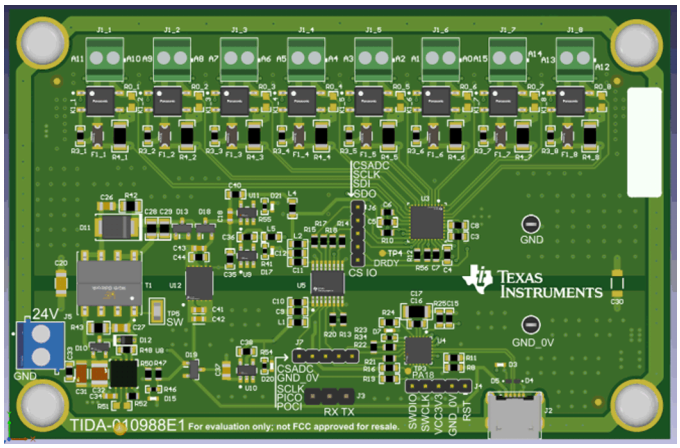


Figure 4-1. TIDA-010988 PCB Top View

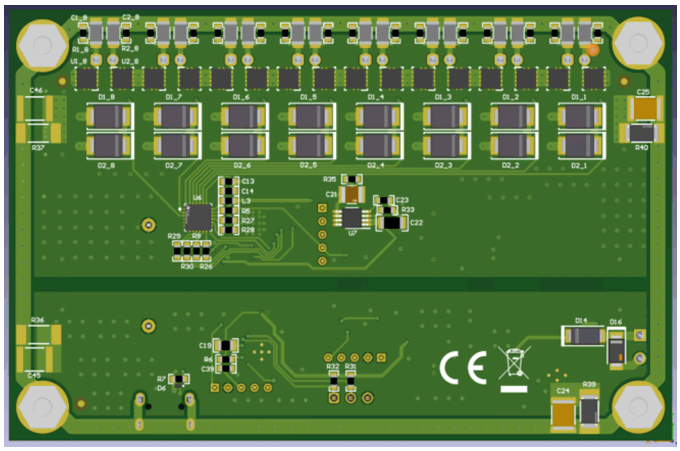


Figure 4-2. TIDA-010988 PCB Bottom View

4.1.2 Connector Description

4.1.2.1 Power Connectors

The board can be powered in either of the following ways:

- A nominal 24V input voltage applied through connector J5.
- A standard micro-USB connection through J2.

4.1.2.2 Input Connectors

Table 4-1 describes the different connectors on TIDA-010988 Board.

Table 4-1. Connector Descriptions

DESIGNATOR	DESCRIPTION
J5	24V field power input
J2	USB connection, and can power the board as well
J1-1 through J1-8	Analog input connectors for the eight channels. The default configuration is voltage input mode
J3	UART Connector, and can be used for backplane communication with CPU module

Table 4-1. Connector Descriptions (continued)

DESIGNATOR	DESCRIPTION
J4	MCU debug connector for firmware programming

4.2 Test Setup and Test Results

4.2.1 ADS125H18 General Configuration

Table 4-2 summarizes the baseline ADS125H18 configuration used during characterization. Unless otherwise noted, all measurements in this section were collected using this configuration.

Table 4-2. ADS125H18 Baseline Configuration Used in Characterization

Item	Setting
Clock source	Internal oscillator
Speed mode	High-speed Mode ($f_{\_MOD}$ = 12.8MHz)
Voltage reference	Internal 2.5V reference
Digital filter	SINC4 (32) + SINC1 (32)
Over-sampling ratio (OSR)	1024
Sequencer mode	Repeat single step continuously

4.2.2 Offset Test

4.2.2.1 Test Setup

Offset testing was performed to evaluate the residual input-referred error of the analog input signal chain under zero-input conditions in both voltage input mode and current input mode.

Measurements were performed at six temperature points: –40°C, –20°C, 25°C, 85°C, 105°C, and 125°C. During testing, the reference design board was placed inside a temperature chamber (Vötsch VT 4002). A TMP119EVM was positioned close to the board to monitor the local temperature near the hardware under test. At each temperature point, the chamber was allowed to stabilize for approximately one hour before data acquisition began.

For voltage input offset testing, all eight channels were configured in voltage mode and shorted at the corresponding input terminals of the reference design board. For current input offset testing, all eight channels were configured in current mode and left open-circuit at the corresponding input terminals of the reference design board. All eight channels were configured in the same input mode during each measurement. Figure 4-3 shows the offset test setup.

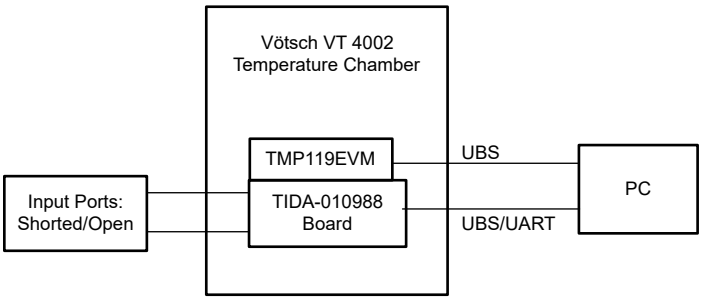


Figure 4-3. Over Temperature Offset Test Setup

The ADS125H18 auto-sequencing function was used to continuously acquire conversion data after device configuration and power-up. Figure 4-4 shows the ADC data acquisition timing used in the measurements. For each channel, 1024 consecutive samples were collected before switching to the next channel in the scan sequence. The acquisition started with CH1 and continued sequentially through CH8. Channel data were therefore acquired sequentially rather than simultaneously. No outlier rejection was applied. Measured data were transferred to a PC through the serial interface for post-processing.

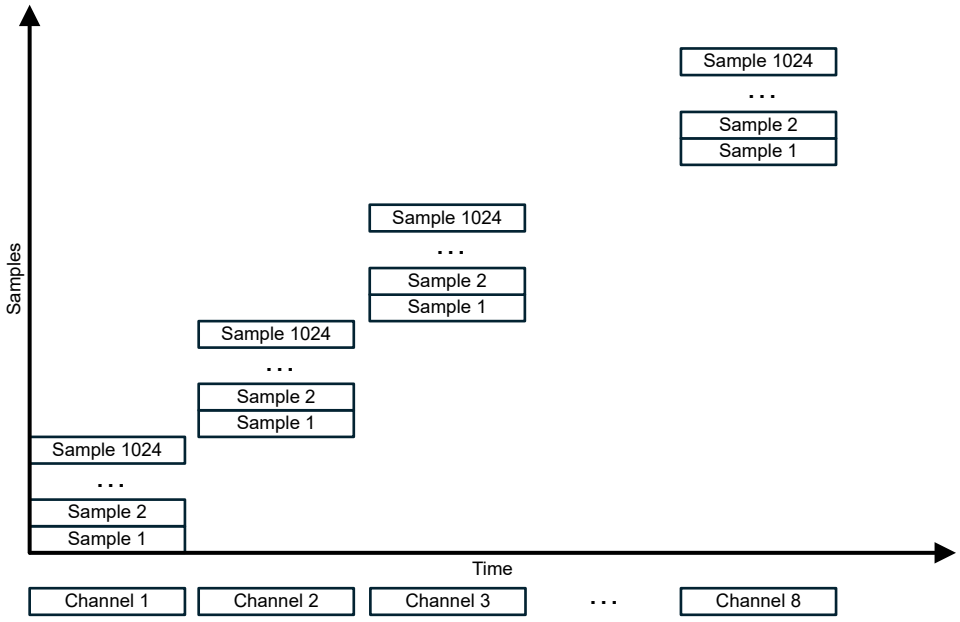


Figure 4-4. Sequential ADC Data Acquisition Timing with 1024 Samples Per Channel

4.2.2.2 Test Results

Offset results were collected for both voltage input mode and current input mode over the full characterized temperature range. The measured results are summarized separately in the following sections.

4.2.2.2.1 Voltage Input Mode

Voltage input offset is summarized as the average absolute offset of the eight channels at each temperature point. Table 4-3 summarizes the average absolute offset in voltage input mode at –40°C, –20°C, 25°C, 85°C, 105°C, and 125°C. The results show that the voltage input offset remains stable over temperature, with the average absolute offset close to 1mV at most temperature points and a lower value observed at 25°C. No abnormal temperature-dependent excursion was observed across the characterized range.

Table 4-3. Voltage Input Mode Average Absolute Offset Over Temperature

Temperature	–40°C	–20°C	25°C	85°C	105°C	125°C
Average Absolute Offset (mV)	1.035	1.031	0.422	1.064	1.047	0.946

Figure 4-5 through Figure 4-10 show the measured offset distribution histograms of representative CH4 at different temperatures. The plots provide a sample-distribution view of offset behavior at each temperature point. In general, the distributions remain single-peaked over the full characterized temperature range, and no abnormal distribution shape is observed. The center of the distribution varies with temperature, consistent with the mean offset trend shown previously. Compared with the other temperature points, the distribution at 25°C is narrower, corresponding to the reduced average absolute offset observed near room temperature.

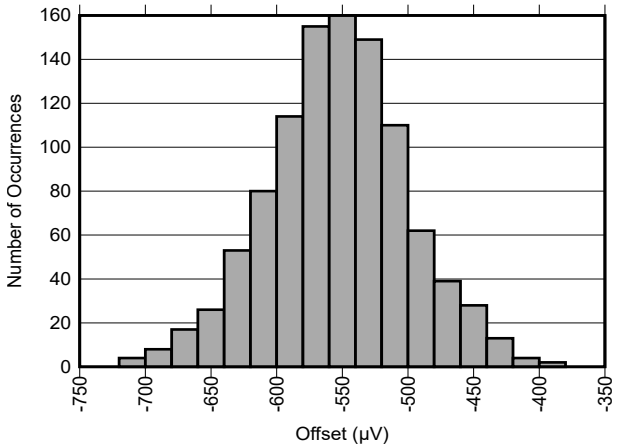


Figure 4-5. Voltage Input Mode Offset Distribution Histograms of Representative CH4 at –40℃

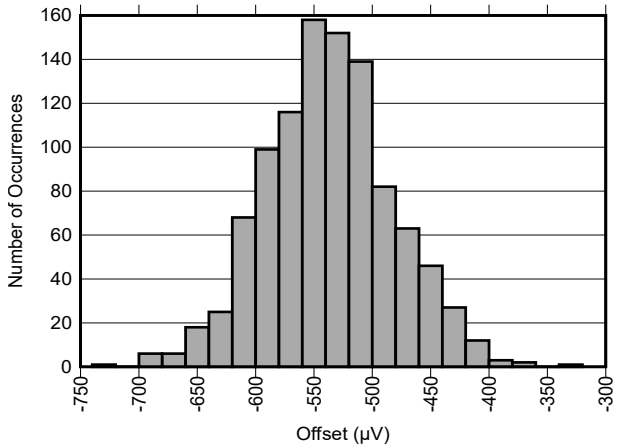


Figure 4-6. Voltage Input Mode Offset Distribution Histograms of Representative CH4 at –20℃

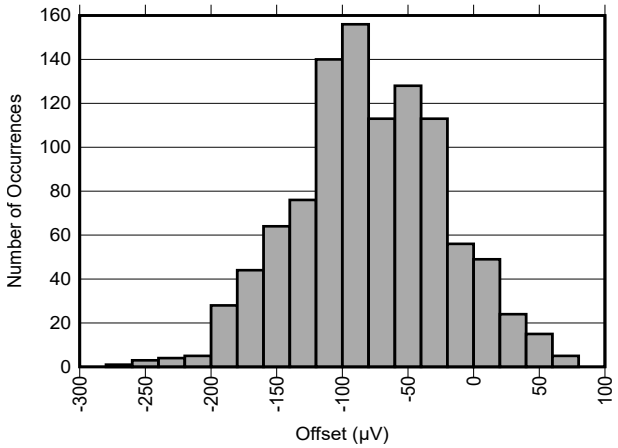


Figure 4-7. Voltage Input Mode Offset Distribution Histograms of Representative CH4 at 25℃

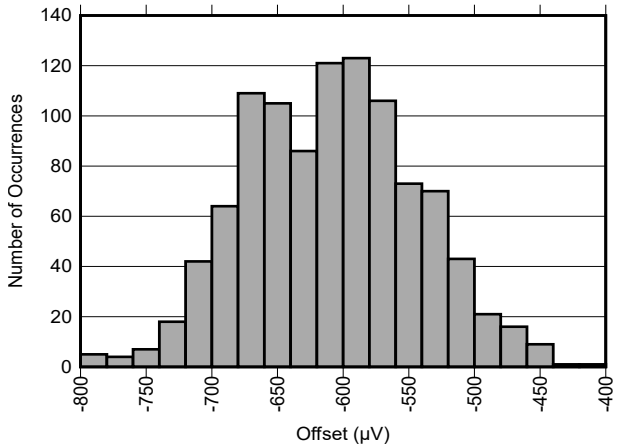


Figure 4-8. Voltage Input Mode Offset Distribution Histograms of Representative CH4 at 85℃

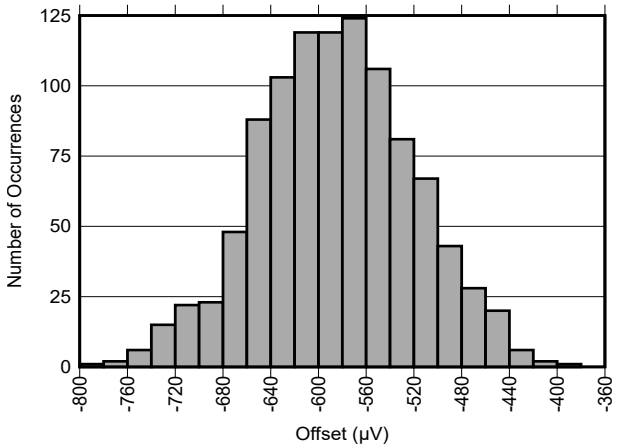


Figure 4-9. Voltage Input Mode Offset Distribution Histograms of Representative CH4 at 105℃

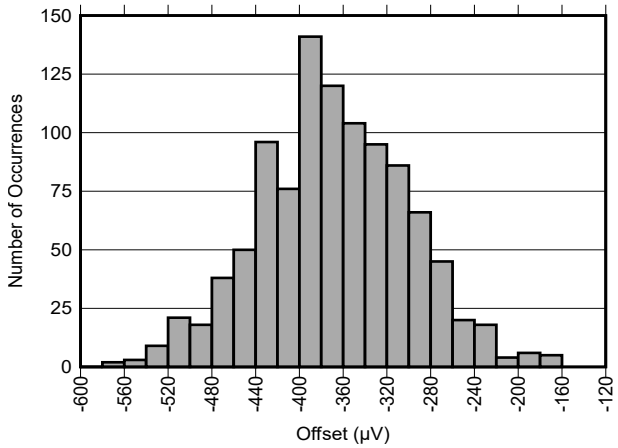


Figure 4-10. Voltage Input Mode Offset Distribution Histograms of Representative CH4 at 125℃

4.2.2.2.2 Current Input Mode

Current input offset is presented as the average absolute offset of the eight channels at each temperature point as well as voltage input mode. Table 4-4 lists the average absolute offset in current input mode at –40°C, –20°C, 25°C, 85°C, 105°C, and 125°C. The measured results indicate that the current input offset is generally

consistent across temperature, with values around 4uA over most of the characterized range. A slightly lower value was observed at 125°C, but no abnormal temperature-related shift is evident.

Table 4-4. Current Input Mode Average Absolute Offset Over Temperature

Temperature	–40°C	–20°C	25°C	85°C	105°C	125°C
Average Absolute Offset (µA)	4.151	4.143	4.126	4.263	4.196	3.800

Figure 4-11 through Figure 4-16 show the measured offset distribution histograms of representative CH4 at different temperatures in current input mode. The histograms show that the sample distribution remains well-behaved at all characterized temperature points, with no evidence of irregular spreading or discontinuity. In general, the distributions remain single-peaked throughout the characterized range, and no abnormal distribution shape is observed. The center of the distribution changes slightly with temperature, consistent with the summarized offset results in Table 4-4.

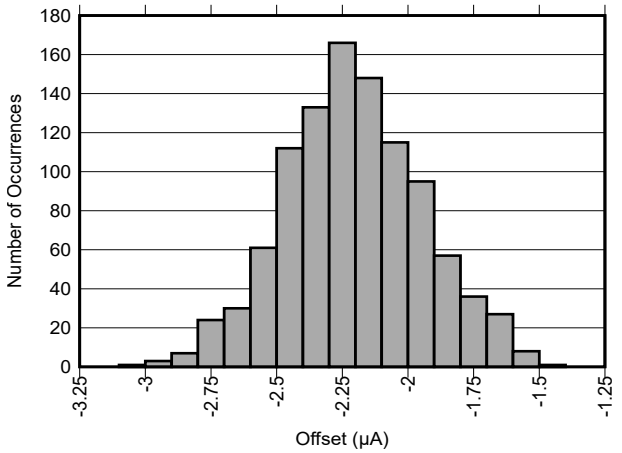


Figure 4-11. Current Input Mode Offset Distribution Histograms of Representative CH4 at –40℃

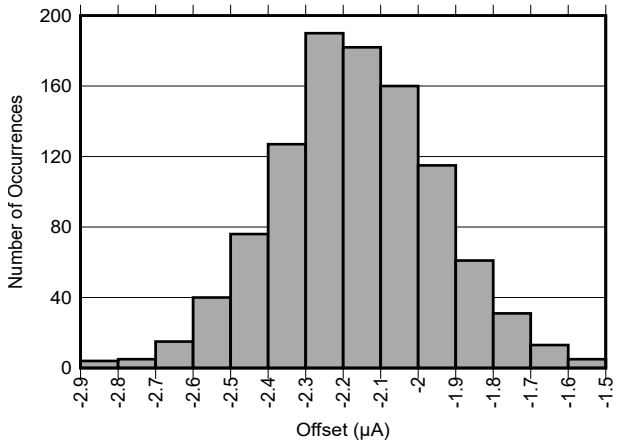


Figure 4-12. Current Input Mode Offset Distribution Histograms of Representative CH4 at –20℃

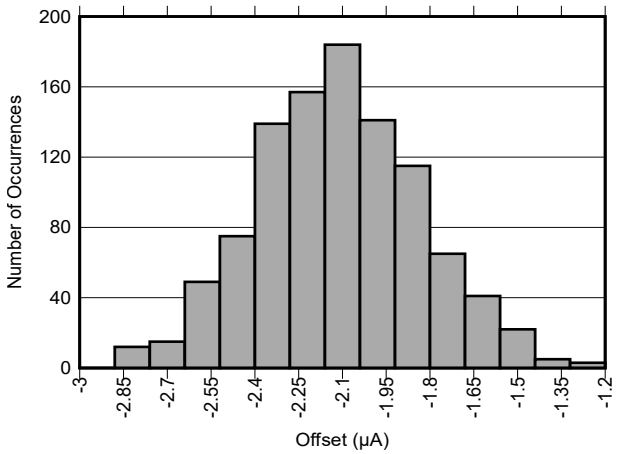


Figure 4-13. Current Input Mode Offset Distribution Histograms of Representative CH4 at 25℃

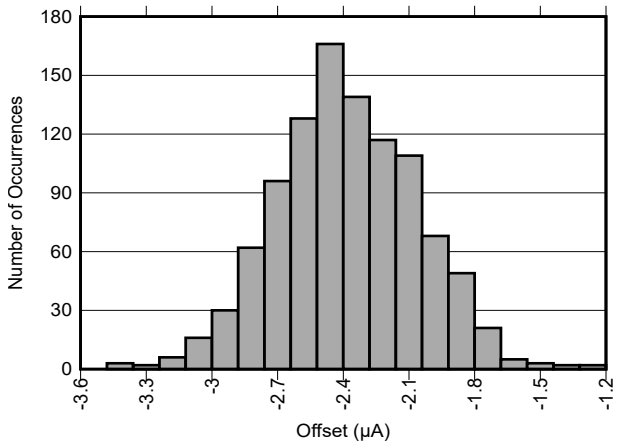


Figure 4-14. Current Input Mode Offset Distribution Histograms of Representative CH4 at 85℃

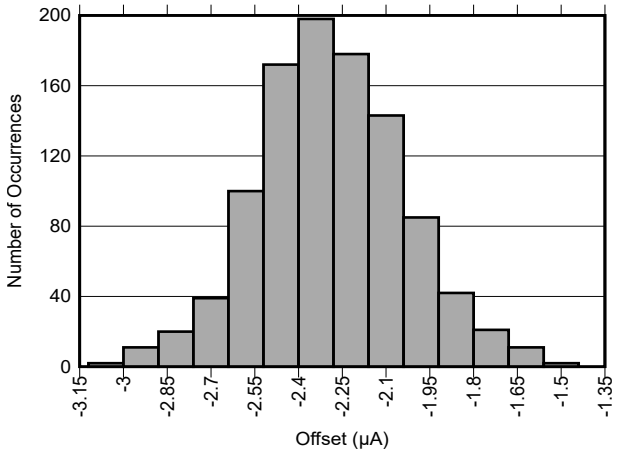


Figure 4-15. Current Input Mode Offset Distribution Histograms of Representative CH4 at 105℃

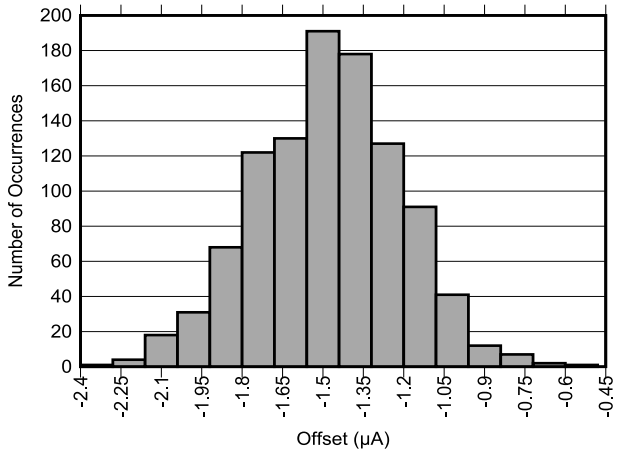


Figure 4-16. Current Input Mode Offset Distribution Histograms of Representative CH4 at 125℃

4.2.3 System Accuracy Error and Noise Performance Test

4.2.3.1 Calculation Method

For each test condition, 1024 samples were collected for each channel. Unless otherwise noted, average measured value, RMS noise, and ENOB were calculated from the raw ADC conversion codes collected under each test condition. System absolute accuracy error was calculated separately using the converted voltage or current value derived from each sample, and was then referenced to the corresponding digital multimeter (DMM) reading.

The average measured value x_{AVG} for each channel was calculated using Equation 1.

$$x_{AVG} = \frac{\sum_{i=1}^{N} x_i}{N} \text{ (codes)} \quad (1)$$

Where

- x_i is the measured value of sample i
- N = 1,024

The RMS noise for each channel was calculated from the same 1024-sample data set using Equation 2. The RMS noise values reported in the following test results are obtained by converting the calculated RMS noise in raw ADC codes to the corresponding input-referred voltage or current values, while ENOB is calculated from the RMS noise in raw ADC codes.

$$\text{RMS Noise} = \sqrt{\frac{\sum_{i=1}^{N} [x_i - x_{AVG}]^2}{N}} \text{ (codes)} \quad (2)$$

Where

- x_{AVG} is the average measured value of the channel
- N = 1,024

System absolute accuracy error for each sample was calculated relative to the corresponding DMM reference reading using Equation 3.

$$\text{System Absolute Accuracy Error} = \left| \frac{x_i - x_{REF}}{x_{REF}} \right| \times 100\% \quad (3)$$

Where

- x_{REF} is the corresponding reference value measured by the DMM

ENOB was calculated from the measured RMS noise using Equation 4.

$$\text{ENOB} = \log_2\left(\frac{2^{24}}{\text{RMS Noise}}\right) \text{(bits)} \quad (4)$$

Where

- 2^{24} is the full-scale code range of the measurement path

4.2.3.2 Test Setup

System accuracy error and noise performance were evaluated in both voltage input mode and current input mode using the baseline ADS125H18 configuration. Unless otherwise noted, the temperature conditions, chamber setup, and data acquisition procedure were the same as those used for the offset test. Measurements were performed at six temperature points: –40°C, –20°C, 25°C, 85°C, 105°C, and 125°C.

For voltage input testing, a battery stack was used as the input source. The applied input levels were +3.3V, –3.3V, +5V, –5V, +10V, and –10V. All eight channels were connected in parallel to the same input source. A 6.5-digit DMM (Keysight 34461A) was connected in parallel at the input terminal of the reference design board to monitor the applied voltage.

For current input testing, the input current was generated using a battery stack in series with a precision resistor. The applied current levels were +4mA, –4mA, +10mA, –10mA, +20mA, and –20mA. CH1 through CH4 were connected in series and tested first, CH5 through CH8 were then tested using the same method. The DMM was inserted in series in the current loop to monitor the applied current.

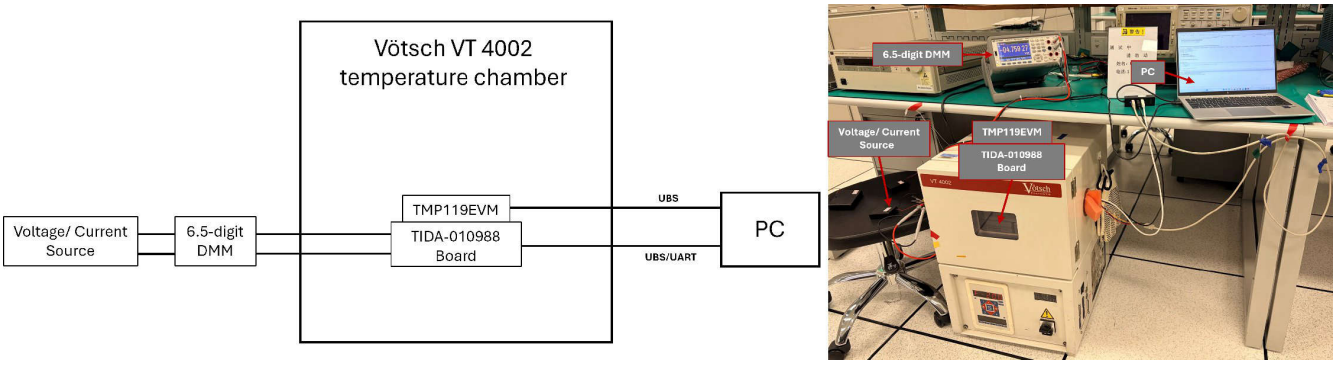


Figure 4-17. Block Diagram and Photograph of the Overtemperature System Accuracy Error and Noise Performance Test Setup

The TIDA-010988 board and TMP119EVM were placed inside the Vötsch™ VT 4002 temperature chamber during testing, while the source instrument, DMM, and PC remained outside the chamber. The PC communicated with the reference design board through the UART interface and was used for data logging and post-processing. Figure 4-17 shows both the system-level test setup diagram and a photograph of the laboratory setup used for over temperature accuracy error and noise evaluation.

4.2.3.3 Test Results

4.2.3.3.1 Voltage Input Mode

Table 4-5 summarizes RMS noise, ENOB, and system absolute accuracy error in voltage input mode over the characterized temperature range. The tested input levels were +3.3V, –3.3V, +5V, –5V, +10V, and –10V. For each test condition, 1024 samples were collected for each channel. RMS noise was calculated for each channel and then averaged across the eight channels. ENOB was calculated from the corresponding RMS noise result. System absolute accuracy error was calculated for each measured sample relative to the corresponding DMM reference value. The 1024 calculated accuracy error values were averaged to obtain one accuracy error result for each channel. The reported table value is the average of the eight channel results. In this table, RMS noise is reported as a converted voltage value.

Table 4-5. Summary of RMS Noise, ENOB, and System Absolute Accuracy Error in Voltage Input Mode

Input Voltage	Temperature	RMS Noise (µV)	ENOB (bits)	Accuracy Error (%)
+3.3V	–40°C	54.99	19.79	0.0486
	–20°C	57.07	19.74	0.0311
	25°C	60.20	19.66	0.0355
	85°C	66.37	19.52	0.0298
	105°C	67.89	19.49	0.0356
	125°C	71.07	19.42	0.0296
–3.3V	–40°C	54.85	19.80	0.0545
	–20°C	56.37	19.76	0.0356
	25°C	61.92	19.62	0.0308
	85°C	65.38	19.54	0.0360
	105°C	68.35	19.48	0.0297
	125°C	69.19	19.46	0.0297
+5V	–40°C	57.84	19.72	0.0449
	–20°C	58.97	19.69	0.0246
	25°C	63.76	19.58	0.0257
	85°C	68.63	19.47	0.0212
	105°C	71.23	19.42	0.0260
	125°C	72.07	19.40	0.0210
–5V	–40°C	56.93	19.74	0.0482
	–20°C	59.34	19.74	0.0255
	25°C	64.04	19.73	0.0212
	85°C	68.74	19.72	0.0255
	105°C	71.06	19.71	0.0201
	125°C	72.66	19.71	0.0206
+10V	–40°C	68.31	19.48	0.0381
	–20°C	72.96	19.39	0.0158
	25°C	76.86	19.31	0.0165
	85°C	83.55	19.19	0.0127
	105°C	87.04	19.13	0.0163
	125°C	88.78	19.10	0.0120
–10V	–40°C	68.66	19.47	0.0412
	–20°C	71.55	19.41	0.0140
	25°C	76.38	19.32	0.0111
	85°C	83.21	19.20	0.0126
	105°C	86.45	19.14	0.0087
	125°C	87.73	19.12	0.0096

As shown in Table 4-5, RMS noise increases with temperature and with input magnitude. ENOB decreases correspondingly at higher temperature points and larger input levels. This behavior is consistent with the measured noise trend. Across the full characterized range, ENOB remains relatively stable and stays above 19 bits for all tested voltage input conditions.

System absolute accuracy error remains stable over temperature and input polarity. In general, the percentage error is smaller at higher input levels and slightly larger at lower input levels, as expected for a normalized accuracy error metric. Positive and negative input conditions show comparable performance across the characterized range, with no abnormal excursion observed at the temperature extremes.

Figure 4-18 shows the worst-case channel system absolute accuracy error versus temperature in voltage input mode for different input levels. At each temperature point, the accuracy error for each channel was obtained by averaging 1024 calculated sample errors, and the plotted value represents the worst-case channel among the eight channels. In contrast, Table 4-5 reports the average of the eight channel results.

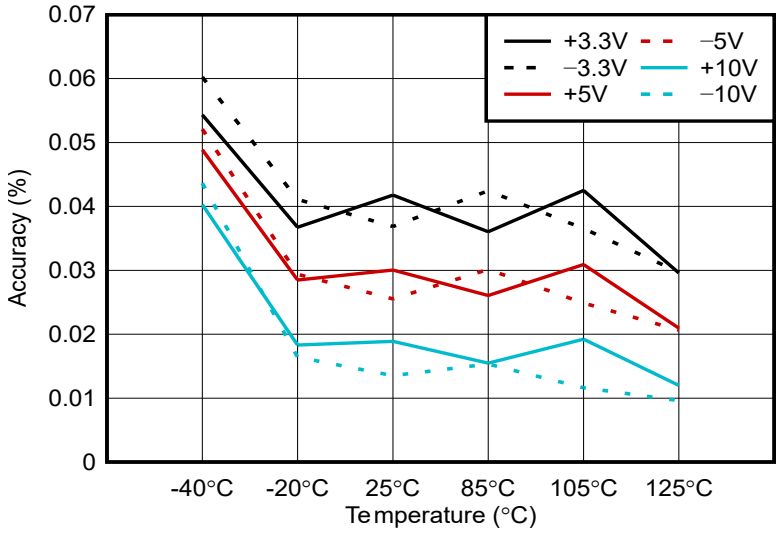


Figure 4-18. Worst-Case Channel System Absolute Accuracy Error vs Temperature in Voltage Input Mode

The results indicate that the worst-case channel system absolute accuracy error is highest at the lowest tested temperature and remains relatively consistent from –20°C to 125°C. As expected for a percentage-based accuracy error metric, the error is generally larger at lower input magnitudes and smaller at higher input magnitudes, with the ±10V conditions showing the lowest error and the ±3.3V conditions showing the highest error. Positive and negative input levels exhibit comparable trends over temperature, indicating balanced performance across input polarity.

Figure 4-19 shows the RMS noise versus temperature in voltage input mode for input levels of +3.3V, –3.3V, +5V, –5V, +10V, and –10V. At each temperature point, the plotted value represents the average RMS noise across the eight channels, where the RMS noise of each channel is calculated from 1024 measured samples.

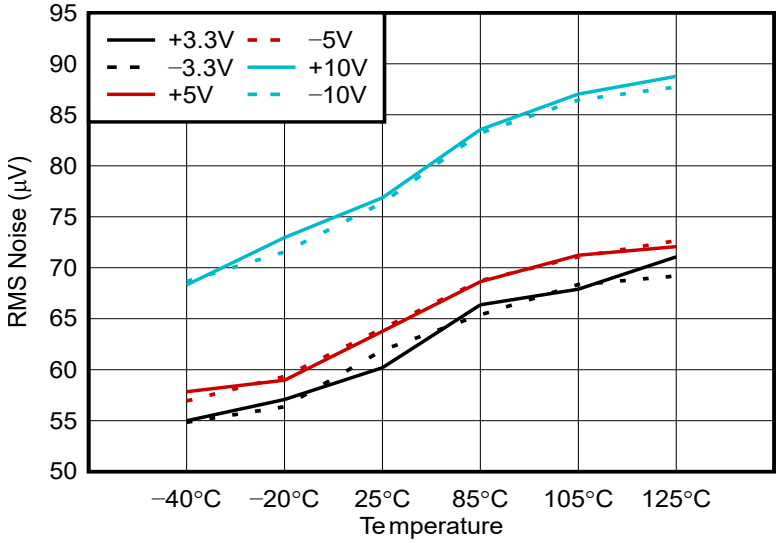


Figure 4-19. Voltage Input Mode RMS Noise vs Temperature

The results show a clear increase in RMS noise with temperature across all tested input levels. Higher input magnitudes also tend to produce higher RMS noise, with the ±10V input conditions exhibiting the largest values

over most of the characterized range. Positive and negative input conditions follow similar trends, indicating consistent voltage input noise performance across input polarity.

Figure 4-20 through Figure 4-22 shows the output distribution histograms for Channel 4 in voltage input mode with a +10V input at –40°C, 25°C, and 125°C. Channel 4 was selected as a representative channel to illustrate the distribution behavior over temperature.

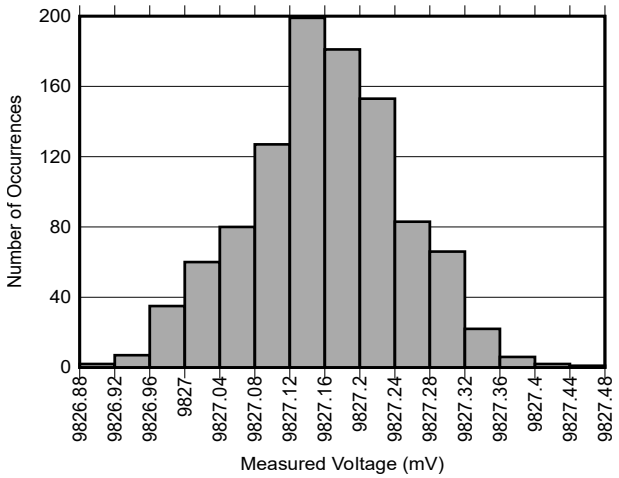


Figure 4-20. Measured Voltage Distribution Histogram for CH4 at +10V at –40℃

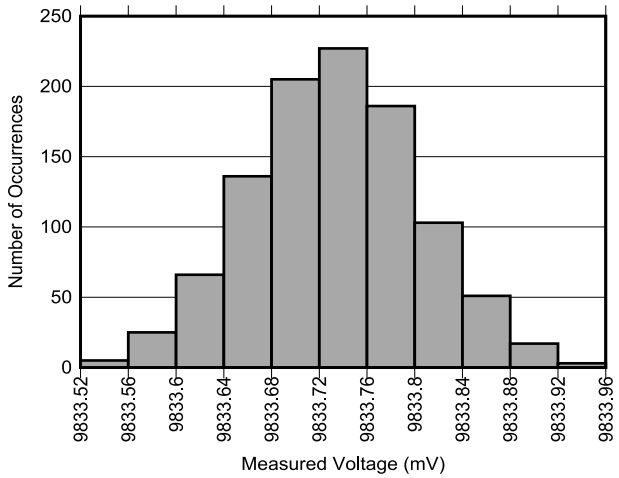


Figure 4-21. Measured Voltage Distribution Histogram for CH4 at +10V at 25℃

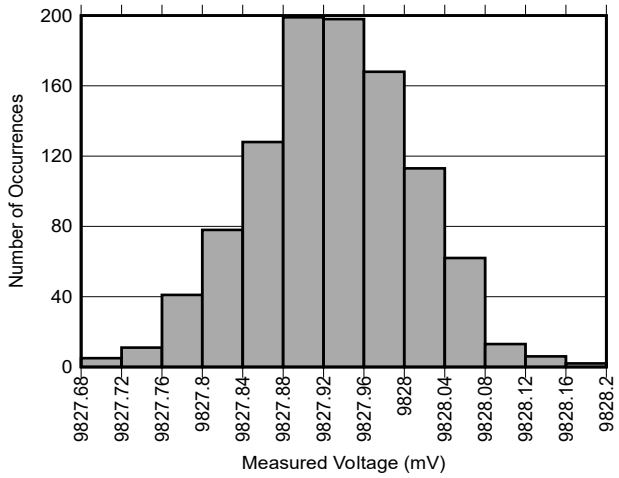


Figure 4-22. Measured Voltage Distribution Histogram for CH4 at +10V at 125℃

The histograms indicate that the output distribution remains unimodal and approximately Gaussian across the characterized temperature range, with no abnormal distortion or discontinuity observed. The distribution width increases with temperature, which is consistent with the RMS noise trend shown in Figure 4-19. These results indicate stable channel behavior and consistent voltage input noise performance over temperature.

4.2.3.3.2 Current Input Mode

Table 4-6 summarizes the RMS noise, ENOB, and system absolute accuracy error in current input mode for input levels of +4mA, –4mA, +10mA, –10mA, +20mA, and –20mA over the characterized temperature range from –40°C to 125°C. The RMS noise is reported as a converted current value.

Table 4-6. Summary of RMS Noise, ENOB, and System Absolute Accuracy Error in Current Input Mode

Input Current	Temperature	RMS Noise (nA)	ENOB (bits)	Accuracy Error (%)
+4mA	–40°C	215.81	19.83	0.1189
	–20°C	223.30	19.78	0.1386
	25°C	242.01	19.66	0.1294
	85°C	260.19	19.56	0.1308
	105°C	265.82	19.53	0.1348
	125°C	272.99	19.49	0.1212
–4mA	–40°C	215.75	19.83	0.1095
	–20°C	223.51	19.78	0.1133
	25°C	240.66	19.67	0.1129
	85°C	258.38	19.57	0.0990
	105°C	265.94	19.53	0.1018
	125°C	267.63	19.52	0.1136
+10mA	–40°C	221.44	19.79	0.0717
	–20°C	229.05	19.74	0.1020
	25°C	247.42	19.63	0.0871
	85°C	263.46	19.54	0.0807
	105°C	269.85	19.51	0.0859
	125°C	280.35	19.45	0.0788
–10mA	–40°C	221.79	19.79	0.0660
	–20°C	229.57	19.74	0.0893
	25°C	245.30	19.64	0.0812
	85°C	264.69	19.53	0.0730
	105°C	272.33	19.49	0.0718
	125°C	278.54	19.46	0.0778
+20mA	–40°C	233.00	19.72	0.0691
	–20°C	244.95	19.65	0.1053
	25°C	265.18	19.53	0.0899
	85°C	285.40	19.42	0.0847
	105°C	284.98	19.43	0.0896
	125°C	296.73	19.37	0.0855
–20mA	–40°C	233.89	19.71	0.0592
	–20°C	242.26	19.66	0.0993
	25°C	259.43	19.56	0.0819
	85°C	283.78	19.43	0.0694
	105°C	286.16	19.42	0.0769
	125°C	300.20	19.35	0.0824

Overall, the RMS noise increases with temperature for all tested input levels, and the ENOB correspondingly decreases as temperature rises. The system absolute accuracy error remains relatively stable across temperature, with the ±10mA and ±20mA input conditions generally exhibiting lower accuracy error than the ±4mA conditions. Across all tested current levels and temperatures, the measured results indicate stable current input measurement performance over temperature.

Figure 4-23 shows the worst-case channel system absolute accuracy error versus temperature in current input mode for different input levels. At each temperature point, the accuracy error for each channel was obtained by averaging 1024 calculated sample errors, and the plotted value represents the worst-case channel among the eight channels. In contrast, Table 4-6 reports the average of the eight channel results.

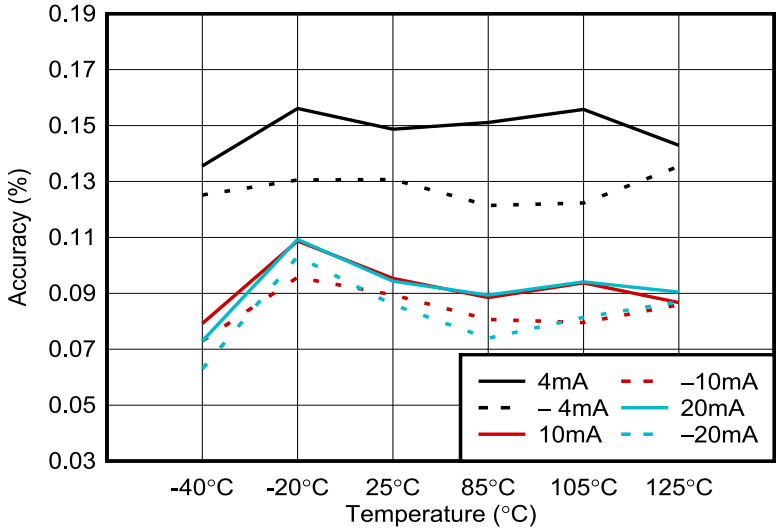


Figure 4-23. Worst-Case Channel System Absolute Accuracy Error vs Temperature in Current Input Mode

The results indicate that the worst-case channel accuracy error is well controlled across the full characterized temperature range for all tested current input levels. The ±10mA and ±20mA input conditions generally show smaller error than the ±4mA conditions. The negative current input conditions also show slightly smaller error than the corresponding positive current input conditions. Overall, the curves show consistent current input accuracy performance over temperature.

Figure 4-24 shows the RMS noise versus temperature in current input mode for different input currents. At each temperature point, the plotted value represents the average RMS noise across the eight channels, where the RMS noise of each channel is calculated from 1024 measured samples.

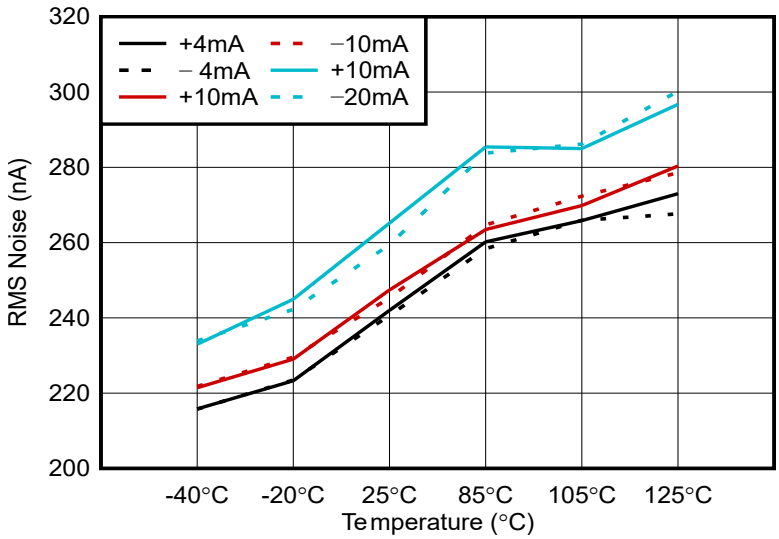


Figure 4-24. Current Input Mode RMS Noise vs Temperature

The results show a clear increase in RMS noise with temperature across all tested current input levels. In general, the ±20mA input conditions exhibit the highest RMS noise over most of the characterized temperature range. Positive and negative current input conditions follow similar temperature trends, indicating consistent noise performance across input polarity.

Figure 4-25 through Figure 4-27 show the measured current distribution histograms for Channel 4 in current input mode with a +20mA input at –40°C, 25°C, and 125°C. At all three temperature points, the measured current distribution remains single-peaked and well behaved, with no visible secondary peak or abnormal shape. These histograms provide a qualitative view of the temperature dependence of current input noise performance.

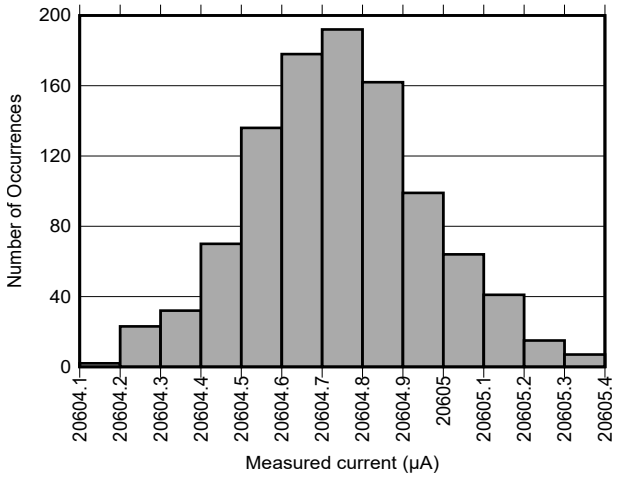


Figure 4-25. Measured Current Distribution Histogram for CH4 at +20mA at –40℃

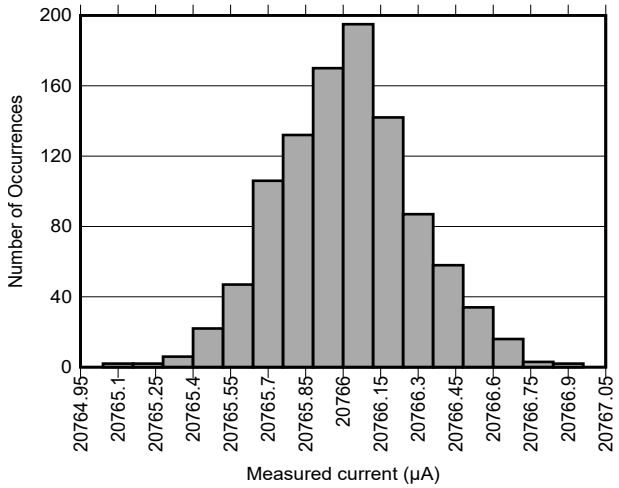


Figure 4-26. Measured Current Distribution Histogram for CH4 at +20mA at 25℃

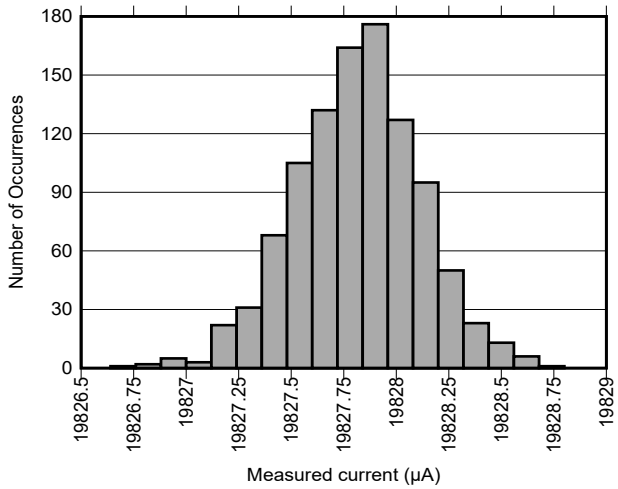


Figure 4-27. Measured Current Distribution Histogram for CH4 at +20mA at 125℃

4.2.4 Input Protection Test

This section evaluates the overvoltage protection network used for the current input mode shunt path. The protection network under test consists of the back-to-back Zener diodes and the PTC fuse used in the current input signal path. The purpose of this test is to verify that the protection circuit clamps the protected node voltage during an input overvoltage event on the current-sense path, limits the sustained fault current, and recovers after the overvoltage is removed. The test focuses on the steady-state overvoltage behavior of current input mode shunt protection network. Protection performance related to TVS devices for transient surge and EMC events is evaluated separately.

4.2.4.1 Test Setup

Figure 4-28 shows the test setup and protection circuit used for the current input mode shunt path. This evaluation targets the shunt-based current input protection circuitry. During the test, the device is configured in current input mode, and a DC overvoltage is applied across the current input terminals to emulate a fault condition.

In current input mode, the shunt path normally converts input current into a measurable voltage. During an overvoltage fault, excessive current can otherwise stress this path. The protection circuit is designed to clamp the protected node voltage and limit sustained fault current. The back-to-back Zener diode network clamps the node to approximately the nominal 11V clamping level, while the PTC fuse heats up and transitions toward

a higher-resistance state, thereby reducing fault current. TVS devices at the input provide additional transient protection.

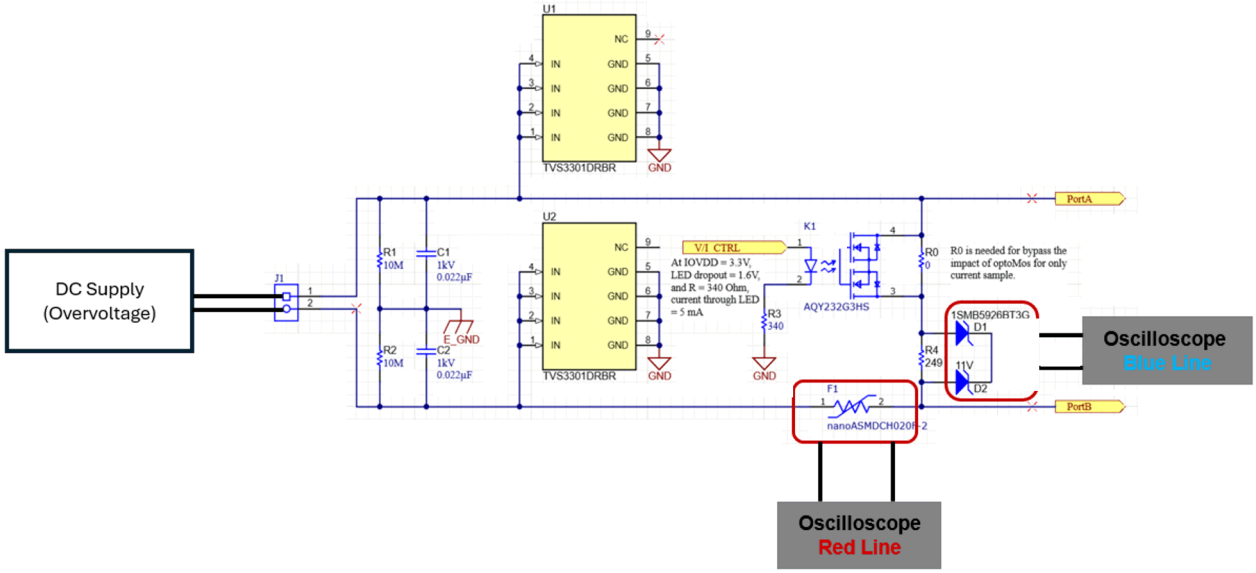


Figure 4-28. Test Setup of Overvoltage for Current Input Mode Protection Circuit

The protection response is monitored using the oscilloscope. The blue oscilloscope trace represents the voltage across the back-to-back Zener diode network, and the red trace represents the voltage across the PTC fuse. These waveforms are used to observe both the protection response after overvoltage is applied and the recovery behavior after the fault is removed. The measured timing values in this section are presented as representative results only because the values depend on the applied fault level, thermal conditions, and waveform threshold definition.

4.2.4.2 Test Results

Figure 4-29 and Figure 4-30 shows the measured protection waveforms in current input mode with 24V and 30V input overvoltage, respectively. In both tests, the blue waveform shows that the back-to-back Zener diode network clamps the protected node voltage to approximately the Zener clamping level during the fault interval. The red waveform shows the voltage across the PTC fuse increasing after the overvoltage is applied, indicating that the PTC responds to the fault condition and transitions toward a higher-resistance state.

These results are consistent with the intended operation of the current input mode shunt protection path. The Zener network provides voltage clamping, while the PTC fuse limits sustained fault current and reduces stress on the shunt path. After the overvoltage source is removed, the voltage across the PTC fuse returns toward the initial level, indicating recovery of the protection path. The measured waveforms are consistent with the intended protection behavior for the shunt network in current input mode.

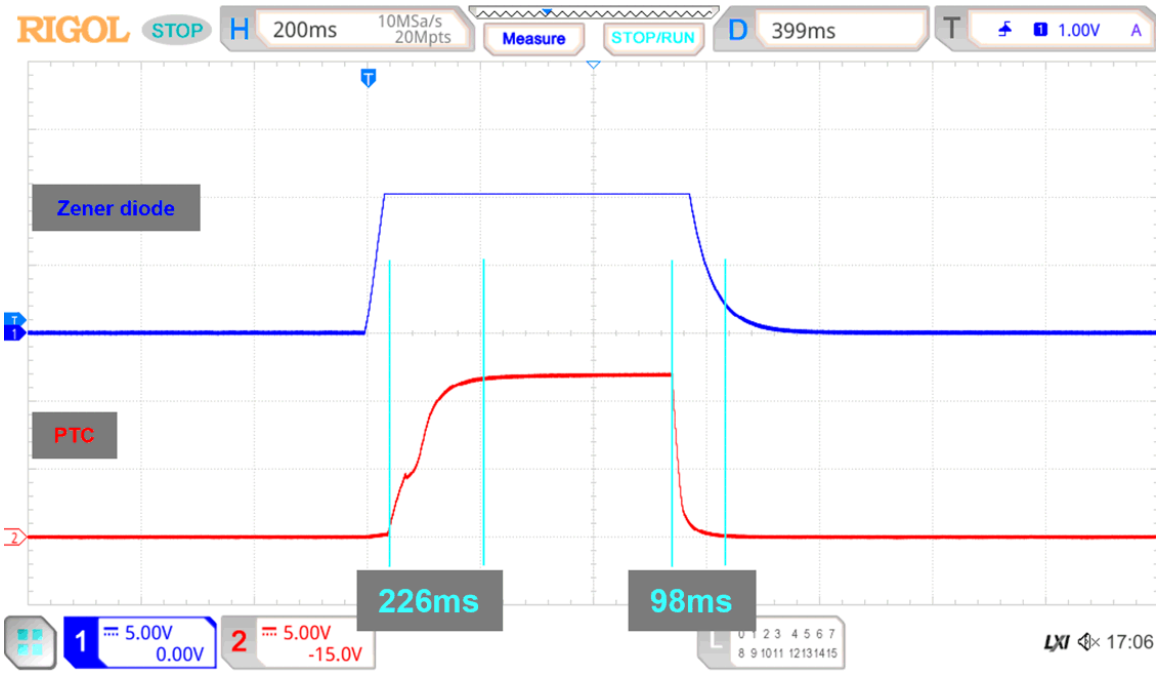


Figure 4-29. Measured Protection Response in Current Input Mode with 24V Overvoltage

Figure 4-30. Measured Protection Response in Current Input Mode with 30V Overvoltage

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010237.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010237.

5.1.3 PCB Layout Recommendations

To download the PCB layout, see the design files at TIDA-010237.

5.1.3.1 Layout Prints

5.2 Tools and Software

5.2.1 Tools

5.2.2 Software

5.3 Documentation Support

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

Trademarks

TI E2E™ is a trademark of Texas Instruments.
Vötsch™ is a trademark of Weiss Technik GmbH.
All trademarks are the property of their respective owners.

6 Revision History

DATE	REVISION	NOTES
May 2026	*	Initial Release

7 About the Author

DONNA XU is a systems engineer at Texas Instruments, where she develops reference designs for industrial applications. She has experience in industrial automation applications, with a focus on PLC I/O modules. She earned her master's degree in electronic information from Fudan University.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025