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| Texas Instruments, Inc. |
| DLPC471TP/DLPC471TE – HSSI Modelling Documentation |
| IBIS and s-parameter/HSPICE models |
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| **8/30/2019** |

The DLPC471TP and DLPC471TE are modelled in two parts. The lower speed digital pins are simulated by means of an IBIS model. The high speed serial interface (HSSI) pins are modelled by means of package s-parameter models and silicon termination HSPICE models. The models are listed below.

DLPC471TP S317

dlpc471tp\_s317.ibs - digital pin IBIS model for the DLPC471TP

dlpc471tp\_s317\_macroA.s36p – S317 package s-parameter model for HSSI macro A interface

dlpc471tp\_s317\_macroB.s36p – S317 package s-parameter model for HSSI macro B interface

rx\_afe\_clocklane\_model\_nom.hsp – nominal HSSI clocklane receiver HSPICE model

rx\_afe\_clocklane\_model\_low.hsp – low termination resistance and fast silicon corner HSSI clocklane receiver HSPICE model

rx\_afe\_clocklane\_model\_high.hsp – high termination resistance and slow silicon corner HSSI clocklane receiver HSPICE model

rx\_afe\_datalane\_model\_nom.hsp – nominal HSSI datalane receiver HSPICE model

rx\_afe\_datalane\_model\_low.hsp – low termination resistance and fast silicon corner HSSI datalane receiver HSPICE model

rx\_afe\_datalane\_model\_high.hsp – high termination resistance and slow silicon corner HSSI datalane receiver HSPICE model

DLPC471E S451

dlpc471te\_s451.ibs - digital pin IBIS model for the DLPC471TE

dlpc471te\_s451\_macroA.s36p – S451 package s-parameter model for HSSI macro A interface

dlpc471te\_s451\_macroB.s36p – S451 package s-parameter model for HSSI macro B interface

rx\_afe\_clocklane\_model\_nom.hsp – nominal HSSI clocklane receiver HSPICE model

rx\_afe\_clocklane\_model\_low.hsp – low termination resistance and fast silicon corner HSSI clocklane receiver HSPICE model

rx\_afe\_clocklane\_model\_high.hsp – high termination resistance and slow silicon corner HSSI clocklane receiver HSPICE model

rx\_afe\_datalane\_model\_nom.hsp – nominal HSSI datalane receiver HSPICE model

rx\_afe\_datalane\_model\_low.hsp – low termination resistance and fast silicon corner HSSI datalane receiver HSPICE model

rx\_afe\_datalane\_model\_high.hsp – high termination resistance and slow silicon corner HSSI datalane receiver HSPICE model

The recommended simulation tool is ADS. Within ADS, the above models can be imported for use in the system simulation. The HSSI interface should be connected as below. The boxes on the left would include the driver model plus the interconnect models from the driver to the receiver. These models will input to the package s-parameter model on the LA/PGA side. The package s-parameter model “DIE” side then interfaces with the corresponding HSPICE models, whose port names are shown on the right.



For questions concerning ADS with how to import a netlist or s-parameter, please see the following documentation on Keysights’ website.

<https://edadocs.software.keysight.com/ads2020/input-output/data-input-output/netlist-translator-for-spice/importing-a-netlist-file>

<https://edadocs.software.keysight.com/ads2020/components/components-analog-rf/introduction-to-circuit-components/data-file-components/snp-n-port-s-parameter-file>