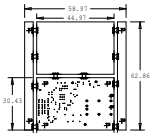
REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

FABRICATION NOTES:

1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012D, CLASS 2; PER IPC-6011.
2. MATERIALS:
   1. LAMINATE AND PREPREG (B-STAGE) TO BE IS ACCORDANCE WITH IPC-4101/126. (MIN.TG 170) FR4 HIGH Tg for Core and Prepreg.
   2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150. UNLESS OTHERWISE SPECIFIED, ALL COPPER WEIGHT FOR INNER SIGNAL LAYERS AND INNER PLANE LAYERS TO BE 1OUM (0.5OZ.). FOR OUTER LAYERS 52UM (1.5OZ). COPPER WEIGHT IS TO BE CONSIDERED "FINISHED". THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.150MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. BOARD FINISHED SHALL BE ACCORDING TO IPC-6012D CLASS 2.
7. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
8. FINISH:
   1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
   2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK. ONLY SOLDER MASK IMAGES THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE GREEN.
   3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON EXPOSED COPPER OR SOLDER PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
   4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 200M [0.0007"].
   5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLIANCE TO IPC6012, CLASS 2.
9. MARKING:
   1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
10. TEST REQUIREMENTS:
   1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
11. THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
12. TEAR DROPS SHALL BE ADDED ON VIA'S AND THROUGH HOLE PADS IN ALL INTERNAL AND OUTER LAYERS.
13. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IF REQUIRED.
14. FINISHED PCB THICKNESS SHALL BE 0.062" +/-10%.
15. MIN TRACE WIDTH/SPACING ON BOARD IS 0.003"/3.004".



DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	8.0	+3.0/-3.0	PLATED	122
•	40.0	+2.0/-2.0	PLATED	8
•	48.0	+3.0/-3.0	PLATED	3
•	32.0	+3.0/-3.0	NON-PLATED	65
⌀	80.0	+3.0/-3.0	NON-PLATED	2
⌀	108.0	+3.0/-3.0	NON-PLATED	8

TEXAS INSTRUMENTS

LAYER STACKUP

LAYER NAME	FINISHED Cu	X-SECTION	DIELECTRIC THICKNESS [INCHES]
PRIMARY SIDE SILKSCREEN			
PRIMARY SIDE SOLDERMASK			
L01 PRIMARY SIDE	1.0oz.		0.0037
L02 GROUND-PLANE-1	1.0oz.		0.004
L03 INNER-SIGNAL-1	1.0oz.		0.038
L04 INNER-SIGNAL-2	1.0oz.		0.004
L05 POWER-PLANE-1	1.0oz.		0.0037
L06 SECONDARY SIDE	1.0oz.		
SECONDARY SIDE SOLDERMASK			
SECONDARY SIDE SILKSCREEN			

IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	MICROSTRIP	L1,L6	5.5	NA	50	L2,L5
02	EDGE COUPLED MICROSTRIP	L1	5.5	5.5	100	L2
03	SUBPLANE	L2,L4	5.2	NA	50	L3,L5

SIGNATURES		DATE
LAYOUT BY	RK	140423
REVIEWED BY	SA	140423
APPROVED BY	ANS	140423

TEXAS INSTRUMENTS

PROC16E1

AM263P AUTOMOTIVE ICSSM ADDON BOARD

SIZE D | Rev B1

SCALE: NONE | SHEET 1 OF 13