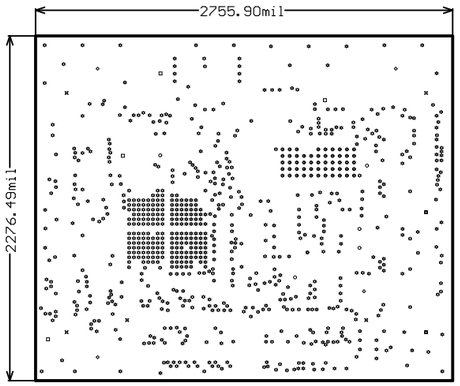
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
◎	54	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	+/-3.00mil
✡	778	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	+/-3.00mil
□	4	37.99mil (0.965mm)	PTH	Round	Top Layer - Bottom Layer	
○	5	37.99mil (0.965mm)	PTH	Round	Top Layer - Bottom Layer	+/-3.00mil
⊠	5	40.00mil (1.016mm)	NPTH	Round	Top Layer - Bottom Layer	+/-3.00mil
▣	2	40.16mil (1.020mm)	NPTH	Round	Top Layer - Bottom Layer	+/-3.00mil
◇	4	159.00mil (4.039mm)	NPTH	Round	Top Layer - Bottom Layer	+/-3.00mil
	852 Total					

SCALE : NTS

NOTES:

1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
2. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING/COVERING" REQUIREMENTS.
3. MANUFACTURER'S IDENTIFICATION,DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
4. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-5 MIL.
5. REFER IMPEDANCE TABLE FOR IMPEDANCE CONTROL TRACES ON LAYER 1, 3, 5 , 8 & 10.
6. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS OTHERWISE SOLDER MASK OPENED IN GERBER.



IMPEDANCE TABLE :

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	5.66 MILS	-	50 OHM	LAYER-2 (GND LAYER)
L3	4.5 MILS	-	50 OHM	LAYER-2 / LAYER-4
L3	3.5 MILS	6.7 MILS	100 OHM	LAYER-2 / LAYER-4
L5	4.0 MILS	-	50 OHM	LAYER-4/LAYER-6
L8	4.5 MILS	-	50 OHM	LAYER-7/LAYER-9
L8	3.5 MILS	6.7 MILS	100 OHM	LAYER-7/LAYER-9
BOTTOM	5.66 MILS	-	50 OHM	LAYER-9(GND LAYER)
BOTTOM	3.7 MILS	7.3 MILS	100 OHM	LAYER-9(GND LAYER)

LAYER STACK-UP :

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.50mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR-4	3.70mil	4	
2	LO2_GND1		1.40mil		
	Dielectric 2	FR-4	5.00mil	4	
3	LO3_SIG1		1.40mil		
	Dielectric 3	FR-4	7.00mil	4	
4	LO4_GND2		1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LO5_SIG2		1.40mil		
	Dielectric 5	FR-4	7.00mil	4	
6	LO6_PWR		1.40mil		
	Dielectric 6	FR-4	4.00mil	4	
7	LO7_GND3		1.40mil		
	Dielectric 7	FR-4	7.00mil	4	
8	LO8_SIG3		1.40mil		
	Dielectric 8	FR-4	5.00mil	4	
9	LO9_GND4		1.40mil		
	Dielectric 9	FR-4	3.70mil	4	
10	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.50mil	3.5	
	Bottom Overlay				
Total board thickness:			61.40mil		

DESIGN INFORMATION

MIN. TRACK WIDTH: 3.5MIL
MIN. CLEARANCE: 4 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☐ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER
☐ MATTE ☒ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV
☐ OTHER
ARRAY/PANEL: ☒ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☐ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
BARE BOARD ELEC. TEST: ☐ NONE ☐ REQUIRED ☒ PER ORDER

☐ OUTER LAYERS 6 MIL WIDE, 6 MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE
☐ INNER LAYERS 5 MIL WIDE, 7 MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE
☐ OUTER LAYERS 6.1 MIL WIDE, 6 MIL SPACE TRACES REQUIRE 90 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: F29H85x controlSOM EVM
DESIGNED FOR: Public Release
FILE NAME: MCU144A.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: MCU144	REV: A	SVN REV: Not in version control
LAYER NAME = ~~M2 Sheet Drawing~~ Dimensions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 11/4/2024 11:15:30 AM		TEXAS INSTRUMENTS

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ENGINEER:	LAYOUT BY:
Gustavo Martinez	Krypton Solutions
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.3.1.35