TMDSCSK388

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REV	REV B
VER	3.0

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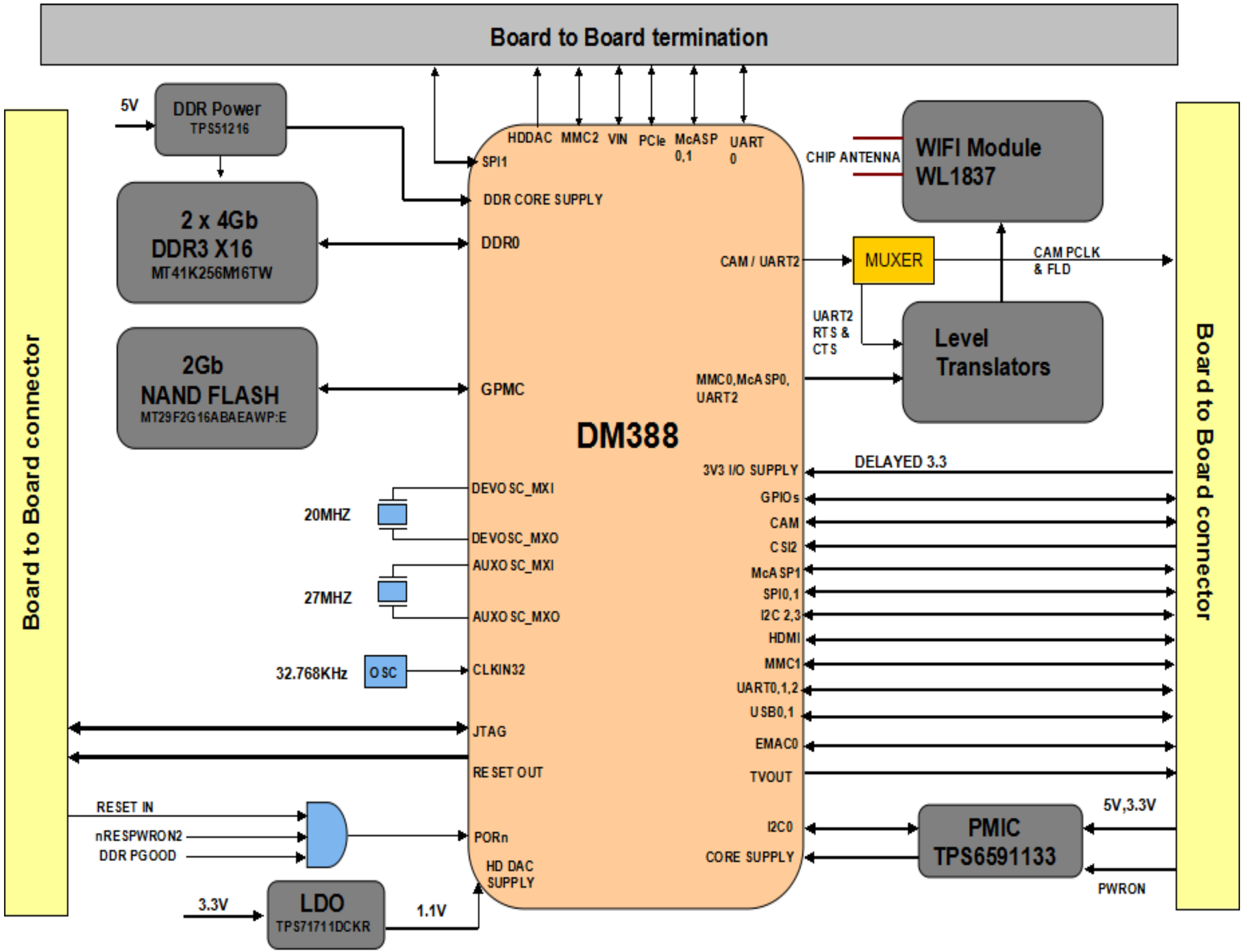
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	22nd SEP 2016	REVA Change List implemented Baselined for REVB	Mistral Design Team	AJIT MB	AJIT MB
0.2	4th NOV 2016	I2C0 SDA and I2C0 SCL lines to PMIC updated	Mistral Design Team	AJIT MB	AJIT MB
1.0	8th NOV 2016	Baselined	Mistral Design Team	AJIT MB	AJIT MB
1.1	6th JAN 2017	SD card Part# added to hardware schematics page	Mistral Design Team	AJIT MB	AJIT MB
2.0	6th JAN 2017	Baselined	Mistral Design Team	AJIT MB	AJIT MB
2.1	13th JAN 2017	Renamed the Schematics from PRDN_REVA to REV B	Mistral Design Team	AJIT MB	AJIT MB
3.0	13th JAN 2017	Baselined	Mistral Design Team	AJIT MB	AJIT MB

BLOCK DIAGRAM



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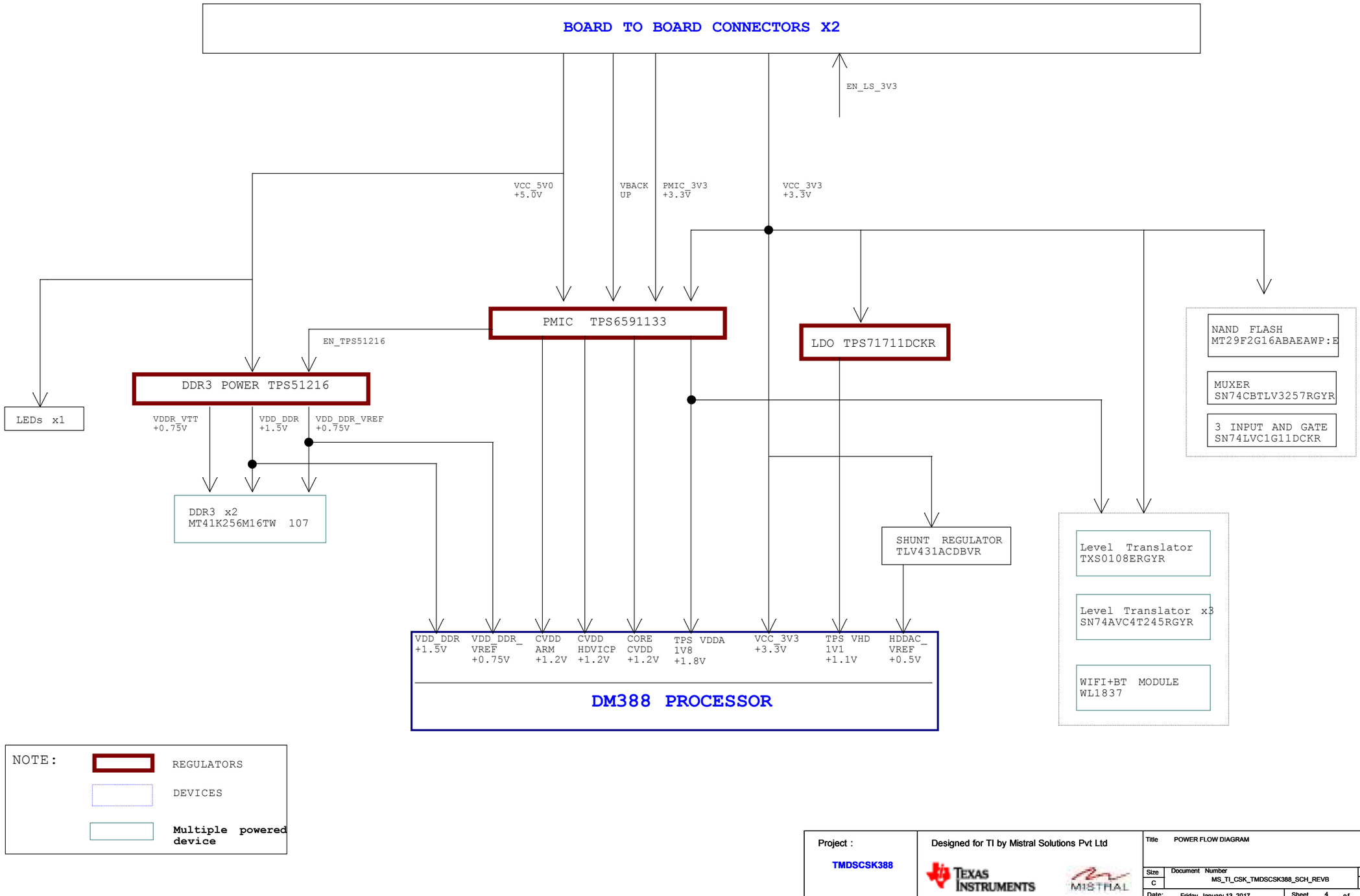
POWER FLOW DIAGRAM



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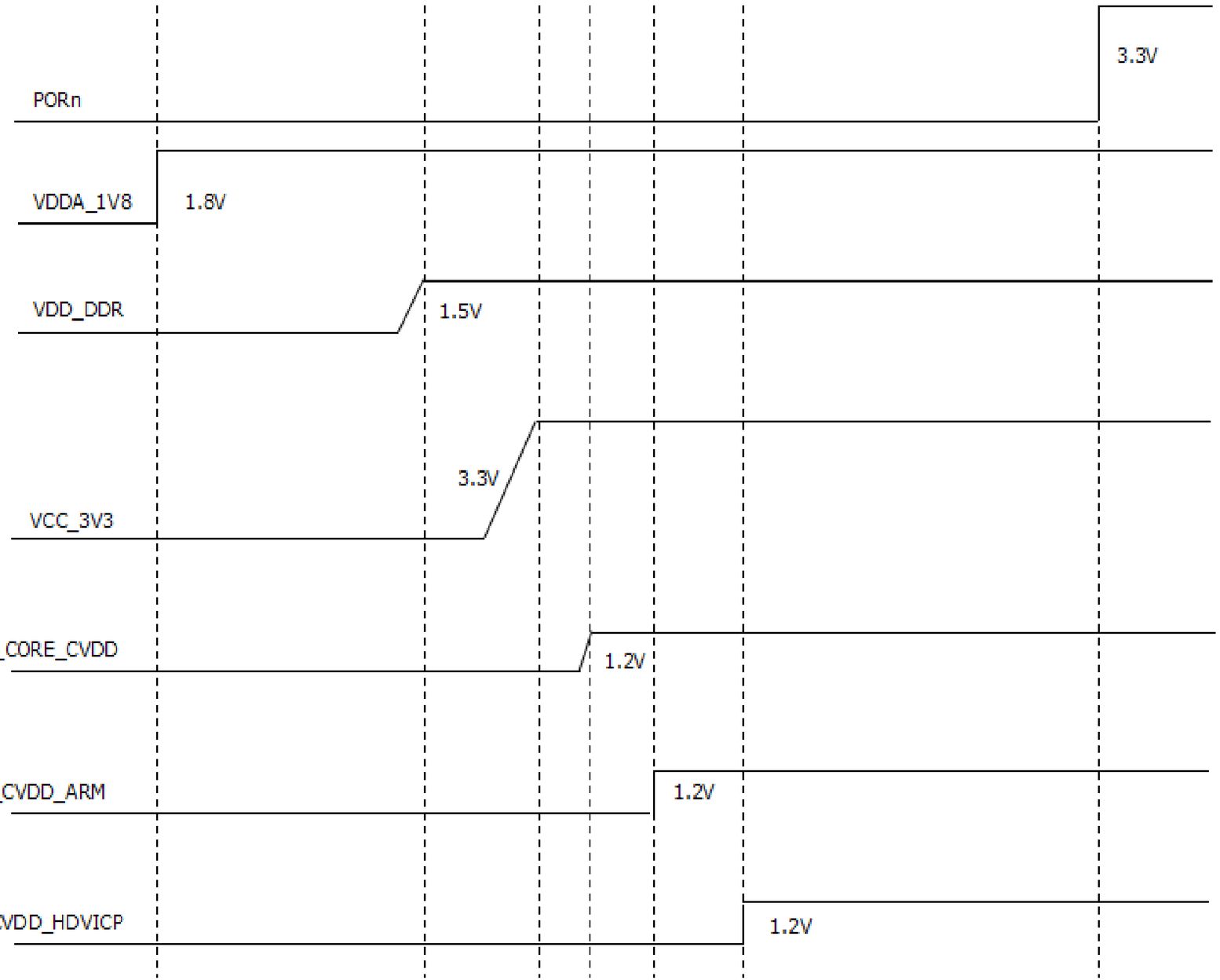
POWER UP SEQUENCE



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POWER CALCULATION

DM388_SOM											
Part Number	QTY	CVDD (CORE_CVDD)	CVDD_ARM (PMIC VDD1)	CVDD_HDVICP (PMIC VDD2)	VDD_1V8 (PMIC VIO)	TPS51216 (VCC_1V5)	TPS71711DCKR (TPS VHD 1V1)	VCC_3V3 (Carrier Card)	DDR_VTT 0.75	PMIC_3V3	VCC_5V0
TMS320DM388	1	1125.00	365.00	0.00	53.00	402.00	150.00	139.00		382.6968984	
DDR3(MT41K256M16TW)	2					520			272		
MT29F4G16ABAEAWP	1							30			
TXS0108EPWR	2				0.036	0.036		0.108			
WL1837MOD	1							909.0909091			
SN74AVC4T245RGYR	3				300			300			
SN74LVC1G11DCKR	1							100			
SN74CBTLV3257RGYR	1							128			
LED	1										3
Total (mA)		1125	365	0	353.036	922.036		1606.198909	272	382.6968984	320.6470588
Input voltage		5	3.3	3.3	3.3	5	3.3	5	1.5	5	5
Efficiency		0.85	0.85	0.8	0.85	0.8		0.85	0.85	0.85	0.75
Quiescent current (mA)											
Output Voltage		1.2	1.2	1.2	1.8	1.5	1.1	3.3	0.75	3.3	3.3
Current Drawn from Input		**317.6470588**	**156.1497326**	**0**	**226.5471658**	**345.7635**	**150**	**1247.166212**	**160**	**297.1528858**	**504**
Current Drawn from VCC_5V0 (mA)	**2210.729656**										

Project :

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Title POWER CALCULATION

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GPIO TABLE

GPIO NAME	PROCESSOR PIN	PURPOSE	Internal/ External PU/PD states
TPS_INT1	NMI	NMIn interrupt from PMIC to DM388 processor	INTERNAL PU
DM388_GPMC_WPn	GP1[26]	WRITE PROTECT TO NAND FLASH	EXTERNAL PU
DM388_WLAN_IRQ	GP1[13]	INTERRUPT FROM WL1837 MOD	EXTERNAL PU
DM388_WLAN_EN	GP2[6]	WLAN ENABLE SIGNAL TO WIFI MODULE (WL1837)	INTERNAL PD
DM388_BT_EN	GP2[5]	BLUETOOTH ENABLE SIGNAL TO WIFI MODULE (WL1837)	INTERNAL PD
DM388_TPS_SLEEP	GP1[15]	PMIC SLEEP INPUT	INTERNAL PU
DM388_MUX_SEL	GP1[16]	SELECTION SIGNAL TO CAMERA & UART MUXER	EXTERNAL PD
ENET_RSTn	GP3[20]	ETHERNET RESET	INTERNAL PU
DM388_MMC1_DAT6 /GP0_I2	GP0[12]	KEYPAD	INTERNAL PU
DM388_MMC1_DAT7 /GP0_I3	GP0[13]	KEYPAD	INTERNAL PU
DM388_GP1[10]	GP1[10]	KEYPAD	INTERNAL PD
DM388_McASP0_AXR5	MCA[0]_AXR[5]	KEYPAD	INTERNAL PD
DM388_GP3[3]	GP3[3]	LED	INTERNAL PD
DM388_GP0[9]	GP0[9]	LED	INTERNAL PD
DM388_GP1[24]	GP1[24]	LED	INTERNAL PU
DM388_GP1[25]	GP1[25]	LED	INTERNAL PU
DM388_GP1[30]	GP1[30]	LED	INTERNAL PD

I2C ADDRESS TABLE

MASTER	I2C USED	SLAVE DEVICE	ADDRESS
DM388 PROCESSOR	I2C0	PMIC	0x2D (General Purpose)
	I2C2	Camera Module	0x10 (Camera Sensor)
			0x2D (LVDS module)
		Audio Codec (TLV320AIC3104)	0x18

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Title: GPIO & I2C ADDRESS TABLE

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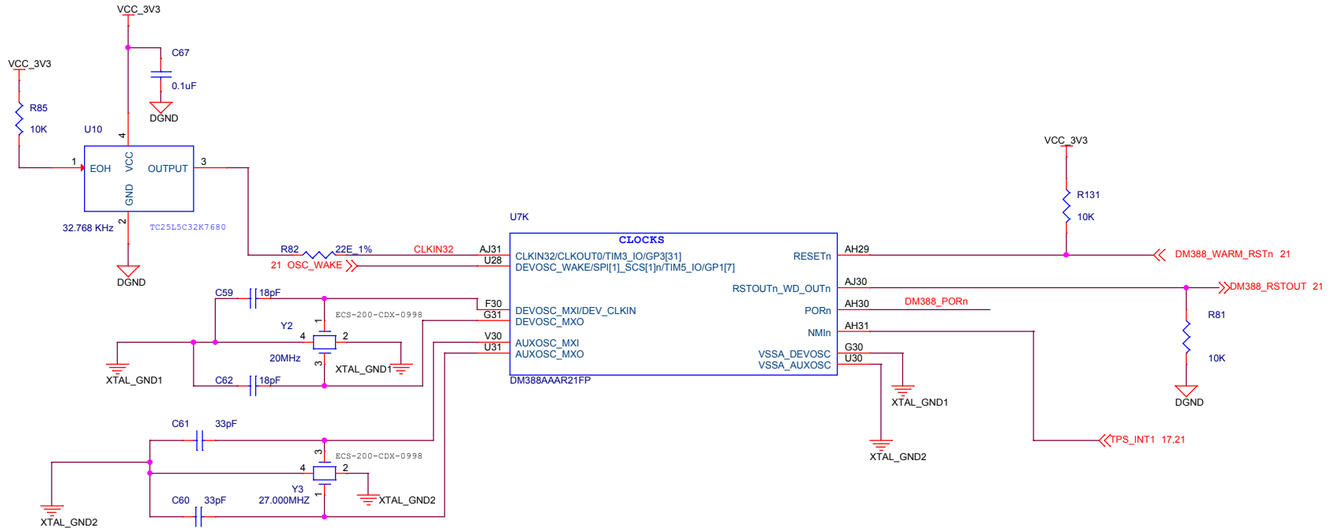
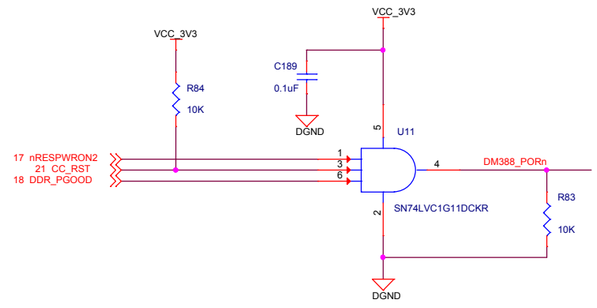
CLOCKS AND RESET





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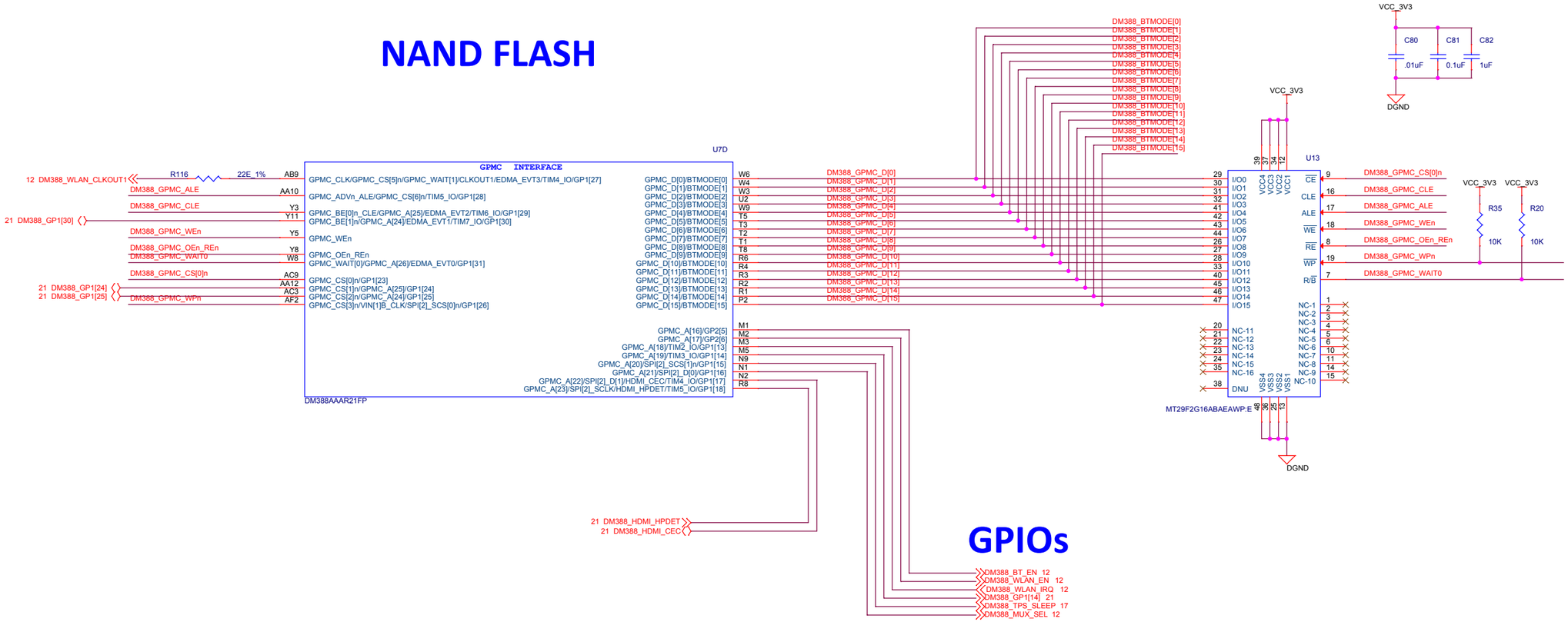
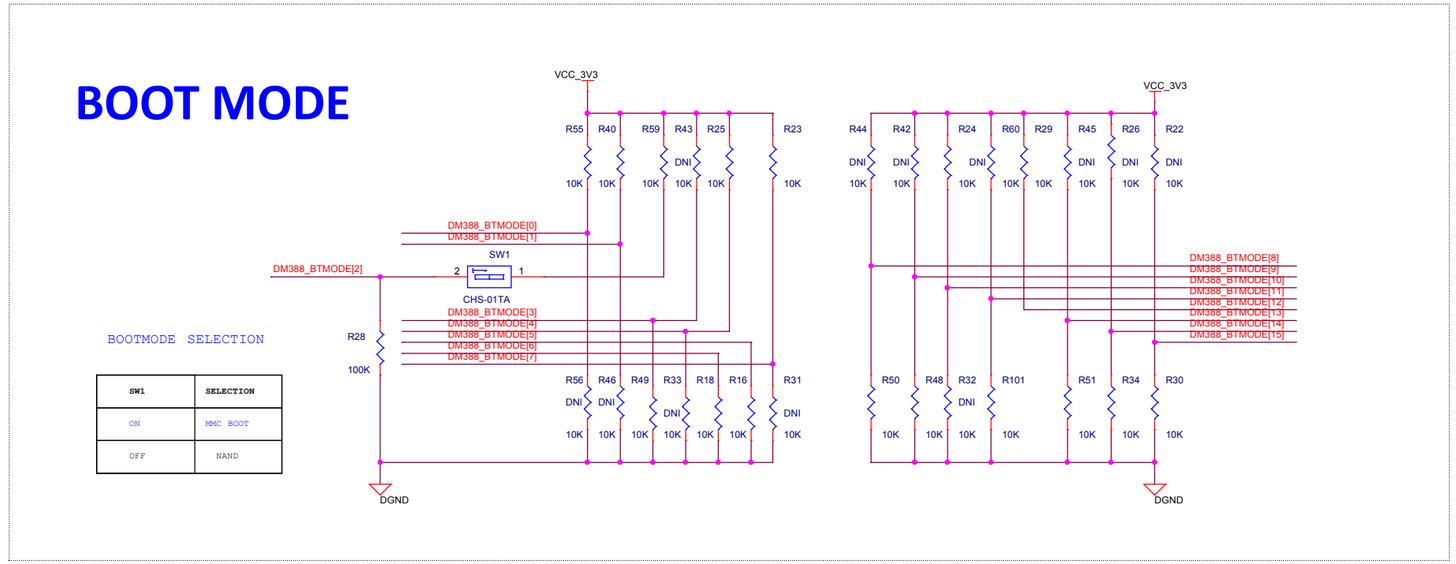
NAND FLASH



BOOT MODE



BOOTMODE TABLE

BOOTMODE PIN	DEFAULT SETTING	DESCRIPTION
BTMODE15	0	GPMC CS0 Wait disabled
BTMODE14	0	GPMC CS0 Address/Data not muxed
BTMODE13	0	
BTMODE12	1	GPMC CS0 16bit Data bus
BTMODE11	0	RSTOUT is asserted when a Watchdog Timer reset, POR, RESET, or Emulation/ Software-Global Cold/Warm reset occurs
BTMODE10	0	GPMC Option A
BTMODE9	0	MII (GMII) Ethernet PHY Mode
BTMODE8	0	
BTMODE7	1	RGMII Internal delay disabled
BTMODE6	0	RSV
BTMODE5	0	RSV
BTMODE[4:0]	10011	NAND BOOT
	10111	MMC BOOT

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Title: NAND FLASH,BOOTMODE & GPIOs

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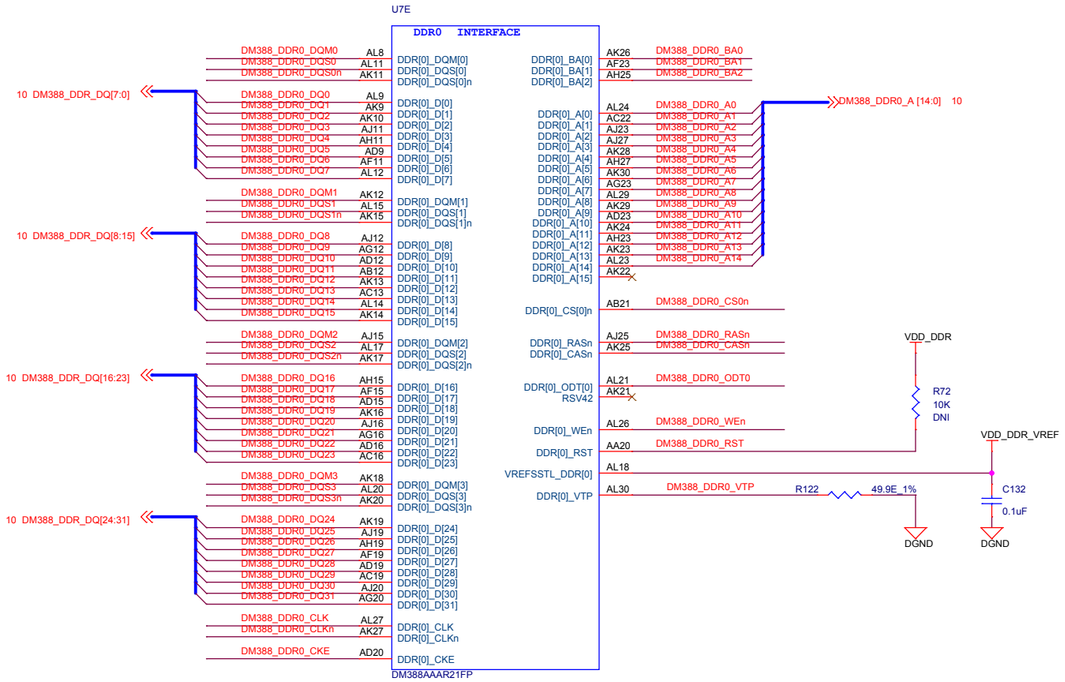
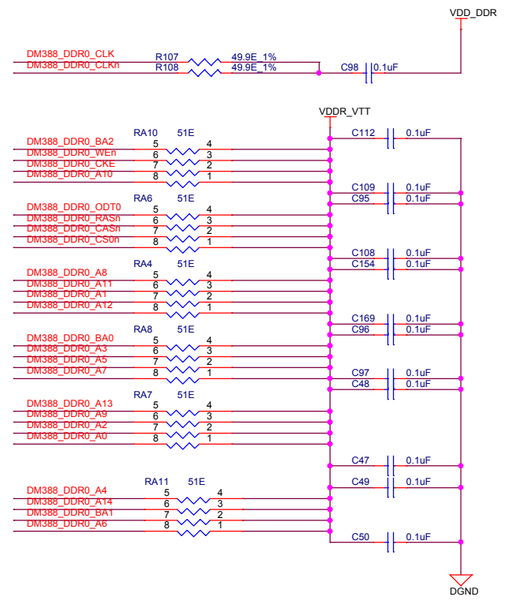
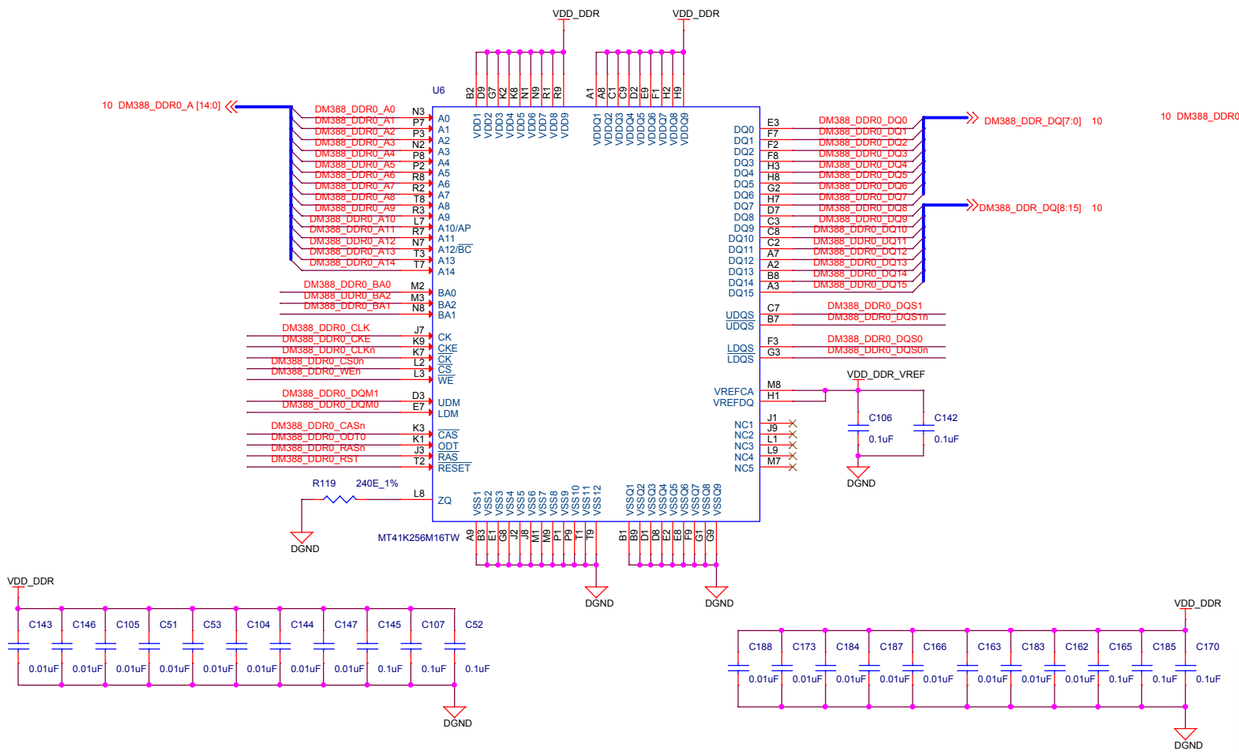
DM388 DDR INTERFACE



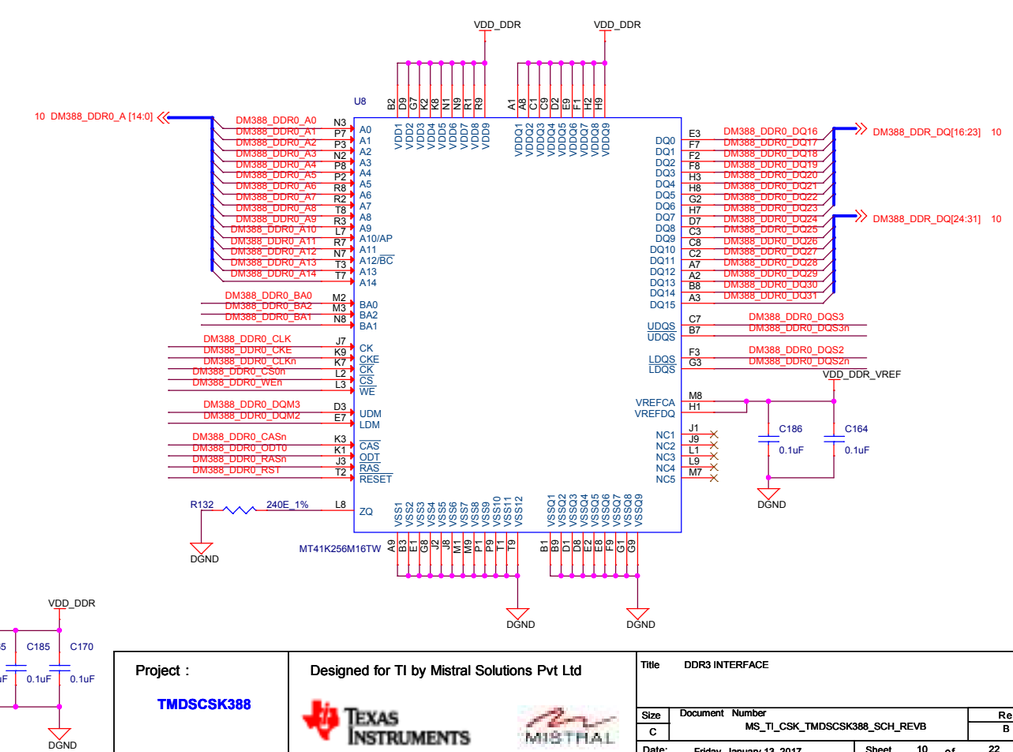
DDR TERMINATION



DDR DEVICE 1



DDR DEVICE 2



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DM388 I/O PERIPHERALS

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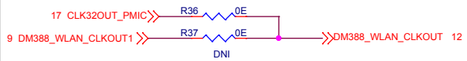
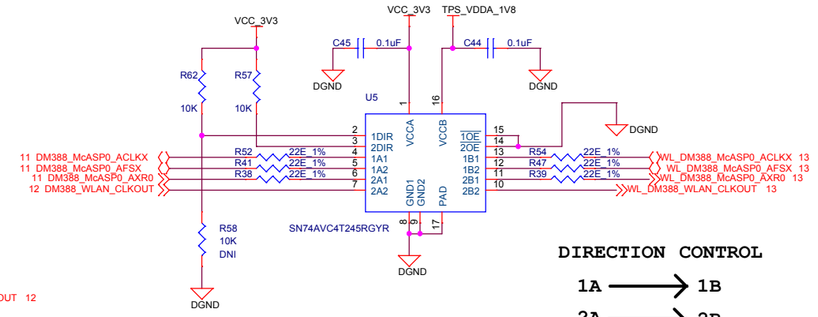
WLAN TRANSLATORS

USE TRIPAD HERE

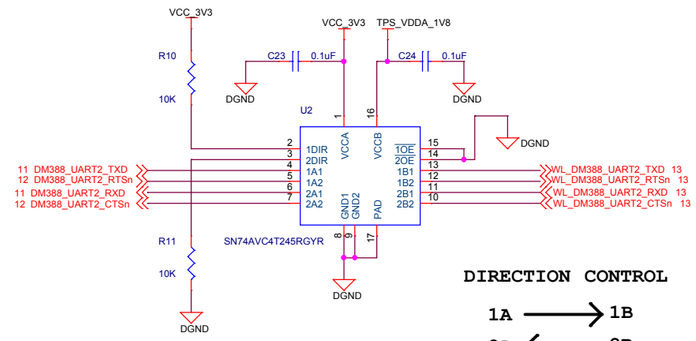




DIRECTION CONTROL

1A ⟶ 1B

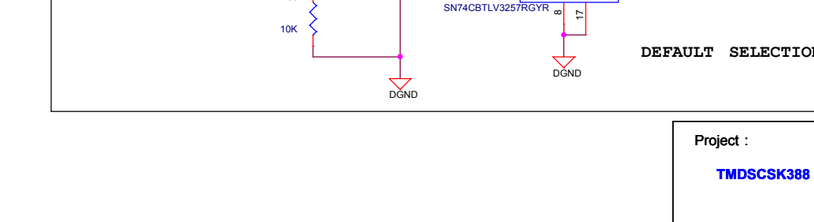
2A ⟶ 2B



DIRECTION CONTROL

1A ⟶ 1B

2A ⟵ 2B



DIRECTION CONTROL

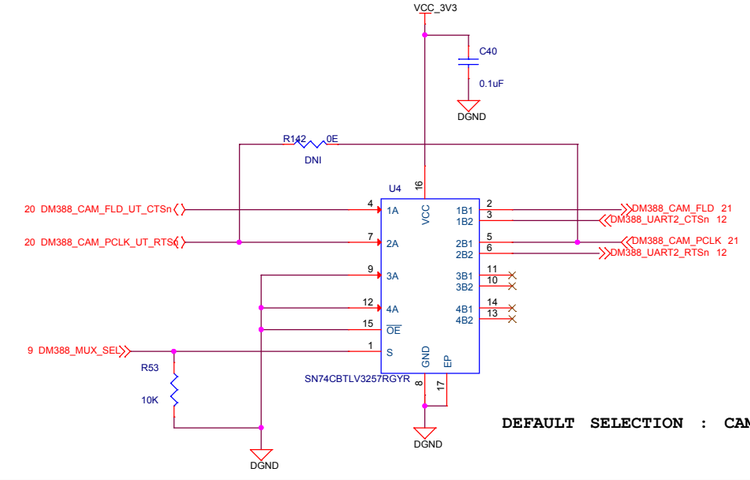
1A ⟶ 1B

2A ⟵ 2B

DIRECTION CONTROL

B ⟷ A

UART & CAM MUXER



DEFAULT SELECTION : CAMERA

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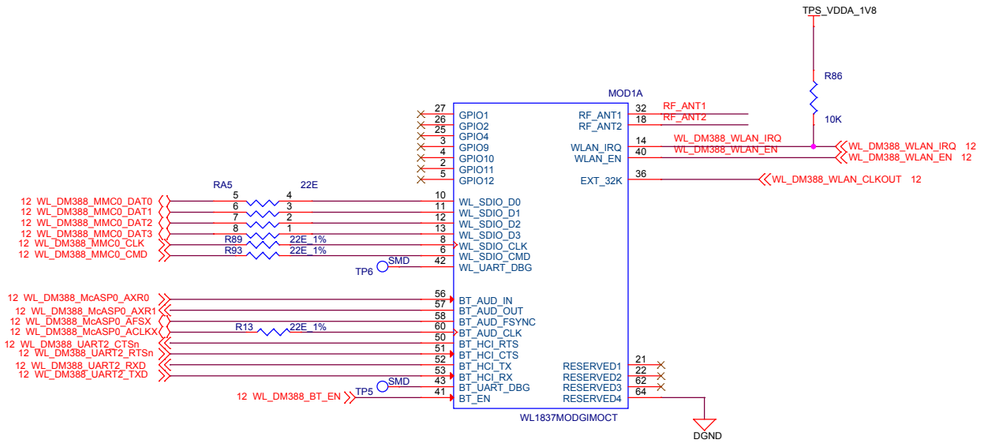
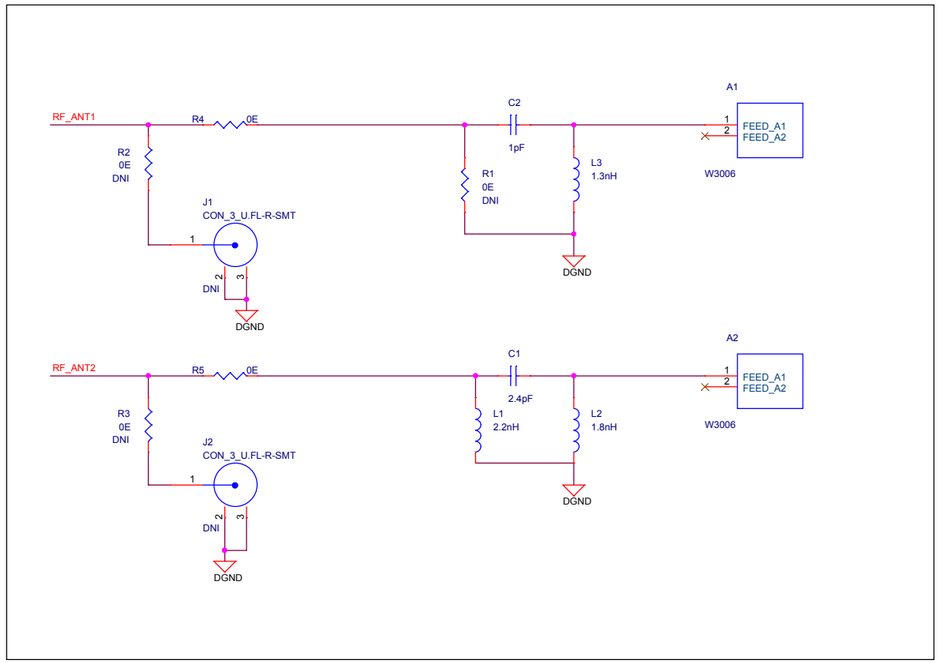
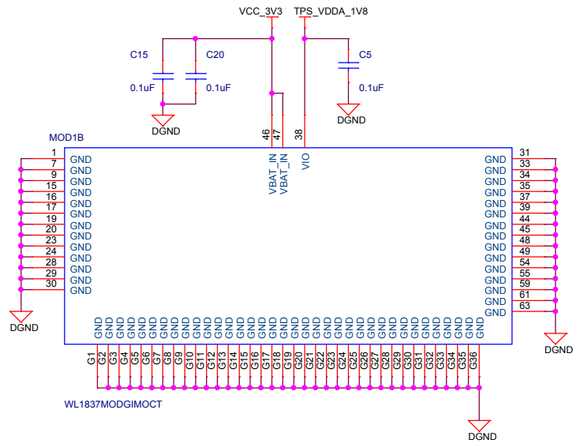
WLAN + BT MODULE







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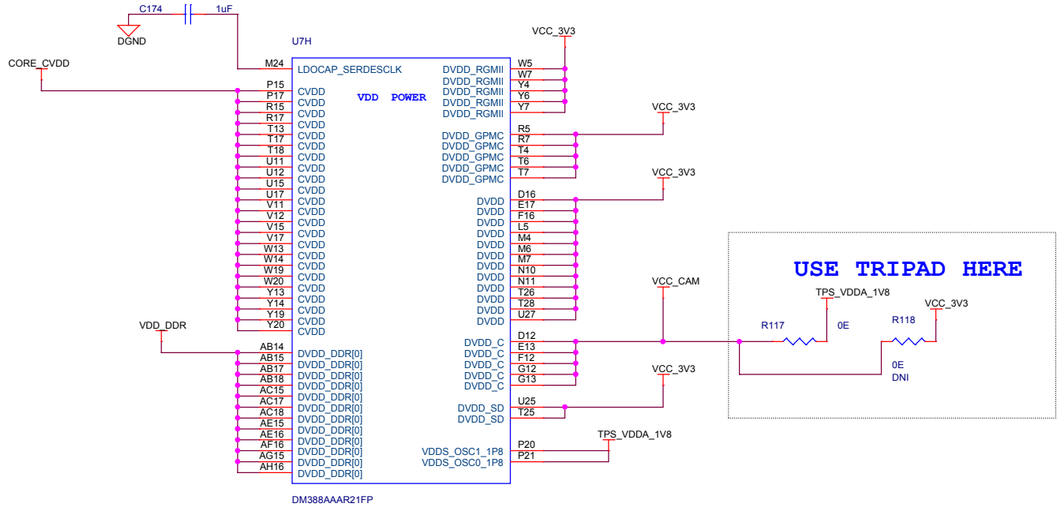
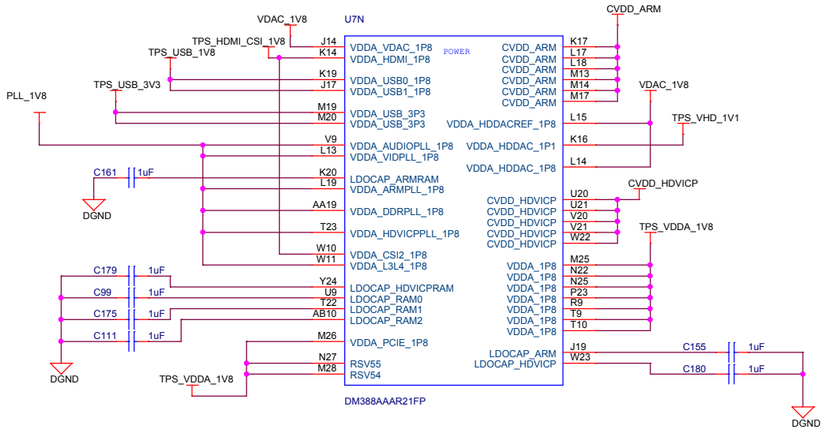
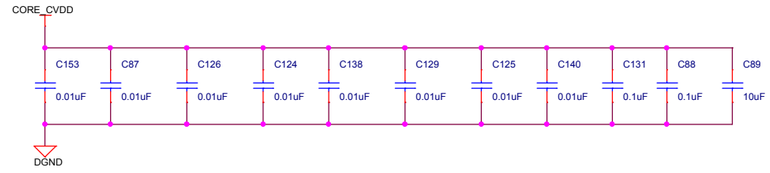
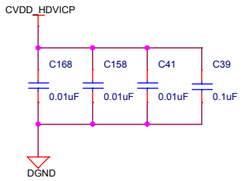
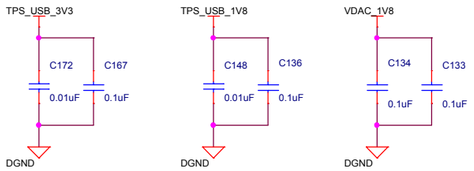
DM388 POWER

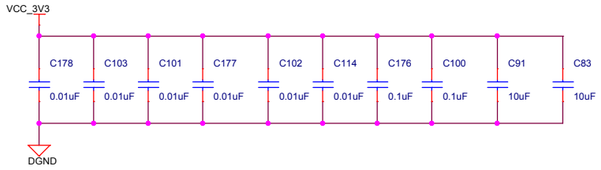


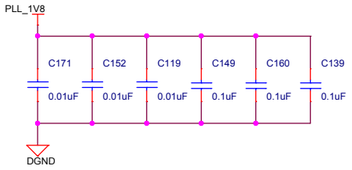


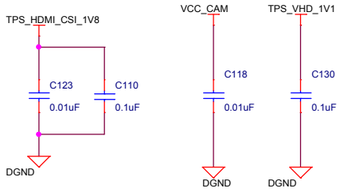


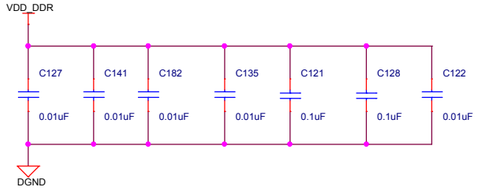


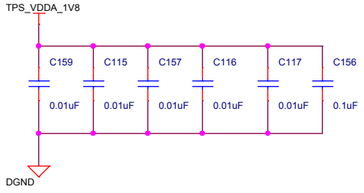


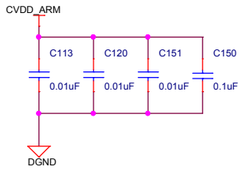












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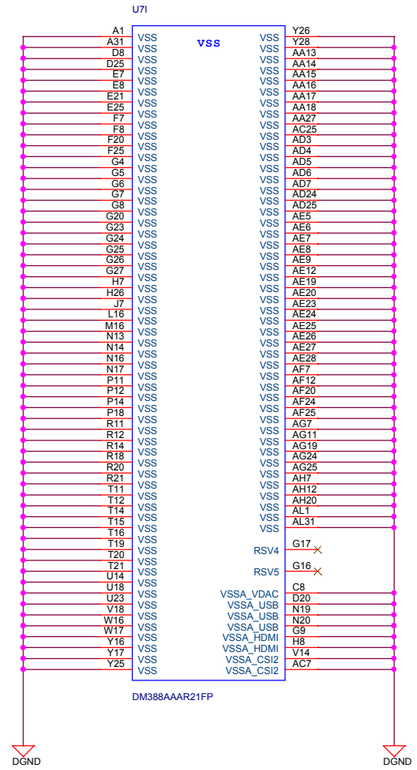
DM388 VSS



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PMIC POWER 1

U1-1

TPS65911XX
BGA

VBACKUP
VCC_5V0
C72 2.2uF DGND
C16 4.7uF DGND
D7 VBACKUP
B6 VCC7
D8 VCC5
L1 VCC4
N3 VCC3
N5 VCC6
E8 VCCS
C6 4.7uF DGND
C78 4.7uF DGND
C22 4.7uF DGND
PMIC_3V3
C74 4.7uF DGND

VRTC B5
LDO3 E7
LDO4 C8
LDO5 K1
LDO8 M1
LDO7 M3
LDO6 M2
LDO1 N6
LDO2 N4
TRAN C6
EN D5
PGOOD C4
DRVH A3
VBST A2
SW A4
DRVL A6
VOUT B4
VFB C5
TRIP B3

TPS_GPIO_3V3
PLL_1V8
TPS_LDO5_3V3
TPS_USB_1V8
TPS_USB_3V3
TPS_LDO6_3V3
TPS_VDAC_1V8
TPS_HDMI_CSI_1V8

DCDC CTRL
External FET range 0.6V/1.45V-6A

C77 0.1uF
C190 0.1uF
R141 100E_0.1%
C75 330pF
R12 100K
GND_DC_DC
0.01uF
C137
DGND

VCC_5V0
C17 1uF
A5 VSIN
A8 GND_CTRL_a
A7 GND_CTRL_b
GND_DC_DC

SMPS

VDD1
Output range 0.6V/1.5V-1.5A
F3 VCC1_a
F2 VCC1_b
E1 VCC1_c
C31 10uF GND_VDD1
PMIC_3V3
D4 VFB1
E2 SW1_a
D2 SW1_b
D1 SW1_c
D3 GND1_a
C2 GND1_b
C1 GND1_c
L6 2.2uH
C25 10uF
C28 0.1uF
GND_VDD1
TPS_CVDD_ARM

VDD2
Output range 0.6V/1.5V-1.5A
G2 VCC2_a
G1 VCC2_b
C32 10uF GND_VDD2
PMIC_3V3
K2 VFB2
H2 SW2_a
H1 SW2_b
J2 GND2_a
J1 GND2_b
L7 2.2uH
C27 10uF
C30 0.1uF
GND_VDD2
TPS_CVDD_HDVICP

VIO
1.5V/1.8V/2.2V/3.3V-1500mA
L8 VCCIO_a
L7 VCCIO_b
N7 VDDIO
C9 10uF GND_VIO
VCC_3V3
H8 VFBIO
K8 SWIO_a
K7 SWIO_b
J8 GNDIO_a
J7 GNDIO_b
L4 2.2uH
C3 10uF
C4 0.1uF
GND_VIO
TPS_VDDA_1V8

GND
DGND_a B2
DGND_b B1
DGND_c A1
AGND_a D6
AGND_b E6
AGND_c E5
AGND_d F5
AGND_e G4
AGND_f H4
AGND_g J3
AGND_h J4
AGND_i J5
AGND_j K3
AGND_k H5
AGND2_a N8
AGND2_b M8
DGND

DGND GND_VIO GND_VDD2 GND_VDD1 GND_DC_DC

Q2 CSD17313Q2
C7 10uF
C13 10uF
C14 10uF
C19 10uF
VCC_5V0
GND_DC_DC
L5 1.5uH
TPS_CORE_CVDD
C12 150uF_6.3V
Q1 CSD17313Q2
CORE_CVDD
GND_DC_DC

TPS_VDAC_1V8 C18 2.2uF DGND
TPS_HDMI_CSI_1V8 C21 2.2uF DGND
TPS_GPIO_3V3 C70 2.2uF DGND
PLL_1V8 C8 2.2uF DGND

TPS_USB_3V3 C79 2.2uF DGND
TPS_USB_1V8 C29 2.2uF DGND
VRTC C73 2.2uF DGND
TPS_LDO5_3V3 C76 2.2uF DGND
TPS_LDO6_3V3 C26 2.2uF DGND

TPS_CVDD_HDVICP — R21 0E — CVDD_HDVICP
TPS_CORE_CVDD — R15 0E — CORE_CVDD
TPS_CVDD_ARM — R17 0E — CVDD_ARM
TPS_VDAC_1V8 — R8 0E — VDAC_1V8

TP15 SMD TPS_VHD_1V1
TP1 SMD TPS_VDDA_1V8
TP3 SMD TPS_CORE_CVDD
TP11 SMD TPS_CVDD_ARM
TP7 SMD TPS_VDAC_1V8

1.1V GENERATION FOR HD DAC

VCC_3V3
C181 1uF DGND
U9 TPS71711DCKR
IN 1 OUT 5
EN 3 NR/FB 4
GND 2
C57 1nF
TPS_VHD_1V1
C58 1uF DGND

Project : TMDSCSK388	Designed for TI by Mistral Solutions Pvt Ltd	Title: PMIC POWER 1	
		Size: C	Document Number: MS_TI_CSK_TMDSCSK388_SCH_REVB — Rev: B
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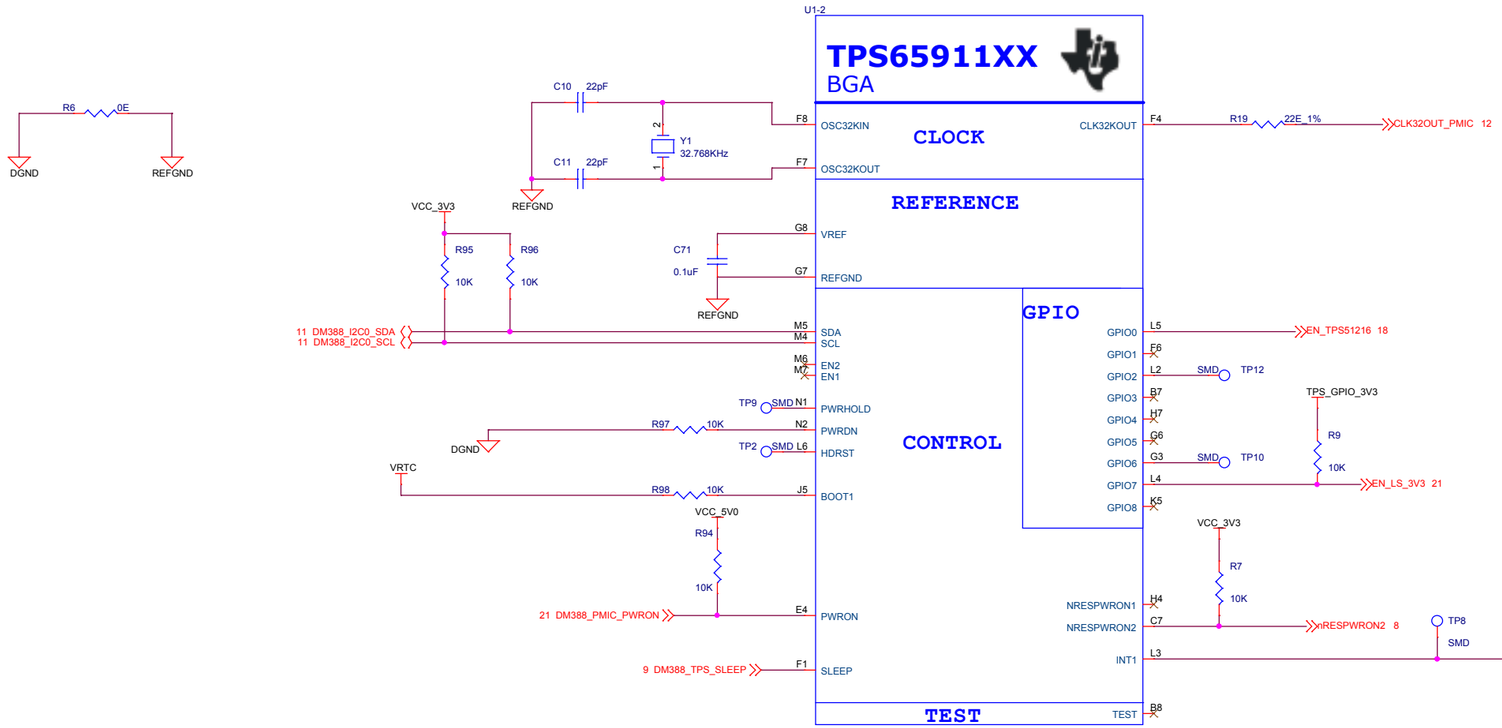
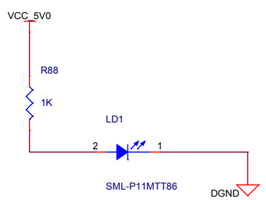
PMIC POWER 2

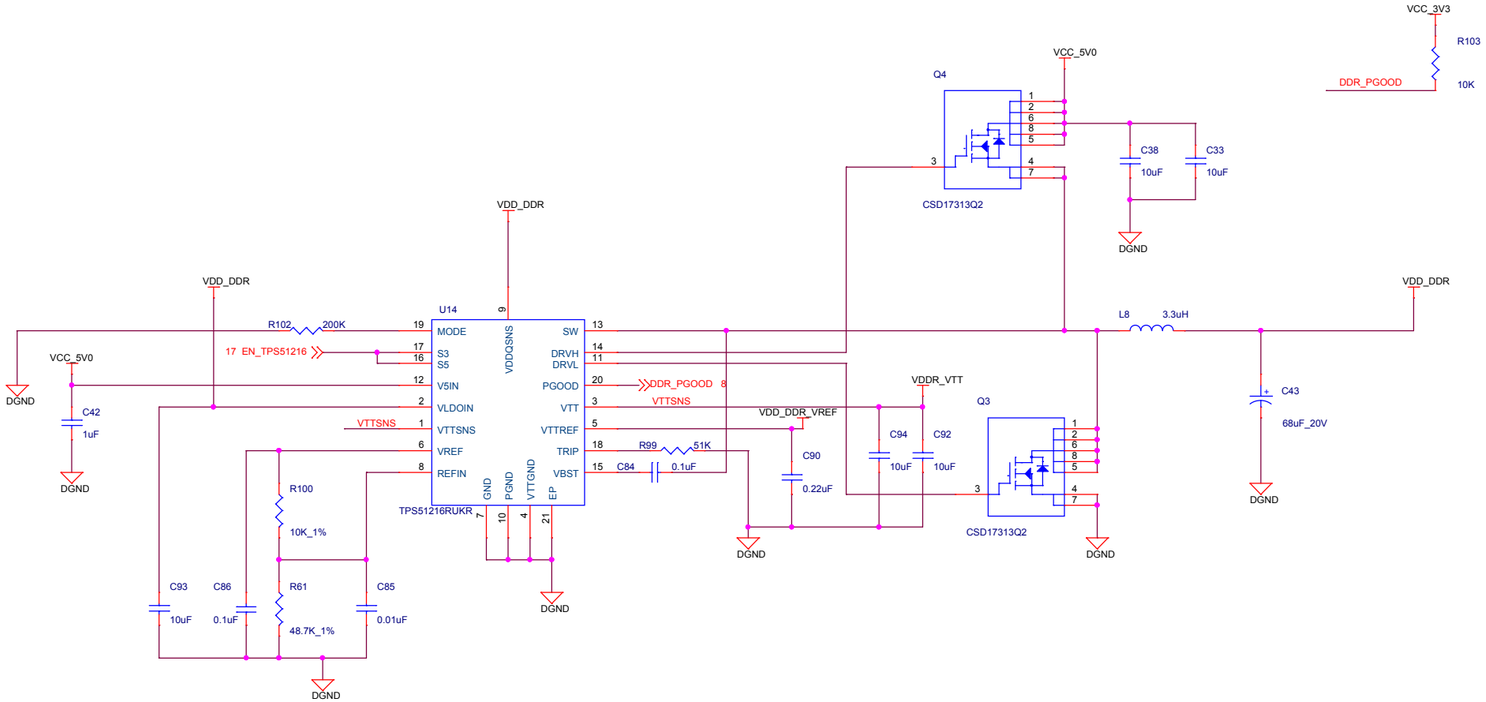


POWER INDICATION



Project : TMDSCSK388	Designed for TI by Mistral Solutions Pvt Ltd	Title: PMIC POWER 2
		Size: C — Document Number: MS_TI_CSK_TMDSCSK388_SCH_REVB — Rev: B
		Date: Friday, January 13, 2017 — Sheet 17 of 22

DDR3 POWER



Project : TMDSCSK388	Designed for TI by Mistral Solutions Pvt Ltd	Title: DDR3 POWER
		Size: C — Document Number: MS_TI_CSK_TMDSCSK388_SCH_REVB — Rev: B
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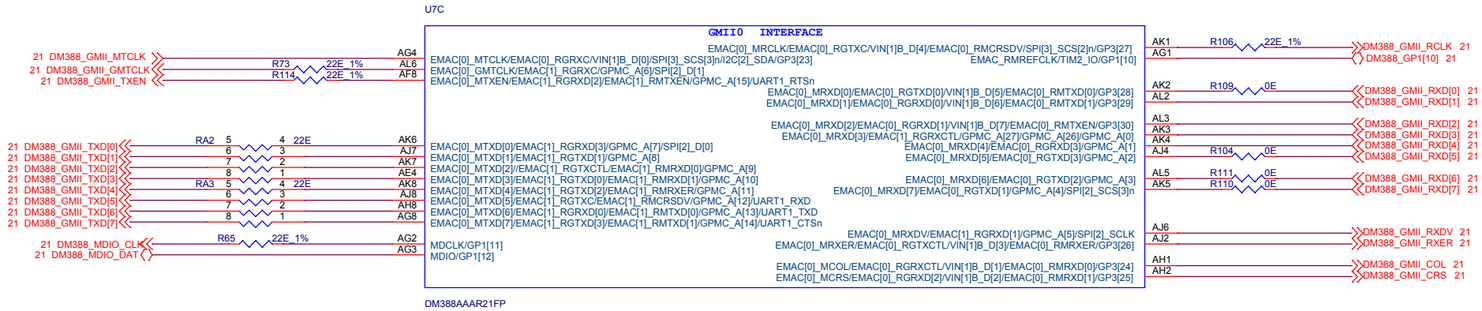
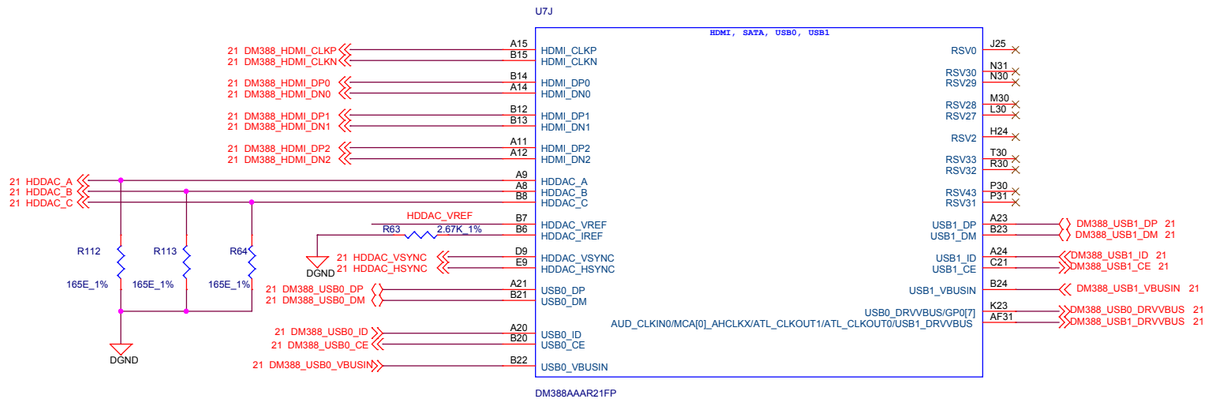
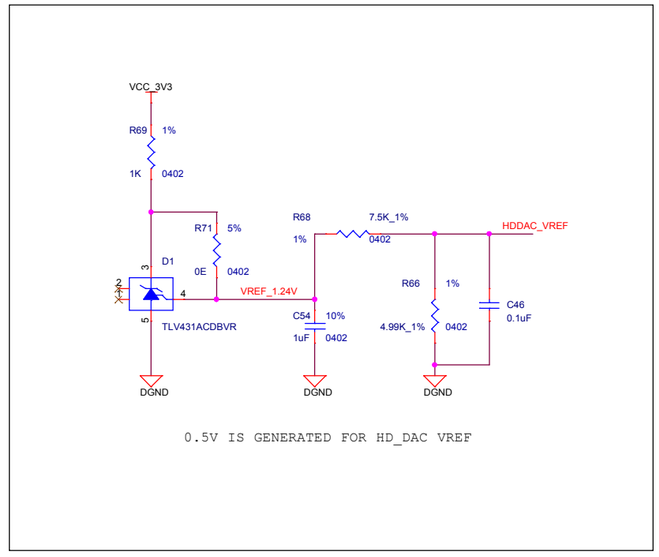
ETHERNET



HDMI & USB





Project : TMDSCSK388	Designed for TI by Mistral Solutions Pvt Ltd	Title: ETHERNET,HDMI & USB
		Size: C — Document Number: MS_TI_CSK_TMDSCSK388_SCH_REVB — Rev: B
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CAMERA

U7G

VIN0,VOUT0,VOUT1

21 DM388_VIN[0]A_CLK	C9	VIN[0]A_CLK/GP2[2]
21 DM388_VIN[0]B_CLK	H12	VIN[0]B_CLK/CLKOUT0/GP1[9]
21 DM388_VIN[0]A_FLD	J13	VIN[0]A_FLD/VIN[0]B_VSYNC/I2C[2]_SCL/GP2[1]
21 DM388_VIN[0]A_DE	C12	VIN[0]A_DE/VIN[0]B_HSYNC/I2C[2]_SDA/GP2[0]
21 DM388_VIN[0]A_D[0]	B18	VIN[0]A_D[0]/GP1[11]
21 DM388_VIN[0]A_D[1]	A17	VIN[0]A_D[1]/GP1[12]
21 DM388_VIN[0]A_D[2]	B17	VIN[0]A_D[2]/GP2[7]
21 DM388_VIN[0]A_D[3]	C17	VIN[0]A_D[3]/GP2[8]
21 DM388_VIN[0]A_D[4]	D17	VIN[0]A_D[4]/GP2[9]
21 DM388_VIN[0]A_D[5]	F17	VIN[0]A_D[5]/GP2[10]
21 DM388_VIN[0]A_D[6]	L20	VIN[0]A_D[6]/GP2[11]
21 DM388_VIN[0]A_D[7]	H20	VIN[0]A_D[7]/GP2[12]
21 DM388_VIN[0]A_D[8]_BD[0]	B16	VIN[0]A_D[8]_BD[0]/GP2[13]
21 DM388_VIN[0]A_D[9]_BD[1]	C16	VIN[0]A_D[9]_BD[1]/GP2[14]
21 DM388_VIN[0]A_D[10]_BD[2]	E16	VIN[0]A_D[10]_BD[2]/GP2[15]
21 DM388_CAM_WEn	H17	VIN[0]A_D[11]_BD[3]/CAM_WEn/GP2[16]
21 DM388_VIN[0]A_D[12]_BD[4]	J16	VIN[0]A_D[12]_BD[4]/CLKOUT1/GP2[17]
21 DM388_CAM_RESET	H16	VIN[0]A_D[13]_BD[5]/CAM_RESET/GP2[18]
21 DM388_CAM_STROBE	F13	VIN[0]A_D[14]_BD[6]/CAM_STROBE/GP2[19]
21 DM388_CAM_SHUTTER	H13	VIN[0]A_D[15]_BD[7]/CAM_SHUTTER/GP2[20]
21 DM388_CAM_DAT8	K11	VIN[0]A_D[16]/CAM_D[8]/I2C[2]_SCL/GP0[10]
21 DM388_CAM_DAT9	E12	VIN[0]A_D[17]/CAM_D[9]/EMAC[1]_RMRXER/GP0[11]
21 DM388_CAM_DAT10	K10	VIN[0]A_D[18]/CAM_D[10]/EMAC[1]_RMRXD[1]/I2C[3]_SCL/GP0[12]
21 DM388_CAM_DAT11	D7	VIN[0]A_D[19]/CAM_D[11]/EMAC[1]_RMRXD[0]/I2C[3]_SDA/GP0[13]
21 DM388_CAM_DAT12	F9	VIN[0]A_D[20]/CAM_D[12]/EMAC[1]_RMCRSDV/SPI[3]_SCS[0]n/GP0[14]
21 DM388_CAM_DAT13	C7	VIN[0]A_D[21]/CAM_D[13]/EMAC[1]_RMTXD[0]/SPI[3]_SCLK/GP0[15]
21 DM388_CAM_DAT14	A6	VIN[0]A_D[22]/CAM_D[14]/EMAC[1]_RMTXD[1]/SPI[3]_D[1]/GP0[16]
21 DM388_CAM_DAT15	A5	VIN[0]A_D[23]/CAM_D[15]/EMAC[1]_RMTXEN/SPI[3]_D[0]/GP0[17]
	F24	VOUT[0]_B_CB_C[2]/EMU2/GP2[22]
	D21	VOUT[0]_B_CB_C[3]/GP2[23]
	J23	VOUT[0]_B_CB_C[4]
	H23	VOUT[0]_B_CB_C[5]
	J24	VOUT[0]_B_CB_C[6]
	E24	VOUT[0]_B_CB_C[7]
	D24	VOUT[0]_B_CB_C[8]
	C24	VOUT[0]_B_CB_C[9]
	C25	VOUT[0]_G_Y_YC[2]/EMU3/GP2[24]
	C26	VOUT[0]_G_Y_YC[3]/GP2[25]
	E26	VOUT[0]_G_Y_YC[4]
	B26	VOUT[0]_G_Y_YC[5]
	A26	VOUT[0]_G_Y_YC[6]
	B25	VOUT[0]_G_Y_YC[7]
	B27	VOUT[0]_G_Y_YC[8]
	A27	VOUT[0]_G_Y_YC[9]
	C28	VOUT[0]_R_CR[2]/EMU4/GP2[26]
	B28	VOUT[0]_R_CR[3]/GP2[27]
	B29	VOUT[0]_R_CR[4]
	A29	VOUT[0]_R_CR[5]
	C30	VOUT[0]_R_CR[6]
	B30	VOUT[0]_R_CR[7]
	A30	VOUT[0]_R_CR[8]
	B31	VOUT[0]_R_CR[9]
12 DM388_CAM_PCLK_UT_RTSn	C20	VOUT[0]_AVID/VOUT[0]_FLD/SPI[3]_SCLK/TIM7_IO/GP2[21]
	B3	VOUT[0]_FLD/CAM_PCLK/GPMC_A[12]/UART2_RTSn/GP2[02]
	F21	VOUT[0]_HSYNC
	E20	VOUT[0]_VSYNC
	K22	VOUT[0]_CLK
	D3	VOUT[1]_CLK/EMAC[1]_MTCLK/VIN[1]A_HSYNC/GP2[28]
	B2	VOUT[1]_G_Y_YC[0]/CAM_D[2]/GPMC_A[6]/GP0[23]
	A2	VOUT[1]_G_Y_YC[1]/CAM_D[3]/GPMC_A[5]/GP0[22]
	L2	VOUT[1]_G_Y_YC[2]/GPMC_A[13]/VIN[1]A_D[21]/HDMI_SCL/SPI[2]_SCS[2]n/I2C[2]_SCL/GP3[20]
	H6	VOUT[1]_G_Y_YC[3]/EMAC[1]_MRXD[6]/VIN[1]A_D[8]/GP3[7]
	J8	VOUT[1]_G_Y_YC[4]/EMAC[1]_MRXD[7]/VIN[1]A_D[9]/GP3[8]
	J1	VOUT[1]_G_Y_YC[5]/EMAC[1]_MRXDV/VIN[1]A_D[10]/GP3[9]
	H4	VOUT[1]_G_Y_YC[6]/EMAC[1]_GMTCLK/VIN[1]A_D[11]/GP3[10]
	J9	VOUT[1]_G_Y_YC[7]/EMAC[1]_MTXD[0]/VIN[1]A_D[12]/GP3[11]
	L3	VOUT[1]_G_Y_YC[8]/EMAC[1]_MTXD[1]/VIN[1]A_D[13]/GP3[12]
	K1	VOUT[1]_G_Y_YC[9]/EMAC[1]_MTXD[2]/VIN[1]A_D[14]/GP3[13]
	C2	VOUT[1]_R_CR[0]/CAM_D[0]/GPMC_A[8]/GP0[25]
	C1	VOUT[1]_R_CR[1]/CAM_D[1]/GPMC_A[7]/GP0[24]
	L6	VOUT[1]_R_CR[2]/GPMC_A[15]/VIN[1]A_D[23]/HDMI_HPDET/SPI[2]_D[1]/GP3[22]
	L4	VOUT[1]_R_CR[3]/GPMC_A[14]/VIN[1]A_D[22]/HDMI_SDA/SPI[2]_SCLK/I2C[2]_SDA/GP3[21]
	H2	VOUT[1]_R_CR[4]/EMAC[1]_MTXD[3]/VIN[1]A_D[15]/SPI[3]_SCS[1]n/GP3[14]
	M11	VOUT[1]_R_CR[5]/EMAC[1]_MTXD[4]/VIN[1]A_D[16]/SPI[3]_SCLK/GP3[15]
	L12	VOUT[1]_R_CR[6]/EMAC[1]_MTXD[5]/VIN[1]A_D[17]/SPI[3]_D[1]/GP3[16]
	M10	VOUT[1]_R_CR[7]/EMAC[1]_MTXD[6]/VIN[1]A_D[18]/SPI[3]_D[0]/GP3[17]
	J2	VOUT[1]_R_CR[8]/EMAC[1]_MTXD[7]/VIN[1]A_D[19]/GP3[18]
	K2	VOUT[1]_R_CR[9]/EMAC[1]_MTXEN/VIN[1]A_D[20]/GP3[19]
	H9	VOUT[1]_B_CB_C[0]/CAM_VS/GPMC_A[10]/UART2_TXD/GP0[27]
	D5	VOUT[1]_B_CB_C[1]/CAM_HS/GPMC_A[9]/UART2_RXD/GP0[26]
	M8	VOUT[1]_B_CB_C[2]/GPMC_A[0]/VIN[1]A_D[7]/HDMI_CEC/SPI[2]_D[0]/GP3[30]
	F2	VOUT[1]_B_CB_C[3]/EMAC[1]_MRCLK/VIN[1]A_D[0]/GP3[0]
	F3	VOUT[1]_B_CB_C[4]/EMAC[1]_MRXD[0]/VIN[1]A_D[1]/GP3[1]
	G1	VOUT[1]_B_CB_C[5]/EMAC[1]_MRXD[1]/VIN[1]A_D[2]/GP3[2]
	G2	VOUT[1]_B_CB_C[6]/EMAC[1]_MRXD[2]/VIN[1]A_D[3]/GP3[3]
	H3	VOUT[1]_B_CB_C[7]/EMAC[1]_MRXD[3]/VIN[1]A_D[4]/GP3[4]
	G3	VOUT[1]_B_CB_C[8]/EMAC[1]_MRXD[4]/VIN[1]A_D[5]/I2C[3]_SCL/GP3[5]
	H5	VOUT[1]_B_CB_C[9]/EMAC[1]_MRXD[5]/VIN[1]A_D[6]/I2C[3]_SDA/GP3[6]
	E2	VOUT[1]_HSYNC/EMAC[1]_MCOL/VIN[1]A_VSYNC/SPI[3]_D[1]/GP2[29]
	F5	VOUT[1]_VSYNC/EMAC[1]_MCRS/VIN[1]A_FLD/VIN[1]A_DE/SPI[3]_D[0]/GP2[30]
	F1	VOUT[1]_AVID/EMAC[1]_MRXER/VIN[1]A_CLK/TIM6_IO/GP2[31]
	J10	VOUT[1]_FLD/CAM_FLD/CAM_WEn/GPMC_A[11]/UART2_CTSn/GP0[28]
	B4	VIN[0]A_FLD/CAM_D[5]/GP0[20]
	C13	VIN[0]A_VSYNC/GP2[4]
	B5	VIN[0]A_DE/CAM_D[7]/GP0[18]
	A3	VIN[0]B_FLD/CAM_D[4]/GP0[21]
	C5	VIN[0]B_DE/CAM_D[6]/GP0[19]
	D13	VIN[0]A_HSYNC/GP2[3]

DM388_CAM_DAT2 21, DM388_CAM_DAT3 21, ENET_RSTn 21, DM388_CAM_DAT0 21, DM388_CAM_DAT1 21, DM388_CAM_VS 21, DM388_CAM_HS 21, DM388_GP3[3] 21, DM388_GP3[4] 21, DM388_CAM_FLD_UT_CTSn 12, DM388_CAM_DAT5 21, DM388_VIN[0]A_VSYNC 21, DM388_CAM_DAT7 21, DM388_CAM_DAT4 21, DM388_CAM_DAT6 21, DM388_VIN[0]A_HSYNC 21

DM388AAAR21FP

CSI

U7B

CSI INTERFACE

21 DM388_CSI_DX0	AB2	CSI2_DX[0]	RSV39 H25
21 DM388_CSI_DY0	AC2	CSI2_DY[0]	
21 DM388_CSI_DX1	AA1	CSI2_DX[1]	RSV40 H29
21 DM388_CSI_DY1	AB1	CSI2_DY[1]	
21 DM388_CSI_DX2	AA2	CSI2_DX[2]	RSV1 H27
21 DM388_CSI_DY2	Y2	CSI2_DY[2]	RSV41 AD8
21 DM388_CSI_DX3	W2	CSI2_DX[3]	
21 DM388_CSI_DY3	W1	CSI2_DY[3]	RSV35 AJ24
21 DM388_CSI_DX4	V1	CSI2_DX[4]	RSV34 AH24
21 DM388_CSI_DY4	V2	CSI2_DY[4]	

DM388AAAR21FP

JTAG, PCIE, TV OUT

U7A

PCIE AND JTAG

	R74 2.7K_1%	B10	TV_VFB0
21 TV_OUT0		B9	TV_OUT0
	R76 4.7K_1%	B11	TV_RSET
21 DM388_PCIe_TXP0	C63 0.1uF	L31	PCIE_TXP0
21 DM388_PCIe_TXN0	C64 0.1uF	K31	PCIE_TXN0
21 DM388_PCIe_RXP0		K30	PCIE_RXP0
21 DM388_PCIe_RXN0		J30	PCIE_RXN0
		H28	RSV3
		N28	TDI
	R133 22E_1%	U26	TDO
		T31	TMS
		T29	TCLK
	R124 22E_1%	N29	RTCK
DM388_TRSTn 21		U24	TRSTn
DM388_EMU1 21	R77 22E_1%	A18	EMU0
DM388_EMU0 21	R78 22E_1%	B19	EMU1
DM388_SERDES_CLKP 21	C65 270pF	H30	SERDES_CLKP
DM388_SERDES_CLKN 21	C66 270pF	H31	SERDES_CLKN

DM388_TDI 21, DM388_TDO 21, DM388_TMS 21, DM388_TCLK 21, DM388_RTCK 21

DM388AAAR21FP

R120 4.7K

DGND

DGND

Project : TMDSCSK388	Designed for TI by Mistral Solutions Pvt Ltd	Title	CAMERA,JTAG,CSI
		Size C	Document Number MS_TI_CSK_TMDSCSK388_SCH_REVB
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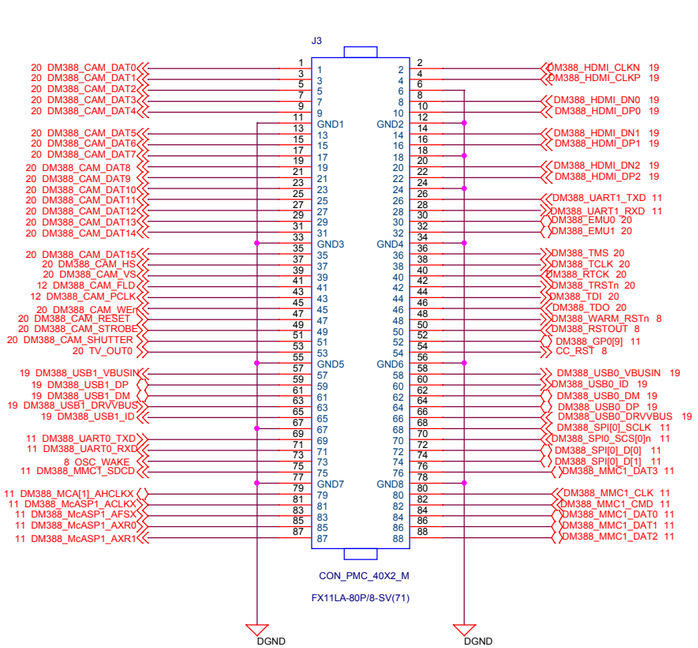
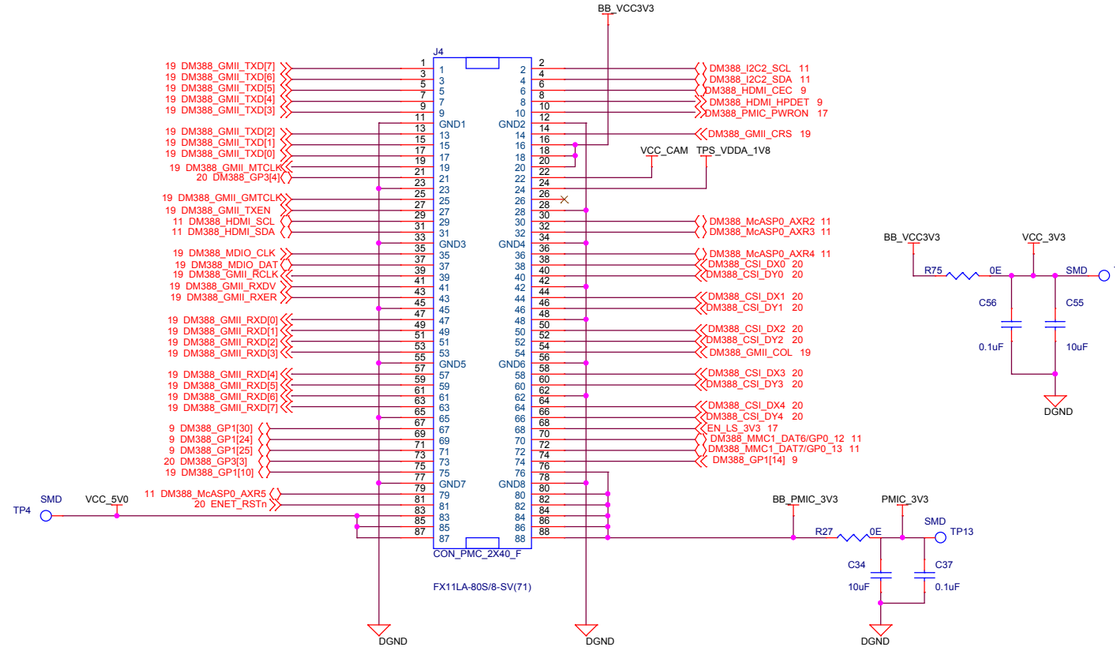
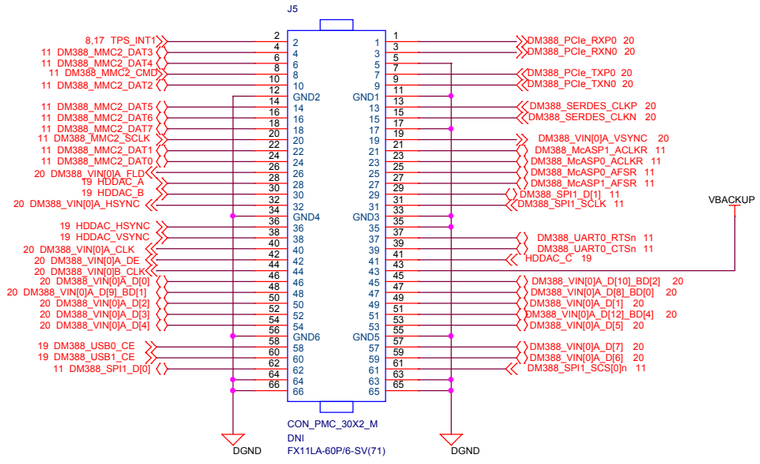
BOARD TO BOARD CONNECTORS





BOARD TO BOARD TERMINATION



Project : TMDSCSK388	Designed for TI by Mistral Solutions Pvt Ltd	Title	BOARD TO BOARD CONNECTORS
		Size: C	Document Number: MS_TI_CSK_TMDSCSK388_SCH_REVB — Rev: B
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HARDWARE SCHEMATICS

FIDUCIALS

FID1
FID_40X80

FID2
FID_40X80

FID3
FID_40X80

FID4
FID_40X80

FID5
FID_40X80

FID6
FID_40X80

MicroSD CARD

SDSDQM-008G-B35
H4

LOGOs & LABELs

PCB
LOGO
Texas Intruments

PCB
LOGO
Pb-Free

PCB
LOGO
For Evaluation only; not FCC approved for resale

PCB_Number=PRJ_Number
PCB Rev:=PCB_Rev
PCB1

Serial No:
PCB Label
Size: 0.9" x 0.12 "
LBL1

ASSY REV
PCB Label
Size: 0.55" x 0.12 "
LBL2

Label_Assembly Note
ZZ1
The boards and components must be baked before assembly

Label_Assembly Note
ZZ2
Provide serial numbers to the assembled boards for identification

Label_Assembly Note
ZZ3
Please carry out the cold points check verification and provide the report for each assembled board

Label_Assembly Note
ZZ4
The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

Label_Assembly Note
ZZ5
All MSL components should be baked as per JEDEC standard

Label_Assembly Note
ZZ6
PCB should be baked at 120 degree for 8 hours

Label_Assembly Note
ZZ7
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Label_Assembly Note
ZZ8
These assemblies are ESD sensitive, ESD precautions shall be observed.

Label_Assembly Note
ZZ9
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Project : TMDSCSK388	Designed for TI by Mistral Solutions Pvt Ltd	Title: HARDWARE SCHEMATICS
		Size: C — Document Number: MS_TI_CSK_TMDSCSK388_SCH_REVB — Rev: B
		Date: Friday, January 13, 2017 — Sheet 22 of 22