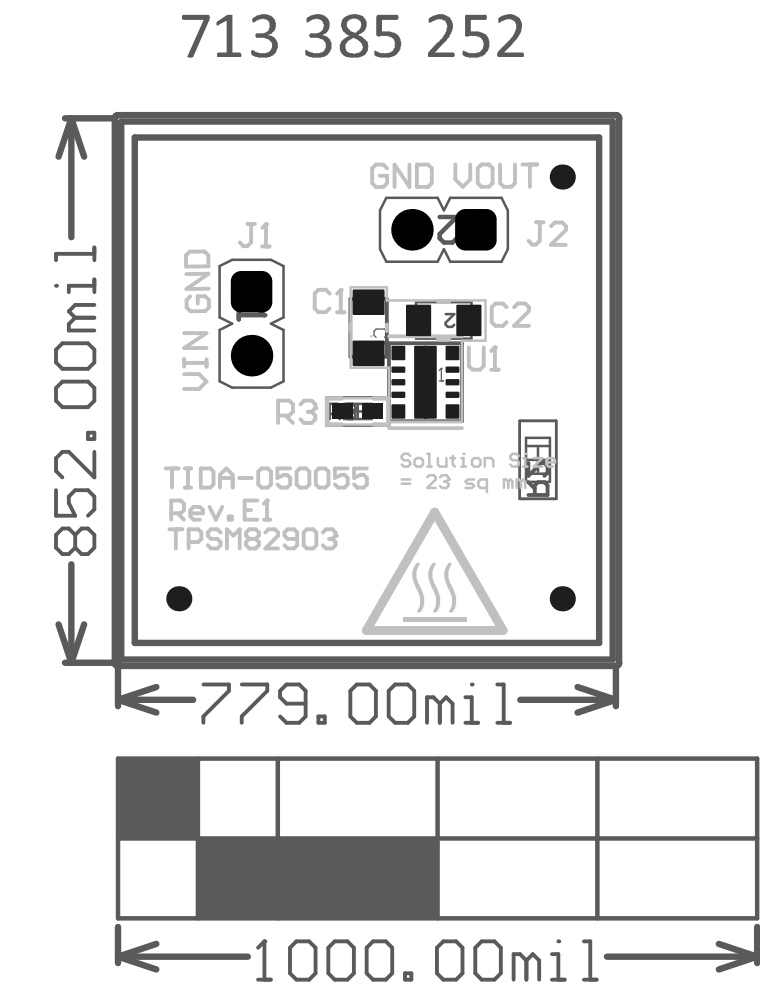


A

B

C

D



COMPONENTS MARKED 'DNP' SHOULD NOT BE COUPLED TO BOARD ASSEMBLY VARIANT: 001

713.385.252	852.00mil	779.00mil	1000.00mil
LAYER NAME =	TOP	TID #:	.TIDGIT.
PLC NAME =	TOP	GENS	7/27/2023

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER:	LAYOUT BY:
Tahar Allag	Fred Illguth
SCALE: 1.00	ALTUM DESIGNER VERSION:
	22.7.1.60

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR-4 High Tg	5.00mil	4.2	
2	Signal Layer 1		1.40mil		
	Dielectric 2	FR-4 High Tg	24.40mil	4.2	
3	Signal Layer 2		1.40mil		
	Dielectric 3	FR-4 High Tg	5.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	

DESIGN INFORMATION

MIN. HOLE SIZE: 10 MIL

MIN. CLEARANCE: 8.9 MIL

MIN. VIA SIZE: 18 MIL

MINIMUM ANNIHILATING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

☐ FR-408 ☒ FR-4 High Tg ☐ OTHER

THICKNESS: ☒ 40 MIL (1.0mm) +/-10% ☐ OTHER

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2 ☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2 ☐ OTHER +/-

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES

PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:

SILKSCREEN: ☒ TOP ☐ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER

SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER

☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG ☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE ☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF: ☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3 ☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☒ 6.1MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:	TPSM8290X
DESIGNED FOR:	Public Release
FILE NAME:	TIDA-050055.PcbDoc

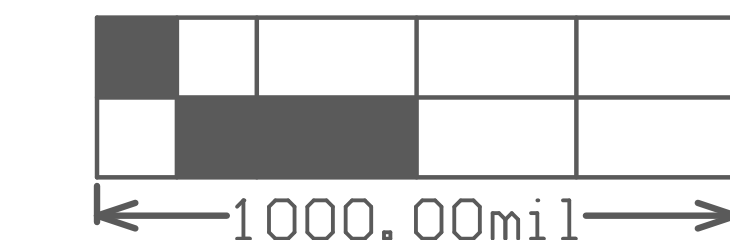
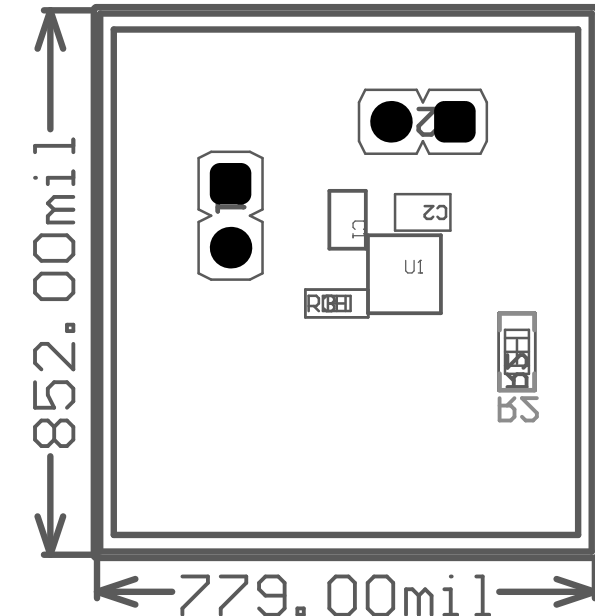
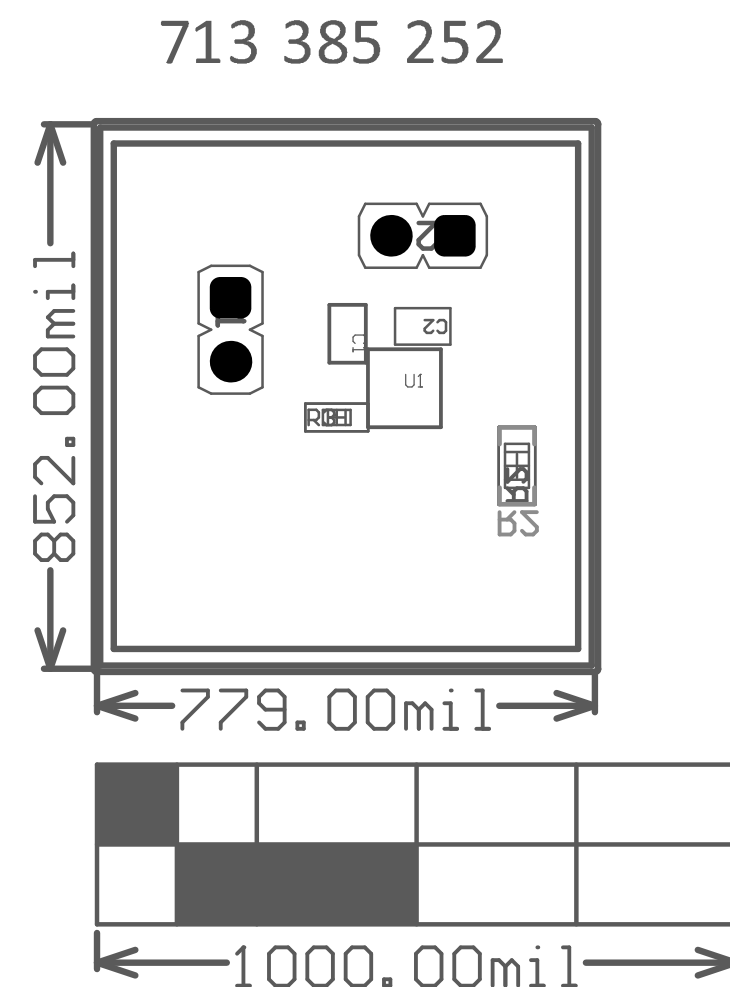
ENGINEER:	LAYOUT BY:
Tahar Allag	Fred Illguth
SCALE: 1.00	ALTUM DESIGNER VERSION:
	22.7.1.60

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED 'DNP' SHOULD NOT BE REPLACED OR TOOK OUT
ASSEMBLY VARIANT: 001

[illegible]

PL021INSTRUMENTS\DATA\Layer 1 Assembly\Drawn\GENERATED\5 :: 7/22/2022 3:14:48 AM\222A1 rev06\TEXASINSTRUMENTS_19

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR-4 High Tg	5.00mil	4.2	
2	Signal Layer 1		1.40mil		
	Dielectric 2	FR-4 High Tg	24.40mil	4.2	
3	Signal Layer 2		1.40mil		
	Dielectric 3	FR-4 High Tg	5.00mil	4.2	
4	Bottom Layer		5.00mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	

MATERIAL: ☐ FR-408 ☒ FR-4 High Tg ☐ OTHER

THICKNESS: ☒ 40 MIL (1.0mm) +/-10% ☐ OTHER

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING: REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES

PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☐ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER

SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV. ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.G. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs
TO MEET OR EXCEED THE REQUIREMENTS OF:

☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3

☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☒ 6.1MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
TPSM8290X

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-050055.PcbDoc

ENGINEER: Tahar Allag	LAYOUT BY: Fred Illguth
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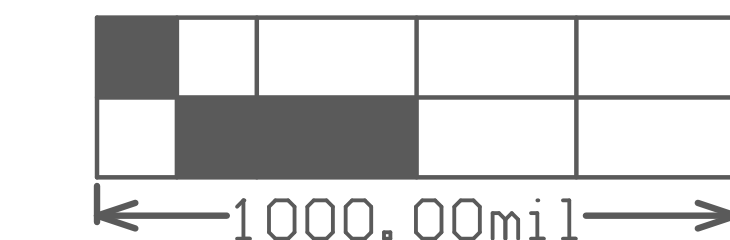
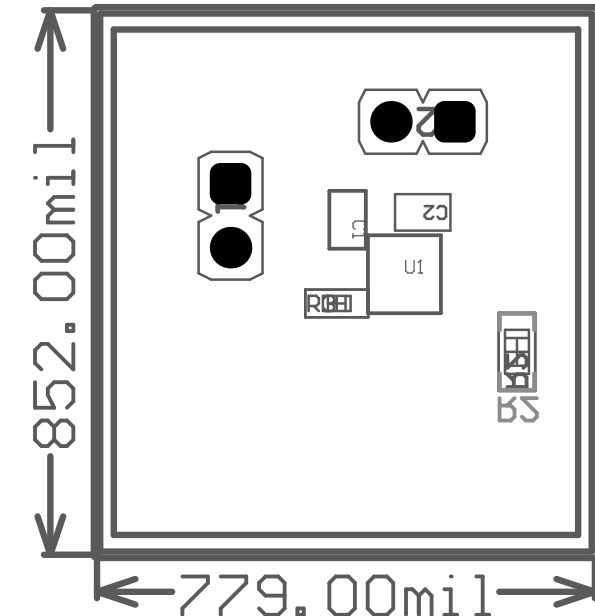
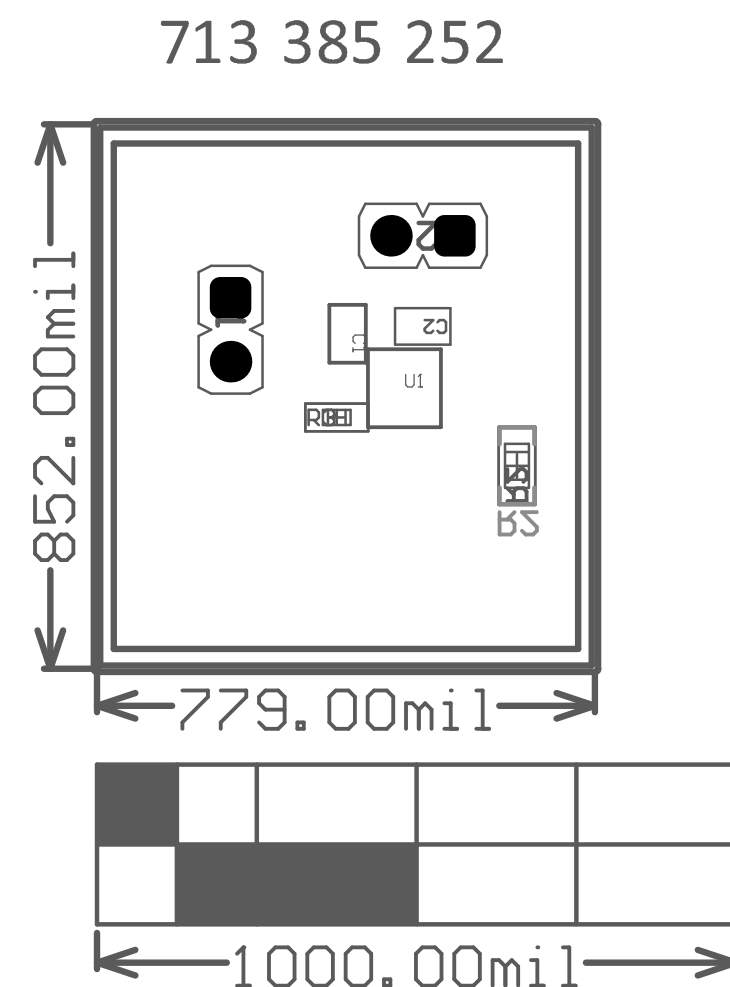
SCALE: 1.00	ALTIUM DESIGNER VERSION: 22.7.1.60
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Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED 'DNP' SHOULD NOT BE INCLUDED IN THE ASSEMBLY
ASSEMBLY VARIANT: 001

[illegible]

PLC21WAVEE2N152KAT Layer 2 Assembly: 01 and GENERATED :: 7/22/2022 10:46:50 AM 1996 TEXAS INSTRUMENTS

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Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR-4 High Tg	5.00mil	4.2	
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	Dielectric 2	FR-4 High Tg	24.40mil	4.2	
3	Signal Layer 2		1.40mil		
	Dielectric 3	FR-4 High Tg	5.00mil	4.2	
4	Bottom Layer		5.00mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	

MATERIAL: ☐ FR-408 ☒ FR-4 High Tg ☐ OTHER

THICKNESS: ☒ 40 MIL (1.0mm) +/-10% ☐ OTHER

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING: REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES

PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☐ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____

SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs
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☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☒ 6.1MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE

TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
TPSM8290X

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-050055.PcbDoc

ENGINEER: Tahar Allag	LAYOUT BY: Fred Illguth
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SCALE: 1.00	ALTUM DESIGNER VERSION: 22.7.1.60
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