**TIDA-00204-revE2: Altium Design Changes**

Rev Who What

151216 KH TIDA-00204\_revE2\_Sitara\_SC\_0.SchDoc & \*.PcbDoc  
 - removed NetLabel & connection “RGMII1/2\_RXCLK” from U15-Pin D17/D18;  
 - placed NetLabel & connection “RGMII1\_RXCLK” to U15 Pin L18;  
 - placed NetLabel & connection “RGMII2\_RXCLK” to U15 Pin T15

- KH moved RGMII1\_TXCTRL\_R from H16 and J16

- KH new LengthMatching of all RGMII-Signals, because of changed signal length of RGMII1\_TXCTRL\_R  
 (and later ReleaseUpdate of Altium AD14 has more accurate LengthCalculation, considering   
 the length of ThruHoleVias)

150319 KH bringing in all the schematic changes according E-Mail correspondence;   
 - Clock-Generator CDCE913 / Ser-R’s in CLK-Signals / V18CDC-Supply

150512 KH Changed C261..C268, C271..C278 to “COG 4.7pF 50V 0201” (GRM0335C1H4R7CA01)

**Changes made within revE1 are listed below:**

0.01 ALL - Initial schematics with updates from meeting at GCD Oct-20, 2014

0.02 KNM - Changed power supply bypass caps for Sitara from 0402 to 0201

0.03 KNM - Removed the lc03\_3v3 diodes(D14,D15, D20, D21) on PHY2  
 - Replaced the lc03\_3v3 diodes(D5,D6, D11, D12) with the TPD4E05U06(2xU?) on PHY1  
 - Assigned differential pair property on all differential signal lines

* 1. KH - Annotation of TPD4E05U06 (🡪U23, U24)  
      - Adding OffSheetConnectors (DiffPairs) to NC-Pins U23-6,7,9,10 and U24-6,7,9,10  
      - Changed C171 (10µ, 1206) to same type, as C169, C170 (🡪10µ, 0603)  
      - Completed DiffPair-SignalNames (added “\_N”, “\_P”) and placed DiffPair-Directives  
      on “\*\_Memory.SchDoc” and “\*\_Sitara\_SC\_0.SchDoc” (DDR\_DQS0.., DDR\_DQS1.., DDR\_CLK..)
  2. MS - Added 22-ohm series termination R? at Sitara MDIO\_CLK and MDIO\_DATA  
      - PHY1: Removed R114, R115, R116  
      - PHY1: Changed R117 from 100k to 4k7  
      - PHY2: Removed R144, R145, R146  
      - PHY2: Changed R147 from 100k to 4k7  
      - PHY2: Add strap resistors 11k (R?) and 2.49k (R?) at RX\_D7  
      - PHY2: Connected R161 and D19 to GND (instead of Vddio)  
      - Sheet “PS\_2”: C25, C26, C31, C33, C34, C35 changed to cap C1608X5R1E106M080AC (X5R) to use same 10uF caps across the board (optimize BOM)  
      - Removed R19 &R20 (each 0.05-ohm). No need to measure power on AM3359 VDD\_CORE and VDD\_MP  
      - PHY1: Add 0-ohm resistor (R1000, R1001) at each 1.8V pin (17 and 64) at each PHY and added 1nF capacitors C221 and C222 directly at pin. Required in case using internal LDO. Then both pins must not be connected to each other.   
      - PHY2: Add 0-ohm resistor (R1002, R1003) at each 1.8V pin (17 and 64) at each PHY and added 1nF capacitors C247 and C248 directly at pin.  
      - PHY1: Protection diode, U23 and U24, changed from GND to SHIELD/Earth.   
      - Changed C146 from 0.01uF (0201) to 2.2F (0402) to add further delay and bigger size to have option change manually. That delay should be longer for the RTC\_PORZn  
      - PHY2: Changed R163, R165, R166 from 0603 to 0402
  3. KH - Sitara\_SC\_0: Renamed series resistors at Sitara MDIO\_CLK and \*\_Data to R200, R201  
      - PHY2: Renamed strap resistors to R168, R169  
      - PHY2: **correction**: placed C248 direct at Pin64 (after R1003)  
      - Sitara\_SC\_0: U9A, SN74AUP08DCU **Pin7 is horizontal mirrored and not connected!**  
      🡪 I’ve drawn the wire “under” symbol, so it’s connected (see junction)  
      - JTAGUSB: renamed OffSheet Connectors “USBD..” to “USBD..\_N”, “USBD..\_P”;  
      placed NetLabel “USBD\_P”, “USBD\_N” on Connector-side;  
      to enable DiffPair-Routing

0.07 KNM - Changed load capacitance of Y1 from 33pF to 27pF(C137-C138) (assuming 4-5pF stray capacitance) [Sitara\_SC\_0]

- Changed load capacitance of Y2 from 22pF to 18pF(C139-C143) (assuming 3-4pF stray capacitance) [Sitara\_SC\_0]

- Changed S1 B3U1100P to B3u-1000P to remove additional pin on button[Sitara\_SC\_0]

- Changed load capacitance of Y3 from 33pF to 27pF(C184-C185) (assuming 4-5pF stray capacitance)[JTAGUSB]

- Changed load capacitance of Y4 from 33pF to 27pF(C200-C201) (assuming 4-5pF stray capacitance)[PHY1]

- Added strap resistors R?, R? on RX\_D6 and RX\_D7[PHY1]

- Changed load capacitance of Y5 from 33pF to 27pF(C228-C229) (assuming 4-5pF stray capacitance)[PHY2]

- Added strap resistors R?, R? on RX\_D6 [PHY2]

- Removed resistor R165 and R166 at Crystal, no decoupling required from external clock [PHY2]

- Added capacitor between gnd and MicroSD\_earth (C?)[Memory]

- Changed resistor R16 from 5% tolerance to 1% [PS\_1]

- Changed vendor of resistor R41 to CRCW04021K00FKED

- Changed vendor of resistor R60 to CRCW0402100KFKED

- Changed vendor of capacitor C152 to CL03A104KP3NNNC

0.08 KH - Updated PCB  
 - Annotation of “R?”- and “C?”-Designators

0.09 KNM - PHY1: LED2, LED1, LED0 connected R120, D9, R119, D8, R118, D7 from VDDIO to GND (active  
 high). No all LEDs are active high.  
 - PHY2: LED2, LED1, LED0 connected R150, D18, R149, D17, R148, D16 from VDDIO to GND (active  
 high). Now all LEDs are active high.  
 - moved termination resistors from [PHY2] to [Sitara\_SC\_0] r137,r138,r139,140,r141,r142  
 - Changed termination resistors R107, R108, R109, R110, R111, R112, R122, R123, R124, R125, R126, R128 into two arrays R?

0.10 KH - Annotation of R-Array-Designators (R? to R176, R177)  
 - Renamed OffSheetConnectors & placed NetNames “..\_R” to wires between Source and Ser-R’s  
 - Corrected OffSheetConnector-Directions (Left/Right) of RX- and TX-Lines  
 - Changed Pins at R-Array “R177 “

0.11 ALL - Changed C6 and C8 from 10n to 100nF/100V  
 - Changed C44 from 10n to 100nF/10V X7R 0402  
 - Updated symbol U9 (fix)  
 - Add second serial termination resistor on MDIO\_CLK and removed PU.

0.12 KH - “..\_PS\_1.SchDoc”; U5: added Pin7 (Thermal Pad) to GND (as recommended in Datasheet)  
 KH - placed Pullup-Resistor (R125, R145; 4k7, 0402) to each PHY, Pin60 (“..\_INTPWDN”)  
 - Removed “RGMII1\_RXCTRL\_R” from R-Array and placed discrete Ser-R (R178)  
 - New Pinning on R-Array R177

0.13 MS/KNM  
 - Added R203 serial termination and split MDIO\_DATA into MDIO\_DATA\_1 (for PHY\_1) and  
 MDIO\_DATA\_2 (for PHY\_2) (sheet SC\_0)  
 - Connected R135 to Sitara Pin MDIO (sheet SC\_0)  
 - Added jumper J200 at 3.3V LDO output (sheet PS\_1)  
 - Changed L1 from LPS3010-102MLB to LPS3010-102MRB PS\_0

0.14 KH - Length Tuning of RMMII..-Signals (difference < 0.5 mm)  
 - Power-Connection from Supply to Sitara-, DDR3-, ..-Devices  
 KNM/KH Unified some Parts for BOM-optimization:   
 - C154 (0402); new: 0201  
 - C146 (0402); new: 0603  
 - R95, R97, R135 (0402); new: 5%  
 KH - modified footprint of U14 according datasheet  
 (Footprint to be found in LocalLibrary “TIIDA-00204.PcbLib” as “DRY0006A\_GCD”)  
 - PCB (v 0.14) transmitted for TI internal Review

0.15 KNM - Change T1 from Hx5008NL to Hx5008FNL[PHY1]  
 - Change R176 from EXB2HV470JV to EXB-2HV220JV [PHY1]  
 - Change Y4 from ABM3-25.000MHZ-D2W-T to ABM3-25.000MHZ-D2Y-T[PHY1]  
 - Change T2 from Hx5008NL to Hx5008FNL[PHY2]  
 - Change Y5 from ABM3-25.000MHZ-D2W-T to ABM3-25.000MHZ-D2Y-T[PHY1]  
 - Change R177 from EXB2HV470JV to EXB-2HV220JV [Sitara\_SC\_0]  
 - Change Y1 from ABM3-24.000MHZ-D2W-T to ABM3-24.000MHZ-D2Y-T[Sitara\_SC\_0]

* 1. KH - Mirrored R177 (was mirrored after last change)  
      - PCB: optimization of Polygons at BottomLayer, MidLayers  
      - PCB: additional Vias connecting GND-Polygons

0.17 KNM - Removed jumper J200 (between Phy Earths)  
 - Re-annotated the schematics old designtors in brackets  
 - Change RGMII termination resistors to 0 Ohm 🡪 R43(R152), R44(R153), R46(R154), R47(R155), R50(R158), R51(R159), R19(R176), R20(R178) [PHY 1 and PHY2]  
 - Corrected spelling of title  
 - Change 10.0k from 1% to 5% 🡪 R83, R85, R79, R68, R69, R70, R71, R72, R73, R96, R97, R98  
 - Defined variant: ‘production’ with DNP and ‘complete’ w/ all parts  
 - Variant ‘production’: Changed to DNP: C12, R129, R148, R131, R132, R133, R134, R135, , R136, R137, R138, R139, R158, R159, R160, R143, R144, J8, C136, R99, R107-112, C140

**Rev E1** ALL Design- and Layout-Freeze:  
 - PHY1/2: - added capacitors (not fitted) between “PHY1/2\_earth” and “GND”  
 - optimized Polygones & Cutouts on bottom (“PHY1/2\_earth” and “GND”)  
 - optimized width for “V25PHY”-Supply  
 - SilkScreen: - additional and modified textures for Voltages, LEDs, etc.  
 - New Annotation of whole Project  
 - PCB no change  
 🡪 **Design Freeze !**

**E1.01** KNM Need to delete and redo Variant “001” change bug fix.(**Annotate is NOT changed**)

Check in the schematic for variant changes by:

PCB no change

24 parts(only C or R) which changed to DNP are referenced with “**Changed to DNP: partnr**”

2 parts(Only R) which changed to populated are referenced with “**Changed to polulate: partnr** ”.

**Changed to populate parts Below see copy from BOM from Design Freeze**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 98 | C136 | 1 | 0.01uF | GRM033R71A103KA01D | MuRata | CAP, CERM, 0.01 µF, 10 V, +/- 10%, X7R, 0201 | 0201 |
| 99 | C140 | 1 | 1uF | CL03A105MP3NSNC | Samsung | CAP, CERM, 1 µF, 10 V, +/- 20%, X5R, 0201 | 0201 |
| 100 | C250 | 1 | 0.1uF | GRM155R71A104KA01D | MuRata | CAP, CERM, 0.1 µF, 10 V, +/- 10%, X7R, 0402 | 0402 |
| 101 | C251 | 1 | 4.7uF | GRM188R61C475KAAJ | MuRata | CAP, CERM, 4.7 µF, 16 V, +/- 10%, X5R, 0603 | 0603 |
| 103 | R131, R135, R137, R148 | 4 | 10k | CRCW040210K0JNED | Vishay-Dale | RES, 10 k, 5%, 0.063 W, 0402 | 0402 |
| 104 | R99 | 1 | 49.9 | CRCW040249R9FKED | Vishay-Dale | RES, 49.9, 1%, 0.063 W, 0402 | 0402 |
| 105 | R107, R108, R109, R110, R111 | 5 | 100k | CRCW0402100KJNED | Vishay-Dale | RES, 100 k, 5%, 0.063 W, 0402 | 0402 |
| 106 | R129 | 1 | 1.00k | CRCW04021K00FKED | Vishay-Dale | RES, 1.00 k, 1%, 0.063 W, 0402 | 0402 |
| 107 | R132 | 1 | 240 | CRCW0402240RJNED | Vishay-Dale | RES, 240, 5%, 0.063 W, 0402 | 0402 |
| 108 | R133 | 1 | 47 | EXB-2HV470JV | Panasonic | RES, 47, 5%, 0.0625 W, Resistor Array - 8x1 | Resistor Array - 8x1 |
| 109 | R134 | 1 | 47 | CRCW040247R0JNED | Vishay-Dale | RES, 47, 5%, 0.063 W, 0402 | 0402 |
| 110 | R136, R138, R158 | 3 | 10.0k | CRCW040210K0FKED | Vishay-Dale | RES, 10.0 k, 1%, 0.063 W, 0402 | 0402 |
| 111 | R139, R143, R144 | 3 | 0 | CRCW06030000Z0EA | Vishay-Dale | RES, 0, 5%, 0.1 W, 0603 | 0603 |

Table 1: parts changed from DNP to populate

**New do not populate parts are:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 60 | R35 | 0 | 22 | CRCW040222R0JNED | Vishay-Dale | RES, 22, 5%, 0.063 W, 0402 | 0402 |
| 52 | R63 | 0 | 0 | CRCW04020000Z0ED | Vishay-Dale | RES, 0, 5%, 0.063 W, 0402 | 0402 |

Table 2 parts changed from populate to DNP

**E1.02 KNM** **Change R16 to 110k Ohm 1% resistor  
 Change R5 to 80.6k Ohm 1% resistor  
 Change R11, R17, R18, R39, R40, C19, C20 and U4 to DNP due to wrong power sequencing on he phys.  
 Added text to all schematics “TI Confidential – NDA Required – Preliminary version, not tested, subject to change without notice”**

PCB no change

Potential changes (Under review, not executed)

* **Move RGMII1\_TXCTRL\_R from H16 and J16**

**Fix: add wire below BGA to connect H16 and J16**